SJSU SAN JOSÉ STATE UNIVERSITY

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Department of Computer Engineering

Real-Time Embedded System
Co-Design
CMPE 146 Section 1
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MCU Timers

MCU Timers

Five different timer types

- System Timer (SysTick)
- Watchdog Timer (WDT)
- Real-Time Clock (RTC)
- Timer32
- Timer_A

System Timer (SysTick)

- Internal to the processor
  - Standard ARM component in the recent Cortex processor architectures
- Clock source: MCLK
- 24-bit, decrementing, wrap-on-zero counter
- Commonly used to generate interrupts for switching RTOS (Real-Time Operating System) tasks
  - Typical time slice: 1 to 10 ms
  - RTOS uses the same timer for task switching across processor types
    - Independent of peripherals outside the processor
- Can be used as a general-purpose timer without the RTOS

Watchdog Timer (WDT)

- Clock sources: SMCLK, ACLK, VLOCLK, BCLK
- 32-bit up counter
  - Counter value not accessible to software
- Eight software-selectable time intervals
  - 2^6, 2^9, 2^{13}, 2^{15}, 2^{19}, 2^{23}, 2^{27}, 2^{31}
- Two usage modes
- Watchdog Mode
  - Generates system reset when counter expires
  - Most embedded systems are unattended
    - There is no one there to reset the system if something really wrong happens
  - RTOS or program must regularly reset it to avoid system reset
    - Absence of a timer reset is a good indication of software malfunctioning
- Interval Timer Mode
  - Just for generating periodic interrupts (no reset on expiration)
  - Can stay active in low-power mode

Real-Time Clock (RTC)

- Clock source: BCLK
  - Must be at 32,768 Hz for proper RTC operation
- Provides seconds, minutes, hours, day of week, day of month, month, and year (including leap year correction)
- Registers are updated once per second
  - Resolution not very useful for many precise timing purposes
- Input clock may be asynchronous to the system clock
  - Reading a register may return an invalid value while it is being updated
  - May check a ready flag before read or read multiple times
  - Read issue can be resolved with shadow register designed in
- Supports flexible alarm functions
  - For example, generate alarm (interrupt) at specific time, day; repeat or not
- Frequency can be calibrated and temperature compensated
  - Calibration register stores difference from true 32-kHz frequency
  - Software can measure temperature change and compensate the frequency
- Active in low-power mode

Timer32

- Two independent and identical counters
- 32-bit or 16-bit, count-down timer
- Clock source: MCLK
  - Can be divided by 1, 16 or 256 for different resolutions and capacities
- Three different timer modes supported for each counter
  - Free-running mode
    - Counter wraps after reaching zero and continues from maximum value
  - Periodic timer mode
    - Counter generates an interrupt after reaching zero and reload value
  - One-shot timer mode
    - Counter generates an interrupt after reaching zero and halts

Timer_A

- Four timers: TA0, TA1, TA2 and TA3
- 16-bit, counts up or down
- Input clock can be asynchronous or synchronous
  - Reading counter may return an invalid value if asynchronous
- Can generate an interrupt when counter overflows
  - To indicate a probable error condition
- Clock sources
  - Internal to MCU: ACLK, SMCLK
  - External to MCU: TAxCLK (4 direct input pins), INCLK (via GPIO)
  - Go through two stages
    - First stage of 1, 2, 4 or 8, then followed by 1, 2, 3, 4, 5, 6, 7 or, 8

Timer Block

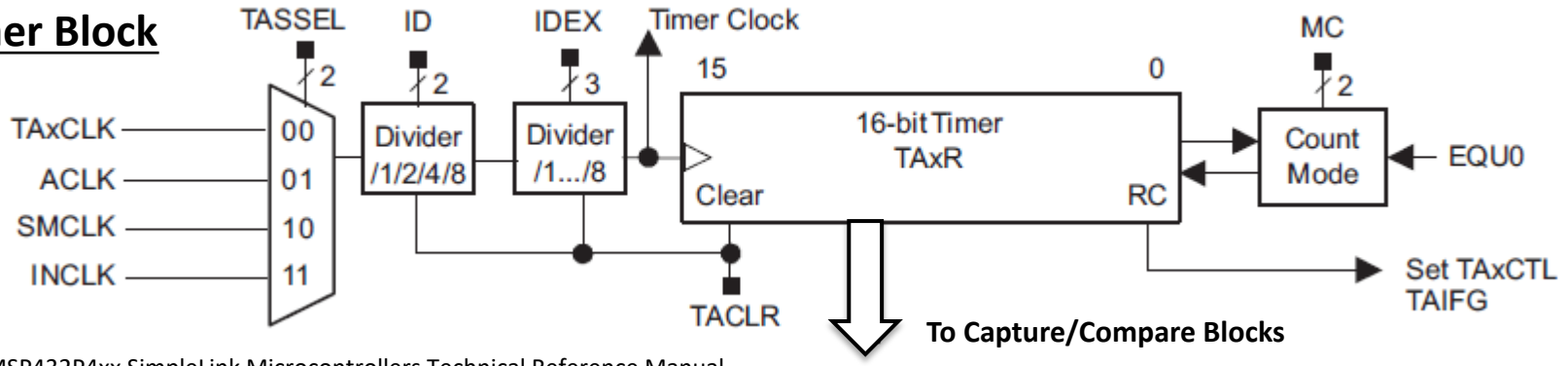
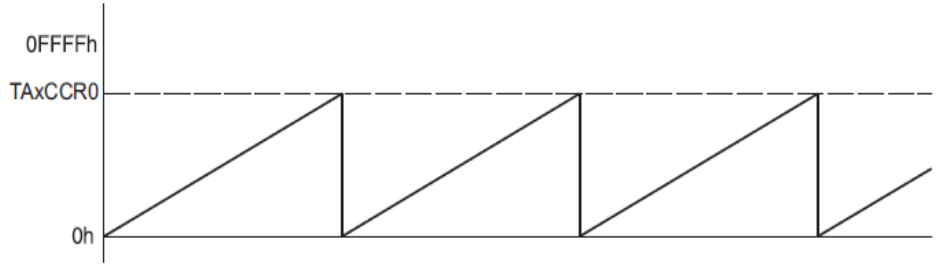


Diagram source: TI MSP432P4xx SimpleLink Microcontrollers Technical Reference Manual

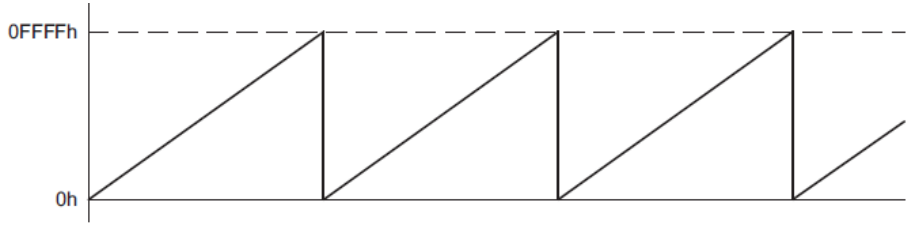
Timer_A Counting Modes

Three counting modes

- Up: Repeatedly counts from zero to the desired value, then restarts from zero
  - Generates two interrupts: at reaching desired value, at reaching zero



- Continuous: Repeatedly counts from zero to 0xFFFF , then restarts from zero
  - Generates one interrupt at reaching zero



- Up/down: Repeatedly counts from zero up to the desired value and back down to zero
  - Generates two interrupts: at reaching desired value, at reaching zero

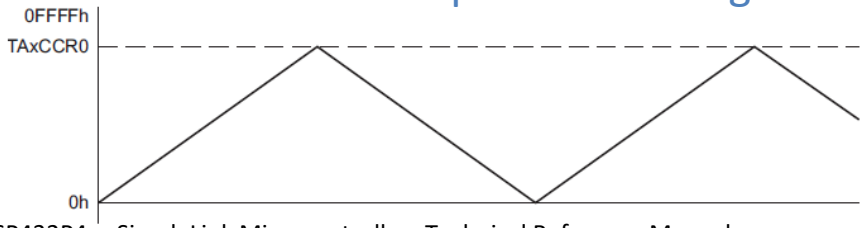
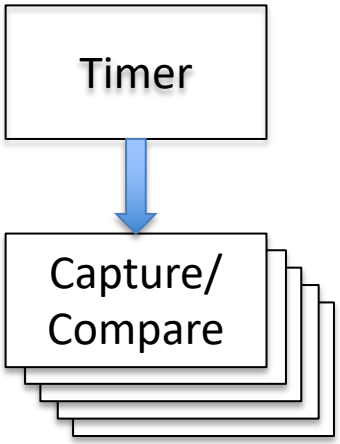


Diagram source: TI MSP432P4xx SimpleLink Microcontrollers Technical Reference Manual

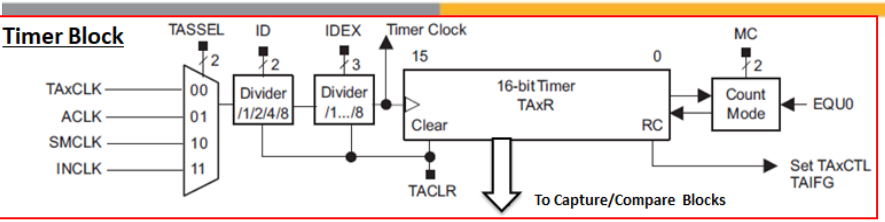
Timer_A Capture/Compare Blocks

Each timer drives five Capture/Compare blocks

- Each block supports two modes
  - Capture
  - Compare
- Capture Mode
  - Used to record events
  - Events sources: external pins or internal signals
  - When event occurs
    - Timer value is stored in register
    - Interrupt is generated
- Compare Mode
  - Generates interrupts at reaching desired timer value
  - Generates PWM (Pulse Width Modulation) output with various counting modes
    - Defines duty cycles and frequencies for control purposes, e.g., motor control



Timer_A Capture/Compare Block



Timer Outputs from Timer Block

Event Inputs

CCIyA
CCIyB
GND
VCC

CCIS
CM
logic
COV
SCS
Capture Mode
Timer Clock
Sync
CCI

15
0
TAxCCRy
Comparator y
EQUy

SCCI
Y
A
EN

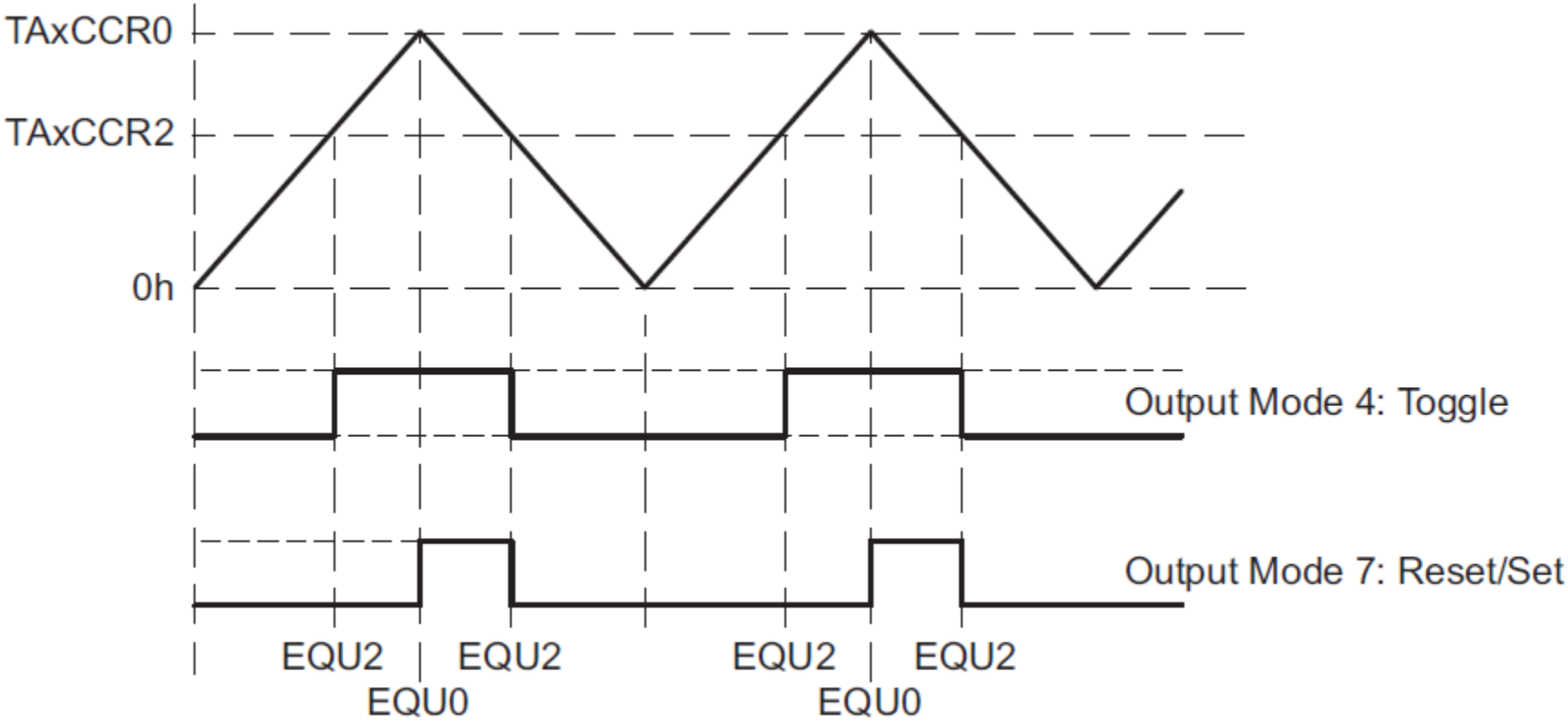
CAP
Interrupt
Set TAxCCRy CCIFG

OUT
EQU0
Output Unit
Timer Clock
D
Set
Q
Reset
OUTy Signal
Output Signal
POR
3
OUTMOD

Diagram source: TI MSP432P4xx SimpleLink Microcontrollers Technical Reference Manual

Timer_A Output Examples

- Timer in Up/Down counting mode
- Mode 4: Output is toggled when timer reaches TAxCCR2
- Mode 7: Output is reset when timer reaches TAxCCR2 and is set when reaches TAxCCR0



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