SJSU SAN JOSÉ STATE UNIVERSITY

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Real-Time Embedded System Co-Design
CMPE 146 Section 1
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Power Management

Motivation

There are many motivations to build low-power systems

- Many embedded systems are battery-powered
  - It would be very annoying if we need to often replace or charge the battery
  - In some systems, recharging is impossible or it is extremely hard to replace the battery
    - For examples, pacemaker, radio collar on an animal being tracked
- Some systems are powered by harvesting very limited amount of energy from the environment
  - Sun or room light
  - Movement of device
  - Body temperature
  - EM wave
- Good for the environment
  - Less demand on resources to provide the required energy
    - Electric grid for charging batteries
    - Materials to make the batteries
  - Also for systems with constant power source

Power Requirements

Vary from application to application

- Operational duty cycle
  - Many embedded applications spend most of the time waiting for something to happen
  - Some may require intense computation to provide quick response
    - Power consumption could be very high for only a short period of time
  - Some can tolerate longer response time
    - Computation can be slower
    - Power consumption can remain constant for a long period of time
- Size restriction
  - Bigger battery would provide longer lifetime
    - Perhaps reduces demand for extreme low consumption
- Power consumption limit
  - Preserving battery life may be the top priority where charging is not possible and size is very restrictive
- I/O requirements
  - Need to drive motors, relays, antennae, etc.

Power Metrics

- Active current
  - Usually measured in mA per MHz
    - MSP432 MCU is rated at 80 µA/MHz in active mode, i.e., 3.84 mA at 48 MHz
  - Mostly caused by dynamic power needed by the memories, peripherals and the processor
    - Proportional to the product of clock frequency and supply voltage squared
- Sleep mode current
  - Usually measured in µA or nA
    - MSP432 MCU can consume from 25 nA to 870 µA
  - Typically, most clock signals are stopped for the lowest power consumption and most peripherals are turned off
  - May be dominated by the leakage current in the transistors - the static power consumption
- Energy efficiency
  - Indicates how much work can be done with a limited amount of energy
  - Based on popular benchmarks
    - Dhrystone (DMIPS/mW)
    - CoreMark (CoreMark/mW)

Power Metrics (cont'd)

- Wake-up latency
  - Usually measured in number of clock cycles
  - The time from a hardware request (e.g., peripheral interrupt) to the time the processor resumes program execution

Low-Power Hardware Features

- ARM embedded processors
  - Simple RISC core
    - Short pipeline, small instruction set, few advanced features
  - Less circuitry: fewer transistors to consume power
  - Better code density
    - More code in the same amount of memory
    - Reduces flash capacity requirement
- Flexible clock distribution system in the MCU
  - Peripherals can have dedicated clock signals of different types
- Variable clock frequency
  - Processor can run at a lower clock frequency to reduce active current
  - Processor can also run at higher frequency to finish tasks quicker and stay in sleep mode longer
- Low-power peripherals and memory
  - Can be individually powered down when not being used
  - Low-power mode to conserve energy (can draw only tens of nA of current)
  - Can be operational while the processor remains in sleep mode

Low-Power Hardware Features (cont'd)

- Integration of accelerators
  - Do specialized computations with dedicated logics
  - Energy-efficient and fast

Real-Time Power Control

- Power consumption of a CMOS circuit can be approximated as

$$P \approx \alpha\, C_L\, V_{DD}^2\, f$$

  where α is the switching activity, C_L is the load capacitance, V_{DD} is the supply voltage and f is the operating frequency
  - Therefore, in real time, we have two parameters V_{DD} and f to tweak
- Frequency adjustment
  - Put system to sleep; stop the clock when there is nothing to do
    - There is delay penalty when waking up
  - Slow down frequency when speed is not needed
    - Reduces active current
- Voltage adjustment
  - Turn off components when they are not needed
    - There is a delay penalty when need to turn them back on
    - Also reduces the leakage current
  - Reduce supply voltage when higher frequencies are not needed
    - Gate propagation delay will increase slightly

Power Operating Modes

- Various power modes available for optimization of power in different execution conditions
- On the ARM Cortex-M processors, two main power operating modes
  - Active Mode (AM): Program execution is possible
    - Processor can go to sleep (Low Power Mode below) under program control
  - Low Power Mode (LPM): Program execution is suspended
    - Program execution resumes (in Active Mode) upon receiving interrupts or events
- AM is further divided to six sub-modes
  - Based on a combination of voltage regulator used, voltage and frequency settings

Power Operating Modes (cont'd)

- LPM is further divided to 12 sub-modes in 3 general categories
  - Sleep
    - Processor clock is stopped
    - Processor is not active but peripherals are
    - Flash memory and SRAM are active
  - Deep Sleep
    - Peripheral functionality is reduced or totally disabled
    - No high-frequency clock, low frequency may be totally disabled as well
    - Flash memory is disabled
    - SRAM not configured for retention are disabled
  - Stop or Shut Down
    - Processor and almost all peripherals are powered down
    - Flash memory is powered down
    - Only Bank 0 of SRAM is under retention or powered down as well

Sleep Mode Hardware Support

Using various power operating modes can save power substantially. However, the following functional units and design are needed

- Clock System (CS)
- State Retention Power Gating (SRPG) design
- Wake-up Interrupt Controller (WIC)
- Power Supply System (PSS)
- Power Control Manager (PCM)

State Retention Power Gating (SRPG)

- In Deep Sleep Mode, elements holding system state information must be remained powered on
  - Processor can resume operation from the point where the program was suspended
  - Non-state holding devices and logic can be completely powered down
    - Leakage current is greatly reduced because most parts of logic are powered down

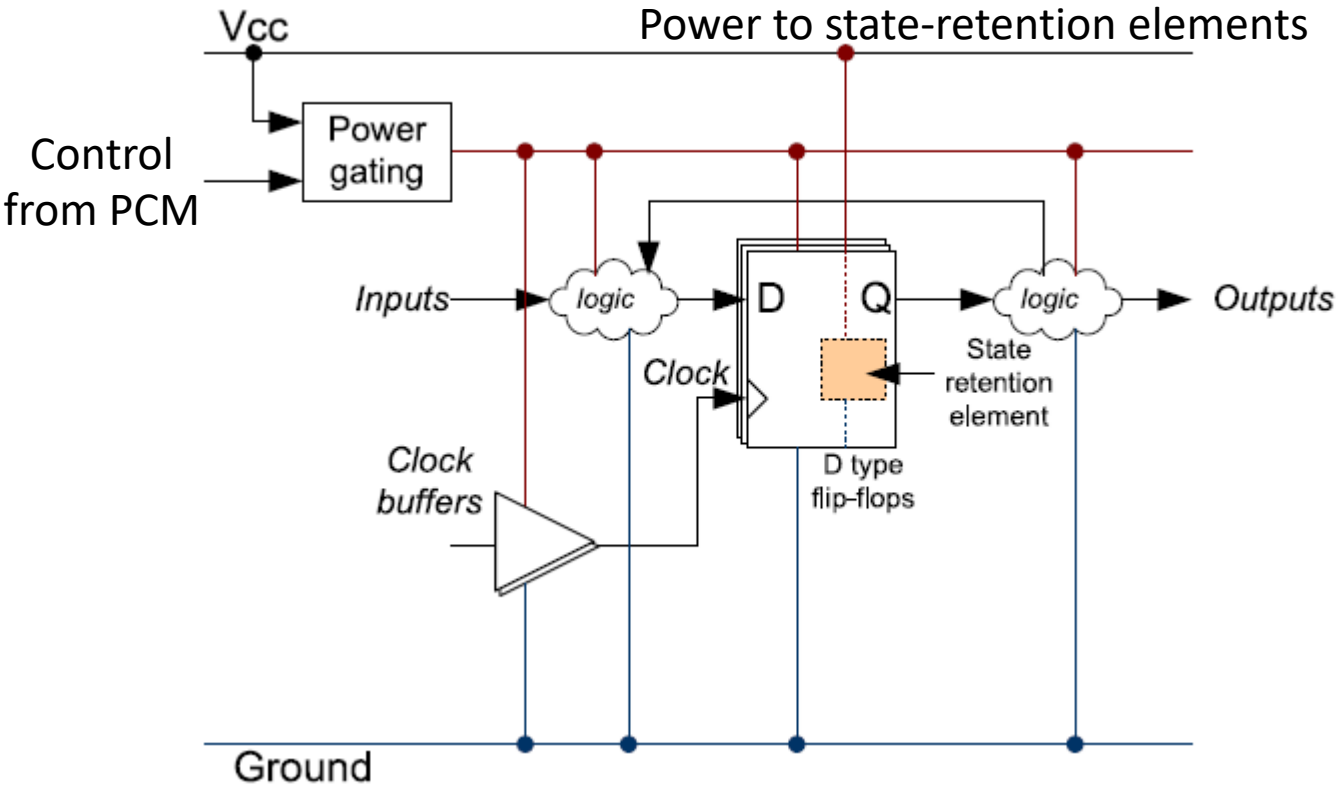
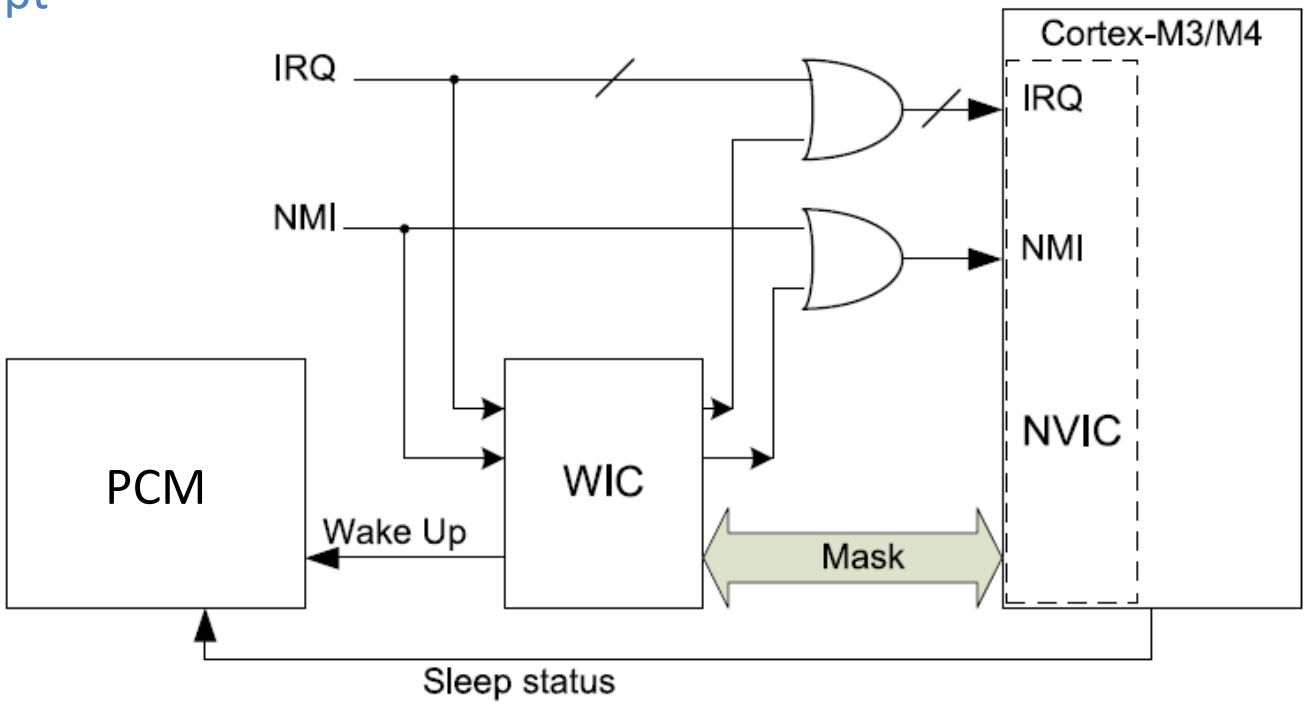


Diagram source: Joseph Yiu, The Definitive Guide to ARM Cortex-M3 and Cortex-M4 Processors, third edition, Elsevier, Inc., 2014.

Wake-up Interrupt Controller (WIC)

- In Deep Sleep Mode, when all the clock signals to the processor are stopped, the NVIC (Nested Vectored Interrupt Controller) cannot detect incoming interrupt requests
- WIC (a very small unit) detects the interrupt signal and signal PCM (Power Control Manager)
- PCM restores clocks and voltage to wake up processor to service the interrupt



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Power Supply System (PSS)

- Regulates device supply voltage V_{CC} to V_{CORE}
  - V_{CORE} is applied to processor, memories and digital modules
    - Programmable to allow power savings
  - V_{CC} is applied to I/Os and analog modules
    - Monitored by the Supply Voltage Supervisor and Monitor for High Side (SVSMH) unit (High side refers to the input side of the regulator)
    - Detection of power on or off condition through the VCC Detect (VCCDET) unit
- Wide input supply voltage range: 1.62 V to 3.7 V
  - 1.65 V is required at start up

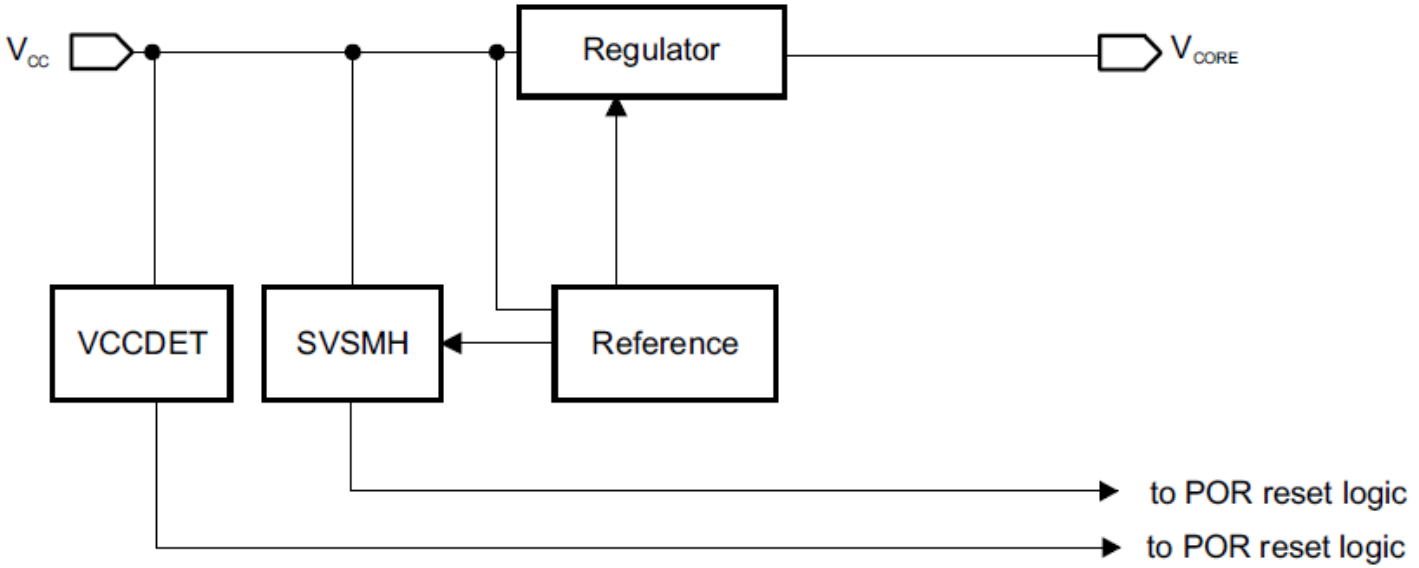
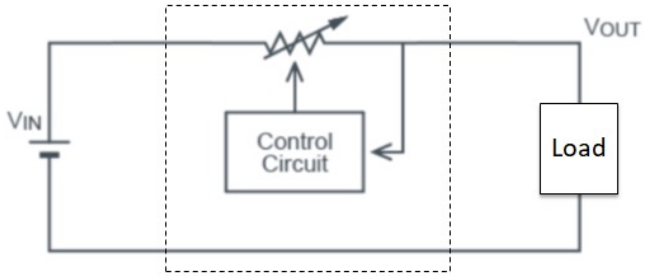


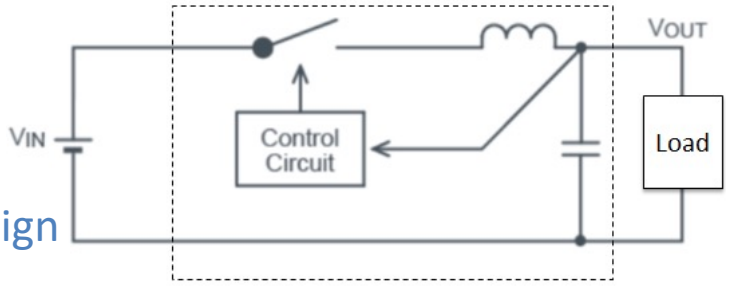
Diagram source: TI MSP432P4xx SimpleLink Microcontrollers Technical Reference Manual

PSS Voltage Regulator

Actually contains two regulators connected in parallel



- Low-DropOut (LDO)
  - Linear regulator
    - Adjusts output voltage with resistive element
  - The default one
  - Advantages: Cost-effective, relatively noise-free output due to no switching component, faster to ramp up and down
  - Disadvantage: Less efficient - might not be ideal for power savings because load current is same as supply current
- DC-to-DC (DCDC)
  - Switching regulator
    - Adjusts output voltage with energy-storing elements (inductor and capacitor) and rapidly turning on and off source voltage
  - As a secondary or optional one
  - Advantage: More efficient compared to LDO
  - Disadvantages: More noise, more complicated design



PSS Voltage Regulator (cont'd)

- A lower V_{CORE} reduces power consumption
- V_{CC} can be regulated to V_{CORE} as one of two levels
  - A lower voltage labeled as VCORE0
    - 1.2 V (typical) on MSP432
  - A higher voltage labeled as VCORE1
    - 1.4 V (typical) on MSP432