SJSU SAN JOSÉ STATE UNIVERSITY

Charles W. Davidson College of Engineering

Department of Computer Engineering

Real-Time Embedded System
Co-Design
CMPE 146 Section 1
Fall 2024

Memory

Memory Map

MSP432 Cortex-M4 MCU Memory Map

- 4-GB space (32-bit addressing)
- 8 zones: 512 MB each
- Two memory zones
  - Code
  - SRAM

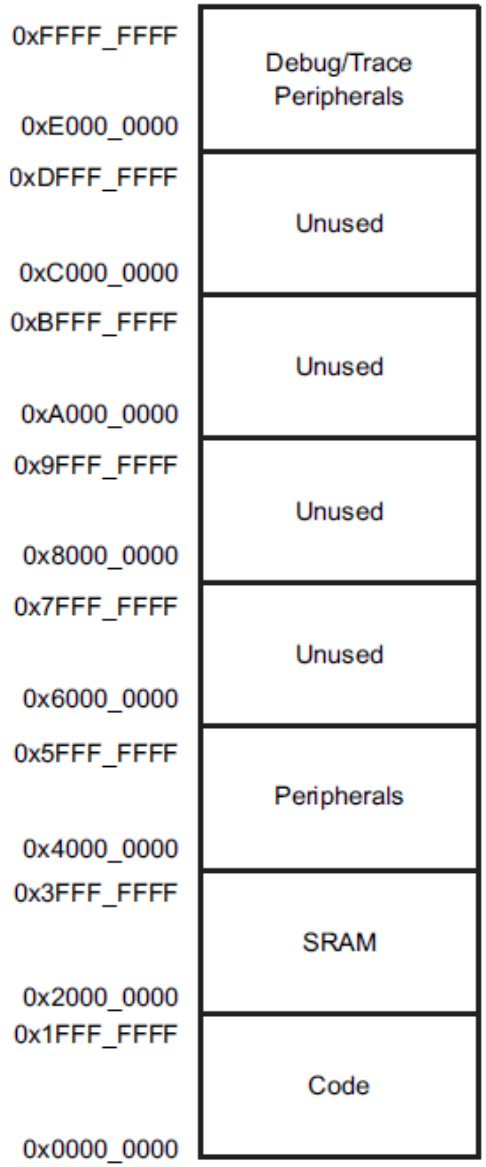
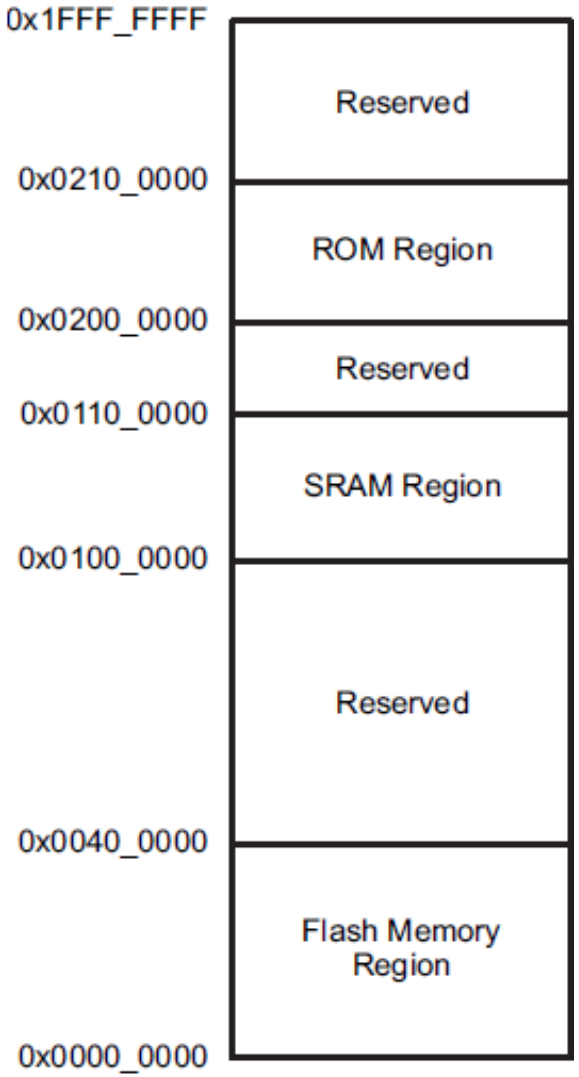


Diagram source: TI MSP432P401R, MSP432P401M SimpleLink Mixed-Signal Microcontrollers Datasheet

Code Zone

- Total 512 MB
- Flash memory
  - 4-MB space
- SRAM
  - 1-MB space
- ROM
  - 1-MB space



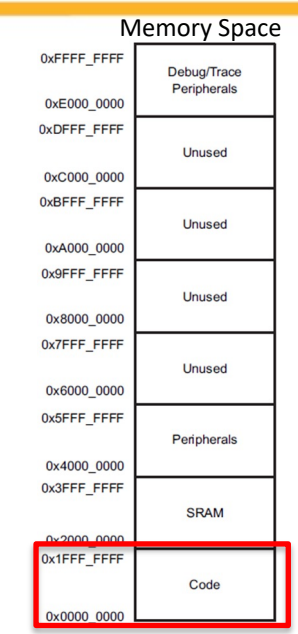
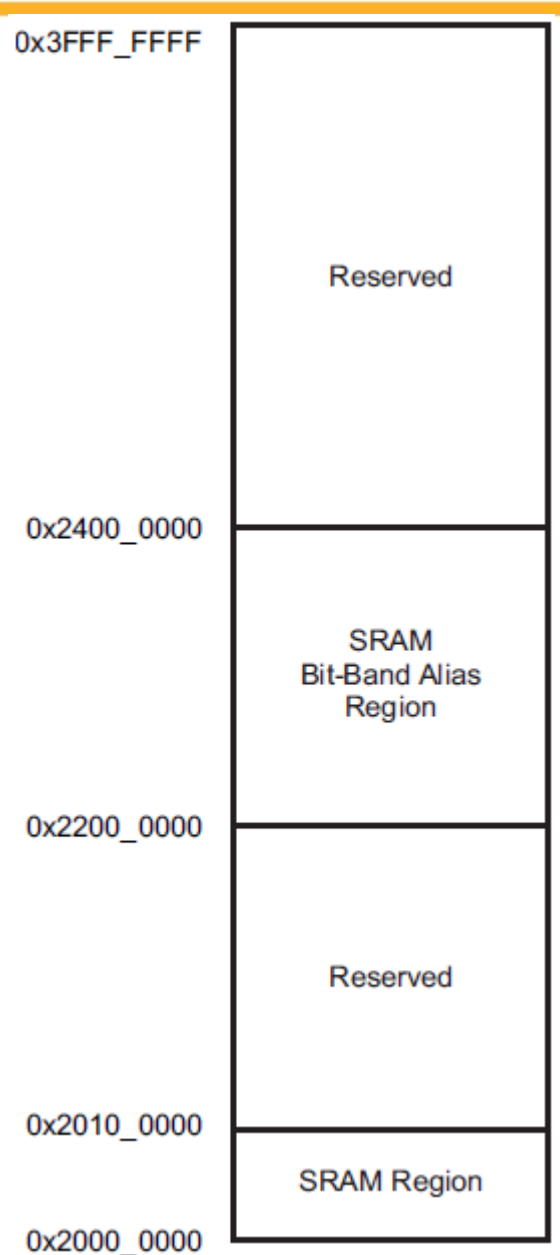


Diagram source: TI MSP432P401R, MSP432P401M SimpleLink Mixed-Signal Microcontrollers Datasheet

SRAM Zone

- SRAM region
  - 1-MB space
- SRAM Bit-Band Alias Region
  - 32 MB



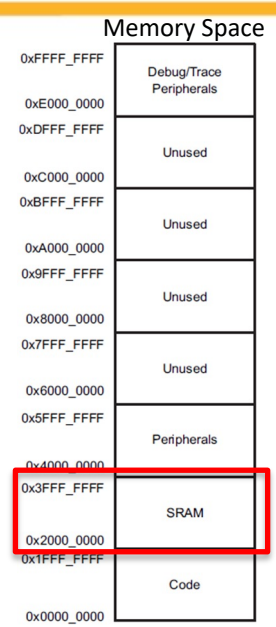


Diagram source: TI MSP432P401R, MSP432P401M SimpleLink Mixed-Signal Microcontrollers Datasheet

Memory Connections

Three buses for memory accesses

- ICODE
  - For instruction access
  - Code zone (flash, SRAM, ROM)
- DCODE
  - For data access
  - Code zone
- SBUS
  - SRAM zone
  - On-chip peripherals

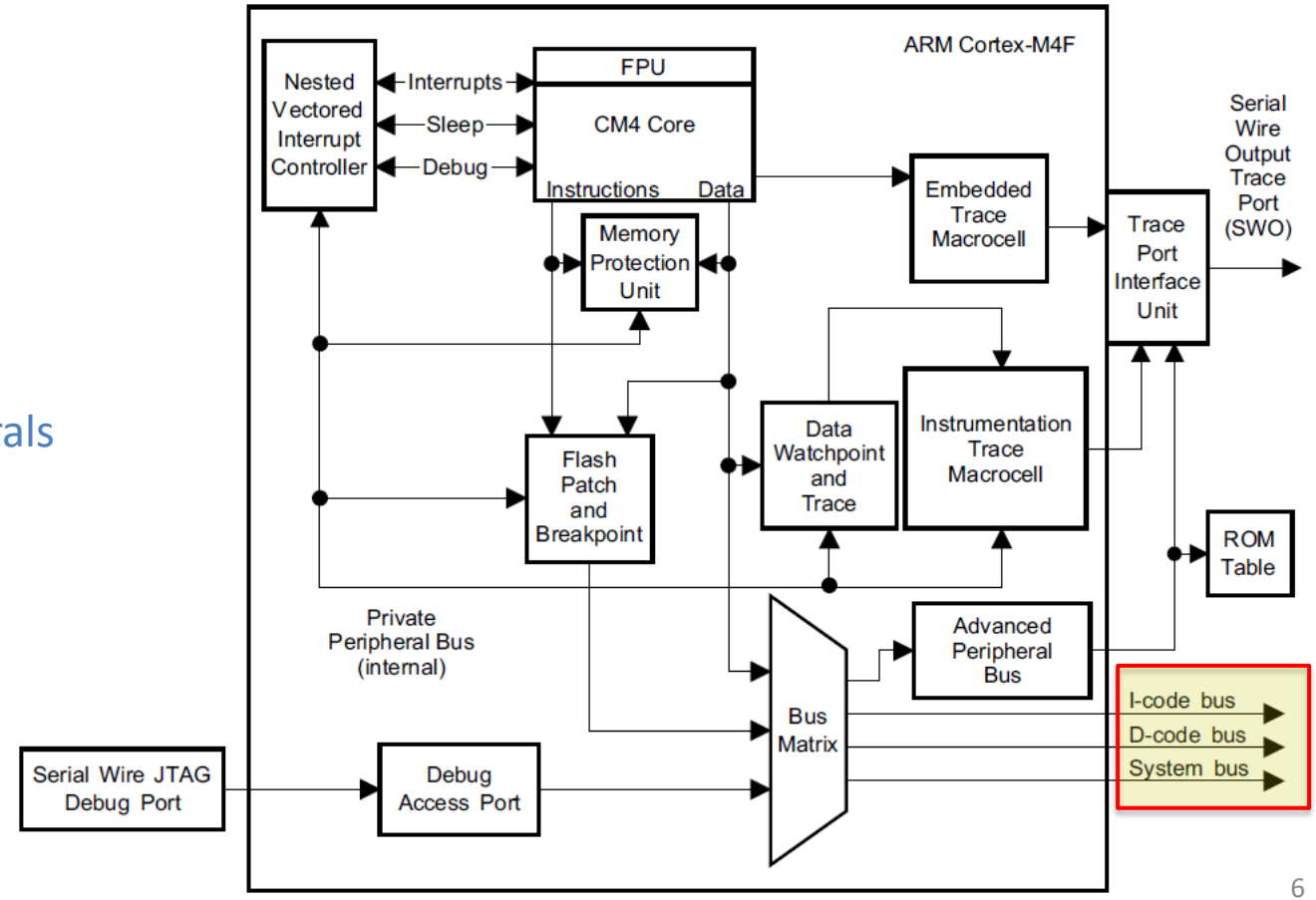
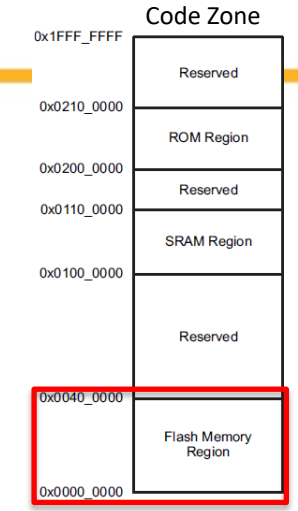


Diagram source: TI MSP432P4xx SimpleLink Microcontrollers Technical Reference Manual

MCU Flash Memory



- Low power consumption
  - Can be powered down or placed in a low-power mode
- Minimum of 20,000 write or erase cycles.
- 128-bits wide access
  - Each instruction fetch returns up to four 32-bit instructions (or up to eight 16-bit instructions)
- Physically divided into two subregions
  - Main Memory and Information Memory
    - Located in independent banks
    - Allows simultaneous operations
- Main Memory
  - 256 KB
  - 64 sectors of 4 KB each
    - Minimum erase granularity of 4KB (1 sector)
  - Two independent banks of 128 KB each
    - Allows simultaneous operations

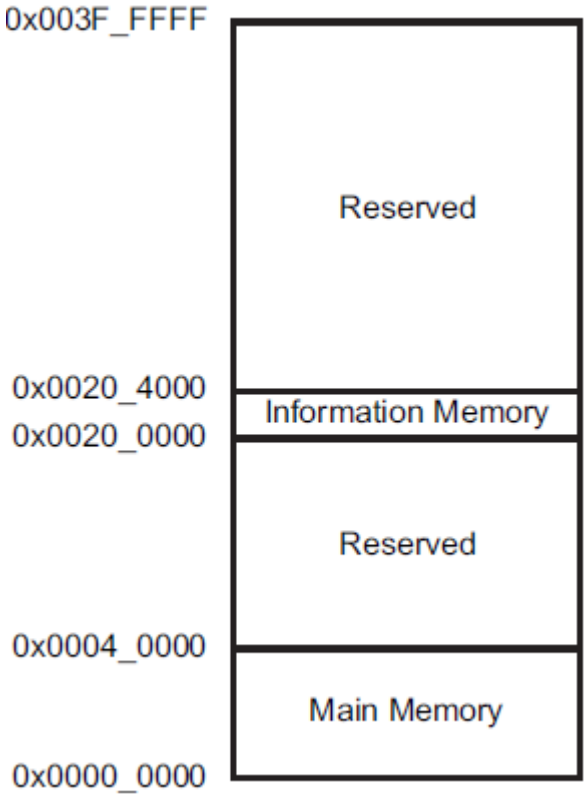


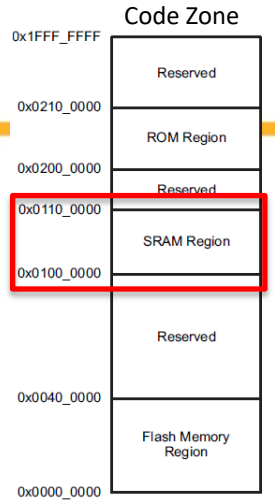
Diagram source: TI MSP432P401R, MSP432P401M SimpleLink Mixed-Signal Microcontrollers Datasheet

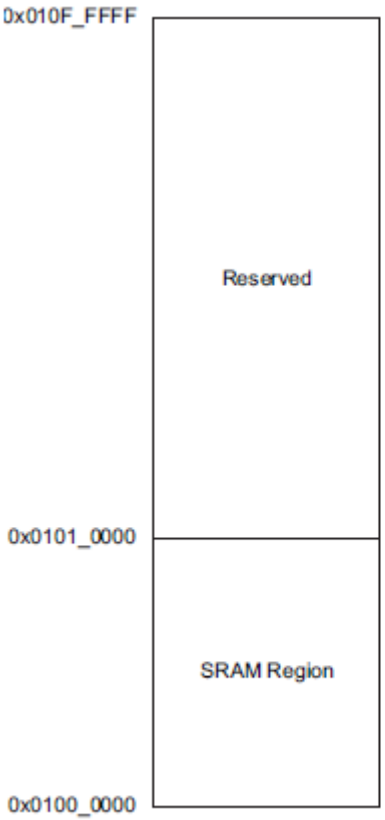
MCU Flash Memory (cont'd)

- Information Memory
  - 16 KB
  - Two banks of 8 KB each
    - 4 sectors of 4 KB each
  - Two sectors contain the bootloader (BSL)
  - One sector is for configuring the boot process
  - One sector contains the device descriptor (TLV)
    - Factory configured for protection against write and erase

MCU SRAM

- 1-MB space each in Code zone and SRAM zone
- MSP432P401x MCUs support
  - 64 KB in each zone
  - Memory aliased in both zones
- Low power consumption
  - Can be powered down or placed in a low-power mode
- Allows single-cycle execution of code
- Memory is divided into 8-K banks
  - For optimization of power consumption
    - Bank can be individually powered down
    - Normal operating current: 100-300 nA
    - Under-retention current: 30-35 nA
  - Entire bank can be enabled/disabled
    - Exception: Bank 0 cannot be disabled
    - Typically 4 µs to enable or disable





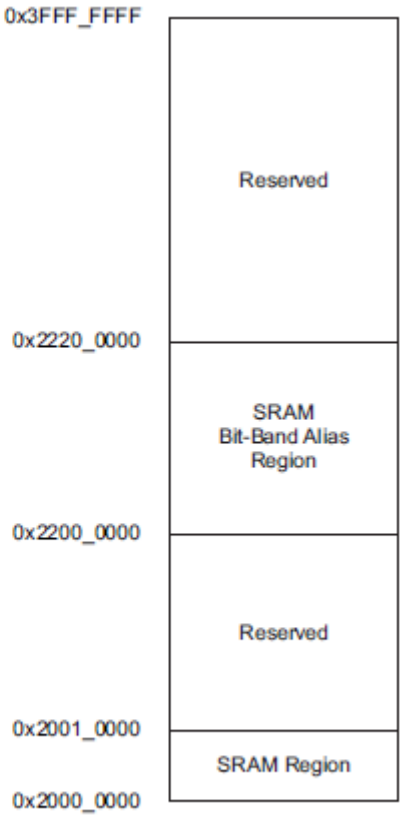
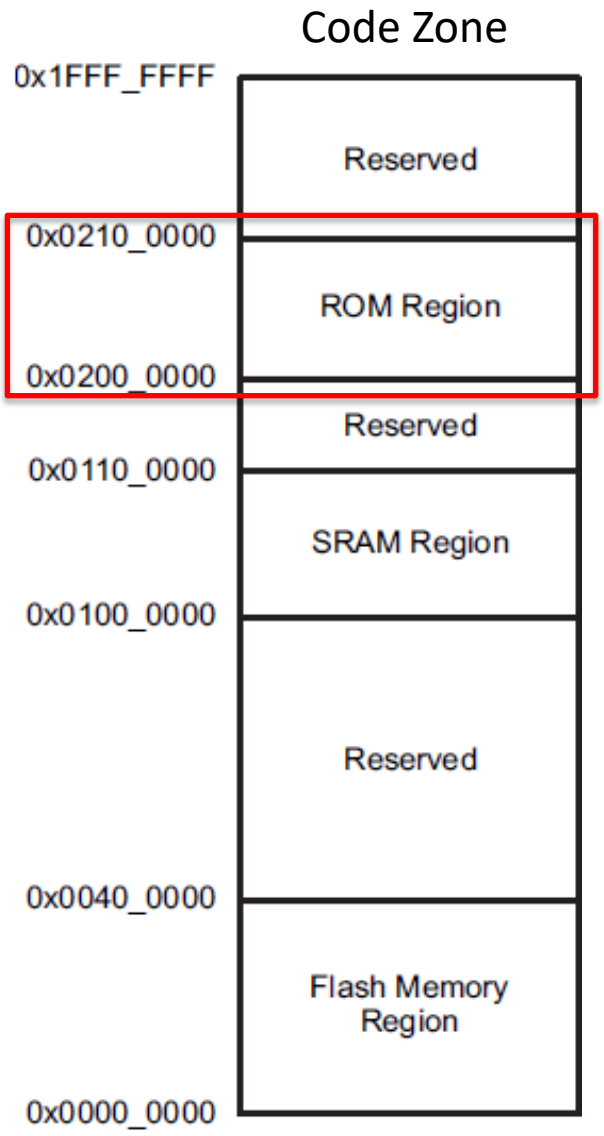


Diagram source: TI MSP432P401R, MSP432P401M SimpleLink Mixed-Signal Microcontrollers Datasheet

MCU ROM

- MSP432P401x MCUs support 32 KB of ROM
  - Total ROM region space is 1 MB
- Upper 30 KB contains driver libraries
- Lower 2KB reserved for TI internal purposes
  - Accesses to this space returns an error response
- Returns an error response for any write accesses



Flash Memory Basics

- Non-volatile
- Operations
  - Read
  - Write or program
  - Erase
- Read
  - Allows random access
  - Likes ordinary memory, in byte (8 bits), half-word (16 bits) or word (32 bits)
  - Latency: tens of ns
- Write or program
  - Allows random access
  - Like ordinary memory, in byte (8 bits), half-word (16 bits) or word (32 bits)
  - Memory cell (holds one bit of information) must be 1 in order to be changed (to 0)
  - Once it is written a 0, it cannot be changed to a 1 without the erase process
  - Number of write cycles in a specific block is limited, ~100K
  - Need elevated voltage (~5 V) to write
  - Slower than read, in µs

Flash Memory Basics (cont'd)

- Erase
  - Must be done on an entire block, typically tens of KB
    - Changes the entire block to 1's
  - A very slow process, in milliseconds
  - Number of erase operations is limited, ~100K
  - Need high voltage (~12 V) to erase

MCU Flash Controller

Main features of the on-chip controller

- Internal programming voltage (higher than supply voltage) generation
- Byte, word (4 bytes), full-word (16 bytes), and burst (up to 4x16 bytes) programmable
- Low-power operation
- Optimized read operations
  - For program instruction fetches or data reads
- Configurable write and erase protection per sector (4 KB)

- Recommended to use TI DriverLib for flash operations (program, erase)
  - Programs portable across various TI MCUs
    - Detailed operation parameters may vary from device to device
  - ROM stores DriverLib
- Common basic operations
  - Read, Program, Erase, Program-and-Erase Protection

MCU Flash Read

- Configurable in terms of the number of memory bus cycles for read command
  - For high-frequency system clock, can insert wait states accordingly
- Read Buffering
  - Flash is organized with a line size of 128 bits
  - When buffering is enabled, always reads an entire 128-bit line
    - Suitable for accessing contiguous program instructions and data items
    - No wait state if data is already in the read buffer
    - Wait states only asserted when crossing line boundary
  - Disabled by default for lower power consumption
  - Each bank (Main or Information) has independent settings
    - Flexibility for instruction and data accesses

MCU Flash Program (Write)

- Set the targeted bits to the value 0
- DriverLib programming functions are required to be executed from either SRAM or ROM
  - Due to the verification requirements
- Master interrupts are disabled throughout the execution of this function
  - Due to the complexity of the verification requirements

MCU Flash Erase

- Set the flash memory values to 1's
- Smallest block size to erase is one sector (4 KB)
- Master interrupts are disabled throughout the operation
- Two modes
  - Sector Erase
    - Erase one sector, can be in the Main or Information bank
  - Mass Erase
    - Erase all unprotected sectors in both banks

MCU Flash Program-and-Erase Protection

- Protect sectors from inadvertent program or erase operations
- One PROT (program and erase protection) bit per sector (4 KB)
  - Set to 1: sector becomes read-only
  - Any program or erase commands on the sector are ignored
- Example of one good usage: Erase half (128 KB) of Main memory (256 KB)
  - Steps to take:
    - Set the PROT bits of the targeted 128 KB to 0
    - Set all other PROT bits for Main and Information memory to 1
    - Initiate a mass erase operation
  - Erase the targeted 128 KB is one erase cycle
    - Save time and energy overhead