SJSU SAN JOSÉ STATE UNIVERSITY

Charles W. Davidson College of Engineering

Department of Computer Engineering

Real-Time Embedded System Co-Design
CMPE 146 Section 1
Fall 2024

MCU Digital Interfaces

I2C

- Inter-Integrated Circuit (I^2C or I2C or IIC)
- Synchronous, half-duplex, NRZ
- Commonly used to connect components within an embedded system
- Two open-drain lines (lines normally high, any device can pull them low)
  - SCL: Serial Clock Line
  - SDA: Serial DAta line
- Multiple-master-multiple-slave architecture

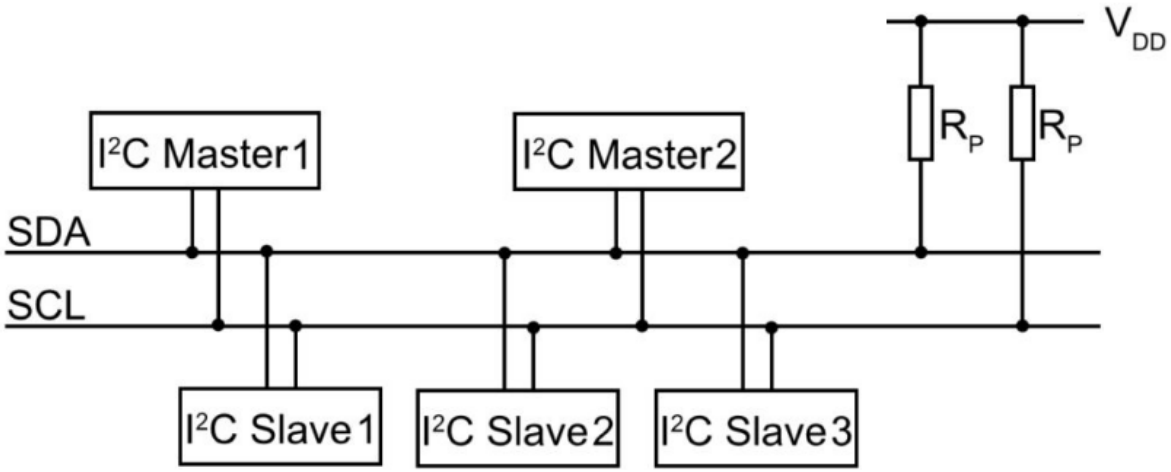


Diagram source: https://stackoverflow.com/tags/i2c/info

I2C - Transaction

- A bus transaction begins with a START condition and ends with a STOP condition
- Beginning of transaction (START condition)
  - Master drives SDA low while SCL remains high
  - All devices on the bus go into listening mode
- Ending of transaction (STOP condition)
  - Master stops generating clock (not driving SCL) and then releases SDA

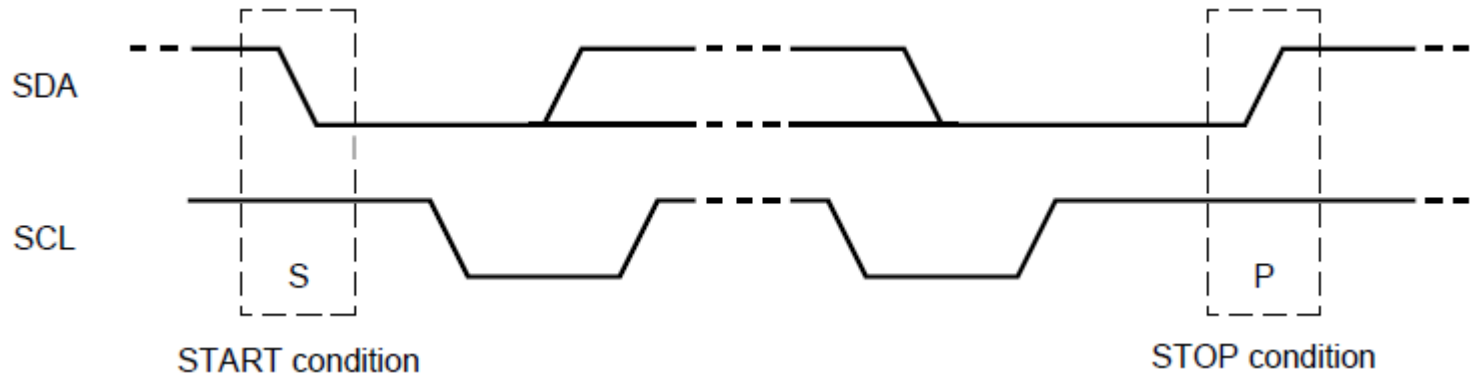


Diagram source: https://www.nxp.com/docs/en/user-guide/UM10204.pdf

I2C- Data Validity

- Data on SDA must be stable during the High period of SCL
- Data can only change when SCL line is Low

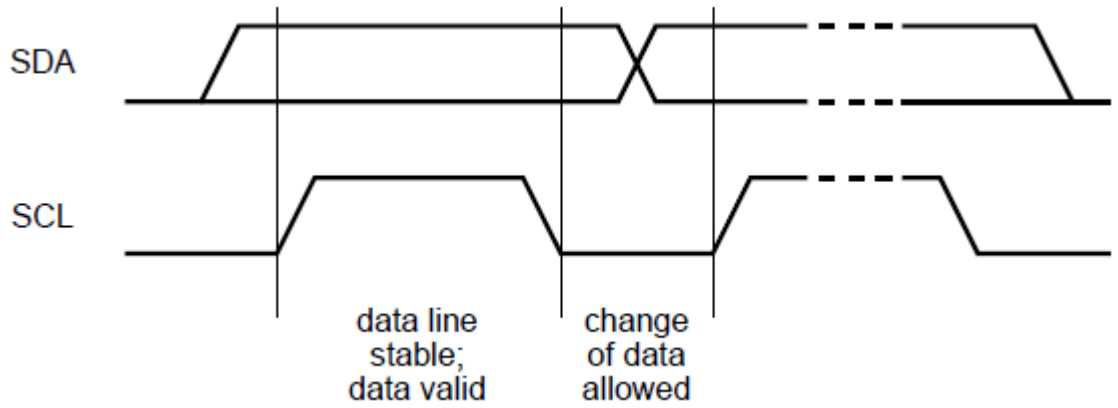


Diagram source: https://www.nxp.com/docs/en/user-guide/UM10204.pdf

I2C - Arbitration

- Who becomes the bus master?
  - Each attempting master initiates the START condition as if it's the bus master
  - Compares what it drives SDA and what it reads from SDA
  - Whoever sees a mismatch drops back to slave mode
  - Winning master goes on to complete its transaction

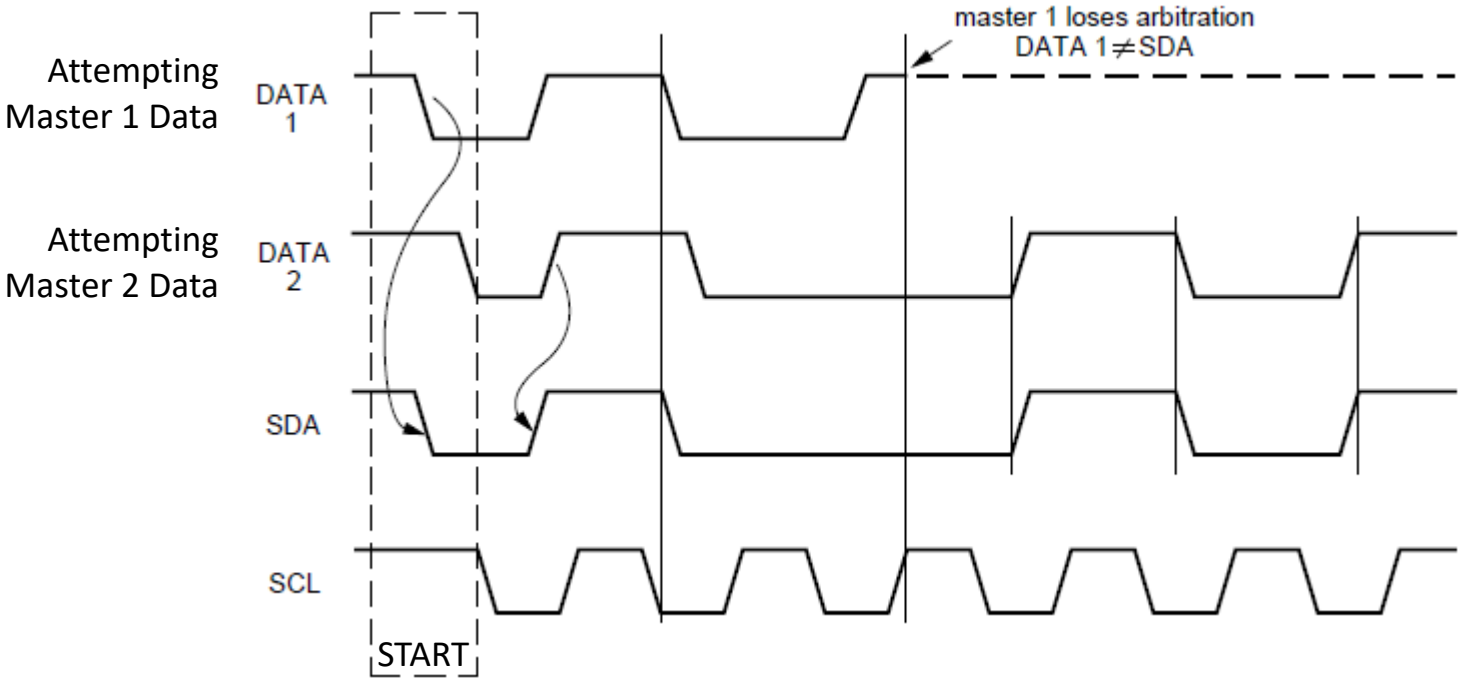


Diagram source: https://www.nxp.com/docs/en/user-guide/UM10204.pdf

I2C - Protocol

- Basic bus transaction
  - After START condition, a 7-bit target address is sent
  - Followed by a data direction bit; zero means write
  - Followed by an ACK bit sent by slave
  - If master writes, master sends data, followed by slave ACK
  - If master reads, slave sends data, followed by master ACK

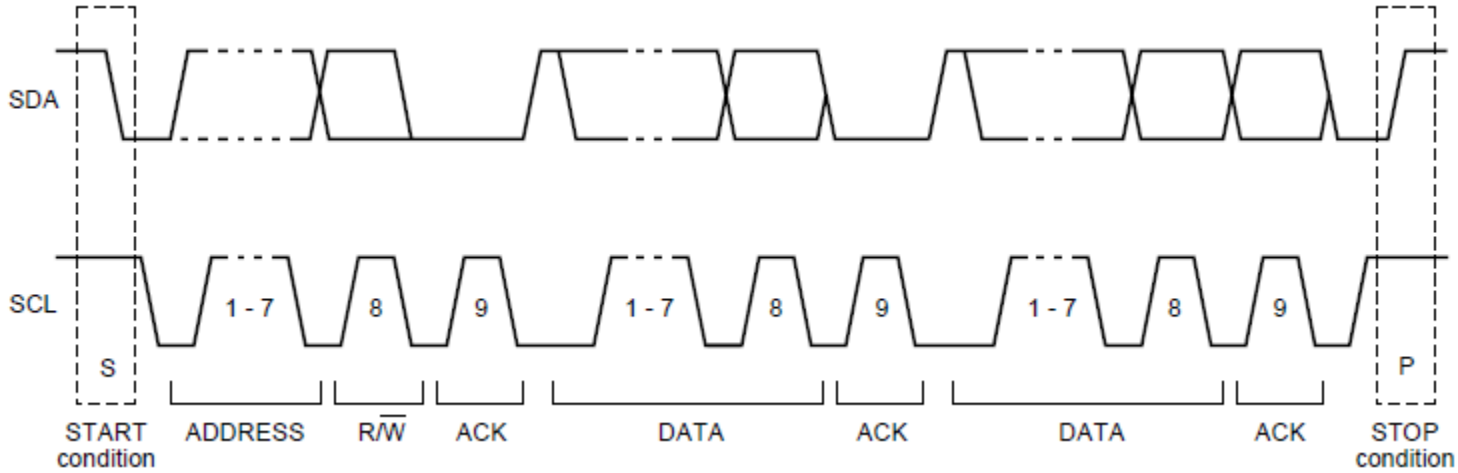
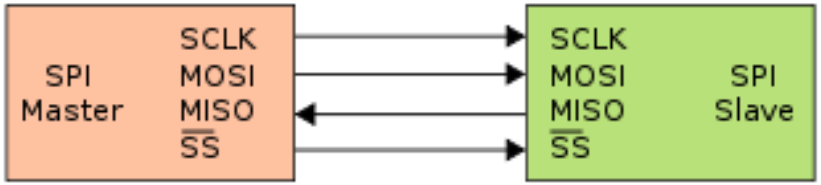


Diagram source: https://www.nxp.com/docs/en/user-guide/UM10204.pdf

SPI

- Serial Peripheral Interface (SPI)
- Synchronous, full-duplex, NRZ
- Commonly used to connect components within an embedded system
- Single-master-multiple-slave architecture

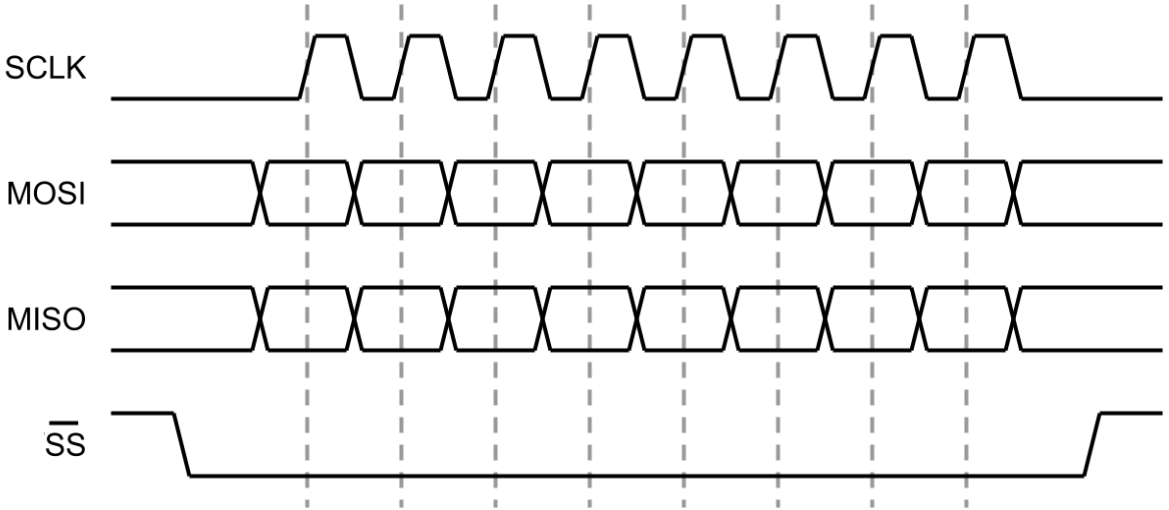


- Four signals
  - SCLK: Serial Clock (output from master)
  - MOSI: Master Output Slave Input (output from master)
  - MISO: Master Input Slave Output (output from slave)
  - SS: Slave Select (active low, output from master)

Diagram source: https://en.wikipedia.org/wiki/Serial_Peripheral_Interface

SPI - Timing and Configuration

- Timing



- Basic multiple-slave configuration
  - Dedicated SS signals for slaves

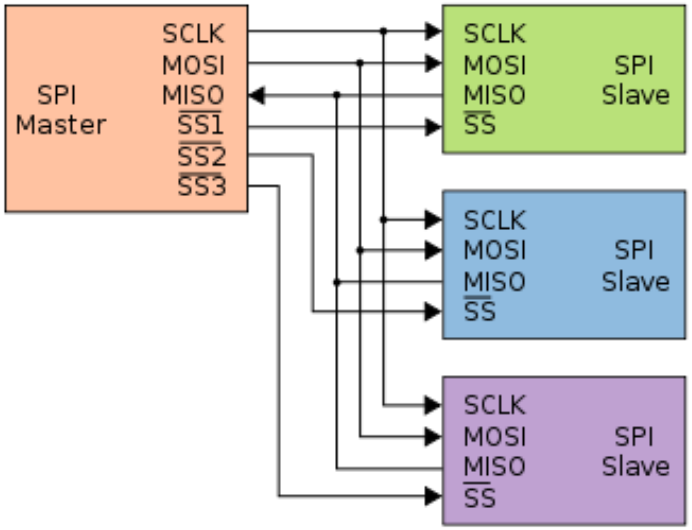


Diagram sources: https://articles.saleae.com/logic-analyzers/spi-vs-i2c-protocol-differences-and-things-to-consider, https://en.wikipedia.org/wiki/Serial_Peripheral_Interface

SPI and I2C Comparison

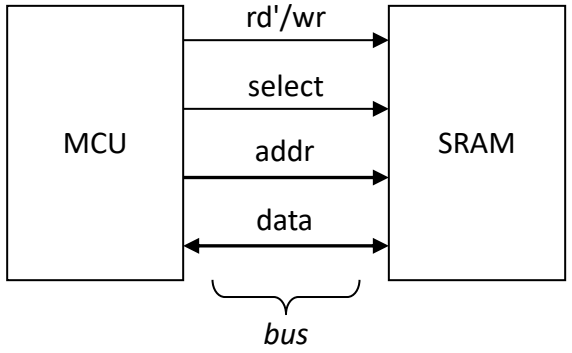
SPI	I2C
Single-master-multiple-slave	Multiple-master-multiple-slave
Full-duplex	Half-duplex
Four wires (or more)	Two wires
No acknowledgment on data received	ACK on each byte received
No device ID, dedicated select signal - Not flexible to add off-board devices	Device address ID in the header - Easy to add off-board devices
No strict frame definition	Frame is well defined
No bus arbitration	Arbitration needed
Flexible clock speed - Only master drives the signal. Can accommodate fast and slow devices	Less flexible clock speed - All master devices can drive the signal. Arbitration requires agreed clock frequency

MCU Parallel Interfaces

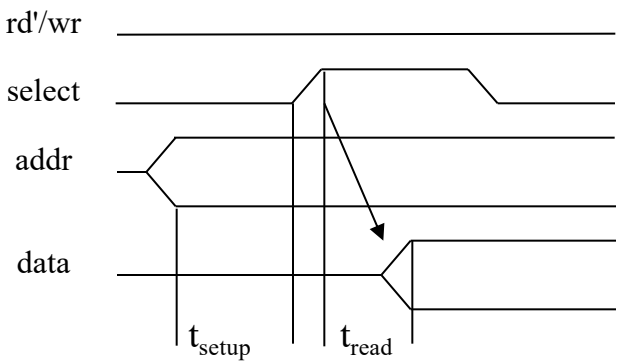
- Commonly used over short distances on a printed circuit board
- Provide smallest delay and highest bandwidth
- Processors process data natively in multiple-bit forms (byte, word, etc.)
  - No overheads of serialization and deserialization as in serial interfaces
  - But require a lot more pins and real estate
- We focus on common interfaces to off-chip memory on board
  - SRAM
  - DRAM

SRAM Interface

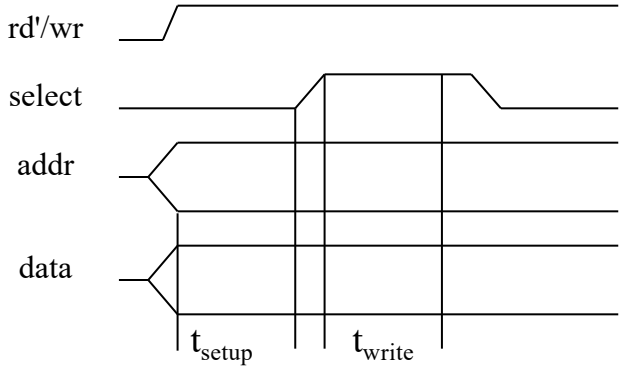
- Main signals
  - Address
  - Data (bi-directional)
  - Read/Write
  - Chip Select



- Read timing

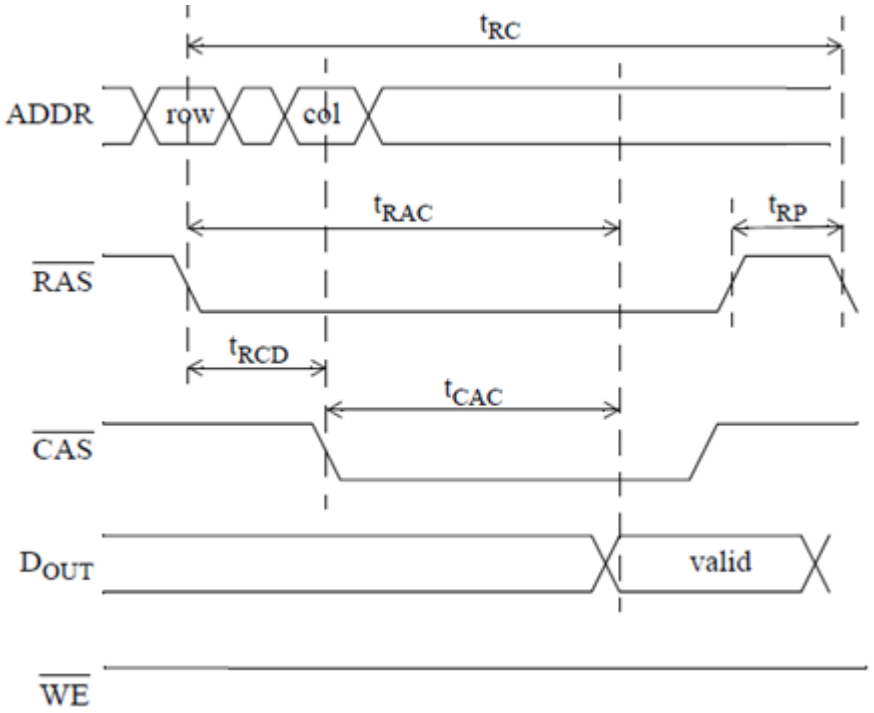


- Write timing



DRAM Interface

- Main signals
  - Address (row and column multiplexed, to save pins)
  - Row Address Strobe (RAS)
    - Select a row in the memory cell array
  - Column Address Strobe (CAS)
    - Select a column in the memory cell array
  - Data (bi-directional)
  - Read/Write
- Read timing
  - t_{RAC}: Read access time
  - t_{RC}: Read cycle time
    - Longer than t_{RAC}



DRAM Interface (cont'd)

- Write timing
  - WE' and D_{IN} must hold longer enough before CAS' goes low