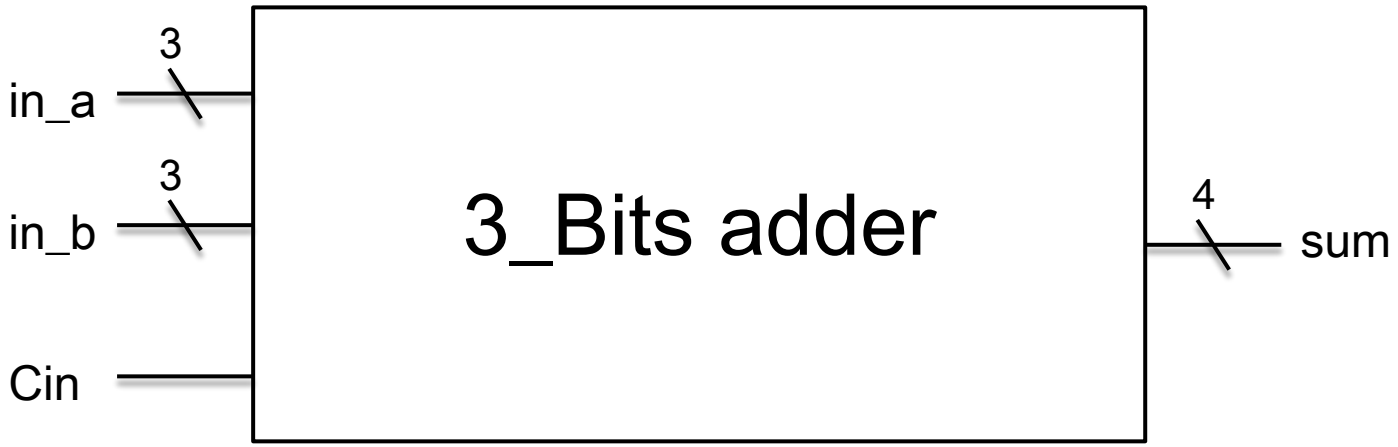
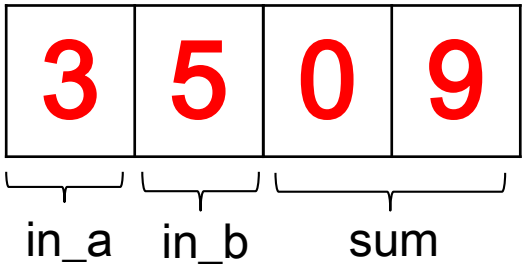
Lab 2a : 7-Seg and Switch

- Design a 3_Bits adder and demo the result on DE0 board with seven-segment display.

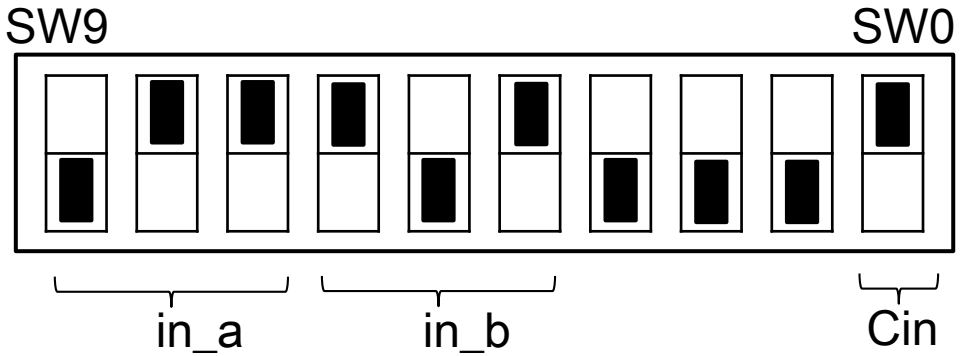


Lab 2a : 7-Seg and Switch



Decimal

$$\begin{array}{rr} & 3_{10} \\ & 5_{10} \\ +) & 1_{10} \\ \hline & 9_{10} \end{array}$$



Binary

$$\begin{array}{rr} & 011_2 \\ & 101_2 \\ +) & 001_2 \\ \hline & 1001_2 \end{array}$$

Lab 2 : 7-Seg and Switch

- Inputs :
  - Use 7 switches on the board to represent the value of the inputs in_a, in_b and Cin.
  - SW9-SW7 for in_a, and SW6-SW4 for in_b, SW0 for Cin.
- Outputs :
  - Show the decimal value of the inputs and outputs on seven-segment display.
  - HEX3 for in_a, HEX2 for in_b, and HEX1-HEX0 for sum.

Pins-Switches

Signal Name	FPGA Pin No.	Description
SW[9]	PIN_D2	Slide Switch[9]
SW[8]	PIN_E4	Slide Switch[8]
SW[7]	PIN_E3	Slide Switch[7]
SW[6]	PIN_H7	Slide Switch[6]
SW[5]	PIN_J7	Slide Switch[5]
SW[4]	PIN_G5	Slide Switch[4]
SW[3]	PIN_G4	Slide Switch[3]
SW[2]	PIN_H6	Slide Switch[2]
SW[1]	PIN_H5	Slide Switch[1]
SW[0]	PIN_J6	Slide Switch[0]

Pins-7Seg

Signal Name	FPGA Pin No.	Signal Name	FPGA Pin No.	Signal Name	FPGA Pin No.	Signal Name	FPGA Pin No.
HEX3_DP	PIN_G16	HEX2_DP	PIN_A18	HEX1_DP	PIN_B15	HEX0_DP	PIN_D13
HEX3_D[6]	PIN_G15	HEX2_D[6]	PIN_F14	HEX1_D[6]	PIN_A15	HEX0_D[6]	PIN_F13
HEX3_D[5]	PIN_D19	HEX2_D[5]	PIN_B17	HEX1_D[5]	PIN_E14	HEX0_D[5]	PIN_F12
HEX3_D[4]	PIN_C19	HEX2_D[4]	PIN_A17	HEX1_D[4]	PIN_B14	HEX0_D[4]	PIN_G12
HEX3_D[3]	PIN_B19	HEX2_D[3]	PIN_E15	HEX1_D[3]	PIN_A14	HEX0_D[3]	PIN_H13
HEX3_D[2]	PIN_A19	HEX2_D[2]	PIN_B16	HEX1_D[2]	PIN_C13	HEX0_D[2]	PIN_H12
HEX3_D[1]	PIN_F15	HEX2_D[1]	PIN_A16	HEX1_D[1]	PIN_B13	HEX0_D[1]	PIN_F11
HEX3_D[0]	PIN_B18	HEX2_D[0]	PIN_D15	HEX1_D[0]	PIN_A13	HEX0_D[0]	PIN_E11

HEX3 HEX2 HEX1 HEX0