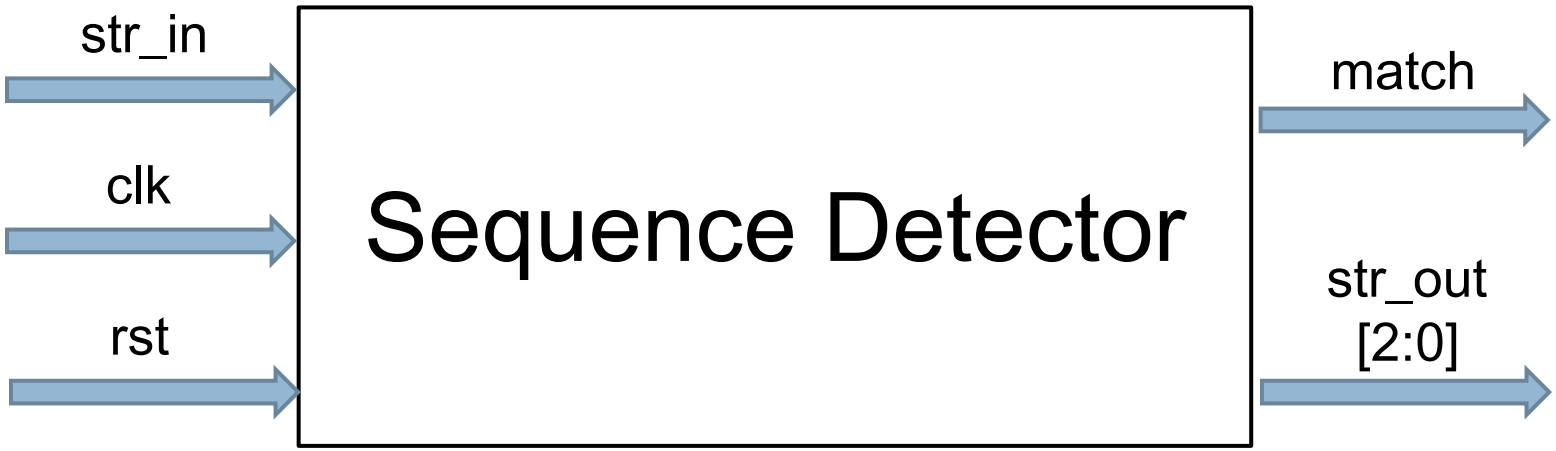
Homework4: Sequence Detector

- Implement a sequence detector that can search the string “110” using Verilog HDL
- str_in (serial input) ; str_out (parallel output)

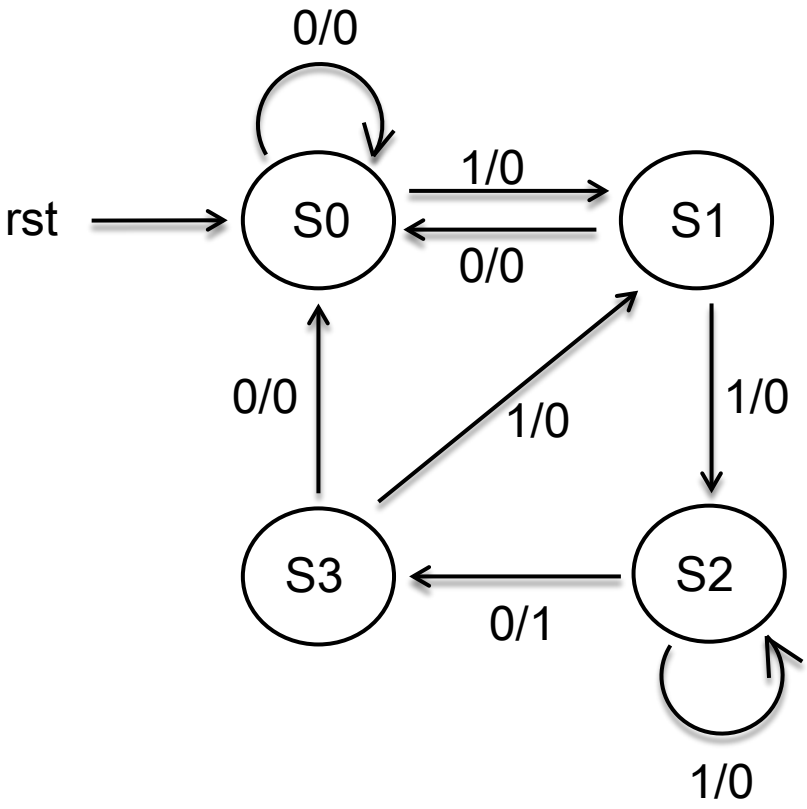
Ex: str_out : 100; match : 0

str_out : 110; match : 1



Homework4: Sequence Detector

- State Transition Diagram



Homework4: Sequence Detector


```
module sequence_detector(str_out, match, rst, str_in, clk);
    input    clk, rst, str_in, ;
    output  [2:0]str_out;
    output  match;
    ……
endmodule
```