Document Number: MMG3H21NT1 Rev. 2, 9/2012

2, 5,2512

√RoHS

Heterojunction Bipolar Transistor Technology (InGaP HBT)

Broadband High Linearity Amplifier

The MMG3H21NT1 is a General Purpose Amplifier that is internally input matched and internally output matched. It is designed for a broad range of Class A, small-signal, high linearity, general purpose applications. It is suitable for applications with frequencies from 0 to 6000 MHz such as Cellular, PCS, BWA, WLL, PHS, CATV, VHF, UHF, UMTS and general small-signal RF.

Features

- Frequency: 0-6000 MHzP1dB: 20.5 dBm @ 900 MHz
- · Small-Signal Gain: 19.3 dB @ 900 MHz
- Third Order Output Intercept Point: 37 dBm @ 900 MHz
- · Single 5 Volt Supply
- · Active Bias
- · Internally Matched to 50 Ohms
- Cost-effective SOT-89 Surface Mount Package
- In Tape and Reel. T1 Suffix = 1,000 Units, 12 mm Tape Width, 7 inch Reel.

MMG3H21NT1

0-6000 MHz, 19.3 dB 20.5 dBm InGaP HBT



CASE 2142-01 SOT-89 PLASTIC

Table 1. Typical Performance (1)

Characteristic	Symbol	900 MHz	2140 MHz	3500 MHz	Unit
Small-Signal Gain (S21)	G _p	19.3	16	14	dB
Input Return Loss (S11)	IRL	-18	-25	-20	dB
Output Return Loss (S22)	ORL	-10	-6	-8	dB
Power Output @1dB Compression	P1dB	20.5	19.8	17.7	dBm
Third Order Output Intercept Point	OIP3	37	34	31	dBm

^{1.} $V_{CC} = 5$ Vdc, $T_A = 25^{\circ}C$, 50 ohm system, in Freescale application circuit.

Table 2. Maximum Ratings

Rating	Symbol	Value	Unit
Supply Voltage	V _{CC}	7	V
Supply Current	I _{CC}	300	mA
RF Input Power	P _{in}	12	dBm
Storage Temperature Range	T _{stg}	-65 to +150	°C
Junction Temperature (2)	TJ	150	°C

For reliable operation, the junction temperature should not exceed 150°C.

Table 3. Thermal Characteristics

Characteristic	Symbol	Value ⁽³⁾	Unit
Thermal Resistance, Junction to Case Case Temperature 84°C, 5 Vdc, 90 mA, no RF applied	$R_{ heta JC}$	38.6	°C/W

3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to http://www.freescale.com/rf. Select Documentation/Application Notes - AN1955.



 $\textbf{Table 4. Electrical Characteristics} \ (V_{CC} = 5 \ \text{Vdc}, \ 900 \ \text{MHz}, \ T_{A} = 25^{\circ}\text{C}, \ 50 \ \text{ohm system, in Freescale Application Circuit})$

Characteristic	Symbol	Min	Тур	Max	Unit
Small-Signal Gain (S21)	G _p	18.3	19.3	_	dB
Input Return Loss (S11)	IRL	_	-18	_	dB
Output Return Loss (S22)	ORL	=	-10	_	dB
Power Output @ 1dB Compression	P1dB	=	20.5	_	dBm
Third Order Output Intercept Point	OIP3	=	37	_	dBm
Noise Figure	NF	=	5.5	_	dB
Supply Current (1)	I _{CC}	75	90	110	mA
Supply Voltage (1)	V _{CC}	_	5	_	V

^{1.} For reliable operation, the junction temperature should not exceed 150 $^{\circ}\text{C}.$

Table 5. Functional Pin Description

Pin Number	Pin Function
1	RF _{in}
2	Ground
3	RF _{out} /DC Supply

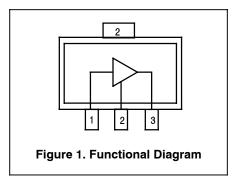


Table 6. ESD Protection Characteristics

Test Conditions/Test Methodology	Class
Human Body Model (per JESD 22-A114)	1C
Machine Model (per EIA/JESD 22-A115)	A
Charge Device Model (per JESD 22-C101)	IV

Table 7. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	1	260	°C

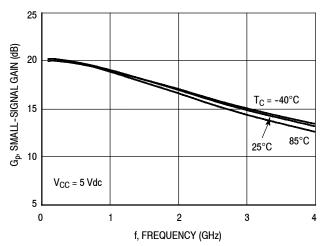


Figure 2. Small-Signal Gain (S21) versus Frequency

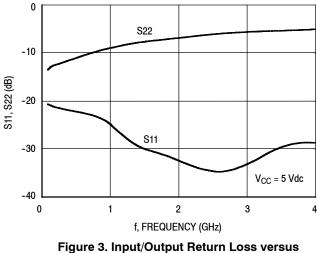


Figure 3. Input/Output Return Loss versus Frequency

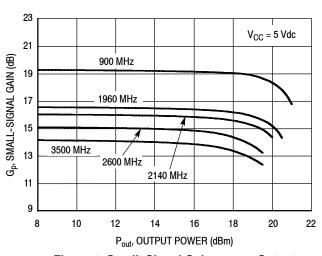


Figure 4. Small-Signal Gain versus Output Power

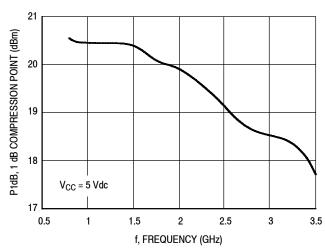


Figure 5. P1dB versus Frequency

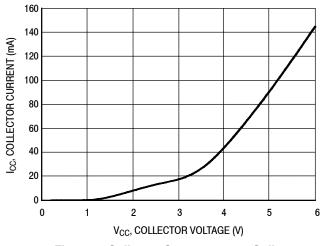


Figure 6. Collector Current versus Collector Voltage

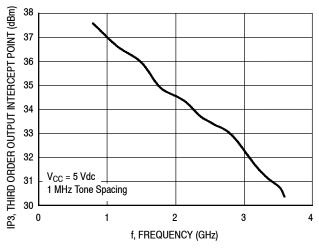


Figure 7. Third Order Output Intercept Point versus Frequency

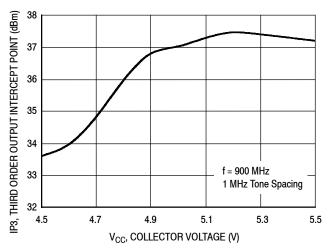


Figure 8. Third Order Output Intercept Point versus Collector Voltage

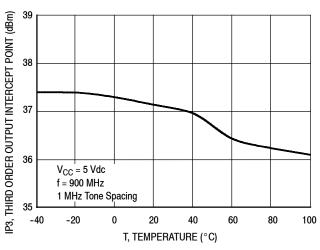


Figure 9. Third Order Output Intercept Point versus Case Temperature

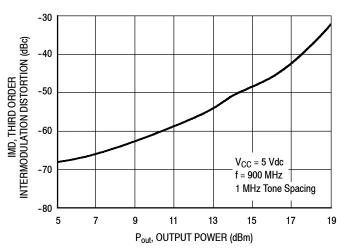
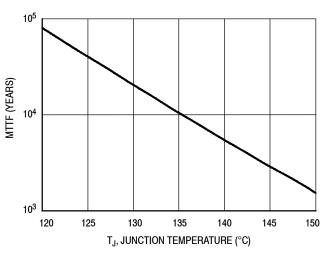


Figure 10. Third Order Intermodulation versus
Output Power



NOTE: The MTTF is calculated with V_{CC} = 5 Vdc, I_{CC} = 90 mA Figure 11. MTTF versus Junction Temperature

V_{CC} = 5 Vdc, f = 2140 MHz
Single-Carrier W-CDMA, 3.84 MHz Channel Bandwidth
Input Signal PAR = 8.5 dB @ 0.01% Probability on CCDF

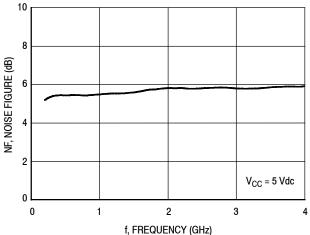


Figure 12. Noise Figure versus Frequency

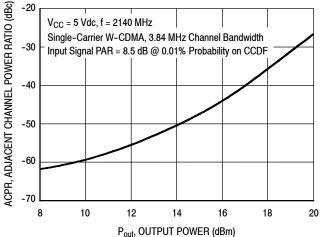


Figure 13. Single-Carrier W-CDMA Adjacent Channel Power Ratio versus Output Power

MMG3H21NT1

50 OHM APPLICATION CIRCUIT: 30-300 MHz

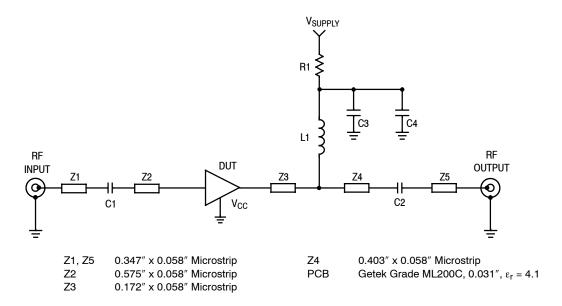
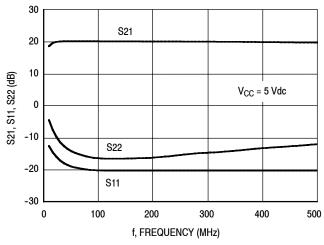


Figure 14. 50 Ohm Test Circuit Schematic



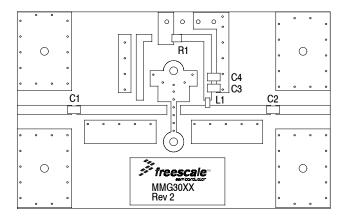


Figure 15. S21, S11 and S22 versus Frequency

Figure 16. 50 Ohm Test Circuit Component Layout

Table 8. 50 Ohm Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2, C3	0.1 μF Chip Capacitors	C0603C104J5RAC	Kemet
C4	1 μF Chip Capacitor	C0603C105J5RAC	Kemet
L1	470 nH Chip Inductor	BK2125HM471-T	Taiyo Yuden
R1	0 Ω Chip Resistor	ERJ3GEY0R00V	Panasonic

50 OHM APPLICATION CIRCUIT: 300-3600 MHz

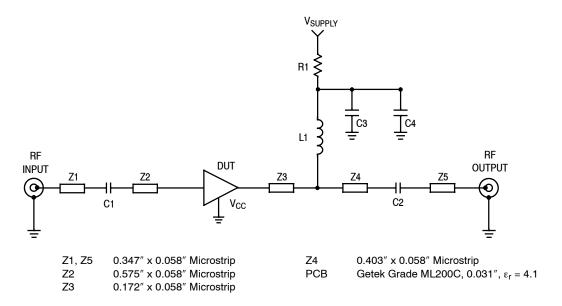


Figure 17. 50 Ohm Test Circuit Schematic

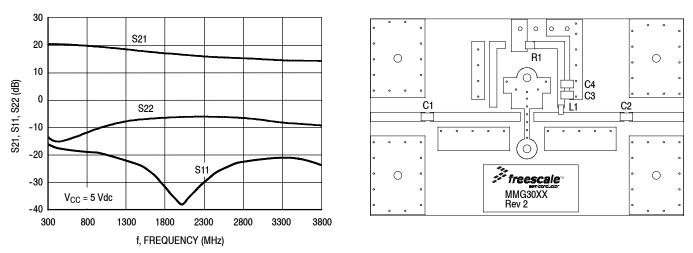


Figure 18. S21, S11 and S22 versus Frequency

Figure 19. 50 Ohm Test Circuit Component Layout

Table 9. 50 Ohm Test Circuit Component Designations and Values

Part	Description	Part Number	Manufacturer
C1, C2	150 pF Chip Capacitors	C0603C104J5RAC	Kemet
C3	0.1 μF Chip Capacitor	C0603C105J5RAC	Kemet
C4	1 μF Chip Capacitor	C0603C105J5RAC	Kemet
L1	56 nH Chip Inductor	HK160856NJ-T	Taiyo Yuden
R1	0 Ω Chip Resistor	ERJ3GEY0R00V	Panasonic

Table 10. Common Source S-Parameters (V_{CC} = 5 Vdc, T_A = 25°C, 50 Ohm System)

f	s	11	S	21	S	12	s	22
MHz	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ ¢
100	0.093	176.9	10.209	175.9	0.0561	0.4	0.214	-7.4
150	0.090	165.2	10.269	171.9	0.0565	-1.4	0.234	-17.0
200	0.087	162.0	10.228	169.1	0.0565	-2.0	0.241	-23.4
250	0.085	157.6	10.184	166.4	0.0563	-2.5	0.246	-29.9
300	0.084	155.6	10.141	163.7	0.0563	-3.0	0.249	-35.4
350	0.082	150.2	10.080	161.1	0.0561	-3.4	0.260	-40.9
400	0.081	147.6	10.025	158.4	0.0561	-3.8	0.265	-46.5
450	0.080	143.7	9.955	155.8	0.0559	-4.3	0.272	-50.9
500	0.078	139.6	9.884	153.3	0.0559	-4.5	0.281	-55.7
550	0.078	136.5	9.815	150.7	0.0557	-5.1	0.289	-60.7
600	0.076	131.9	9.729	148.2	0.0555	-5.3	0.297	-64.6
650	0.075	127.5	9.645	145.6	0.0553	-5.9	0.306	-69.2
700	0.074	124.7	9.556	143.1	0.0552	-6.2	0.315	-73.0
750	0.074	121.7	9.465	140.7	0.0550	-6.5	0.323	-77.0
800	0.071	118.2	9.365	138.2	0.0548	-6.8	0.329	-80.8
850	0.071	116.4	9.267	135.9	0.0548	-7.0	0.337	-84.5
900	0.068	113.1	9.168	133.5	0.0545	-7.3	0.348	-87.9
950	0.067	111.2	9.059	131.1	0.0543	-7.6	0.353	-91.3
1000	0.064	109.8	8.966	128.8	0.0543	-7.8	0.361	-94.5
1050	0.055	113.6	8.884	126.5	0.0542	-8.2	0.360	-98.5
1100	0.050	107.1	8.779	124.3	0.0543	-8.3	0.370	-101.2
1150	0.046	101.8	8.676	122.1	0.0543	-8.5	0.378	-103.2
1200	0.043	95.4	8.572	120.0	0.0542	-8.6	0.385	-105.6
1250	0.040	86.3	8.459	117.8	0.0542	-8.9	0.394	-107.9
1300	0.037	79.4	8.354	115.8	0.0541	-9.1	0.397	-110.1
1350	0.035	72.3	8.255	113.7	0.0541	-9.3	0.404	-112.2
1400	0.034	64.0	8.152	111.7	0.0540	-9.3	0.409	-114.5
1450	0.032	57.1	8.061	109.6	0.0540	-9.5	0.414	-116.7
1500	0.031	51.1	7.962	107.6	0.0541	-9.8	0.417	-118.6
1550	0.031	44.3	7.860	105.6	0.0541	-10.0	0.422	-121.1
1600	0.031	37.9	7.767	103.6	0.0542	-10.0	0.426	-123.3
1650	0.030	33.0	7.675	101.6	0.0541	-10.3	0.428	-125.5
1700	0.030	28.6	7.586	99.7	0.0542	-10.6	0.433	-127.9
1750	0.029	22.7	7.501	97.7	0.0543	-10.7	0.436	-130.0
1800	0.028	21.9	7.414	95.7	0.0545	-11.1	0.440	-132.5
1850	0.028	18.7	7.327	93.7	0.0545	-11.4	0.443	-134.9
1900	0.026	16.5	7.236	91.8	0.0546	-11.5	0.447	-137.3
1950	0.025	19.0	7.144	89.8	0.0547	-11.8	0.452	-139.7
2000	0.025	17.3	7.057	87.9	0.0548	-12.2	0.455	-142.2
2050	0.023	18.5	6.966	86.0	0.0549	-12.4	0.459	-144.5
2100	0.023	22.9	6.876	84.1	0.0551	-12.8	0.463	-146.9
2150	0.022	23.0	6.789	82.2	0.0552	-13.0	0.469	-149.1
2200	0.021	27.2	6.698	80.3	0.0553	-13.4	0.474	-151.4
2250	0.021	29.4	6.611	78.5	0.0555	-13.7	0.478	-153.4
2300	0.020	31.4	6.526	76.7	0.0557	-14.0	0.482	-155.4

(continued)

Table 10. Common Source S-Parameters (V_{CC} = 5 Vdc, T_A = 25 $^{\circ}C$, 50 Ohm System) (continued)

f	S-	11	S	21	S	12	s	22
MHz	S ₁₁	∠ φ	S ₂₁	∠ φ	S ₁₂	∠ φ	S ₂₂	∠ φ
2350	0.019	35.6	6.440	74.9	0.0558	-14.3	0.487	-157.5
2400	0.020	39.7	6.356	73.1	0.0560	-14.6	0.490	-159.5
2450	0.019	42.0	6.276	71.4	0.0561	-15.0	0.494	-161.4
2500	0.019	48.6	6.196	69.7	0.0563	-15.2	0.499	-163.1
2550	0.018	52.4	6.121	68.0	0.0564	-15.6	0.502	-164.9
2600	0.018	59.8	6.047	66.3	0.0567	-16.0	0.506	-166.6
2650	0.018	66.3	5.974	64.6	0.0568	-16.3	0.509	-168.4
2700	0.018	73.3	5.903	62.9	0.0570	-16.6	0.514	-170.1
2750	0.019	81.4	5.832	61.3	0.0572	-16.9	0.516	-171.7
2800	0.019	86.0	5.769	59.7	0.0575	-17.2	0.518	-173.4
2850	0.020	93.6	5.706	58.1	0.0578	-17.5	0.522	-174.8
2900	0.021	101.3	5.642	56.4	0.0581	-17.8	0.521	-176.5
2950	0.021	107.6	5.581	54.8	0.0584	-18.2	0.524	-177.8
3000	0.022	113.4	5.520	53.3	0.0587	-18.5	0.526	-179.3
3050	0.023	120.3	5.461	51.7	0.0592	-19.0	0.529	179.1
3100	0.023	127.4	5.407	50.1	0.0595	-19.1	0.532	177.9
3150	0.024	134.5	5.357	48.5	0.0600	-19.6	0.533	176.5
3200	0.026	139.1	5.299	47.0	0.0603	-20.1	0.536	175.2
3250	0.028	145.9	5.250	45.4	0.0606	-20.5	0.537	173.8
3300	0.030	149.0	5.198	43.8	0.0610	-21.1	0.537	172.3
3350	0.030	155.3	5.144	42.3	0.0613	-21.6	0.538	171.2
3400	0.032	157.4	5.096	40.8	0.0617	-22.0	0.540	169.9
3450	0.033	162.3	5.050	39.2	0.0620	-22.5	0.541	168.6
3500	0.034	167.0	5.004	37.7	0.0625	-22.9	0.542	167.3
3550	0.035	169.1	4.956	36.1	0.0629	-23.5	0.543	166.1
3600	0.035	171.2	4.911	34.6	0.0633	-23.9	0.546	164.6
3650	0.037	172.3	4.864	33.0	0.0637	-24.6	0.546	163.3
3700	0.037	173.3	4.817	31.5	0.0641	-25.1	0.549	162.1
3750	0.037	172.4	4.771	30.0	0.0644	-25.5	0.551	160.7
3800	0.038	171.4	4.724	28.4	0.0647	-26.3	0.551	159.2
3850	0.037	170.9	4.679	26.9	0.0652	-26.7	0.553	157.8
3900	0.037	169.3	4.635	25.4	0.0655	-27.4	0.557	156.3
3950	0.037	166.8	4.589	23.9	0.0659	-28.0	0.559	154.6
4000	0.037	161.6	4.543	22.3	0.0662	-28.6	0.561	153.3

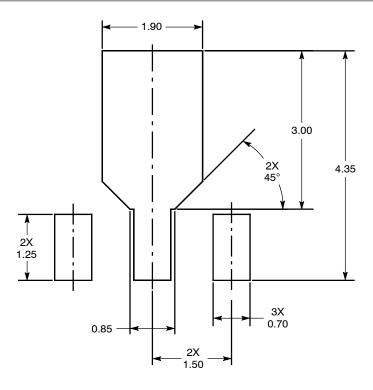
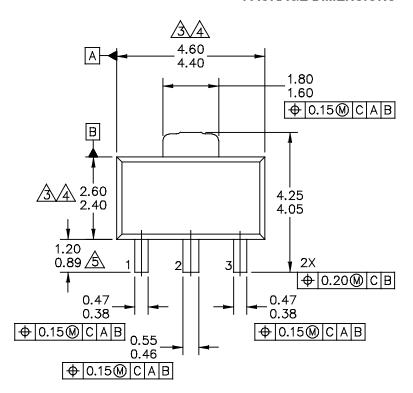


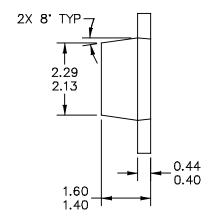
Figure 20. PCB Pad Layout for SOT-89A

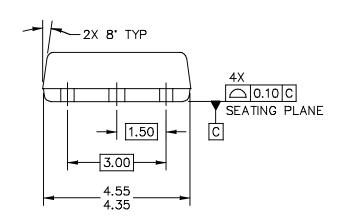


Figure 21. Product Marking

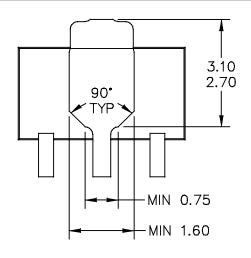
PACKAGE DIMENSIONS







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TITLE:	DOCUMENT NO): 98ASA00241D	REV: 0	
SOT-89A, 3 LEAD	•	CASE NUMBER	R: 2142–01	15 JUL 2010
4.5 X 2.5 PKG, 1.5 MM	PIICH	STANDARD: NO	N-JEDEC	



BOTTOM VIEW

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		CASE NUMBER: 2142-01		15 JUL 2010
4.5 X 2.5 PKG, 1.5 MM	PIICH	STANDARD: NO	N-JEDEC	

NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M 1994.
- 2. ALL DIMENSIONS ARE IN MILLIMETERS.



DIMENSIONS DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.5 MM PER END. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.5 MM PER SIDE.



DIMENSION ARE DETERMINED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.

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TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.

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TITLE: SOT-89A, 3 LEAD, 4.5 X 2.5 PKG, 1.5 MM PITCH		DOCUMENT NO: 98ASA00241D		REV: 0
		CASE NUMBER: 2142-01		15 JUL 2010
		STANDARD: NON-JEDEC		

MMG3H21NT1

PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers
- AN3100: General Purpose Amplifier and MMIC Biasing

Software

.s2p File

Development Tools

· Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the "Part Number" link. Go to the Software & Tools tab on the part's Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Apr. 2008	Initial Release of Data Sheet
1	Jan. 2011	Corrected temperature at which ThetaJC is measured from 25°C to 84°C and added "no RF applied" to Thermal Characteristics table to indicate that thermal characterization is performed under DC test with no RF signal applied, p. 1
		Removed I _{CC} bias callout from applicable graphs as bias is not a controlled value, p. 4-7
		Removed I _{CC} bias callout from Table 10, Common Source S-Parameters heading as bias is not a controlled value, 9-10
		Added .s2p file and Printed Circuit Boards availability to Software and Tools, p. 14
2	Sept. 2012	Replaced the PCB Pad Layout drawing, the package isometric and mechanical outline for Case 1514-02 (SOT-89) with Case 2142-01 (SOT-89) as a result of the device transfer from a Freescale wafer fab to an external GaAs wafer fab and new assembly site. The new assembly and test site's SOT-89 package has slight dimensional differences., p. 1, 10-13. Refer to PCN13337, GaAs Fab Transfer.
		Table 6, ESD Protection Characterization, removed the word "Minimum" after the ESD class rating. ESD ratings are characterized during new product development but are not 100% tested during production. ESD ratings provided in the data sheet are intended to be used as a guideline when handling ESD sensitive devices, p. 3
		Added Fig. 21, Product Marking, p. 10

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Document Number: MMG3H21NT1 Rev. 2, 9/2012