Operation of HVDC Modular Multilevel Converters under DC pole imbalances

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Keywords

<<Fault handling strategy>>, <<Converter control>>, <<Multilevel Converters>> and <<HVDC>>.

Abstract

Operation of HVDC converters under HVDC pole voltage imbalances is analysed. Asymmetrical HVDC pole current injection is achieved by directing current to the ground return path through a device installed in the AC side of the converter. Several operation modes, including asymmetric monopole, are presented and their sizing requirements are discussed.

Introduction

Current carbon emission policies demand a reduction of conventional generation in favour of carbon free sources. Such a scenario requires a more flexible grid capable of adapting to the availability of renewable power and the requirement to exchange power between distant regions. Voltage Source Converter High Voltage Direct Current (VSC-HVDC) transmission has the potential to enable this flexibility. VSC-HVDC power transmission is an alternative to the conventional Line Commutated Converter HVDC (LCC-HVDC) transmission which has been used for long distance bulk power transmission for the last 50 years. VSC-HVDC presents some advantages compared to LCC-HVDC; namely, it provides enhanced controllability, black-start capability and islanded operation [1]. Also, unlike LCC-HVDC, it does not require voltage polarity reversal to change the direction of the power flow. Thus, it simplifies building multi-terminal networks with multiple converters connected together forming an HVDC grid.

Early VSC-HVDC designs used two-level IGBT converters, a common topology for lower voltage and lower power drive applications developed during the 1990s. However, the need to achieve higher power levels to compete with classic LCC-HVDC technology has recently led manufacturers to switch to new topologies known as Modular Multilevel Converters (MMC). Such topologies take different forms depending on their manufacturer [2, 3, 4] but they are based in scalable structures with individual modules connected in series to reach the desired DC voltage.

HVDC transmission systems can be classified according to different criteria [5]. A system is said to be an asymmetric monopole when one conductor is at a high voltage whereas the other is at ground potential. In contrast, it is said to be a symmetric monopole when both conductors are at a high voltage with opposite sign. For LCC-HVDC it is common to design the converters to be asymmetric monopoles and to connect two converters in series in a so called bipolar arrangement to achieve symmetric pole voltage operation. By providing an auxiliary current path at ground potential, this also provides redundancy so that the system can transfer power at reduced loading even if one of the converters or conductors is lost.

Two-level VSC-HVDC transmission systems are usually designed to be symmetric monopoles in order to minimize the DC insulation levels required in their cables and transformers. In order to achieve a

symmetric voltage difference between the poles and the ground, the middle point of the capacitors in one end of the link is connected to the ground and symmetric equalization resistors are connected between the poles and the ground in order to balance their voltages [6, 7].

Unlike two-level converters, MMC do not necessarily have a stack of capacitors permanently connected in series withstanding the pole to pole voltage of the HVDC link. The capacitors in an MMC are located in each separate module of the converter; thus, MMC may require a different grounding scheme. One particular scheme currently employed by Siemens [8] uses a device known as Star-point Reactor (SR). This device consists of three star-connected inductors with their neutral connected to the ground and it is installed on the AC side of the converter, between the converter and the transformer (see Figure 1). This provides a low impedance path to the ground for DC current from the AC side of the converter without requiring DC current flowing through the transformer windings [9].

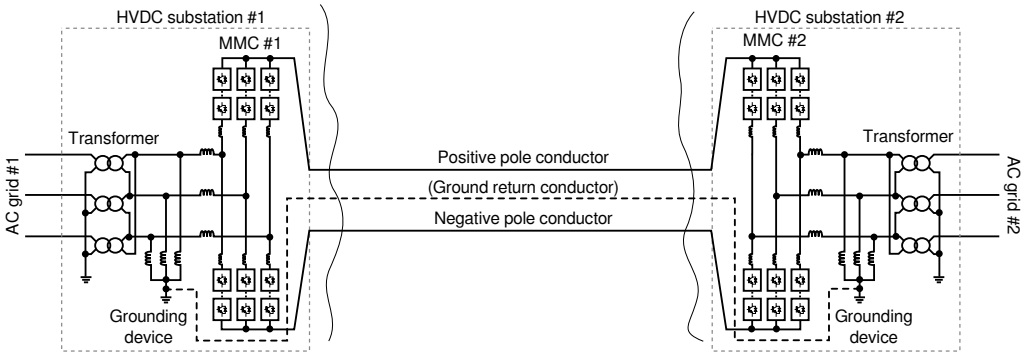

Figure 1: Point to point HVDC interconnector with SR grounding in both stations

Controlling an MMC is more complex than controlling a two-level converter. The voltage of each of its modules has to be actively controlled and recirculating currents have to be regulated to avoid additional losses and energy balancing distortions in the converter. A number of publications have already addressed how to control an MMC [10, 11, 12, 13, 14]. Using the proposed schemes, the converter is capable of following orders of power exchange between the HVDC system and the AC grid or providing HVDC link voltage regulation, depending on the role of the converter.

Regarding HVDC link voltage regulation, previous work has described how to control the difference of voltage between the positive and the negative pole of the HVDC system, assuming the pole balancing would be guaranteed by passive means. However, grounding schemes such as the SR have the potential to allow the converters to control the current circulating to the ground, thus making it possible to actively control the balance between the HVDC pole voltages.

If a suitable ground return path is provided, by means of a properly designed set of grounding electrodes or by installing a metallic return conductor, this opens a range of new interesting possibilities such as: allowing to tap loads between one single pole and the ground, sharing the duty of controlling pole balancing between different converters depending on their available headroom, etc. It also allows converters to export power at reduced loading if one of the HVDC conductors is lost by directing the return DC current through a properly sized SR.

This paper discusses the operation of MMC-based VSC-HVDC systems under pole voltage imbalances and the implications of directing DC current to the ground through the grounding device in the sizing of the HVDC converter stations.

1 Causes of HVDC pole voltage imbalances and actions required

HVDC pole voltage imbalances may range from small to severe and may follow either fast transient evolutions or slow drifts requiring different actions from converter stations.

HVDC cables for VSC-HVDC transmission are usually single core with grounded sheath. When a cable is severely damaged, the conductor is likely to touch the sheath. This creates a low impedance path resulting in a quick discharge of the energy stored in the damaged cable. If no DC circuit breaker is available to quickly isolate the damaged cable during the first few milliseconds after the fault, the stray capacitance of the healthy pole will charge through the HVDC converters and its voltage will build up until the AC-side circuit breakers isolate the transmission system from the grid [15, 16]. Afterwards, in a system capable of operating as an asymmetric monopole, DC switchgear could be used to disconnect the damaged cable and the system could be re-energised to carry on exporting power at reduced loading using the healthy cable.

On the other hand, slow drifting and small pole imbalance can occur when there is a mismatch of the impedance between the poles and the ground. Such situation can happen when high impedance short

circuits exist in the cable, due to mechanical damage or ageing of the cable, or when small loads are tapped in an asymmetric way from one pole to the ground. The action required in such situations may depend on the source of the imbalance, which could be identified by different means [17, 18]. If the cable is only lightly damaged, it is desirable to keep the system operating to give the transmission system operator (TSO) time to reallocate generation and bring the HVDC link to a safe stop afterwards. In contrast, if the imbalance is caused by an asymmetric load, HVDC power converters will be required to be able to operate in this state indefinitely by controlling the current injected to the ground return to balance the pole voltages.

2 System description and modelling

The analysis focusses on a VSC-HVDC transmission system based on half-bridge cell MMC. In order to study the steady-state operation of the converter, a simplified equivalent circuit of the MMC is used (see Figure 2). Such circuit aggregates each arm of the converter as a voltage source capable of applying a positive voltage obtained as the addition of an AC plus a DC component in order to control the power exchange between the converter modules and the AC and DC grids [10]. A simplified model of the AC grid plus the transformer is also included in the model. The connection of the transformers is delta in the converter side; however, a star-equivalent with an infinite impedance, Z_{gn}, connected between the neutral and the ground is used in the model to simplify the derivation of the equations. The SR is modelled as a three-legged-core star-connected inductor with the neutral grounded through an impedance Z_{0n}. The DC grid is modelled as an ideal DC bus. The parameters of a hypothetical system that will be used in the examples shown in the following sections are summarised in Table I.

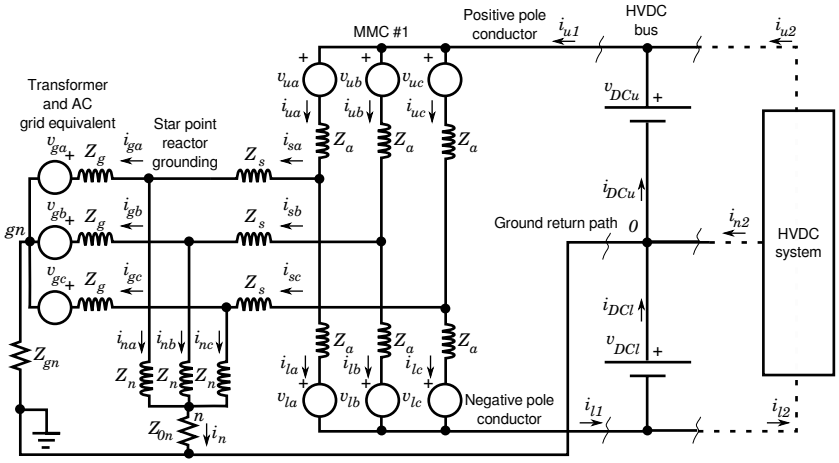

Figure 2: Equivalent circuit of the HVDC converter station.

Table I: MMC equivent circuit parameters.

Parameter	Symbol	Value	Units
Rated power	S	526	MVA
Rated power factor	$\cos\varphi$	0.95	1 leading
AC-side voltage	U	320	kV rms phase-phase
HVDC link voltage	V_{DC}	$\pm$320	kV pole-to-ground
Grid equivalent impedance	$\underline{Z}_g$	0.01+j 0.1	pu
Grid zero sequence impedance	$\underline{Z}_{gn}$	∞	pu
Phase reactor impedance	$\underline{Z}_s$	j 0.05	pu
Arm reactor impedance	$\underline{Z}_a$	0.01+j 0.2	pu
Star reactor positive seq. impedance	$\underline{Z}_n$	0.01+j 1000	pu
Star reactor neutral impedance	$R_n + 3\underline{Z}_{0n}$	0.01	pu
Converter modules per arm	N_{arm}	400	1
Average module voltage	V_{module}	1.6	kV

2.1 System steady state equations

In order to simplify the equations, it is convenient to introduce a change of variables and define the additive and subtractive voltages and the additive current, V_{sum}, V_{diff} and I_{sum} respectively, as:

$$\begin{cases} \underline{V}_{diff} \triangleq \frac{1}{2}\left(-\underline{V}_u + \underline{V}_l\right) \\ \underline{V}_{sum} \triangleq \underline{V}_u + \underline{V}_l \\ \underline{I}_{sum} \triangleq \frac{1}{2}\left(\underline{I}_u + \underline{I}_l\right) \end{cases} \tag{1}$$

which implies

$$\begin{cases} \underline{V}_u = -\underline{V}_{diff} + \frac{1}{2}\underline{V}_{sum} \\ \underline{V}_l = \underline{V}_{diff} + \frac{1}{2}\underline{V}_{sum} \\ \underline{I}_u = \frac{1}{2}\underline{I}_s + \underline{I}_{sum} \\ \underline{I}_l = -\frac{1}{2}\underline{I}_s + \underline{I}_{sum} \end{cases} \tag{2}$$

Also, in order to simplify the equations further, it is convenient to apply the Fortescue transformation to the three-phase AC variables. The Fortescue transformation is defined as:

$$\underline{\Theta}^{0+-} \triangleq F\underline{\Theta}^{abc} \tag{3}$$

with

$$F \triangleq \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & \underline{\alpha} & \underline{\alpha}^2 \\ 1 & \underline{\alpha}^2 & \underline{\alpha} \end{bmatrix}, \qquad \text{and } \underline{\alpha} \triangleq e^{j\frac{2}{3}\pi} \tag{4}$$

The power exchange between the converter and the AC grid is controlled through the subtractive voltage. Neglecting the star-reactor AC current, the current injected to the grid becomes:

$$\underline{I}_g^{+-} \approx \underline{I}_s^{+-} \approx \frac{1}{\underline{Z}_s + \underline{Z}_g + \frac{1}{2}\underline{Z}_a}\left(\underline{V}_{diff}^{+-} - \underline{V}_g^{+-}\right) \tag{5}$$

The actual positive and negative sequence current flowing through the SR can be calculated as:

$$\underline{I}_n^{+-} = \frac{1}{\underline{Z}_s\underline{Z}_g + \frac{1}{2}\underline{Z}_a\underline{Z}_g + \underline{Z}_n\left(\underline{Z}_s + \underline{Z}_g + \frac{1}{2}\underline{Z}_a\right)}\left(\underline{Z}_g\underline{V}_{diff}^{+-} + \left(\underline{Z}_s + \frac{1}{2}\underline{Z}_a\right)\underline{V}_g^{+-}\right) \tag{6}$$

The zero-sequence AC current flowing through the SR and returning through the DC grid is controlled to be zero using the zero-sequence subtractive voltage of the converter:

$$\underline{I}_s^0 = \underline{I}_n^0 = \frac{1}{3}\underline{I}_n = \frac{1}{\underline{Z}_s + \frac{1}{2}\underline{Z}_a + R_n + 3\underline{Z}_{0n}}\underline{V}_{diff}^0 \tag{7}$$

The internal power exchange between the upper and the lower arms of the converter can be achieved using positive and negative sequence additive current, whereas the zero sequence additive current is controlled to be zero. These variables depend on the additive voltage as:

$$\underline{I}_{sum}^{0+-} = -\frac{1}{2\underline{Z}_a}\underline{V}_{sum}^{0+-} \tag{8}$$

For the analysis of the DC variables, the Clarke transformation is used instead of Fortescue. The Clarke transformation is defined as:

$$\Theta^{0\alpha\beta} \triangleq C\Theta^{abc} \tag{9}$$

with

$$C \triangleq \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 2 & -1 & -1 \\ 0 & -\sqrt{3} & \sqrt{3} \end{bmatrix} \tag{10}$$

Under normal operation, the power exchange between the converter and the DC grid is achieved using the zero-sequence additive DC current; this can be controlled using the zero sequence additive DC voltage:

$$I_{sum}^{0DC} = \frac{1}{2R_a}\left(V_{DCu} + V_{DCl} - V_{sum}^{0DC}\right) \tag{11}$$

Internal power exchange between the arms of the three phases of the converter is achieved using α and β additive DC currents; both are controlled using the additive DC voltage:

$$I_{sum}^{\alpha\beta DC} = -\frac{1}{2R_a}V_{sum}^{\alpha\beta DC} \tag{12}$$

Positive and negative subtractive DC current flows through the AC of the converter, which can cause saturation of the transformer and the SR, therefore it is controlled to be zero using the positive and negative subtractive DC voltage:

$$I_{s}^{\alpha\beta DC} = \frac{R_g + R_n}{R_s R_g + \frac{1}{2}R_a R_g + R_n\left(R_s + R_g + \frac{1}{2}R_a\right)}V_{diff}^{\alpha\beta DC} \tag{13}$$

Finally, DC current injection through the SR, which is required for the asymmetric operation described here, can be controlled using the zero-sequence subtractive DC voltage:

$$I_{n}^{0DC} = I_{s}^{0DC} = \frac{1}{R_s + R_n + 3R_{0n} + \frac{1}{2}R_a}\left(V_{diff}^{0DC} + \frac{1}{2}\left(V_{DCu} - V_{DCl}\right)\right) \tag{14}$$

2.2 Approximate steady state voltages

The rough estimation of the steady state converter voltages can be obtained from the previous equations by assuming the impedances to be very small:

$$\begin{cases} \underline{V}_{diff}^{0} \approx 0 \\ \underline{V}_{diff}^{+-} \approx \underline{V}_{g}^{+-} \\ \underline{V}_{sum}^{0+-} \approx 0 \\ \underline{V}_{diff}^{0DC} \approx \frac{1}{2}\left(V_{DCu} - V_{DCl}\right) \\ \underline{V}_{diff}^{\alpha\beta DC} \approx 0 \\ \underline{V}_{sum}^{0DC} \approx V_{DCu} + V_{DCl} \\ \underline{V}_{sum}^{\alpha\beta DC} \approx 0 \end{cases} \tag{15}$$

2.3 SR requirements

The SR provides a suitable path to the ground for DC current injected by the converter. The SR has to be designed to draw little AC current to avoid adding additional losses to the system; hence, its impedance should be in the same range as the magnetising inductance of the transformers. Such high impedance could undermine the dynamic response of the DC current injection control. One way to overcome this problem is to use a three-legged-core SR with low zero-sequence impedance (see Figure 3). This is also convenient to reduce the size of the core, as zero-sequence DC current would not cause core saturation. Among the different possible core shapes, conventional E cores (Figure 3a) are convenient from the manufacturing point of view; however, symmetric core shapes such as triangular (Figure 3b) and star cores (Figure 3c) are preferable because of their decoupling between the zero, the positive and the negative sequences.

Current MMC designs usually have a delta connection on the converter side of the transformers with very high zero-sequence impedance. This is convenient for the design of the converter because it allows to maximise the output voltage capabilities of the converter by using the so-called third-harmonic voltage injection. By installing a SR with low zero-sequence impedance, this technique would cause third-harmonic current on the AC side of the converter. For example, considering the converter described in Table I, according to (7), a 0.17 pu third-harmonic voltage would cause 0.38 pu third-harmonic current, which would be unacceptable. In order to overcome this problem, an additional single-phase reactor, $\underline{Z}_{0n}$, could be installed between the star point of the SR, n, and the ground. In the previous example, a 1.8 pu reactor would reduce the third-harmonic current to 0.01 pu. This would penalise the dynamics of the DC current injection. Alternatively, the AC side voltage could be chosen to be 87% lower to avoid the need of third-harmonic injection; however, this would result in 15% higher AC current. A practical solution would involve a trade-off between these two options.

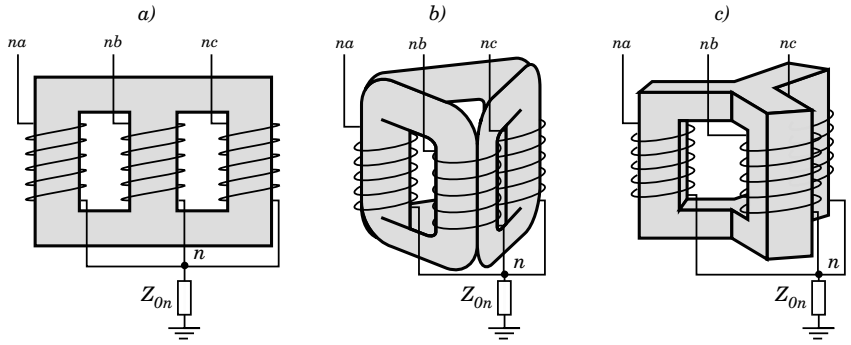

Figure 3: Examples of different possible SR core types. (a) stacked E core, (b) triangle (or D) core and (c) three-leg star (or Y) core.

3 Operation under DC pole imbalances

The steady state characteristics under different conditions and operation modes can be easily obtained from the analysis of the equations of the aforementioned equivalent circuit. Here, the following situations are discussed:

1. Normal operation at rated power.
2. Controlled floating mode under HVDC pole voltage imbalance.
3. Controlled SR current injection under HVDC pole voltage imbalance.
4. Asymmetric monopole operation using controlled SR current injection.

3.1 Normal operation without pole imbalance

Voltage, current, instantaneous power in the AC grid, the DC grid and the MMC are calculated using the parameters of the system described in Table I. The calculation is done for exporting and importing power modes. A plot of the variables is shown in Figure 4 and the numerical values can be found in columns A1 of Table II and B1 of Table III.

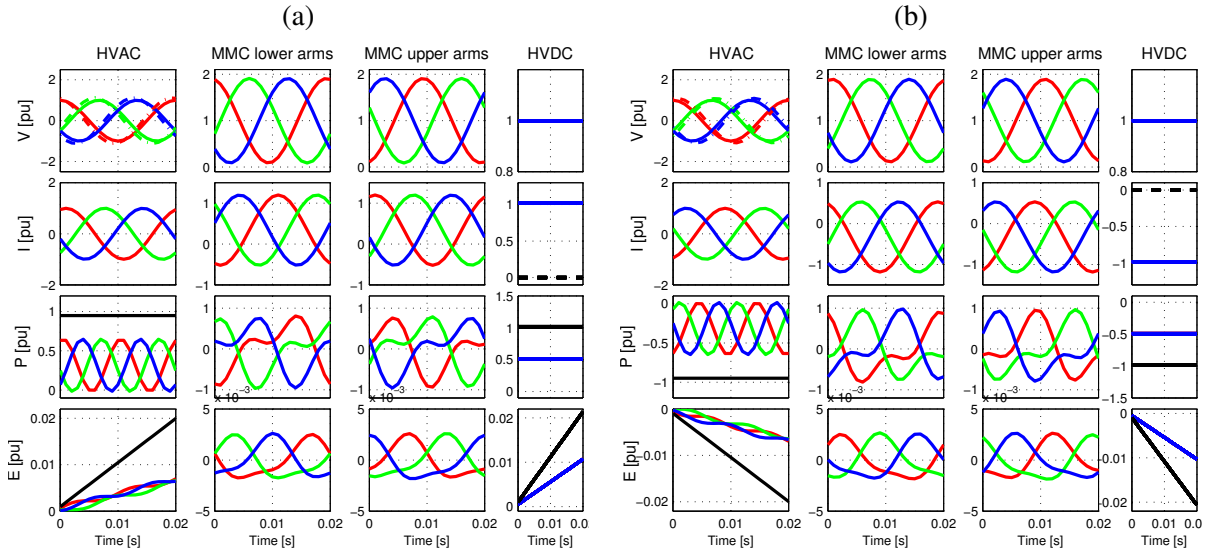

Figure 4: Normal operation without pole imbalance. Importing power to the AC grid in (a) and exporting in (b). Traces in colour correspond to *abc* variables, black traces show the addition of *abc*, discontinuous black corresponds to SR DC current and discontinuous colour corresponds to the converter output AC voltage.

The output voltage of the converter arms is the addition of the subtractive AC voltage and the additive DC voltage. These are used to control the power exchange with the AC and the DC systems without need of internal balancing action between the upper and lower arms nor the three phases of the MMC. Note

that because of the half-bridge modules, the MMC arms can not apply negative voltage, therefore there is small margin available to withstand AC over-voltages or DC voltage depressions, in this example this margin corresponds to 8% of the nominal HVDC pole voltage.

3.2 Controlled floating mode under HVDC pole voltage imbalance

In some situations, when a pole imbalance appears in the HVDC grid, it may be desirable to block the current going through the SR to create a controlled floating mode. Such situation, with a 5% offset, is shown in Figure 5 and columns A2 of Table II and B2 of Table III.

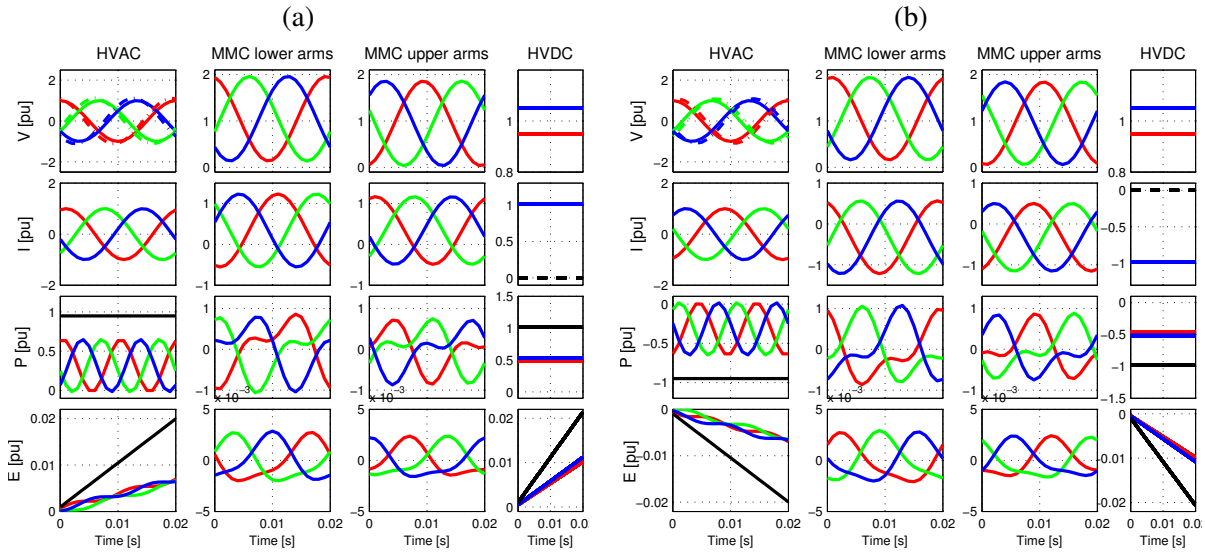

Figure 5: Controlled floating mode under 5% HVDC pole voltage imbalance. Importing power to the AC grid in (a) and exporting in (b).

The DC current on the AC side is blocked using the subtractive zero sequence DC voltage; thus, the converter needs to have enough margin to avoid crossing zero. In this example, the voltage margin is reduced to 3% because of the imbalance. If the voltage offset increased beyond this limit, the MMC would need to use a special strategy to avoid losing control over the current. Such strategy could involve using third harmonic injection (with the aforementioned problems) or disconnecting the SR, which would expose the transformers to significant DC voltage offset.

Another issue caused by this operation mode is that power exchange between upper and lower arms and the DC system becomes different. Circulating additive AC current enables balancing between the upper and lower arms, however it causes the AC current of the arms with pole over-voltage to be higher (in this case 4% more AC current). This also causes the energy ripple of the modules to be higher. Thus, sustained operation in this mode requires proper sizing of the current rating of the IGBTs and the voltage margins of the converter cells.

3.3 Controlled SR current injection under HVDC pole voltage imbalance

The previous mode blocked the SR current during pole imbalances. This causes a symmetric current exchange between the MMC and each pole. This has a positive effect when the MMC is importing power to the AC grid, because it draws less power from the depressed pole. However, it has the opposite effect when the converter exports power. By injecting current to the ground return through the SR, it is possible to control the power going to each pole independently. Such situation is shown in Figure 6 and columns A3 of Table II and B3 of Table III.

In this example, the current flowing through the SR is chosen to be enough to balance the upper and lower arms without requiring additive AC current. In contrast with the previous mode, this causes an increase of the current of the arms and the pole with depressed voltage. From the DC system perspective, this has the implications discussed above. However, from the converter design perspective, this suggests that a combination of both modes could be used to produce a lower and symmetric increase of the current and the energy ripple in the upper and lower arms converter, which would reduce its sizing requirements.

3.4 Asymmetric monopole operation using controlled SR current injection

The previous examples showed how SR current injection enables individual control of the power exchanged with each pole of the HVDC system, how this affects the energy balance between the upper and

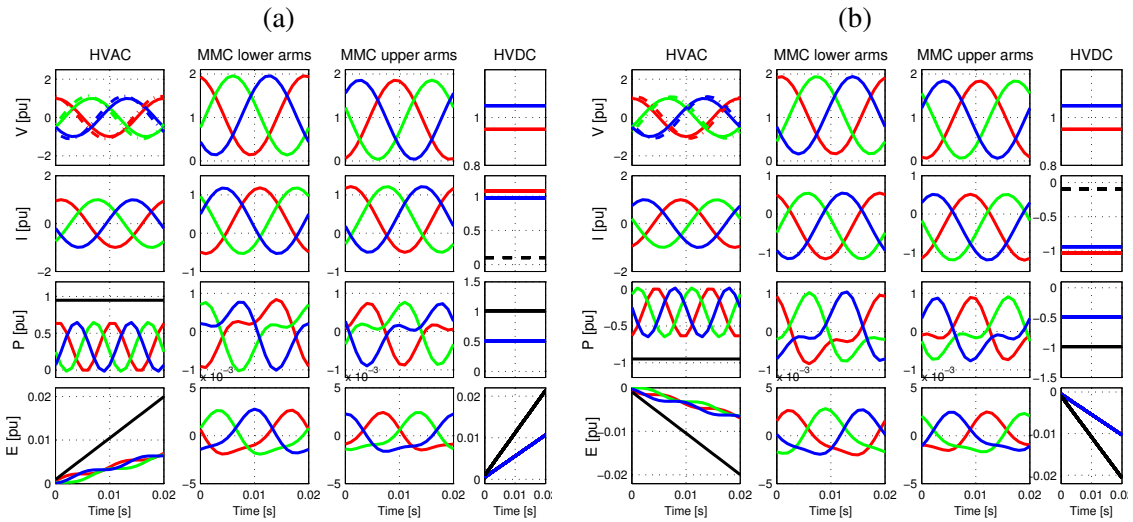

Figure 6: Controlled SR current injection under HVDC pole voltage imbalance under 5% HVDC pole imbalance. Importing power to the AC grid in (a) and exporting in (b)

lower arms and how this can be compensated using circulating AC current. An interesting outcome is the possibility to cut the current exchanged with one of the HVDC poles using the SR for the return path. Such situation is shown in Figure 7 and columns A4 of Table II and B4 of Table III.

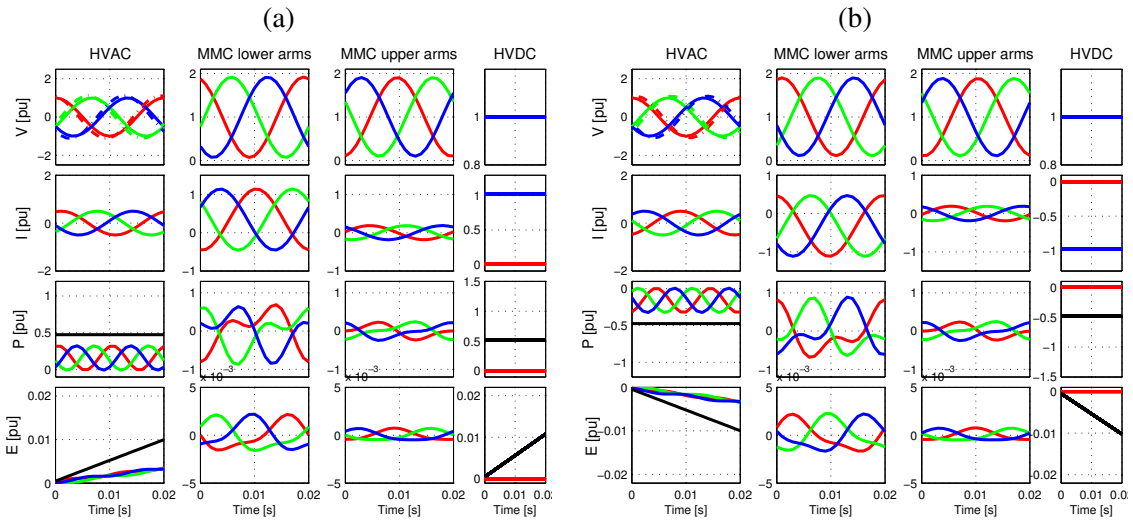

Figure 7: Asymmetric monopole operation at 50% rated power using controlled SR current injection and open circuit HVDC pole. Importing power to the AC grid in (a) and exporting in (b).

In this example, the MMC is not exchanging power with the positive pole of the HVDC system and the loading of the converter is reduced to 50%, assuming the rated current of the cable can not be exceeded. When operating in this mode, the power exchanged with the AC grid is split equally between the upper and lower arms. As the upper arms can not export energy through the upper HVDC pole, circulating AC current is used to exchange the power with the lower arms instead. Finally, SR current is used to exchange power between the lower arms and the lower HVDC pole.

The results show that the loading of the upper arms is very low in terms of current and energy ripple, as the DC current is zero and the only AC current corresponds to reactive power exchange with the AC grid. On the other hand, the loading of the lower arms is comparable to the loading under normal operation at rated power.

4 Conclusions

This paper discussed the operation of MMC HVDC systems under pole imbalances. The analysis showed that a grounding device providing a low impedance path for DC current on the AC side of the converter would enable a number of interesting features. Namely, it would enable independent control of the power exchanged with each pole of the HVDC system, which could be used to enable tapping loads from single poles and ultimately enable asymmetric monopole operation. This feature would make MMC capable of exchanging power through an HVDC link at reduced loading when a cable was lost without requiring a bipolar converter arrangement nor HVDC transformers with high DC voltage isolation requirements. On the other hand, low impedance grounding has been found to interfere with third-harmonic voltage injection and therefore its use has implications on the sizing of the voltage margins of the MMC.

Table II: Steady state parameters for different operating modes to import power to the AC system

Parameter	A1	A2	A3	A4	Units
P_g	0.95	0.95	0.95	0.475	pu (rated S)
Q_g	-0.3125	-0.3125	-0.3125	-0.1563	pu (rated S)
V_g	1	1	1	1	pu AC
I_g	1∠-18.2°	1∠-18.2°	1∠-18.2°	0.5∠-18.2°	pu AC
V_{diff}	1.117∠12°	1.117∠12°	1.117∠12°	1.117∠12°	pu AC
I_s	1∠-18.2°	1∠-18.2°	1∠-18.2°	0.5∠-18.2°	pu AC
V_u	1.117∠-168°	1.117∠-168°	1.117∠-168°	1.109∠-173°	pu AC
V_l	1.117∠12°	1.117∠12.3°	1.117∠12°	1.132∠16.6°	pu AC
I_u	0.5∠-18.2°	0.4814∠-19.5°	0.5∠-18.2°	0.1075∠-82.6°	pu AC
I_l	0.5∠162°	0.5188∠163°	0.5∠162°	0.4638∠174°	pu AC
P_{DCu}	0.5087	0.4833	0.5089	0	pu (rated P)
P_{DCl}	0.5087	0.5342	0.5086	0.5134	pu (rated P)
V_{DCu}	1	0.95	0.95	1	pu DC
V_{DCl}	1	1.05	1.05	1	pu DC
I_{DCu}	1.017	1.017	1.071	0	pu DC
I_{DCl}	1.017	1.017	0.9687	1.027	pu DC
V_u^{DC}	0.9984	0.9484	0.9481	1.003	pu DC
V_l^{DC}	0.9984	1.048	1.049	0.9935	pu DC
I_u^{DC}	0.3391	0.3391	0.3571	0	pu DC
I_l^{DC}	0.3391	0.3391	0.3229	0.3422	pu DC
I_n^{DC}	0	0	0.1027	-1.027	pu DC
V_{sum}^{DC}	1.997	1.997	1.997	1.997	pu DC
$Vdiff^{DC}$	0	0	0.05024	-0.004877	pu DC
I_{sum}^{DC}	0.3391	0.3391	0.34	0.1711	pu DC
V_{sum}	0	0.008666∠98.9°	0	0.1806∠94.4°	pu AC
I_{sum}	0	0.02164∠-168°	0	0.2254∠-173°	pu AC

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Table III: Steady state parameters for different operating modes to export power from the AC system

Parameter	B1	B2	B3	B4	Units
P_g	-0.95	-0.95	-0.95	-0.475	pu (rated S)
Q_g	-0.3125	-0.3125	-0.3125	-0.1563	pu (rated S)
V_g	1	1	1	1	pu AC
I_g	1∠-162°	1∠-162°	1∠-162°	0.5∠-162°	pu AC
V_{diff}	1.091∠-12.8°	1.091∠-12.8°	1.091∠-12.8°	1.091∠-12.8°	pu AC
I_s	1∠-162°	1∠-162°	1∠-162°	0.5∠-162°	pu AC
V_u	1.091∠167°	1.091∠167°	1.091∠167°	1.092∠172°	pu AC
V_l	1.091∠-12.8°	1.091∠-13°	1.091∠-12.8°	1.098∠-17.5°	pu AC
I_u	0.5∠-162°	0.4818∠-160°	0.5∠-162°	0.1108∠-98.1°	pu AC
I_l	0.5∠18.2°	0.5185∠17°	0.5∠18.2°	0.4617∠5.79°	pu AC
P_{DCu}	-0.4913	-0.4668	-0.4912	0	pu (rated P)
P_{DCl}	-0.4913	-0.5159	-0.4915	-0.487	pu (rated P)
V_{DCu}	1	0.95	0.95	1	pu DC
V_{DCl}	1	1.05	1.05	1	pu DC
I_{DCu}	-0.9827	-0.9827	-1.034	0	pu DC
I_{DCl}	-0.9827	-0.9827	-0.9362	-0.974	pu DC
V_u^{DC}	1.002	0.9516	0.9518	0.9969	pu DC
V_l^{DC}	1.002	1.052	1.051	1.006	pu DC
I_u^{DC}	-0.3276	-0.3276	-0.3447	0	pu DC
I_l^{DC}	-0.3276	-0.3276	-0.3121	-0.3247	pu DC
I_n^{DC}	0	0	-0.0979	0.974	pu DC
V_{sum}^{DC}	2.003	2.003	2.003	2.003	pu DC
$Vdiff^{DC}$	0	0	0.04977	0.004626	pu DC
I_{sum}^{DC}	-0.3276	-0.3276	-0.3284	-0.1623	pu DC
V_{sum}	0	0.008564∠-105°	0	0.1795∠-101°	pu AC
I_{sum}	0	0.02138∠-12.6°	0	0.2241∠-8.1°	pu AC

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