Positive and negative sequence currents to improve voltages during unbalanced faults

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1 Introduction

Grid faults constitute a group of unfortunate events that cause severe perturbations in the grid. The voltages can take values below the established minimum, or on the contrary, exceed the maximum in non-faulted phases. The currents are also susceptible to vary considerably. Traditional power systems based on synchronous generators could encounter currents surpassing the nominal values, and therefore, the fault could be clearly detected. However, the increasing integration of renewables [1] supposes a change of paradigm, in which currents can be controlled but are limited so as not to damage the Isolated-Gate Bipolar Transistors (IGBT) found in the Voltage Source Converter (VSC) [2].

Transmission System Operators (TSO) are responsible for imposing requirements related to the operation under voltage sags to generators and converters [3, 4]. Such requirements are gathered in the respective grid codes. There seems to be no clear consensus on how to restore the voltage. In this sense, even if for instance the Low Voltage Ride Through (LVRT) profiles present similarities [5], analysis aimed at determining analytically the optimal injection of positive and negative sequence currents are not numerous. As far as the author is aware, only Camacho et al. offer an optimal solution regarding the injection of active and reactive powers [6].

Consequently, this work focuses on finding the most convenient positive and negative sequence currents (and not powers) to raise the voltage at the point of common coupling. First, a simple model is discussed, and then, the results are shown together with the corresponding discussion. The challenge to solve the optimization problem in a closed-form is specially described.

2 Problem definition

The system we are considering is formed by an ideal grid (only positive sequence voltage is present) coupled to a VSC. The model is depicted in Figure 1. The VSC will be controlled in a way that leads to an improvement in the voltage at the PCC.

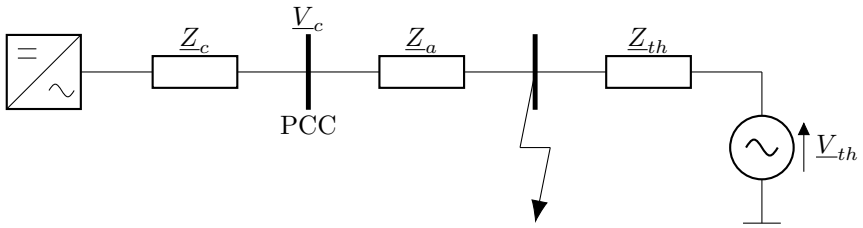

Figure 1: Single-phase representation of the simple system under a fault

The point of common coupling (PCC) is where the VSC together with its filter are connected. There are two restrictions to take into account in a VSC, one related to the maximum current and another to the voltage. The current limitation is likely the most relevant when operating under faults. Since the current is limited and the filter used to connect the VSC to the PCC takes rather low values, we can expect the voltage drop to not be substantial. Because of that, and taking into consideration the voltage sag at the grid side, the voltage limit is hardly ever surpassed. Thus, in the analysis that follows, we only impose the current restriction. As future work, we could also add the voltage limitations as a constraint, although probably the conclusions will not vary from the ones extracted here.

Note that Figure 1 is general, in the sense that it does not specify the type of fault. Besides, there will be a fault impedance, denoted by $\underline{Z}_f$. We believe every type of fault deserves to be studied separately. We are going to employ the symmetrical components, which are meant to simplify the analysis. In each fault, the voltage $\underline{V}_c$ will be decomposed in positive and negative sequence voltage and expressed as a function of the voltage at the grid together with the injected positive and negative sequence currents. It makes sense to model the VSC and its filter as a current source for this purpose.

2.1 Balanced fault

In a three-phase representation, we model the system shown in Figure 1 as in [7], where the VSC is modeled with controlled current sources. This approach, although not typical, makes physical sense. In the end we are controlling these currents. Figure 2 displays the scheme for a balanced fault.

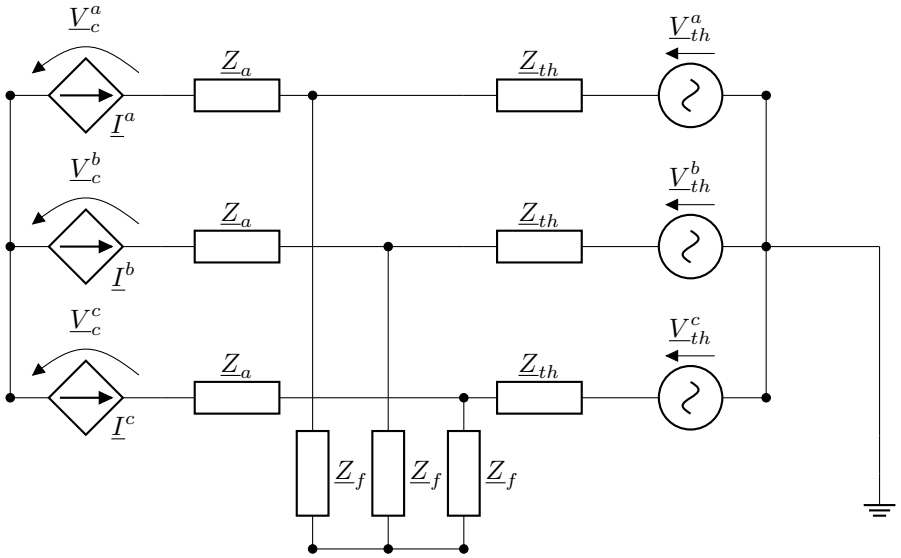

Figure 2: Balanced fault schematic

For this type of fault, the *abc* voltages we are looking for are

$$\begin{cases} \underline{V}_c^a = \dfrac{1}{\underline{Z}_f + \underline{Z}_{th}}[\underline{V}_{th}^a \underline{Z}_f + \underline{I}_a(\underline{Z}_a\underline{Z}_{th} + \underline{Z}_{th}\underline{Z}_f + \underline{Z}_f\underline{Z}_a)] \\ \underline{V}_c^b = \dfrac{1}{\underline{Z}_f + \underline{Z}_{th}}[\underline{V}_{th}^b \underline{Z}_f + \underline{I}_b(\underline{Z}_a\underline{Z}_{th} + \underline{Z}_{th}\underline{Z}_f + \underline{Z}_f\underline{Z}_a)] \\ \underline{V}_c^c = \dfrac{1}{\underline{Z}_f + \underline{Z}_{th}}[\underline{V}_{th}^c \underline{Z}_f + \underline{I}_c(\underline{Z}_a\underline{Z}_{th} + \underline{Z}_{th}\underline{Z}_f + \underline{Z}_f\underline{Z}_a)] \end{cases} \tag{1}$$

The balanced fault is the most severe one in terms of current, but fortunately, also the most unlikely to happen [8]. Its analysis becomes the most simplistic one as the equivalent circuits of all faults are disconnected one from the other. Figure 3 shows the full equivalent circuit.

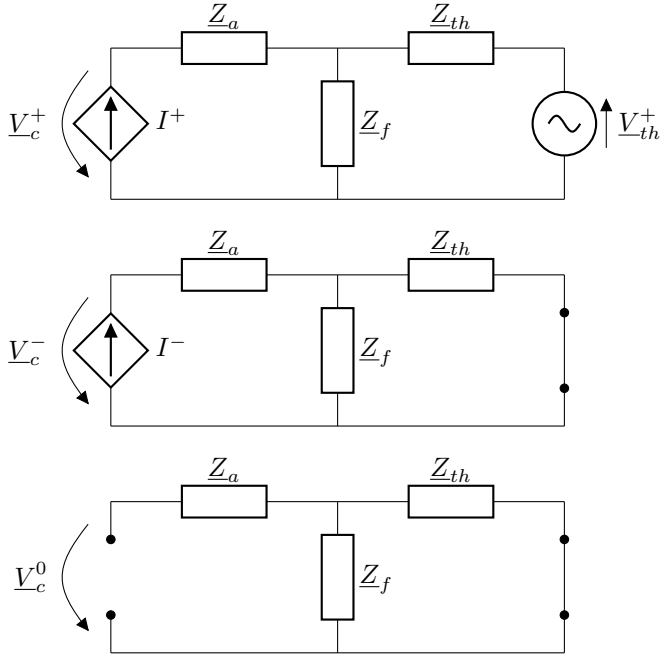

Figure 3: Equivalent circuit for the balanced fault analysis

The equations that define the positive and negative sequence voltages at the PCC for the balanced fault are

$$\begin{cases} \underline{V}_c^+ = \dfrac{1}{\underline{Z}_f + \underline{Z}_{th}}[\underline{V}_{th}^+ \underline{Z}_f + \underline{I}^+(\underline{Z}_a\underline{Z}_f + \underline{Z}_a\underline{Z}_{th} + \underline{Z}_f\underline{Z}_{th})] \\ \underline{V}_c^- = \dfrac{1}{\underline{Z}_f + \underline{Z}_{th}}[\underline{I}^-(\underline{Z}_{th}\underline{Z}_f + \underline{Z}_a\underline{Z}_{th} + \underline{Z}_a\underline{Z}_f)] \end{cases} \tag{2}$$

2.2 Line to ground fault

Just like for the balanced fault, we also show the schematic for the line to ground fault in this case, as depicted in Figure 4.

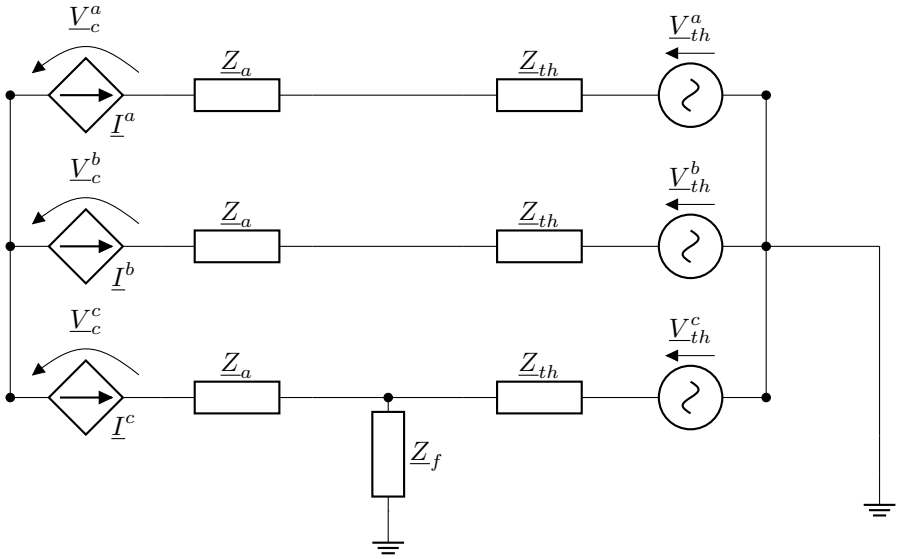

Figure 4: Line to ground fault schematic

A line to ground (LG) fault involves the series connection of the equivalent circuit of the three symmetrical components. Transforming the circuit in Figure 1 to an equivalent circuit in the positive, the negative and the homopolar component results in the representation shown in Figure 5.

The equations that define the positive and negative sequence voltages at the PCC for the line to ground fault are

$$\begin{cases} \underline{V}_c^+ = \dfrac{1}{3\underline{Z}_f + 3\underline{Z}_{th}}[\underline{V}_{th}^+(3\underline{Z}_f + 2\underline{Z}_{th}) + \underline{I}^+(3\underline{Z}_a\underline{Z}_f + 3\underline{Z}_a\underline{Z}_{th} + 3\underline{Z}_{th}\underline{Z}_f + 2\underline{Z}_{th}^2) + \underline{I}^-(-\underline{Z}_{th}^2)] \\ \underline{V}_c^- = \dfrac{1}{3Z_f + 3Z_{th}}[\underline{V}_{th}^+(-\underline{Z}_{th}) + \underline{I}^+(-\underline{Z}_{th}^2) + \underline{I}^-(3\underline{Z}_a\underline{Z}_f + 3\underline{Z}_a\underline{Z}_{th} + 3\underline{Z}_f\underline{Z}_{th} + 2\underline{Z}_{th}^2)] \end{cases} \tag{3}$$

2.3 Line to line fault

The line to line fault schematic is shown in Figure 6. Notice that the fault impedance is meant to be represented by a single impedance connected between the faulted phases.

A line to line (LL) fault involves the parallel connection of the equivalent circuit of the positive and negative sequences. In this case, the homopolar sequence can be ignored, as no current flows through it. This time we are only going to work with the positive and the negative components. Figure 7 presents the equivalent circuit.

The equations that define the positive and negative sequence voltages at the PCC for the line to

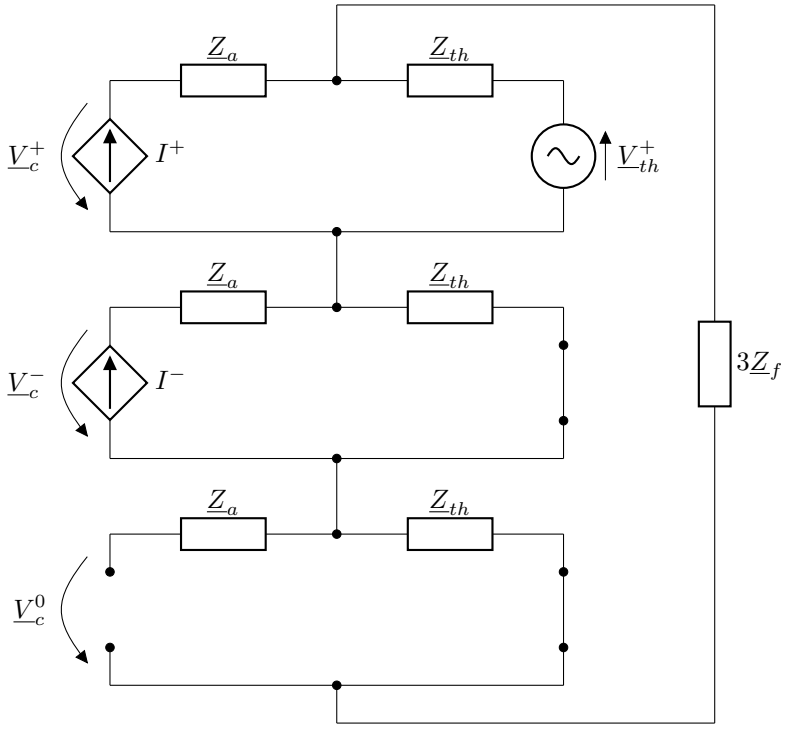

Figure 5: Equivalent circuit for the LG fault analysis

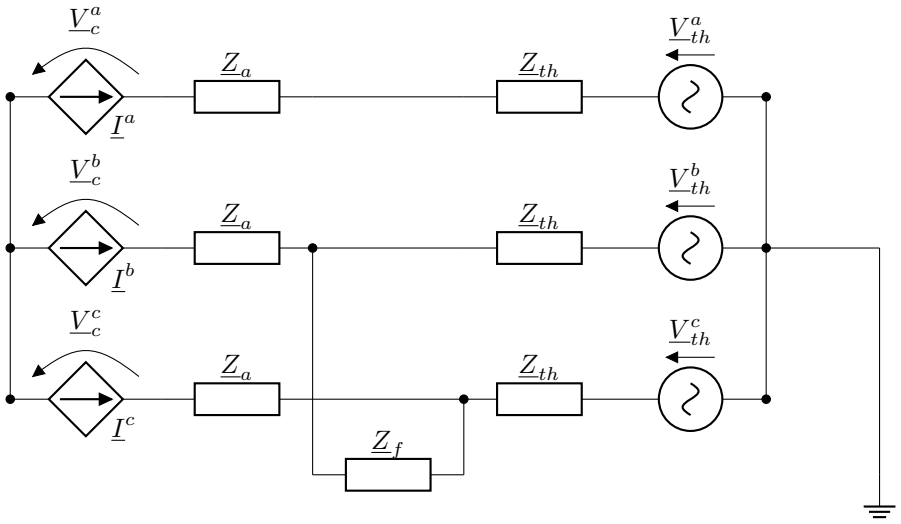

Figure 6: Line to line fault schematic

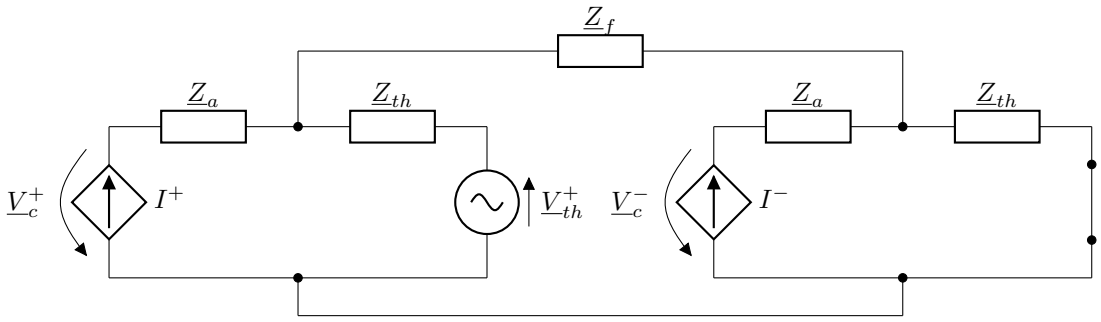

Figure 7: Equivalent circuit for the LL fault analysis

line fault are

$$\begin{cases} \underline{V}_c^+ = \dfrac{1}{\underline{Z}_f^2 + 3\underline{Z}_{th}\underline{Z}_f + 2\underline{Z}_{th}^2}[\underline{V}_{th}(\underline{Z}_f^2 + \underline{Z}_{th}^2 + 2\underline{Z}_{th}\underline{Z}_f) + \underline{I}^+(2\underline{Z}_a\underline{Z}_{th}^2 + 3\underline{Z}_a\underline{Z}_{th}\underline{Z}_f + 2\underline{Z}_{th}^2\underline{Z}_f \\ \qquad + 2\underline{Z}_a\underline{Z}_{th}^2 + \underline{Z}_{th}^3) + \underline{I}^-(\underline{Z}_{th}^2\underline{Z}_f + \underline{Z}_{th}^3)] \\ \underline{V}_c^- = \dfrac{1}{\underline{Z}_f + 2\underline{Z}_{th}\underline{Z}_f}[\underline{V}_{th}^+\underline{Z}_{th}\underline{Z}_f + \underline{I}^+(\underline{Z}_{th}^2\underline{Z}_f) + \underline{I}^-(\underline{Z}_a\underline{Z}_f^2 + \underline{Z}_{th}\underline{Z}_f^2 + 2\underline{Z}_a\underline{Z}_{th}\underline{Z}_f + \underline{Z}_{th}^2\underline{Z}_f)] \end{cases} \tag{4}$$

2.4 Double line to ground fault

The double line to ground fault schematic appears in Figure 8. This time, the fault impedance is connected between the faulted phases and ground.

A double line to ground (LLG) fault involves the parallel connection of the equivalent circuit of the three sequences. This time, in contrast to the line to line fault, the homopolar sequence can not be ignored. Furthermore, the fault impedance connects it to the negative sequence circuit. Figure 9 presents the complete equivalent circuit. Again, an homopolar voltage will be present, but we have no way to control it since the converter is incapable of injecting homopolar currents in a three-wire system like this one.

The equations that define the positive and negative sequence voltages at the PCC for the double line to ground fault are

$$\begin{cases} \underline{V}_c^+ = \dfrac{1}{3\underline{Z}_{th} + 6\underline{Z}_f}\left[\underline{V}_{th}^+(\underline{Z}_{th} + 3\underline{Z}_f) + \underline{I}^+(3\underline{Z}_{th}\underline{Z}_a + 6\underline{Z}_f\underline{Z}_a + \underline{Z}_b^2 + 3\underline{Z}_f\underline{Z}_{th}) + \underline{I}^-(\underline{Z}_{th}^2 + 3\underline{Z}_{th}\underline{Z}_f)\right] \\ \underline{V}_c^- = \dfrac{1}{3\underline{Z}_{th} + 6\underline{Z}_f}\left[\underline{V}_{th}^+(\underline{Z}_{th} + 3\underline{Z}_f) + \underline{I}^+(\underline{Z}_{th}^2 + 3\underline{Z}_{th}\underline{Z}_f) + \underline{I}^-(\underline{Z}_{th}^2 + 3\underline{Z}_{th}\underline{Z}_f + 3\underline{Z}_a\underline{Z}_{th} + 6\underline{Z}_f\underline{Z}_a)\right] \end{cases} \tag{5}$$

3 Results and discussion

4 Conclusions

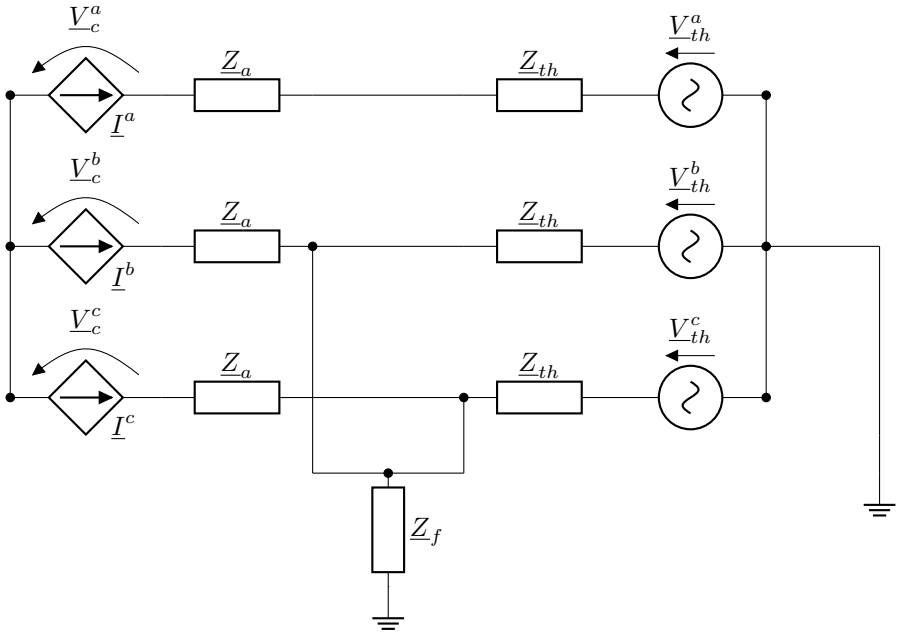

Figure 8: Double line to ground fault schematic

References

[1] Ahmed Sharique Anees. "Grid integration of renewable energy sources: Challenges, issues and possible solutions". In: *2012 IEEE 5th India International Conference on Power Electronics (IICPE)*. IEEE. 2012, pp. 1–6.

[2] AF Abdou, Ahmed Abu-Siada, and HR Pota. "Improving the low voltage ride through of doubly fed induction generator during intermittent voltage source converter faults". In: *Journal of Renewable and Sustainable Energy* 5.4 (2013), p. 043110.

[3] Marina Tsili and S Papathanassiou. "A review of grid code technical requirements for wind farms". In: *IET Renewable power generation* 3.3 (2009), pp. 308–332.

[4] Florin Iov et al. "Mapping of grid faults and grid codes". In: (2007).

[5] JF Conroy and R Watson. "Low-voltage ride-through of a full converter wind turbine with permanent magnet generator". In: *IET Renewable power generation* 1.3 (2007), pp. 182–189.

[6] Antonio Camacho et al. "Positive and negative sequence control strategies to maximize the voltage support in resistive–inductive grids during grid faults". In: *IEEE Transactions on Power Electronics* 33.6 (2017), pp. 5362–5373.

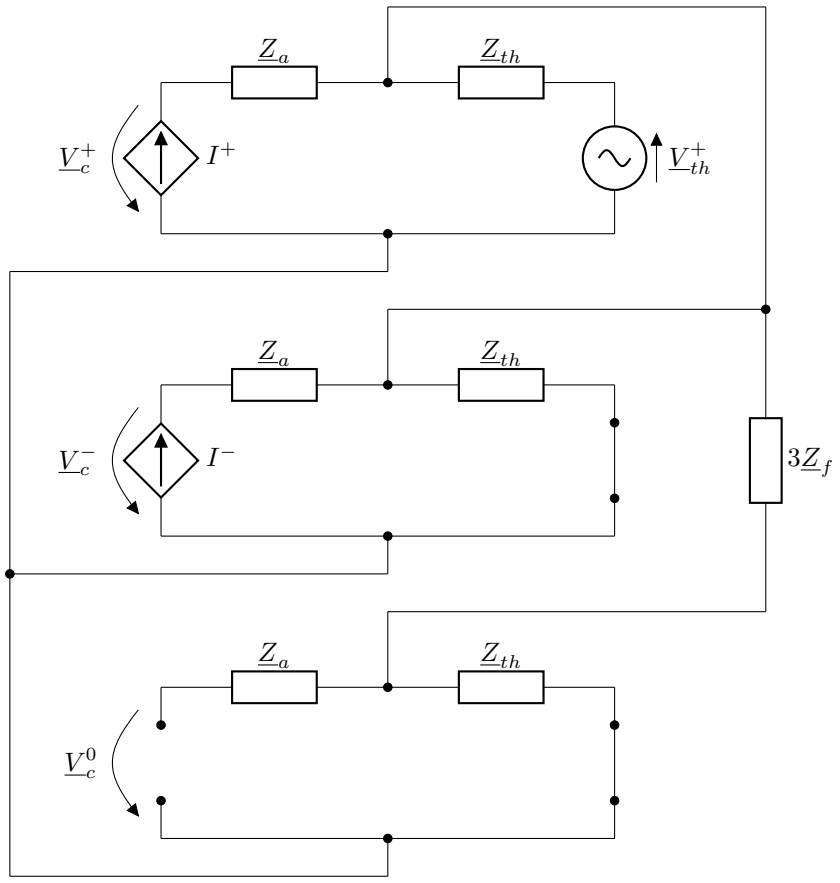

Figure 9: Equivalent circuit for the LLG fault analysis

[7] Mads Graungaard Taul et al. "Modeling of Converter Synchronization Stability under Grid Faults: The General Case". In: *IEEE Journal of Emerging and Selected Topics in Power Electronics* (2020).

[8] Nasser Tleis. *Power systems modelling and fault analysis: theory and practice*. Elsevier, 2007.