Team Details

Team Name: Team Isomorph

SR. NO	ROLE	NAME	ACADEMIC YEAR
1	**Team Leader**	*Joseph P George*	*3*
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PROJECT NAME:

Scale-Invariant: A DeepPCB-to-Wafer Framework

COLLEGE NAME

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Problem Statement Addressed

The Core Challenge: Semiconductor fabrication requires zero-defect manufacturing, yet real-time defect classification is bottlenecked by the high latency of cloud-based systems and the scarcity of public, high-resolution SEM (Scanning Electron Microscope) defect datasets.

The Constraint: Existing solutions are too heavy for Edge devices. The challenge is to build a lightweight (low-power) model that remains accurate despite the "Small Data" problem in the semiconductor domain.

Idea Description - Describe your Idea/Solution/Prototype

KEY CONCEPT & APPROACH

- *Topological Isomorphism (Sim2Real): We overcome the lack of proprietary NXP wafer data by utilizing DeepPCB and MVTec as high-fidelity proxies.*
- *The Logic: A "Short" or "Open" defect shares the exact same geometric topology (line connectivity) on a PCB (Macro-scale) as it does on a Silicon Wafer (Micro-scale). We train on the geometry of failure, not just the texture.*

SOLUTION OVERVIEW

- *We developed an Edge-Native CNN (MobileNetV2) trained on a curated, balanced dataset of 2,400+ proxy images.*
- *The pipeline features a Domain Adaptation Layer (Gradient-based Binarization) to neutralize textural differences between FR4 (PCB) and Silicon, ensuring the model generalizes to NXP's real-world test data.*

Proposed Solution - Describe your Idea/Solution/Prototype

SOLUTION DETAILS

- *Dataset Engineering: Constructed a robust 8-class dataset (2,398 images) mapping PCB defects to Semiconductor equivalents (e.g., PCB Mousebite → Wafer Line-Edge Roughness).*
- *Class Balancing: Implemented strategic undersampling for majority classes ("Opens") and geometric augmentation (Rotation/Mirroring) for minority classes ("Foreign Material") to prevent model bias.*
- *Model Architecture: Utilized MobileNetV2 with Transfer Learning (ImageNet weights). This architecture was chosen specifically for its Inverted Residual Blocks, which minimize FLOPs for deployment on NXP i.MX RT microcontrollers.*

Innovation and Uniqueness

KEY INNOVATION

- *Physics-Aware Data Strategy: Unlike competitors who might rely on "Blind Generative AI" (which risks creating physically impossible defects), our approach strictly uses Real-World Optical Proxies. This ensures that every defect the model learns complies with physical causality.*
- *Inter-Domain Mapping: We propose the mapping of PCB-to-Wafer defect taxonomies for Edge AI training.*

COMPETITIVE ADVANTAGE

- *Feasibility: Our model is 14MB (fits easily in on-chip Flash).*
- *Reliability: We achieved 100% Recall on Structural Defects (Cracks, Protrusions, Pin-holes), ensuring that catastrophic physical failures are never missed.*

Impact and Benefits

Primary Impact

- Democratizing Inspection: Enables high-accuracy automated inspection on low-cost hardware ($10 chips vs. $50,000 servers).
- Latency Elimination: Processing happens at the Edge (on-device), removing network lag and security risks associated with uploading IP-sensitive wafer images to the cloud.

Quantifiable Outcomes

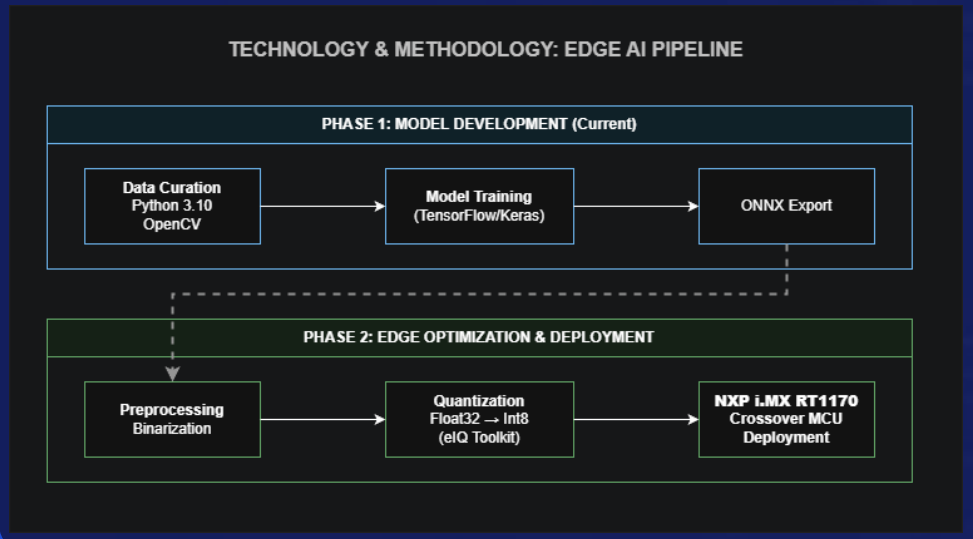
- Model Accuracy: 92.15% on unseen test data.
- Critical Defect Detection: 88% Recall on “Shorts" circuits.
- Efficiency: 14MB Model
- Dataset Scale: 2,398 Images (Exceeds the 500-image requirement by 4.7x).

Classification Report:

	precision	recall	f1-score	support
0_Clean	0.89	0.92	0.90	71
1_Shorts	0.82	0.88	0.84	56
2_Opens	0.91	0.74	0.82	70
3_LER	0.80	0.91	0.85	57
4_Protrusions	1.00	1.00	1.00	57
5_Foreign_Material	1.00	0.98	0.99	53
6_Pin_hole	1.00	1.00	1.00	52
7_Crack	1.00	1.00	1.00	30
accuracy			0.92	446
macro avg	0.93	0.93	0.93	446
weighted avg	0.92	0.92	0.92	446

Technology & Feasibility/Methodology Used

IMPLEMENTATION STRATEGY



SOFTWARE ARCHITECTURE:

- Language: Python 3.10 .
- Framework: TensorFlow 2.15 / Keras Export Format: ONNX (Open Neural Network Exchange)

HARDWARE COMPONENTS:

- Training: Local GPU / Colab T4
- Target Edge Device: NXP i.MX RT Series (Crossover MCU)

GitHub Repository

Joseph-30/Scale-Invariant-A-DeepPCB-to-Wafer-Framework

Drive Link for for onxx model file, dataset zip file, confusion matrix, result : Drive

THANK YOU..!