6.11 A binary ripple counter uses flip-flops that trigger on the positive-edge of the clock. What will be the count if:

(a) the normal outputs of the flip-flops are connected to the clock; and

(b) the complement outputs of the flip-flops are connected to the clock?

6.12 Draw the logic diagram of a four-bit binary ripple countdown counter using:

(a) flip-flops that trigger on the positive-edge of the clock; and

(b) flip-flops that trigger on the negative-edge of the clock.

6.13 Show that a BCD ripple counter can be constructed using a four-bit binary ripple counter with asynchronous clear and a NAND gate that detects the occurrence of count 1010. (HDL—see Problem 6.35(k))

6.19 The flip-flop input equations for a BCD counter using *T* flip-flops are given in Section 6.4. Obtain the input equations for a BCD counter that uses (a) *JK* flip-flops and (b)* *D* flip-flops. Compare the three designs to determine which one is the most efficient.

6.27 Using *JK* flip-flops:

(a) Design a counter with the following repeated binary sequence: 0, 1, 2, 3, 4, 5, 6. (HDL—see Problem 6.50(a), 6.51).

(b) Draw the logic diagram of the counter.

the lower gate (instead of the inverter output).

5.2 Construct a *JK* flip-flop using a *D* flip-flop, a two-to-one-line multiplexer, and an inverter. (HDL—see Problem 5.34)

[illegible] *JK* flip-flop is

5.6 A sequential circuit with two *D* flip-flops *A* and *B*, two inputs, *x* and *y*; and one output *z* is specified by the following next-state and output equations (HDL—see Problem 5.35):

$$A(t+1) = xy' + xB$$
$$B(t+1) = xA + xB'$$
$$z = A$$

(a) Draw the logic diagram of the circuit.
(b) List the state table for the sequential circuit.
(c) Draw the corresponding state diagram.

5.9 A sequential circuit has two JK flip-flops A and B and one input x. The circuit is described by the following flip-flop input equations:

$$J_A = x\ K_A = B$$
$$J_B = x\ K_B = A'$$

(a)* Derive the state equations $A(t + 1)$ and $B(t + 1)$ by substituting the input equations for the J and K variables.

(b) Draw the state diagram of the circuit.

5.10 A sequential circuit has two JK flip-flops A and B, two inputs x and y, and one output z. The flip-flop input equations and circuit output equation are

$$J_A = Bx + B'y' \quad K_A = B'xy'$$
$$J_B = A'x \qquad K_B = A + xy'$$
$$z = Ax'y' + Bx'y'$$

(a) Draw the logic diagram of the circuit.

(b) Tabulate the state table.

(c)* Derive the state equations for A and B.

5.12 For the following state table

	Next State		Output	
Present State	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

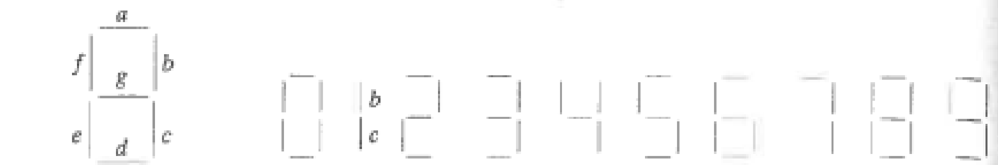
(a) Draw the corresponding state diagram.

(b)* Tabulate the reduced state table.

(c) Draw the state diagram corresponding to the reduced state table.

Chapter 4

4.9 A BCD-to-seven-segment decoder is a combinational circuit that converts a decimal digit in BCD to an appropriate code for the selection of segments in an indicator used to display the decimal digit in a familiar form. The seven outputs of the decoder *(a, b, c, d, e, f, g)* select the corresponding segments in the display, as shown in Fig. P4.9(a). The numeric display chosen to represent the decimal digit is shown in Fig. P4.9(b). Using a truth table and Karnaugh maps, design the BCD-to-seven-segment decoder using a minimum number of gates. The six invalid combinations should result in a blank display. (HDL—see Problem 4.51)



(a) Segment designation

(b) Numerical designation for display

FIGURE P4.9

(b) Write and verify a HDL dataflow model of the circuit.

4.21 Design a combinational circuit that compares two 4-bit numbers to check if they are equa The circuit output is equal to 1 if the two numbers are equal and 0 otherwise.

4.22* Design an excess-3-to-binary decoder using the unused combinations of the code a don't-care conditions. (HDL—see Problem 4.42)

4.23 Draw the logic diagram of a 2-to-4-line decoder using (a) NOR gates only and (b) NANI gates only. Include an enable input. (HDL—see Problems 4.36 and 4.45)

4.24 Design a BCD-to-decimal decoder using the unused combinations of the BCD code a don't-care conditions.

4.25 Construct a 5-to-32-line decoder with four 3-to-8-line decoders with enable and a 2-tc 4-line decoder. Use block diagrams for the components. (HDL—see Problem 4.62)

4.26 Construct a 4-to-16-line decoder with five 2-to-4-line decoders with enable. (HDL—se Problem 4.63)

4.27 A combinational circuit is specified by the following three Boolean functions:

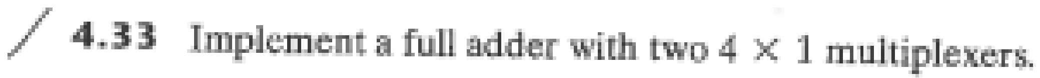
$$F_1(A, B, C) = \Sigma(1, 4, 6)$$
$$F_2(A, B, C) = \Sigma(3, 5)$$
$$F_3(A, B, C) = \Sigma(2, 4, 6, 7)$$

Implement the circuit with a decoder constructed with NAND gates (similar to Fig. 4.19) and NAND or AND gates connected to the decoder outputs. Use a block diagram for the decoder. Minimize the number of inputs in the external gates.

4.28 Using a decoder and external gates, design the combinational circuit defined by the following three Boolean functions:

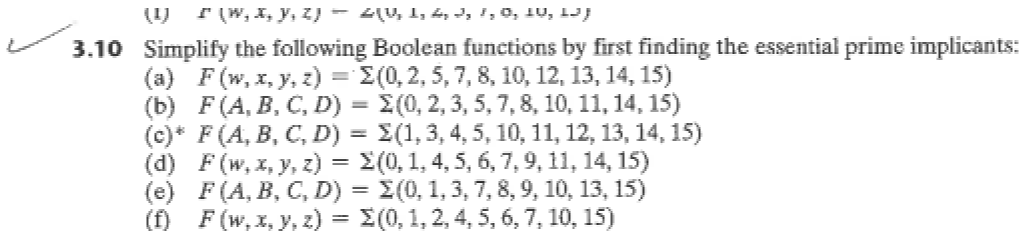
(a)* $F_1 = x'yz' + xz$
$F_2 = xy'z' + x'y$
$F_3 = x'y'z' + xy$

(b) $F_1 = (y' + x)z$
$F_2 = y'z' + x'y + yz'$
$F_3 = (x + y)z$



4.33 Implement a full adder with two 4 × 1 multiplexers.

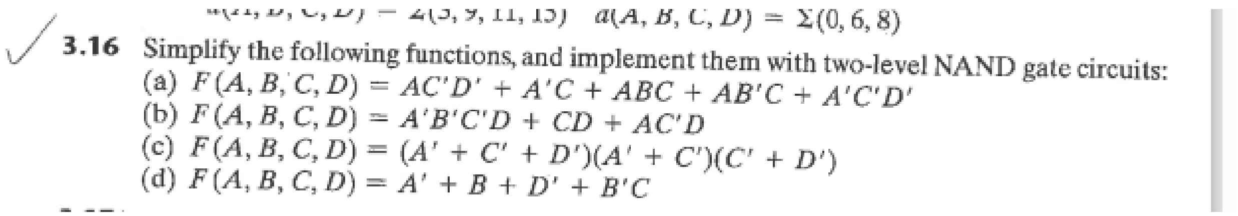
Chapter 3



(f) $F(w, x, y, z) = \Sigma(0, 1, 2, 3, 7, 8, 10, 15)$

3.10 Simplify the following Boolean functions by first finding the essential prime implicants:

(a) $F(w, x, y, z) = \Sigma(0, 2, 5, 7, 8, 10, 12, 13, 14, 15)$
(b) $F(A, B, C, D) = \Sigma(0, 2, 3, 5, 7, 8, 10, 11, 14, 15)$
(c)* $F(A, B, C, D) = \Sigma(1, 3, 4, 5, 10, 11, 12, 13, 14, 15)$
(d) $F(w, x, y, z) = \Sigma(0, 1, 4, 5, 6, 7, 9, 11, 14, 15)$
(e) $F(A, B, C, D) = \Sigma(0, 1, 3, 7, 8, 9, 10, 13, 15)$
(f) $F(w, x, y, z) = \Sigma(0, 1, 2, 4, 5, 6, 7, 10, 15)$

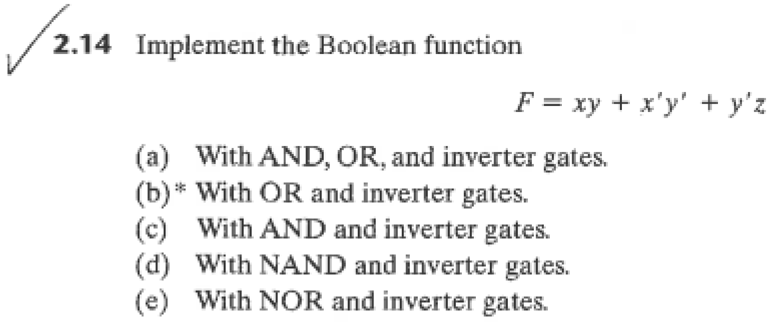


$F(A, B, C, D) = \Sigma(3, 9, 11, 15)$ $d(A, B, C, D) = \Sigma(0, 6, 8)$

3.16 Simplify the following functions, and implement them with two-level NAND gate circuits:

(a) $F(A, B, C, D) = AC'D' + A'C + ABC + AB'C + A'C'D'$
(b) $F(A, B, C, D) = A'B'C'D + CD + AC'D$
(c) $F(A, B, C, D) = (A' + C' + D')(A' + C')(C' + D')$
(d) $F(A, B, C, D) = A' + B + D' + B'C$

Chapter 2



2.14 Implement the Boolean function

$$F = xy + x'y' + y'z$$

(a) With AND, OR, and inverter gates.
(b)* With OR and inverter gates.
(c) With AND and inverter gates.
(d) With NAND and inverter gates.
(e) With NOR and inverter gates.

Chapter 1

✓ **1.3** Convert the following numbers with the indicated bases to decimal:

(a)* $(4310)_5$ (b)* $(198)_{12}$
(c) $(445)_8$ (d) $(345)_6$

✓ **1.7*** Convert the hexadecimal number 64CD to binary, and then convert it from binary to octal.

1.8 Convert the decimal number 431 to binary in two ways: (a) convert directly to binary; (b) convert first to hexadecimal and then from hexadecimal to binary. Which method is faster?

✓ **1.9** Express the following numbers in decimal:

(a)* $(10110.0101)_2$ (b)* $(16.5)_{16}$
(c)* $(26.24)_8$ (d) $(\text{DABA.B})_{16}$
(e) $(1011.1001)_2$

1.10 Convert the following binary numbers to hexadecimal and to decimal: (a) 1.10010 (b) 110.010. Explain why the decimal answer in (b) is four times that in (a).

1.11 Perform the following division in binary: 111011 ÷ 101.

1.12* Add and multiply the following numbers without converting them to decimal:

(a) Binary numbers 1011 and 101.
(b) Hexadecimal numbers 2E and 34.

✓ **1.13** Do the following conversion problems:

(a) Convert decimal 27.315 to binary.
(b) Calculate the binary equivalent of 2/3 out to eight places. Then convert from binary to decimal. How close is the result to 2/3?
(c) Convert the binary result in (b) into hexadecimal. Then convert the result to decimal. Is the answer the same?

✓ **1.14** Obtain the 1's and 2's complements of the following binary numbers:

(a) 10010000 (b) 00000000
(c) 11011010 (d) 10101010
(e) 10100101 (f) 11111111.

(c) 25,000,000 (d) 00,000,000.

✓ **1.16** (a) Find the 16's complement of C3AF.
(b) Convert C3AF to binary.
(c) Find the 2's complement of the result in (b).
(d) Convert the answer in (c) to hexadecimal and compare with the answer in (a).

✓ **1.17** Perform subtraction on the given unsigned numbers using the 10's complement of the subtrahend. Where the result should be negative, find its 10's complement and affix a minus sign. Verify your answers.

(a) 6,473 − 5,297 (b) 125 − 1,800
(c) 1,076 − 3,217 (d) 1,631 − 745

✓ **1.18** Perform subtraction on the given unsigned binary numbers using the 2's complement of the subtrahend. Where the result should be negative, find its 2's complement and affix a minus sign.

(a) 10011 − 10010 (b) 100010 − 100110
(c) 1001 − 110101 (d) 101000 − 10101