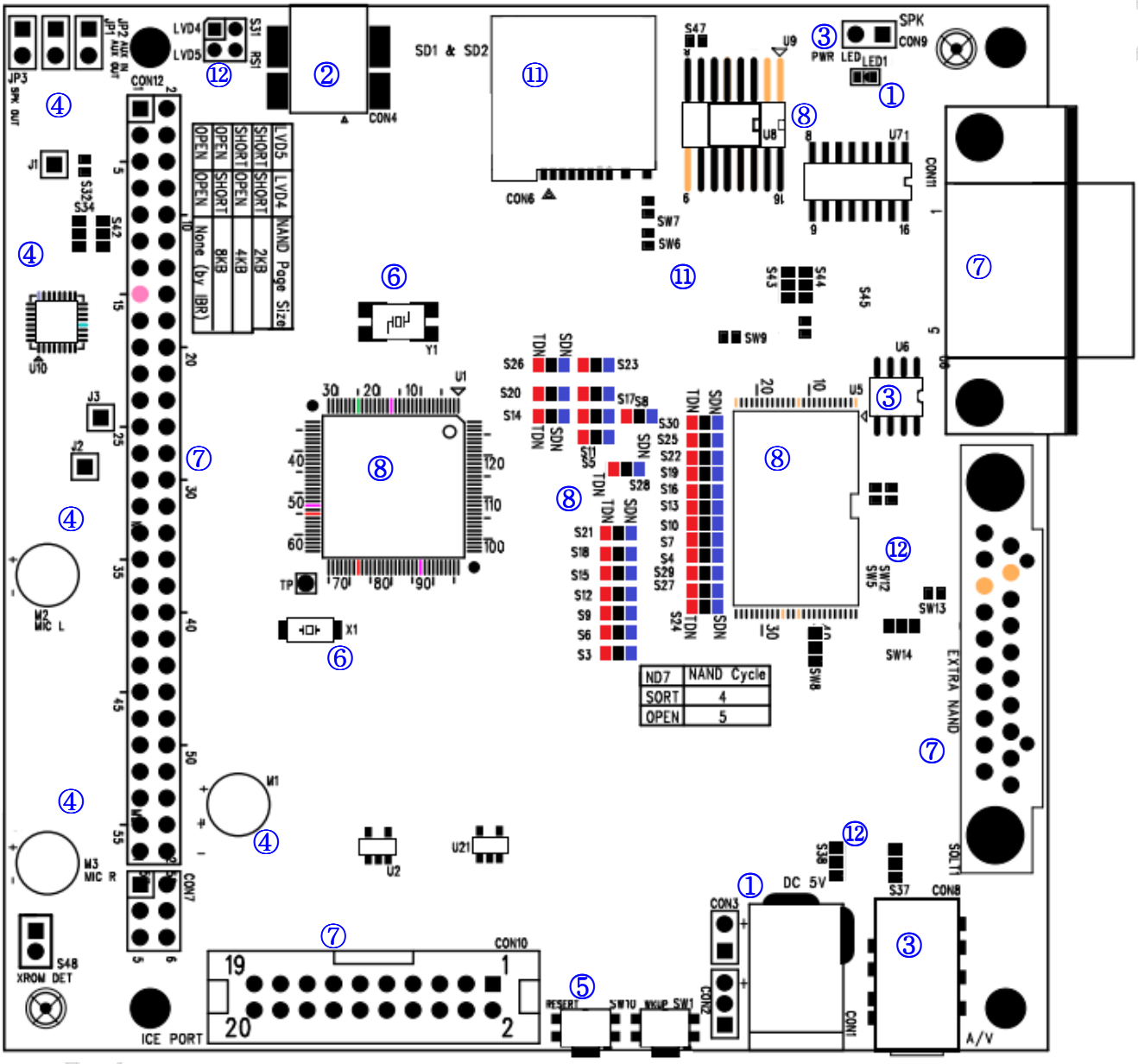
# NHS-55FA93-1-IN-1M14 Demo Board User Manual

## (NHS-55FA93-1-IN-1M14 & NHS-55FA93-1-IN-1D13)

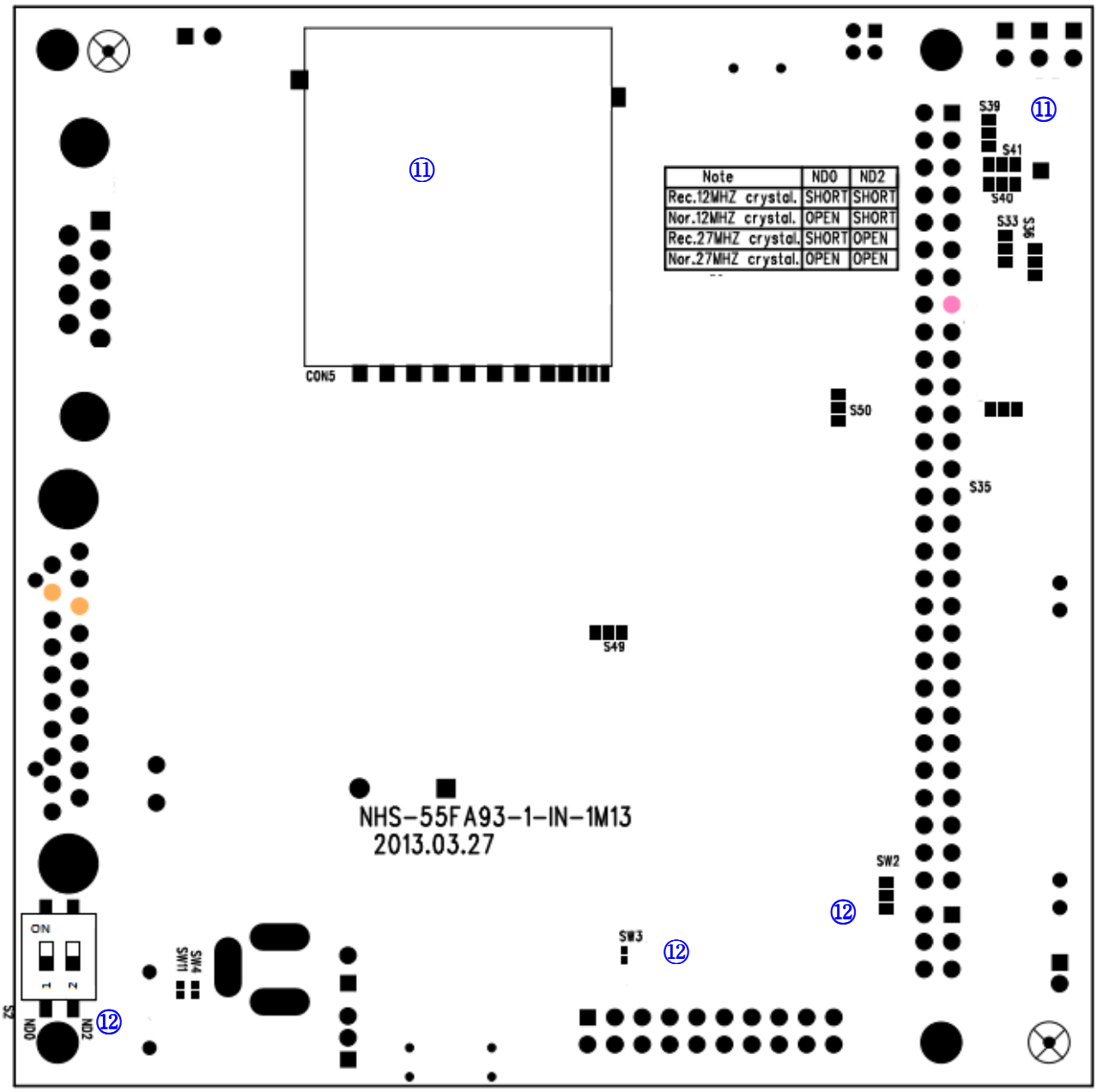
## Rev. A2.4

# 1. NHS-55FA93-1-IN-1M14 Demo Board Functional Description

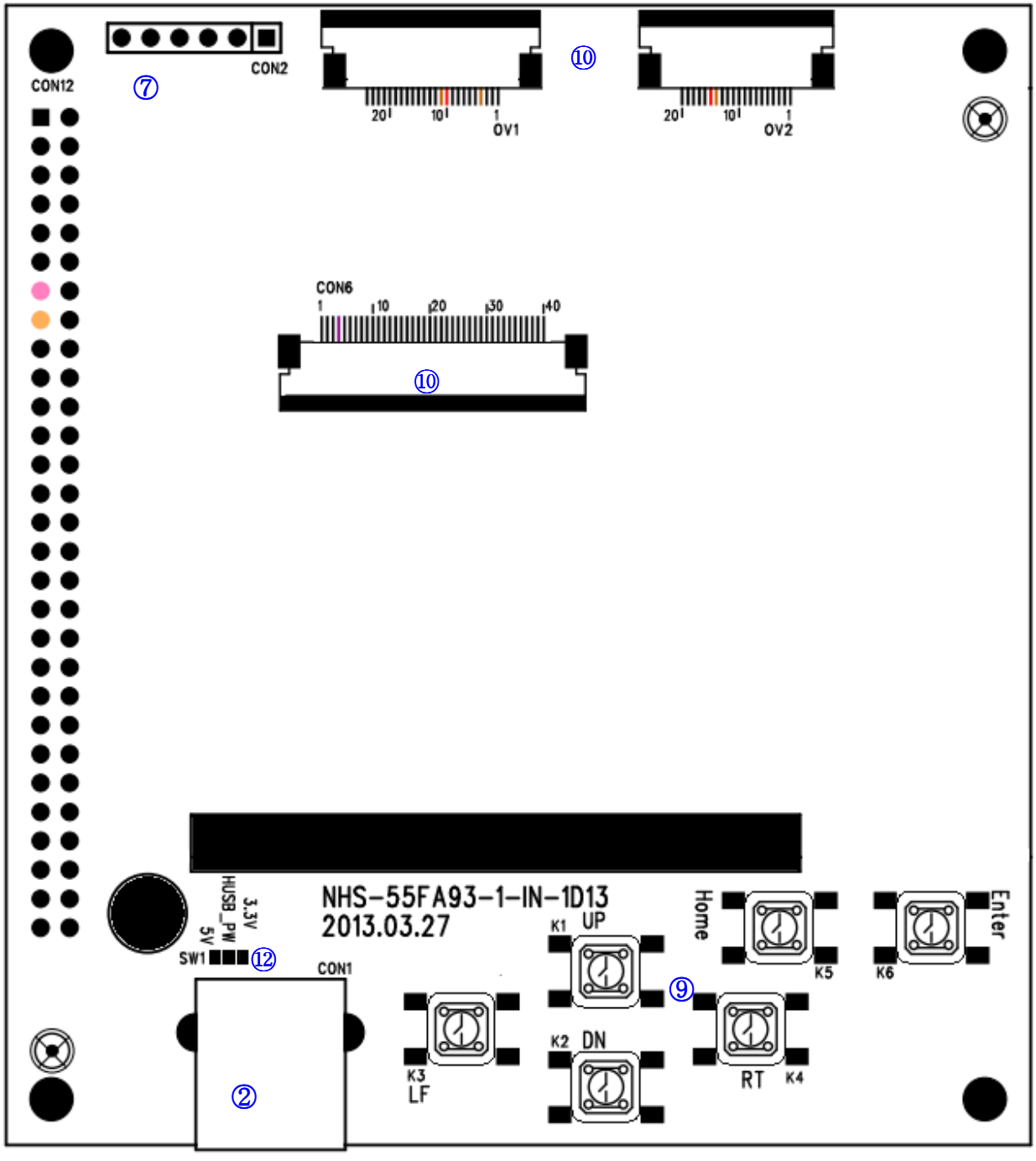
### PCB NHS-55FA93-1-IN-1M14 – Front View:



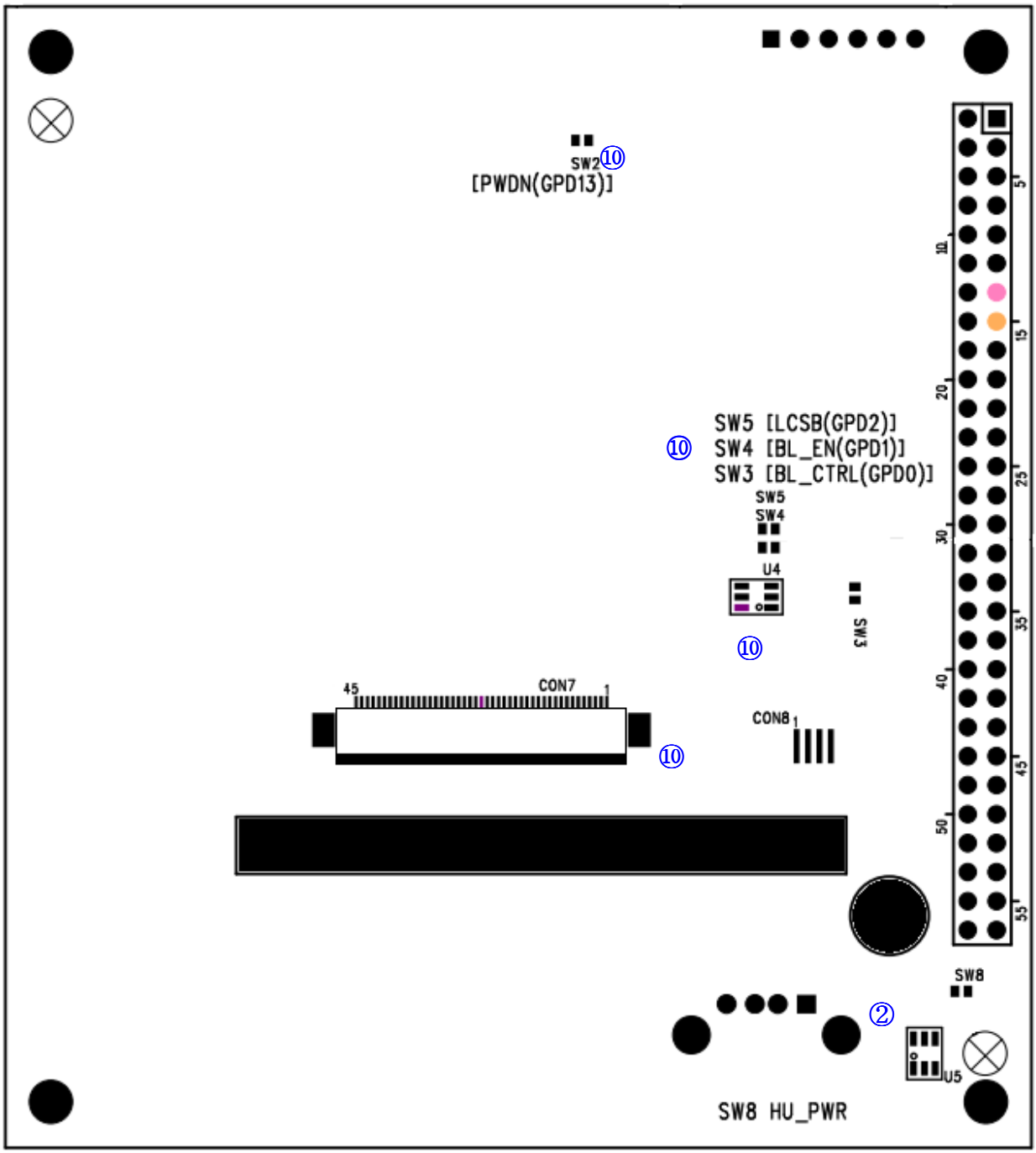
## PCB NHS-55FA93-1-IN-1M14 – Back View:



## PCB NHS-55FA93-1-IN-1D13 – Front View:



## PCB NHS-55FA93-1-IN-1D13 – Back View:



## ① Power Unit:

Generate the power required for system operation.
System operation voltage: 3.3V and 1.8V.

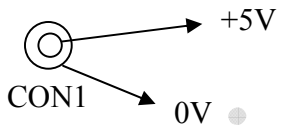


Fig.1 Power adaptor input

- CON1：Power adaptor input, 5V input, polarity as Fig.1
- SW1：When system power is off state and push the SW1 key then PWR LED (LED1) will be lighting and system power will be turn on. When system power is on state and push the SW1 key and holding about 6~7 second, the system power should be auto turn off.
- CON2, 3 (optional)：External battery input connector, if want to connect external battery, the voltage range keep on 3.7V to 4.2V and properly voltage polarity

## ② USB Connector:

- USB connector: CON4, mini-B type USB device port.
- USB connector: CON1(on 1D12 board), A-type USB host port.
- U5: USB host power supply, DC-DC step-up.
- SW8: U5 enable control by GPD3.
- SW1: USB host power selection, one is DC-DC, another is DC 3.3V.

## ③ Audio and Video Ports:

Audio and video output connector:
- CON8：Earphone Jack left and right audio channel out and video composite output.
- CON9：The connector is for Audio power amplifiers speak output.
- U6：ISD8101, audio power amplifier to magnify audio signals DAC0/1 of U1.

## ④ Microphone:

- M1：Condenser microphone, it outputs through RC network to ADC inputs of U1.
- M2 & M3 (optional): Dual auxiliary microphone control by audio codec of U10.
- U10 (optional): External codec, NAU8501, NAU8520 or NAU882x.
- JP1: Auxiliary audio output, for NUA882x only,
- JP2: Auxiliary audio inputs, for NUA882x only.
- JP3: Speaker outputs, for NUA8822 only.
- Selector: S32 ~ S36, the detail setting need to reference external codec specification.

## ⑤ Reset:

- SW10：System reset tack switch, when it pressed once the whole circuits will be enter reset condition.

## ⑥ Main clock source:

- X1：RTC clock source, 32.768KHz.
- Y1：Main clock source, 12MHz or 27MHz, it depends on U1 is N32905U1DN and N32903U1DN or N32905U2DN.

## ⑦ GPA/B/C/D/E/TP, JTAG and UART Extension port:

- GPA/B/C/D/E, Reset, TP, VDD33, VDD18, VSS and VIN control pins as follow :

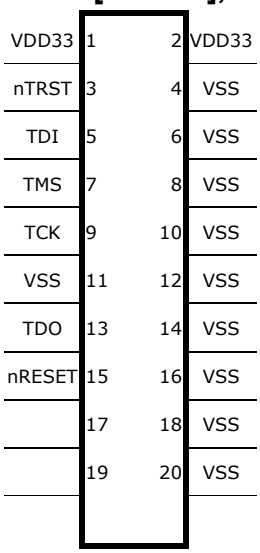
## CON12 (Top board, 1D13) Header 29x2, 2.54mm Male:

| | | | |
|---|---|---|---|
| GPA10 | 1 | 2 | GPA11 |
| GPB6 | 3 | 4 | GPB5 |
| GPB4 | 5 | 6 | GPB3 |
| GPB2 | 7 | 8 | GPB1 |
| GPB0 | 9 | 10 | GPB14 |
| GPA7 | 11 | 12 | GPB13 |
| VDD18 | 13 | 14 | VSS |
| VDD33 | 15 | 16 | VSS |
| GPE0 | 17 | 18 | GPE1 |
| GPC14 | 19 | 20 | GPC15 |
| GPC12 | 21 | 22 | GPC13 |
| GPC10 | 23 | 24 | GPC11 |
| GPC8 | 25 | 26 | GPC9 |
| GPC6 | 27 | 28 | GPC7 |
| GPC4 | 29 | 30 | GPC5 |
| GPC2 | 31 | 32 | GPC3 |
| GPC0 | 33 | 34 | GPC1 |
| GPD10 | 35 | 36 | GPD11 |
| GPB15 | 37 | 38 | GPD9 |
| TP3 | 39 | 40 | TP4 |
| TP1 | 41 | 42 | TP2 |
| nRESET | 43 | 44 | GPD13 |
| GPA6 | 45 | 46 | GPA5 |
| GPA4 | 47 | 48 | GPA3 |
| GPA2 | 49 | 50 | GPA1 |
| GPA0 | 51 | 52 | GPD0 |
| GPD1 | 53 | 54 | GPD2 |
| GPD3 | 55 | 56 | GPD4 |
| VIN | 57 | 58 | VSS |

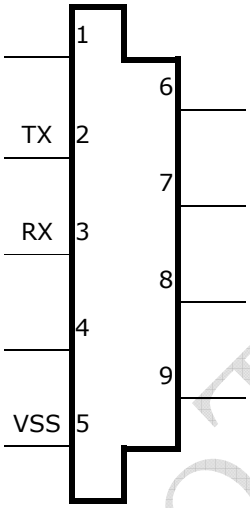
## CON12 (Bottom board, 1M14), Header 29x2, 2.54mm Female:

| | | | |
|---|---|---|---|
| | 1 | 2 | |
| GPB6 | 3 | 4 | GPB5 |
| GPB4 | 5 | 6 | GPB3 |
| GPB2 | 7 | 8 | GPB1 |
| GPB0 | 9 | 10 | GPB14 |
| GPA7 | 11 | 12 | GPB13 |
| VDD18 | 13 | 14 | VSS |
| VDD33 | 15 | 16 | VSS |
| GPE0 | 17 | 18 | GPE1 |
| GPC14 | 19 | 20 | GPC15 |
| GPC12 | 21 | 22 | GPC13 |
| GPC10 | 23 | 24 | GPC11 |
| GPC8 | 25 | 26 | GPC9 |
| GPC6 | 27 | 28 | GPC7 |
| GPC4 | 29 | 30 | GPC5 |
| GPC2 | 31 | 32 | GPC3 |
| GPC0 | 33 | 34 | GPC1 |
| GPD10 | 35 | 36 | GPD11 |
| GPB15 | 37 | 38 | GPD9 |
| TP3 | 39 | 40 | TP4 |
| TP1 | 41 | 42 | TP2 |
| nreset | 43 | 44 | GPD13 |
| GPA6 | 45 | 46 | GPA5 |
| GPA4 | 47 | 48 | GPA3 |
| GPA2 | 49 | 50 | |
| | 51 | 52 | GPD0 |
| GPD1 | 53 | 54 | GPD2 |
| GPD3 | 55 | 56 | |
| VIN | 57 | 58 | VSS |

## JTAG [CON10], Header 10x2 with Housing, 2.54mm 90˚.




## UART [ CON11], D-SUB 9 pins Female :



- **SLOT1, External Flash card Connector.**

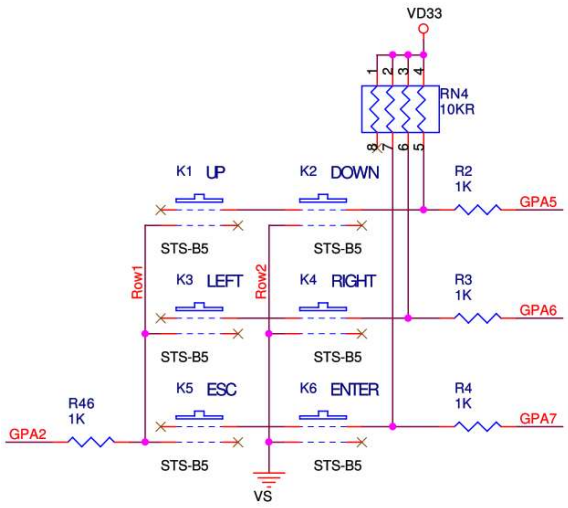
| | | | |
|---|---|---|---|
| RnB2 | 1 | 2 | nRE |
| nCE2 | 3 | 4 | NVDD33 |
| NVDD33 | 5 | 6 | nWP2 |
| nWR | 7 | 8 | ALE |
| CLE | 9 | 10 | MVS |
| MVS | 11 | 12 | ND3 |
| ND2 | 13 | 14 | ND1 |
| ND0 | 15 | 16 | CDET |
| ND4 | 17 | 18 | ND5 |
| ND6 | 19 | 20 | ND7 |

## ⑧ N3290x Series, NAND Memory and Others:

- U1：LQFP128 package of N32905U1DN, N32905U2DN or N32903U1DN.
- U7：UART transceiver, TRS3232EC, TI.
- U5：NAND Flash (optional), HY27UF081G2A, 1Gb memory size.
- U8 or U9：SPI Flash.
- S3~S30: U1 chip control paths selector.

## ⑨ Key Pads:

- Keys：K1~K6.
- Keys input source (GPA2, VSS), output path had GPA5/6/7.
- Key matrix block diagram:




## ⑩ LCM and Sensor Port:

Dedicated connector for proper LCM and CMOS：

- CON6 (optional) for GPG48273QS5 or HSD04319W1-A LCM module pins assignment.
- CON7 for GPM1006E0 LCM module pins assignment.
- CON8 for touch panel on LCM module.
- OV1 for CCS6003 (OV7670 or YT99050CX) CMOS sensor module.
- OV2 (optional) for NK-0314 (OV7725) CMOS sensor module.
- U4, LCM back light LED driver.
- Selector (on 1D12 board):
    - SW3: Back light intensity control by GPD0.
    - Back light enable selection:
        - SW4: Control by GPD1.

- SW9: Always enable by pull-up.
- SW9 & SW5: Control by GPD2.
- SW9 & SW10 (Pin 1 & Pin 2 shorted): Control by GPD11.

- SW10 (Pin & Pin3 shorted): LCM's VDEN signal control by GPD11.
- SW2: CMOS sensor Power down control by GPD13.

## ⑪ SD Card Port:

- CON5 (1M11 board, back side): SD card connector.
- CON6 (1M11 board, front side): mini-SD card connector.
- S39~S44: CON6 control signal selector:
  - S39: SD's D2 signal selection by GPD6 or GPB5.
  - S40: SD's D3 signal selection by GPD5 or GPB4.
  - S41: SD's CMD signal selection by GPD8 or GPB3.
  - S42: SD's CLK signal selection by GPD7 or GPB2.
  - S43: SD's D0 signal selection by GPE9 or GPB1.
  - S44: SD's D1 signal selection by GPE8 or GPB0.

## ⑫ Jumper Setting selection:

- **Power on setting selection (S2, RS1, RS3, RS4 and RS5):**

The Selection definition as follow:

| ND2 | ND0 | Note (S2) |
|---|---|---|
| ON | ON | Recovery mode, 12MHz Crystal |
| ON | OFF | Normal mode, 12MHz Crystal |
| OFF | ON | Recovery mode, 27MHz Crystal |
| OFF | OFF | Normal mode, 27MHz Crystal |

| ND7 (RS3) | NAND Cycles |
|---|---|
| SHORT | 4 |
| OPEN | 5 |

| LVD5 (RS2) | LVD4 (RS1) | NAND Page Size |
|---|---|---|
| SHORT | SHORT | 2KB |
| SHORT | OPEN | 4KB |
| OPEN | SHORT | 8KB |
| OPEN | OPEN | None (by IBR) |

| ND5 (RS5) | ND4 (RS4) | Memory Type |
|---|---|---|
| SHORT | SHORT | SDRAM |
| SHORT | OPEN | LPDDR |
| OPEN | SHORT | DDR |
| OPEN | OPEN | DDR II |

## ⑬ Control function pins assignment:

**NHS-W55FA93xxx Pins Definition**

| N3290xU2DN | | N3290xU1DN | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| No. | Name | No. | Name | GPIO | SPI 0 | SD 0 | SD 1 | SD 2 | USB | HUSB | MPU LCM | LCM(8) | SENSOR | NAND 0 | NAND 1 | UART | I2C | PWR | KEY | AMP | MIC | I2S | TV |
| 1 | SPCLK | 1 | SPCLK | GPB1 | | | D0 | | | | | | SCLK | | | | | | | | | | |
| 2 | SCLKO | 2 | SCLKO | GPB0 | | | D1 | | | | | | SCLKO | | | | | | | | | | |
| 3 | ISDA | 3 | ISDA | GPB14 | | | | | | | | SDA | SIO_D | | | | SDA | | | | | | |
| 4 | ISCK | 4 | ISCK | GPB13 | | | | | | | | SCL | SIO_C | | | | SCL | | | | | | |
| 5 | SPI0_CLK | 5 | SPI0_CLK | GPD12 | CLK | | | | | | | | | | | | | | | | | | |
| 6 | SPI0_CS_ | 6 | SPI0_CS_ | GPD13 | CS | | | | | | | | PWRDN | | | | | | | | | | |
| 7 | SPI0_DI | 7 | SPI0_DI | GPD14 | DO | | | | | | | | | | | | | | | | | | |
| 8 | SPI0_DO | 8 | SPI0_DO | GPD15 | DI | | | | | | | | | | | | | | | | | | |
| 9 | SDDAT[2] | 9 | SDDAT[2] | GPE4 | | D2 | | | | | | | | | | | | | | | | | |
| 10 | SDDAT[3] | 10 | SDDAT[3] | GPE5 | | D3 | | | | | | | | | | | | | | | | | |
| 11 | SDCMD | 11 | SDCMD | GPE6 | | CMD | | | | | | | | | | | | | | | | | |
| 12 | SDCLK | 12 | SDCLK | GPE7 | | CLK | | | | | | | | | | | | | | | | | |
| 13 | SDDAT[0] | 13 | SDDAT[0] | GPE2 | | D0 | | | | | | | | | | | | | | | | | |
| 14 | SDDAT[1] | 14 | SDDAT[1] | GPE3 | | D1 | | | | | | | | | | | | | | | | | |
| 26 | UD_DM | 26 | UD_DM | | | | | | DM | | | | | | | | | | | | | | |
| 27 | UD_DP | 27 | UD_DP | | | | | | DP | | | | | | | | | | | | | | |
| 29 | UD_REXT | 29 | UD_REXT | | | | | | Rext | | | | | | | | | | | | | | |
| 32 | LVDATA[17] | 32 | LVDATA[17] | GPE1 | | | | | | | | | SVSYNC | | | | | | | HP_DET | | | |
| 33 | LVDATA[16] | 33 | LVDATA[16] | GPE0 | | | | | | | | | SHSYNC | | | | | | | AMP_EN | | | |
| 34 | LVDATA[15] | 34 | LVDATA[15] | GPC15 | | | | | | | LD15 | | SPD7 | | | | | | | | | | |
| 35 | LVDATA[14] | 35 | LVDATA[14] | GPC14 | | | | | | | LD14 | | SPD6 | | | | | | | | | | |
| 36 | LVDATA[13] | 36 | LVDATA[13] | GPC13 | | | | | | | LD13 | | SPD5 | | | | | | | | | | |
| 37 | LVDATA[12] | 37 | LVDATA[12] | GPC12 | | | | | | | LD12 | | SPD4 | | | | | | | | | | |
| 38 | LVDATA[11] | 38 | LVDATA[11] | GPC11 | | | | | | | LD11 | | SPD3 | | | | | | | | | | |
| 39 | LVDATA[10] | 39 | LVDATA[10] | GPC10 | | | | | | | LD10 | | SPD2 | | | | | | | | | | |
| 40 | LVDATA[9] | 40 | LVDATA[9] | GPC9 | | | | | | | LD09 | | SPD1 | | | | | | | | | | |

| | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 41 | LVDATA[8] | 41 | LVDATA[8] | GPC8 | | | | | | | LD08 | | SPD0 | | | | | | | | | | |
| 42 | LVDATA[7] | 42 | LVDATA[7] | GPC7 | | | | | | | LD07 | LD07 | | | | | | | | | | | |
| 43 | LVDATA[6] | 43 | LVDATA[6] | GPC6 | | | | | | | LD06 | LD06 | | | | | | | | | | | |
| 44 | LVDATA[5] | 44 | LVDATA[5] | GPC5 | | | | | | | LD05 | LD05 | | | | | | | | | | | |
| 45 | LVDATA[4] | 45 | LVDATA[4] | GPC4 | | | | | | | LD04 | LD04 | | | | | | | | | | | |
| 46 | LVDATA[3] | 46 | LVDATA[3] | GPC3 | | | | | | | LD03 | LD03 | | | | | | | | | | | |
| 47 | LVDATA[2] | 47 | LVDATA[2] | GPC2 | | | | | | | LD02 | LD02 | | | | | | | | | | | |
| 48 | LVDATA[1] | 48 | LVDATA[1] | GPC1 | | | | | | | LD01 | LD01 | | | | | | | | | | | |
| 49 | LVDATA[0] | 49 | LVDATA[0] | GPC0 | | | | | | | LD00 | LD00 | | | | | | | | | | | |
| 50 | LVDEN | 50 | LVDEN | GPD11 | | | | | | | RS | LVDEN | | | | | | | | | | | |
| 51 | LVSYNC | 51 | LVSYNC | GPD10 | | | | | | | RD | LVSYNC | | | | | | | | | | | |
| 52 | LHSYNC | 52 | LHSYNC | GPD9 | | | | | | | WR | LHSYNC | | | | | | | | | | | |
| 54 | LPCLK | 54 | LPCLK | GPB15 | | | | | | | CS | LPCLK | | | | | | | | | | | |
| 57 | ADC_TP_YM | 57 | ADC_TP_YM | | | | | | | | YM | YM | | | | | | | | | | | |
| 58 | ADC_TP_XM | 58 | ADC_TP_XM | | | | | | | | XM | XM | | | | | | | | | | | |
| 59 | ADC_TP_XP | 59 | ADC_TP_XP | | | | | | | | XP | XP | | | | | | | | | | | |
| 60 | ADC_TP_YP | 60 | ADC_TP_YP | | | | | | | | YP | YP | | | | | | | | | | | |
| 62 | ADC_AIN[0] | 62 | ADC_AIN[0] | | | | | | | | | | | | | | | | | | MICP | | |
| 63 | ADC_AIN[1] | 63 | ADC_AIN[1] | | | | | | | | | | | | | | | | | | MICN | | |
| 64 | ADC_AIN[2] | 64 | ADC_AIN[2] | | | | | | | | | | | | | | | | | | | | |
| 66 | ADC_AIN[3] | 66 | ADC_AIN[3] | | | | | | | | | | | | | | | | | | | | |
| 69 | RTC_WAKE_ | 69 | RTC_WAKE_ | | | | | | | | | | | | | | | ON/OFF | | | | | |
| 70 | RTC_PWREN_ | 70 | RTC_PWREN_ | | | | | | | | | | | | | | | EN | | | | | |
| 108 | GPA[7] | 103 | GPA[7] | GPA7 | | | | | | | | | | | | | | | OUT | | | | |
| 73 | GPA[6] | 73 | GPA[6] | GPA6 | | | | | | | | | | | | | | | OUT | | | | |
| 74 | GPA[5] | 74 | GPA[5] | GPA5 | | | | | | | | | | | | | | | OUT | | | | |
| 75 | GPA[4] | 75 | GPA[4] | GPA4 | | | | | | H_DM | | | | | | | | | | | | | |
| 76 | GPA[3] | 76 | GPA[3] | GPA3 | | | | | | H_DP | | | | | | | | | | | | | |
| 77 | GPA[2] | 77 | GPA[2] | GPA2 | | | | | | | | | | | | | | | IN | | | | |
| 78 | GPA[1] | 78 | GPA[1] | GPA1 | | CD | | | | | | | | | | | | | | | | | |
| 79 | GPA[0] | 79 | GPA[0] | GPA0 | | WP | | | | | | | | | | | | | | | | | |
| 81 | TCK | 81 | TCK | DPD0 | | | | | | | BL_CTRL | BL_CTRL | | | | | | | | | | | |
| 82 | TMS | 82 | TMS | GPD1 | | | | | | | BL_EN | BL_EN | | | | | | | | | | | |

| | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 83 | TDI | 83 | TDI | GPD2 | | | | | | | | CS | | | CARD_DET | | | | | | | | |
| 84 | TDO | 84 | TDO | GPD3 | | | | | | PWR_EN | | | | | | | | | | HP_DET | | | |
| 85 | TRST_ | 85 | TRST | GPD4 | | | | | | | | | | | | | | | | AMP_EN | | | |
| 86 | UD_CDET | 86 | UD_CDET | | | | | | Det | | | | | | | | | | | | | | |
| 95 | AO_HPOUT_L | 95 | AO_HPOUT_L | | | | | | | | | | | | | | | | | L | | | L |
| 97 | AO_HPOUT_R | 97 | AO_HPOUT_R | | | | | | | | | | | | | | | | | R | | | R |
| 102 | TV_OUT | | | | | | | | | | | | | | | | | | | | | | TV |
| 109 | ND[0] | 104 | ND[0] | | | | | | | | | | | ND0 | ND0 | | | | | | | | |
| 110 | ND[1] | 105 | ND[1] | | | | | | | | | | | ND1 | ND1 | | | | | | | | |
| 111 | ND[2] | 106 | ND[2] | | | | | | | | | | | ND2 | ND2 | | | | | | | | |
| 112 | ND[3] | 107 | ND[3] | | | | | | | | | | | ND3 | ND3 | | | | | | | | |
| 113 | ND[4] | 108 | ND[4] | | | | | | | | | | | ND4 | ND4 | | | | | | | | |
| 114 | ND[5] | 109 | ND[5] | | | | | | | | | | | ND5 | ND5 | | | | | | | | |
| 115 | ND[6] | 110 | ND[6] | | | | | | | | | | | ND6 | ND6 | | | | | | | | |
| 116 | ND[7] | 111 | ND[7] | | | | | | | | | | | ND7 | ND7 | | | | | | | | |
| 117 | NBUSY1_ | 112 | NBUSY1_ | GPD6 | | | | D2 | | | | | | | NBSY | | | | | | | | |
| 118 | NBUSY0_ | 113 | NBUSY0_ | GPD5 | | | | D3 | | | | | | NBSY | | | | | | | | | |
| 119 | NWR_ | 114 | NWR_ | GPD8 | | | | CMD | | | | | | nNWR | nNWR | | | | | | | | |
| 120 | NRE_ | 115 | NRE_ | GPD7 | | | | CLK | | | | | | nNRE | nNRE | | | | | | | | |
| 121 | NCLE | 116 | NCLE | GPE11 | | | CD | CD | | | | | | nNCLE | nNCLE | | | | | | | | |
| 122 | NALE | 117 | NALE | GPE10 | | | | | | | | | | nNALE | nNALE | | | | | | | | |
| 123 | NCS1_ | 118 | NCS1_ | GPE9 | | | | D0 | | | | | | | nNCS | | | | | | | | |
| 125 | NCS0_ | 120 | NCS0_ | GPE8 | | | | D1 | | | | | | nNCS | | | | | | | | | |
| 127 | URTXD | 122 | URTXD | GPA10 | | | | | | | | | | | | TXD | | | | | | | |
| 128 | URRXD | 123 | URRXD | GPA11 | | | | | | | | | | | | RXD | | | | | | | |
| | | 124 | SPDATA[1] | GPB6 | | | CD | CD | | | | | | | CARD_DET | | | | | | | DI | |
| | | 125 | SPDATA[0] | GPB5 | | | D2 | | | | | | | | | | | | | | | DO | |
| | | 126 | SFIELD | GPB4 | | | D3 | | | | | | | | | | | | | | | WS | |
| | | 127 | SVSYNC | GPB3 | | | CMD | | | | | | | | | | | | | | | BCLK | |
| | | 128 | SHSYNC | GPB2 | | | CLK | | | | | | | | | | | | | | | MCLK | |

# 2. Document Revision History

| Date | Revision | Remarks |
|---|---|---|
| 10/31/2012 | A1.0 | Formal release version A1.0 |
| 06/06/2013 | A2.0 | Circuit modify, add memory selection and voltage setting. |
| 07/03/2013 | A2.1 | Modified Control Funcion Pin Assignment Table, Page 15. |
| 08/06/2013 | A2.2 | Add Schematic Revision History on Circuit Drawing. |
| 01/08/2013 | A2.3 | 1. Change Components layout footprint:<br>(1M14: CON5 (Page 5), CP14 (Page 2), S2 (Page 6), CP25 & M1(Page 7)).<br>2. Add CB37 for ADC power noise filter (1M14, Page 2).<br>3. Add R37 & R38 for microphone input cascade resisters (1M14, Page 7).<br>4. Add S51 for de-selected Winbond SPI flash 256Mb reset input (1M14, Page 6). |
| 12/09/2014 | A2.4 | Change document title with NHS-55FA93-1-IN-1M14 DEMO BOARD USER MANUAL. |



**Important Notice**

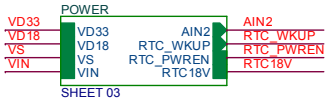
**NuvoTon products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Furthermore, NuvoTon products are not intended for applications wherein failure of NuvoTon products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.**

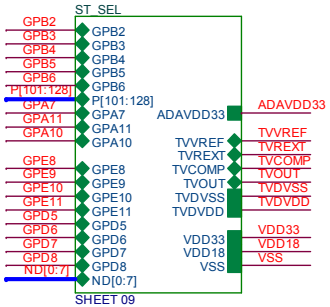
**NuvoTon customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify NuvoTon for any damages resulting from such improper use or sales.**

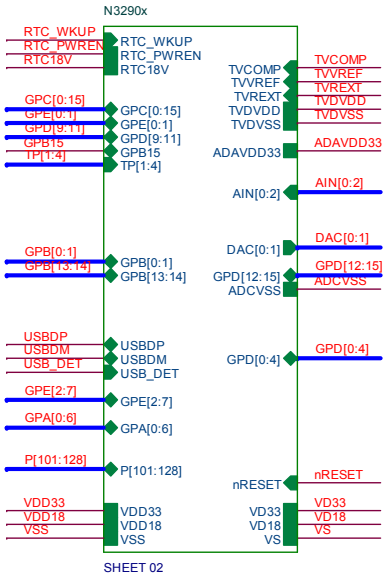
# 3. Schematics

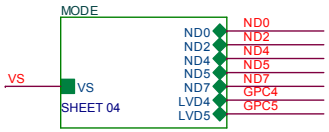
Schematic 1：NHS-55FA93-1-IN-1M14 V1.0, TOP

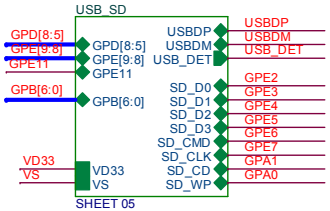
| Revision | Date | Comments |
|---|---|---|
| NHS-55FA93TDN DB V1.0 | 2010/11/1 | New Created. |
| NHS-55FA93TDN DN V2.0<br>NHS-55FA95TDN DN ADD-ON V2.0 | 2010/12/6<br>2010/12/8 | 1. Fixed MVDD/s L5 power source from 3.3V to 1.8V (Page 2).<br>2. Add over-voltage protect circuit from input power supply (Page 3).<br>3. Move Sensor interface circuit to ADD-ON board.<br>4. Move LCM interface circuit to ADD-ON board.<br>5. Add S3~S30 selector for SDN & TDN chip different pins selection. |
| NHS-55[redacted]A93[redacted]DN DB V2.1<br>NHS-55[redacted]A93[redacted]DN DN ADD-ON V2.1 | 2011/7/8<br>2011/6/27 | 1. Add SD2 interface, CON6 & CON2 (DN board, Page 5; ADD-ON, Page1).<br>2. Add extraROM interface, U4 (Page 6).<br>3. Add I2S connector, CON7 (Page 8).<br>4. Add another sensor interface on ADD-ON board, OV2 (Page 2).<br>5. Add USB host-lite interface on ADD-ON board (Page 3).<br>6. Modify key pads from 3x3 to 2x3 on ADD-ON board (Page 3). |
| NHS-55FA93-1-IN-1M11 | 2011/11/25 | 1. Add SD1 interface share with SD2, select by S39~S44 switch pads(1M11, Page 5).<br>2. Change extraROM circuit to external connector, SOLT1 (1M11, Page 6).<br>3. Add NUA8501 & NUA8520 audio optional circuit (1M11, Page 10). |
| NHS-55FA93-1-IN-1D11 | 2011/11/25 | Rename ADD-ON board name from ADD-ON V2.1 to 1D11. |
| NHS-55FA93-1-IN-1M13<br>NHS-55FA93-1-IN-1D13 | 2013/3/28<br>2013/3/28 | 1. Add MCP's memory power selector S49 & S50 from 3.3V or 1.8V (1M11, Page 2).<br>2. Change mode selection with S2 slide switch and RS4/5 for memory type selection (1M13, Page 4).<br>3. Add RS1 for sensor power supply 3.3V selection (1D13, Page 2).<br>4. Add GPM1006E0 3.5" LCM interface (1D13, Page 4). |
| NHS-55FA93-1-IN-1M14 | 2013/10/11 | 1. Change Components layout footprint:<br>(1M14: CON5 (Page 5), CP14 (Page 2), S2 (Page 6), CP25 & M1(Page 7)).<br>2. Add CB37 for ADC power noise filter (1M14, Page 2).<br>3. Add R37 & R38 for microphone input cascade resisters (1M14, Page 7).<br>4. Add S51 for de-selected Winbond SPI flash 256Mb reset input (1M14, Page 6). |

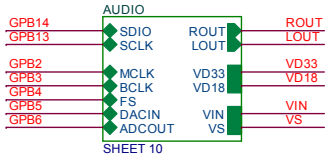


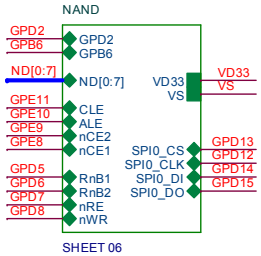



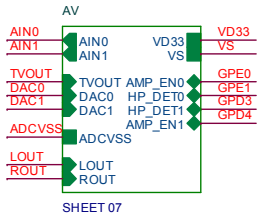



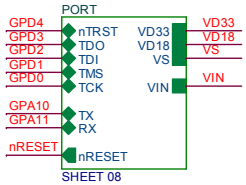



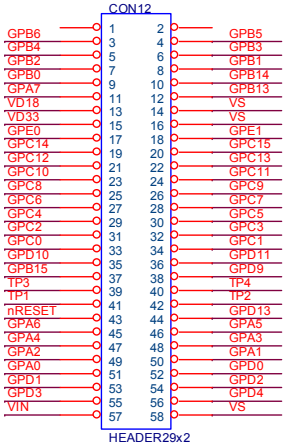



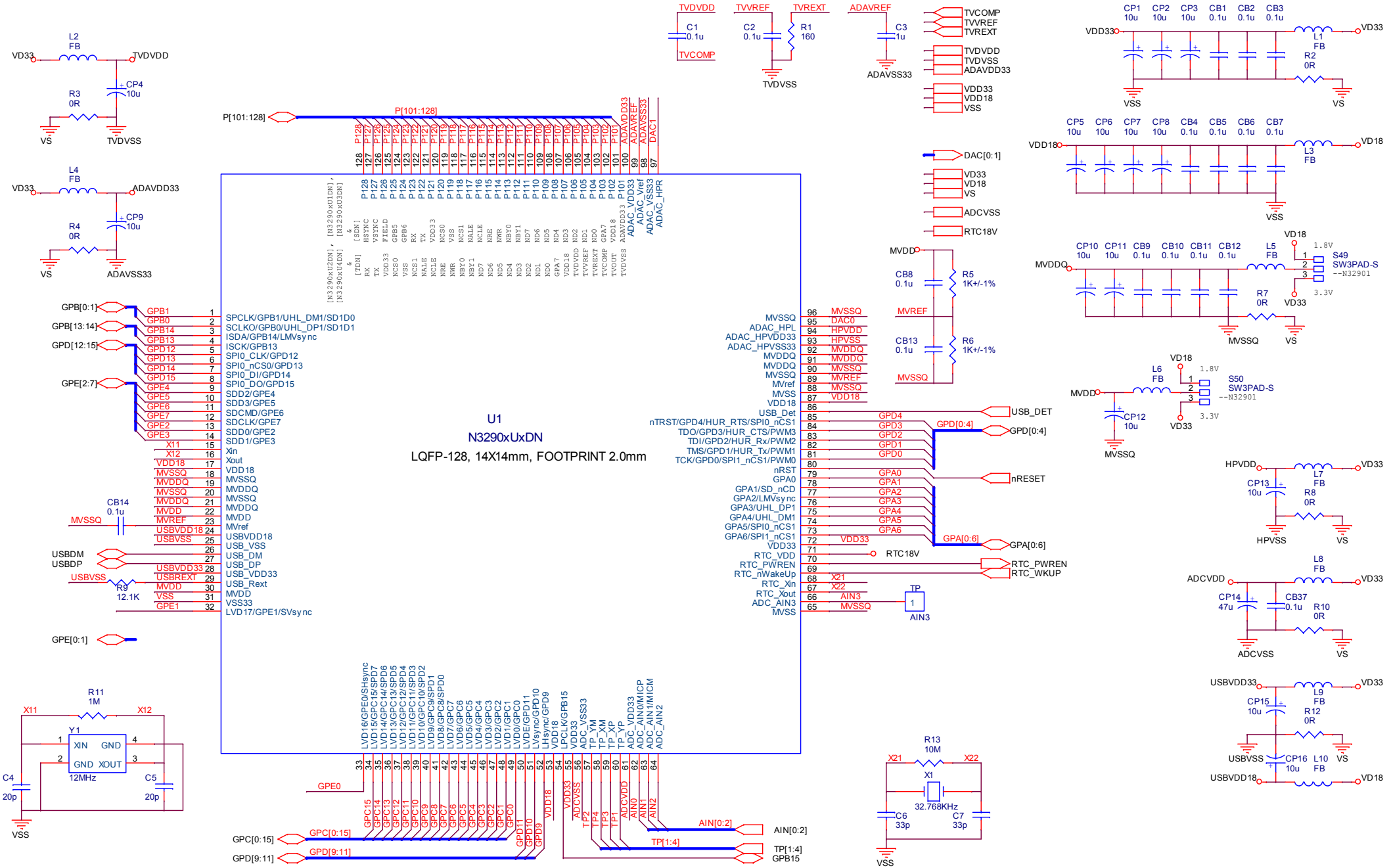



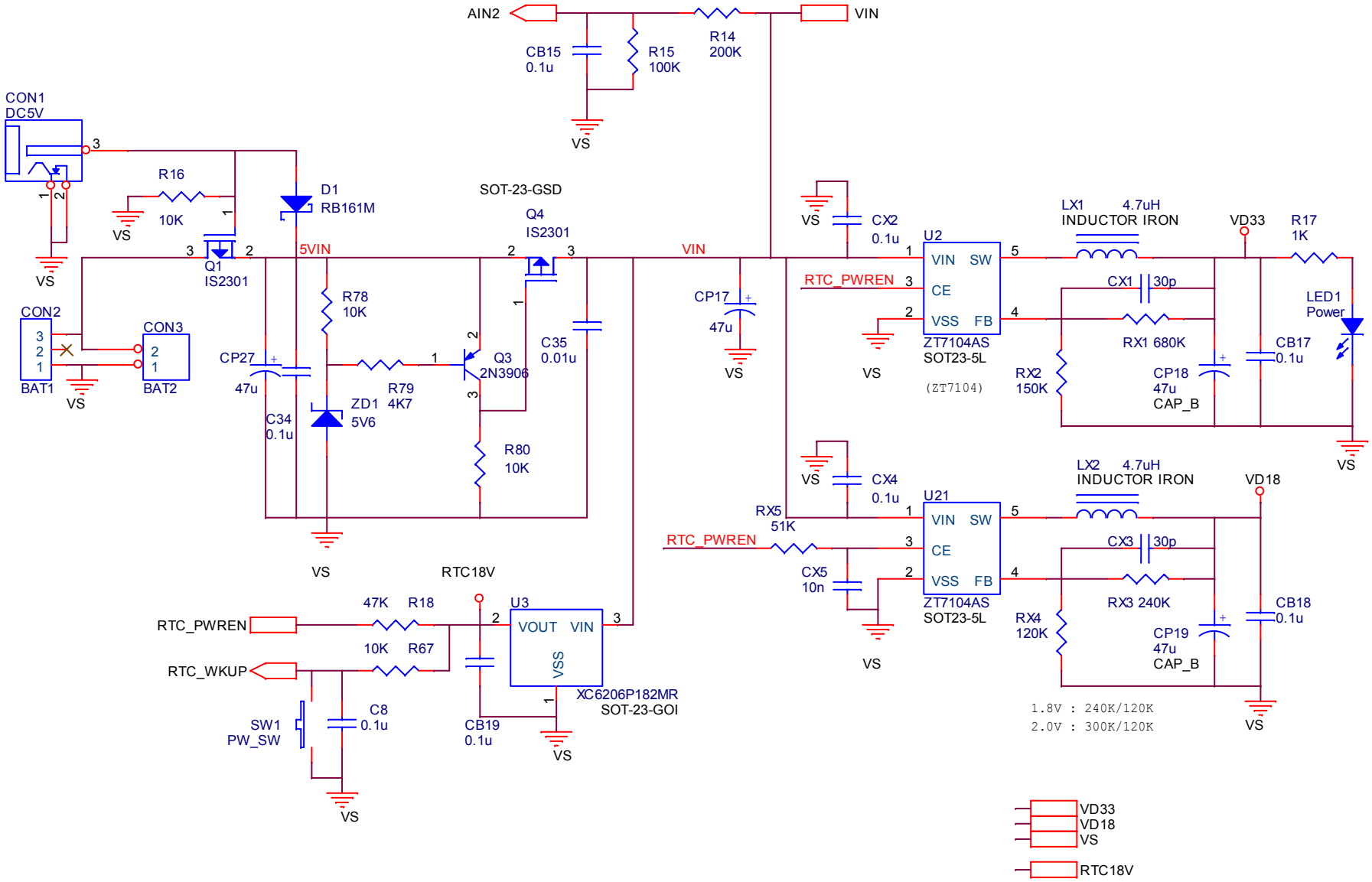



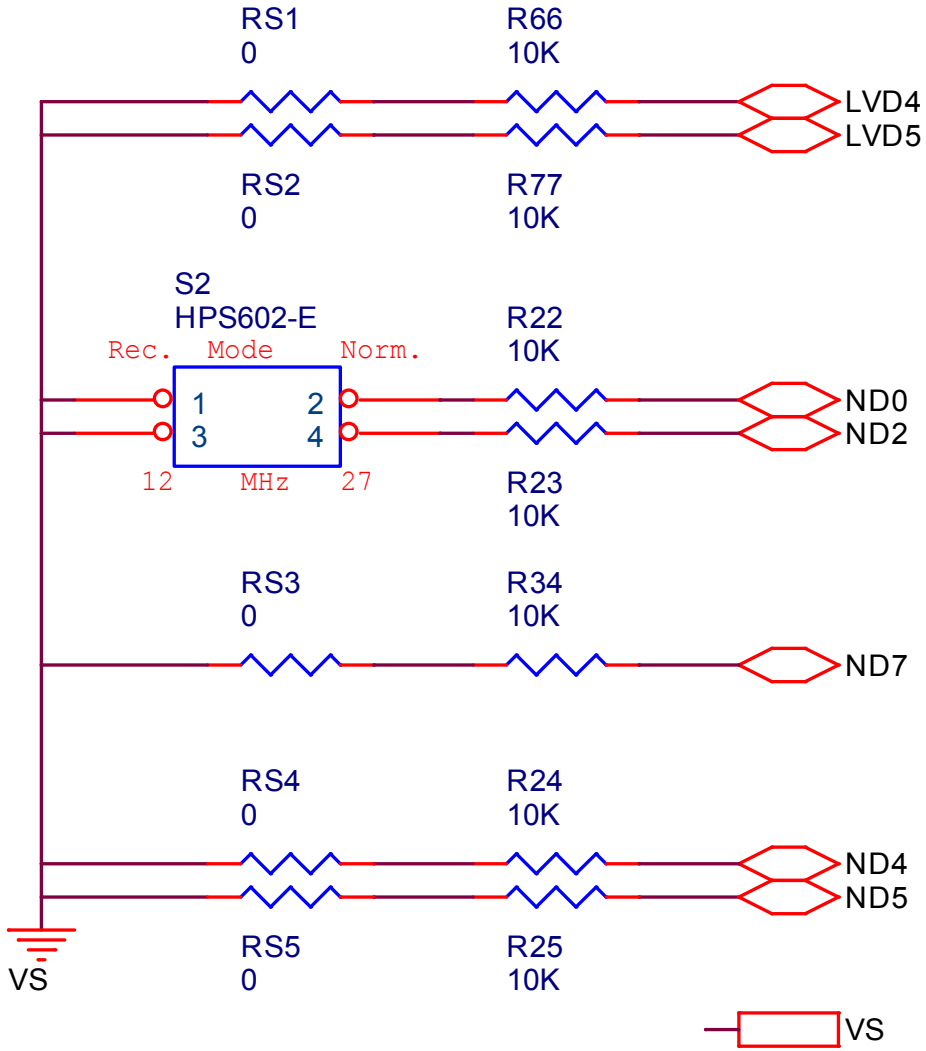
Schematic 2：NHS-55FA93-1-IN-1M14 V1.0, N3290x



Schematic 3：NHS-55FA93-1-IN-1M14 V1.0, POWER



Schematic 4：NHS-55FA93-1-IN-1M14 V1.0, MODE

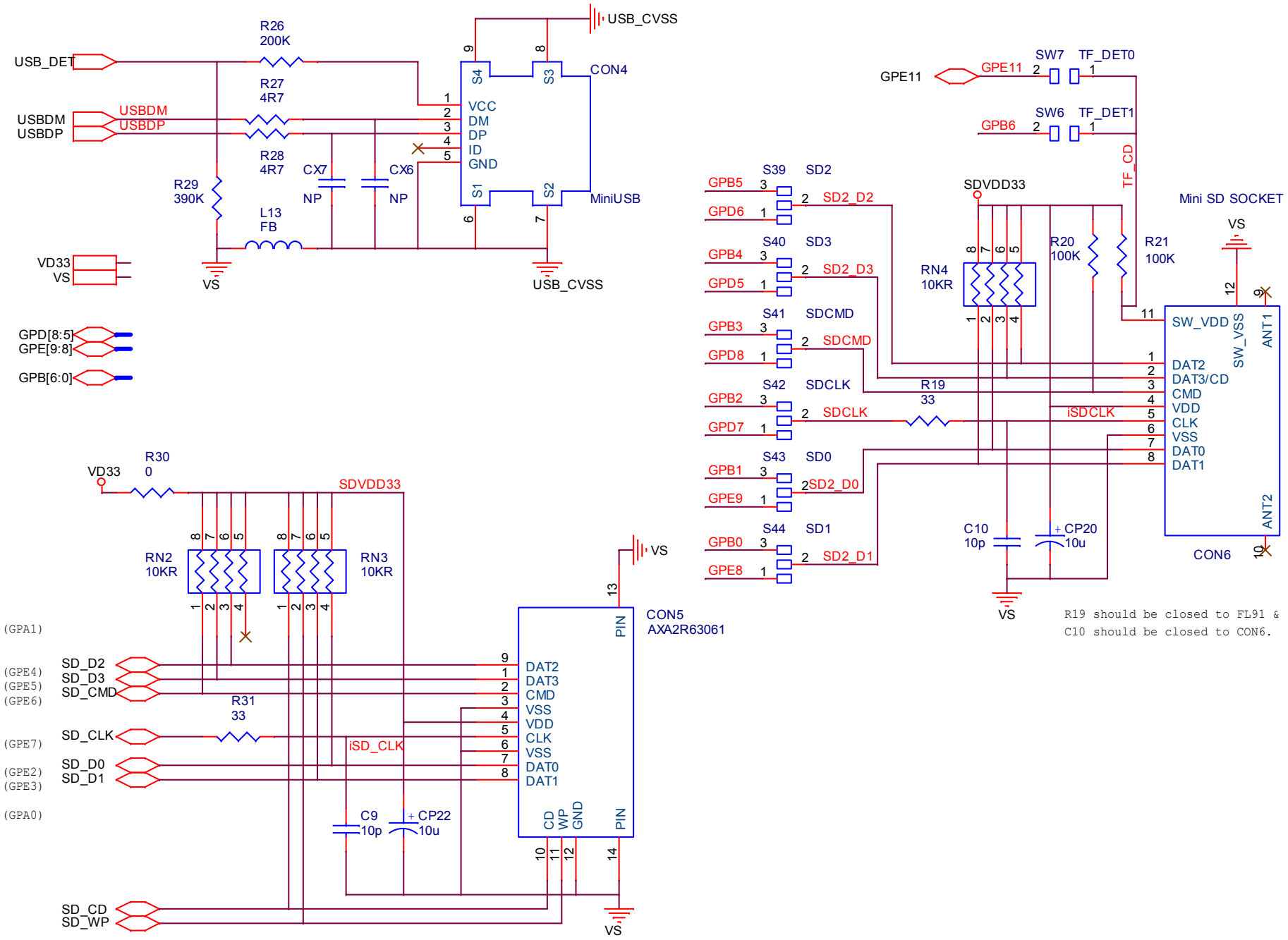



| LVD5(RS2) | LVD4(RS1) | NAND Page Size |
|---|---|---|
| SHORT | SHORT | 2KB |
| SHORT | OPEN | 4KB |
| OPEN | SHORT | 8KB |
| OPEN | OPEN | None (by IBR) |

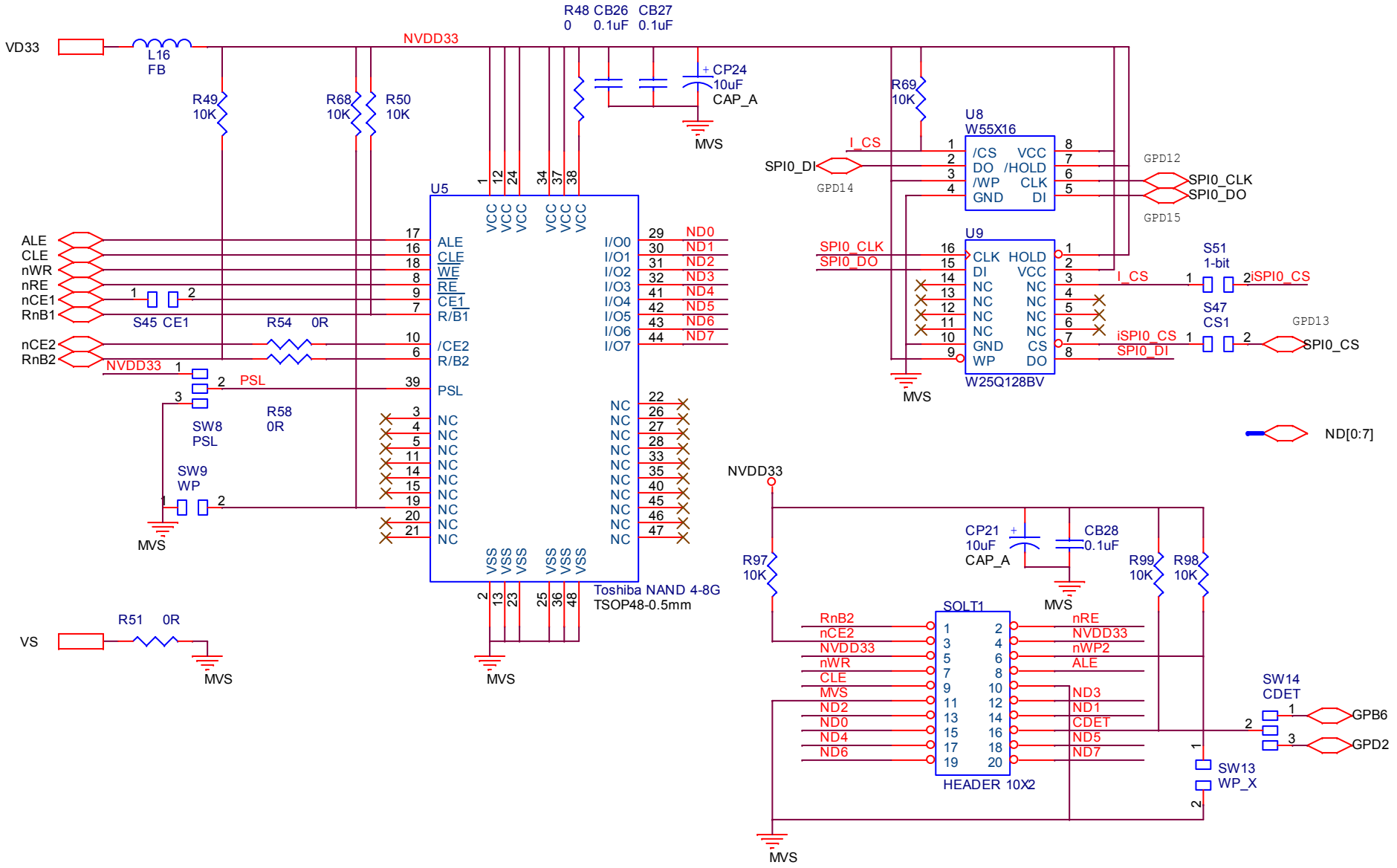
| ND7(RS3) | NAND Cycle |
|---|---|
| SORT | 4 |
| OPEN | 5 |

| ND2 | ND0 | Note |
|---|---|---|
| SHORT | SHORT | Rec. 12MHz crystal. |
| SHORT | OPEN | Nor. 12MHz crystal. |
| OPEN | SHORT | Rec. 27MHz crystal. |
| OPEN | OPEN | Nor. 27MHz crystal. |

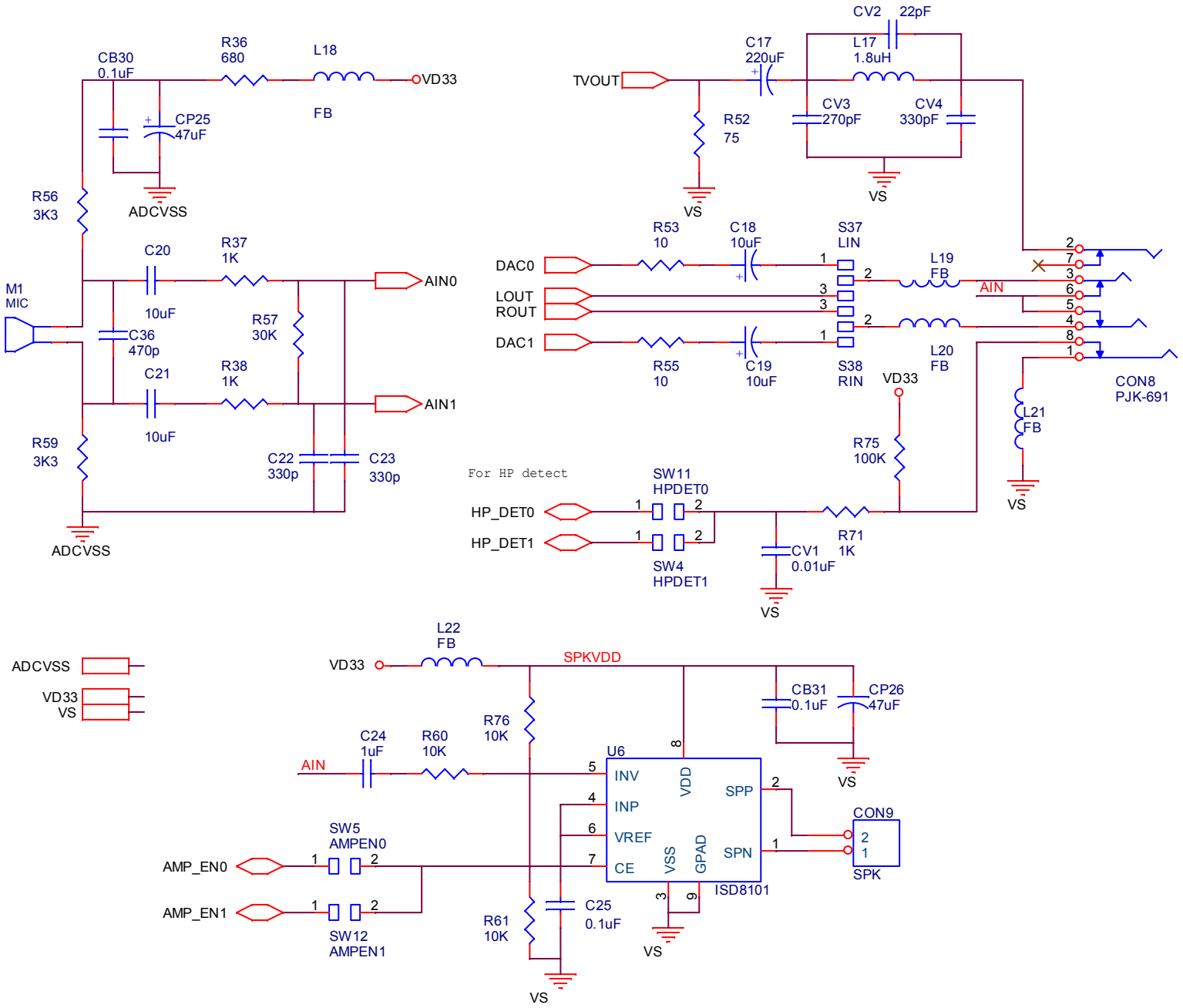
| ND5(RS5) | ND4(RS4) | MEMORY TYPE |
|---|---|---|
| SHORT | SHORT | SDRAM |
| SHORT | OPEN | LPDDR |
| OPEN | SHORT | DDR2 |
| OPEN | OPEN | DDR |

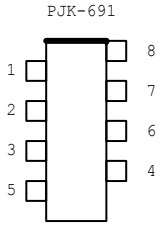


Schematic 6：NHS-55FA93-1-IN-1M14 V1.0, NAND

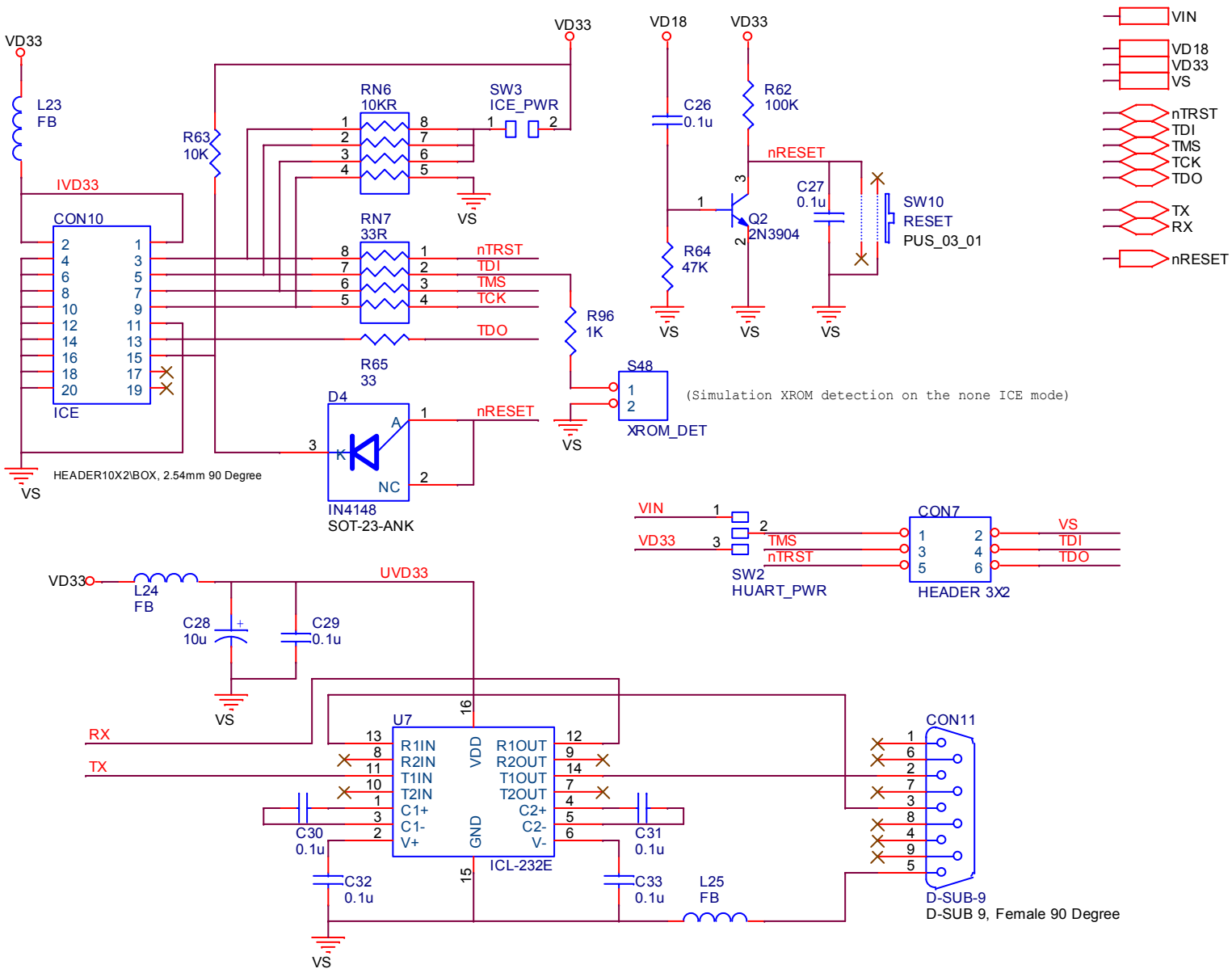


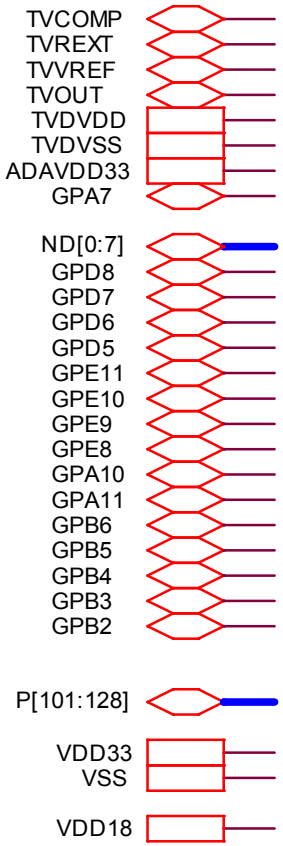
Schematic 7：NHS-55FA93-1-IN-1M14 V1.0, AV



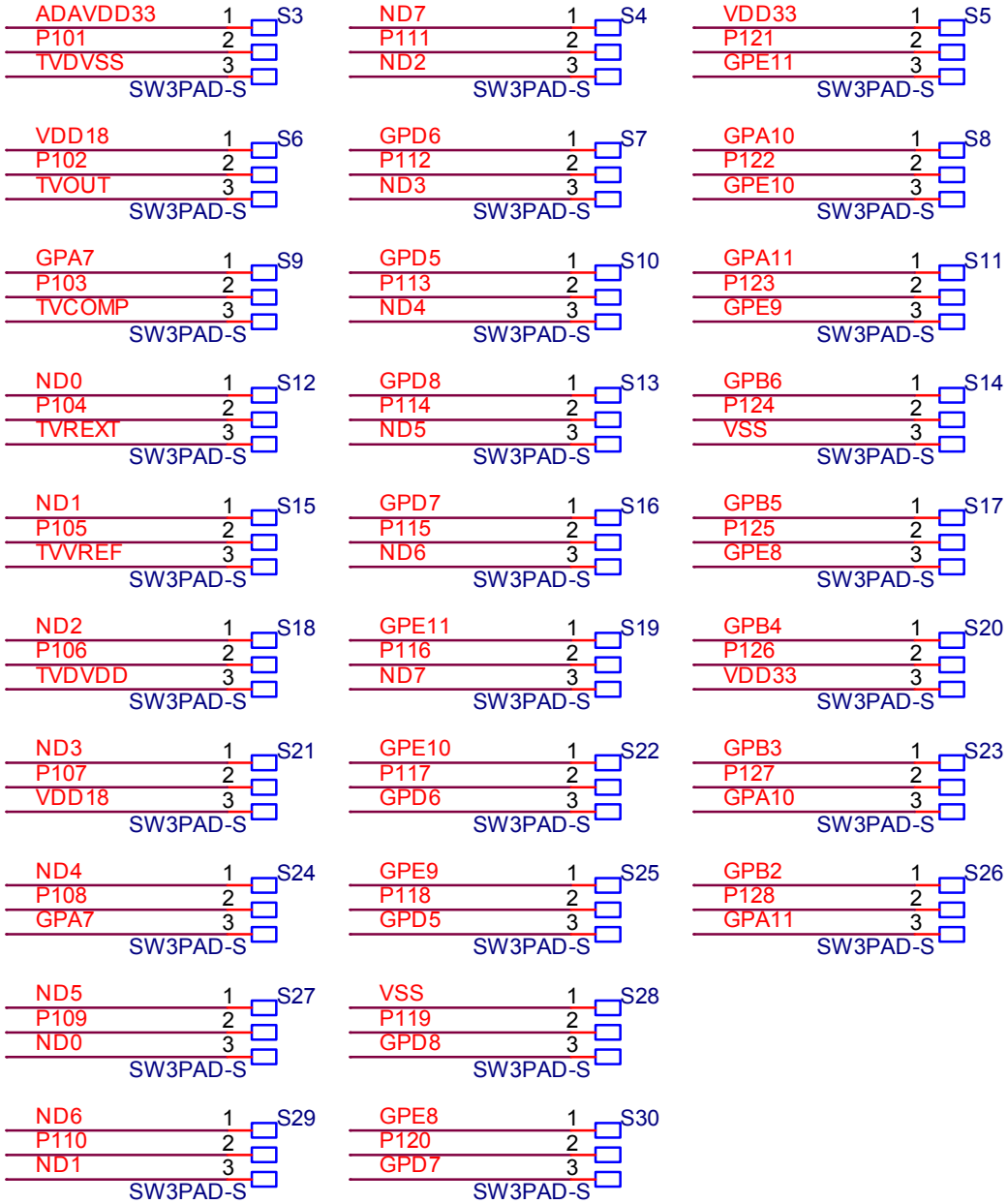
Schematic 8：NHS-55FA93-1-IN-1M14 V1.0, PORT

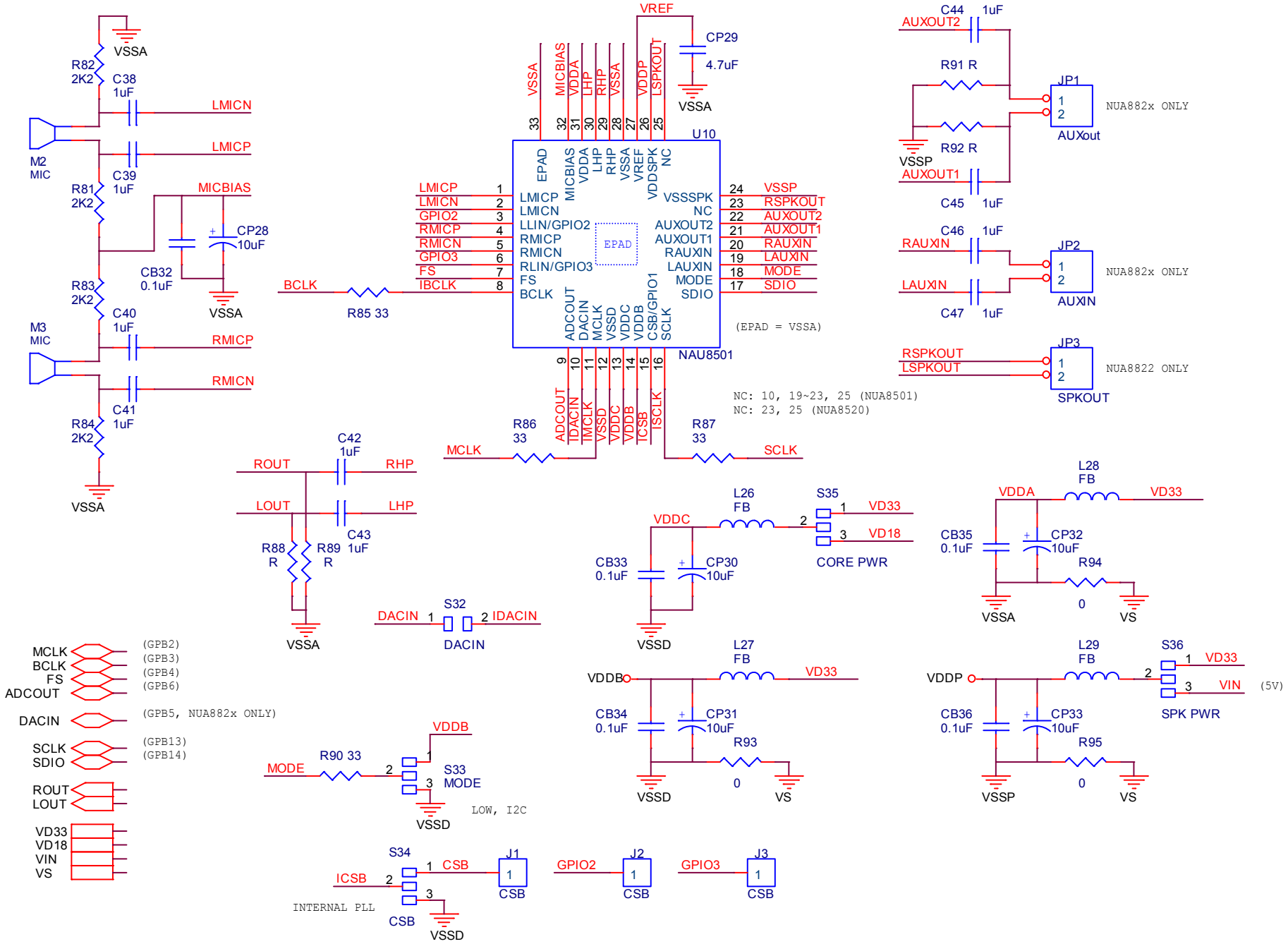


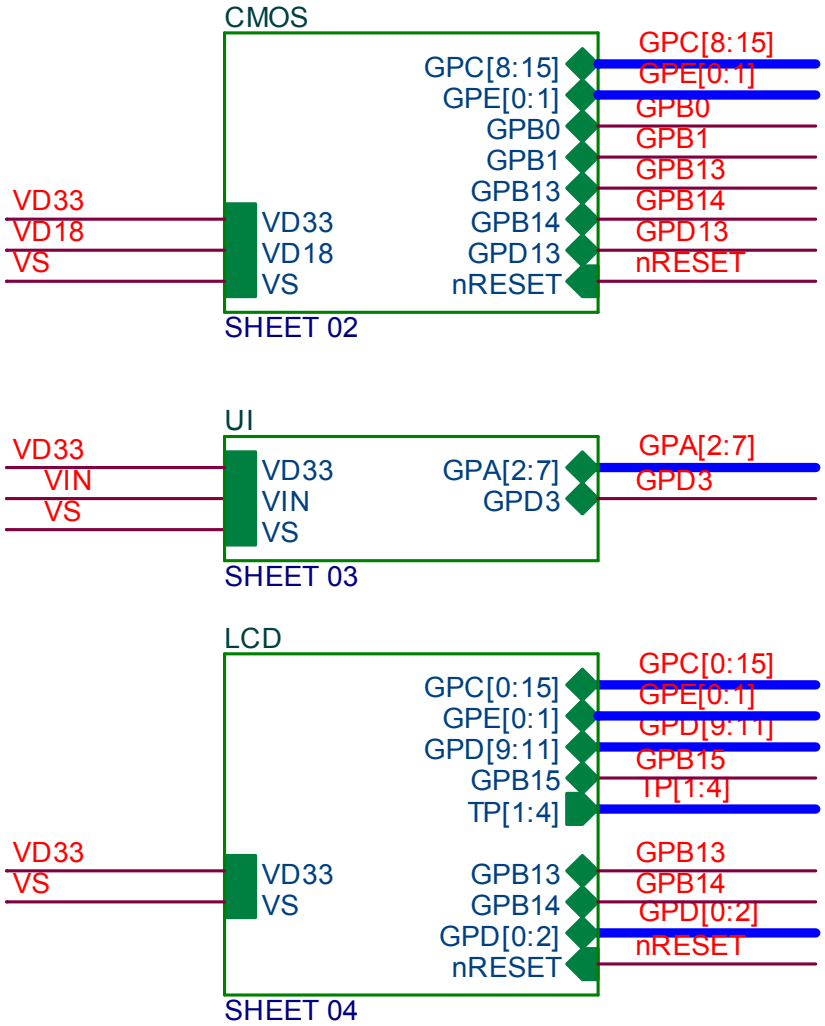



1-2 : N3290xU1DN, N3290xU3DN & W55FA93SDN

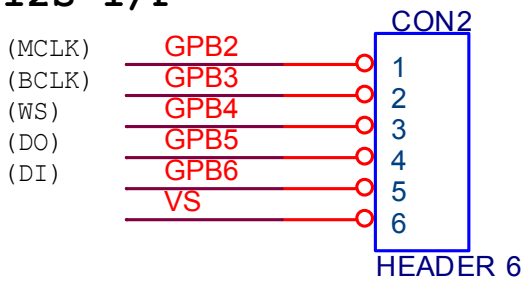
2-3 : N3290xU2DN, N3290xU4DN & W55FA93TDN

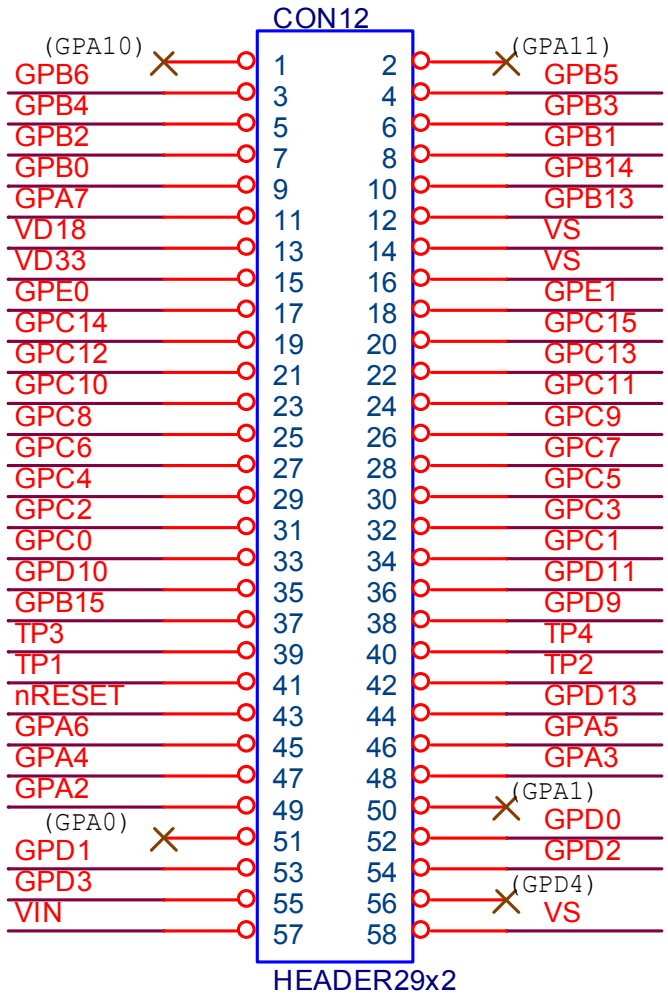


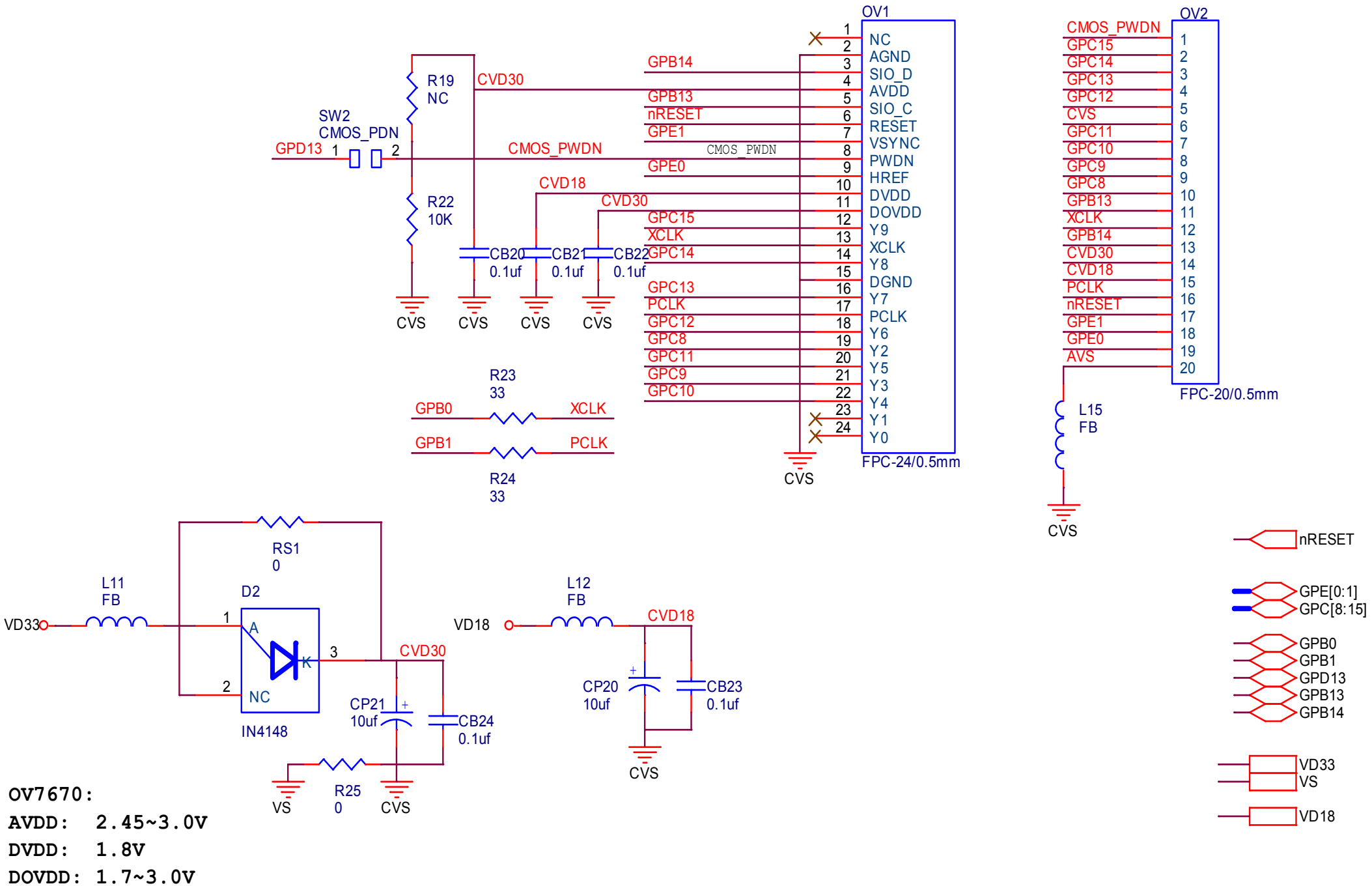





## I2S I/F






**OV7670:**

**AVDD: 2.45~3.0V**

**DVDD: 1.8V**

**DOVDD: 1.7~3.0V**