Experiment No: 10   Date: 24-10-2024

FAMILIARIZATION OF DSP HARDWARE

Aim: To familiarize with the input and output ports of dsp board.
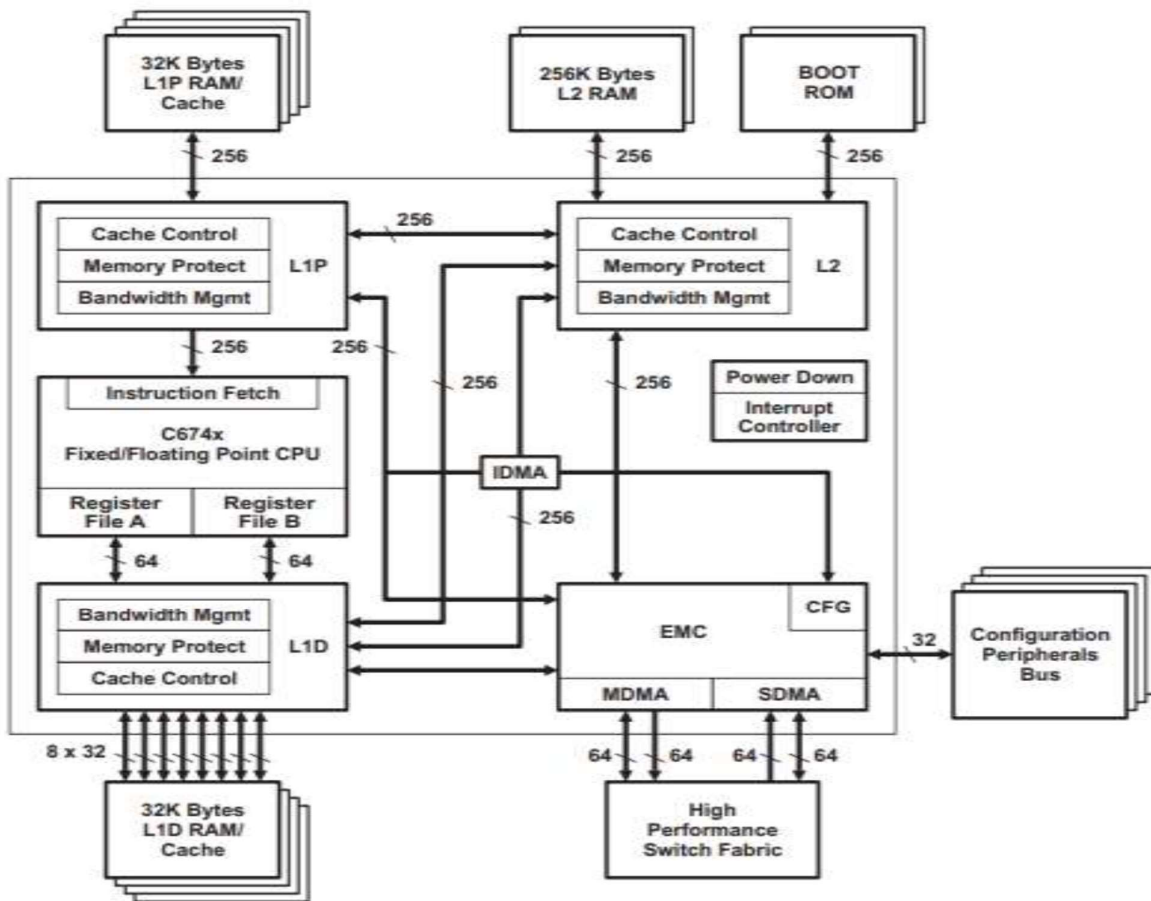
Theory:

TMS 320C674x DSP CPU

FIGURE: TMS320C 674X DSP CPU BLOCK DIAGRAM

The TMS320C674X DSP CPU consists of eight functional units, two register files, and two data paths as shown in Figure. The two general-purpose register files (A and B) each contain 32 32- bit registers for a total of 64 registers. The general-purpose registers can be used for data or can be data address pointers. The data types supported include packed 8-bit data, packed 16-bit data, 32-bit data, 40- bit data, and 64-bit data. Values larger than 32 bits, such as 40-bit-long or 64-bit-long values are stored in register pairs, with the 32 LSBs of data placed in an even register and the remaining 8 or 32 MSBs in the next upper register (which is always an odd-numbered register). The eight functional units (.M1, .L1, .D1, .S1, .M2, .L2, .D2, and .S2) are each capable of executing one instruction every clock cycle. The .M functional units perform all multiply operations. The .S and .L units perform a general set of arithmetic, logical, and branch functions. The .D units primarily load data from memory to the register file and store results from the register file into memory.

Multichannel Audio Serial Port (McASP):
The McASP serial port is specifically designed for multichannel audio applications.
Its key features are:
• Flexible clock and frame sync generation logic and on-chip dividers
• Up to sixteen transmit or receive data pins and serializers
• Large number of serial data format options, including: – TDM Frames with 2 to 32 time slots
per frame (periodic) or 1 slot per frame (burst) – Time slots of 8,12,16, 20, 24, 28, and 32 bits
– First bit delay 0, 1, or 2 clocks – MSB or LSB first bit order – Left- or right-aligned data words within time slots
• DIT Mode with 384-bit Channel Status and 384-bit User Data registers
• Extensive error checking and mute generation logic
• All unused pins GPIO-capable
• Transmit & Receive FIFO Buffers allow the McASP to operate at a higher sample rate by making it more tolerant to DMA latency.
• Dynamic Adjustment of Clock Dividers – Clock Divider Value may be changed without resetting the McASP. The DSK board includes the TLV320AIC23 (AIC23) codec for input and output.
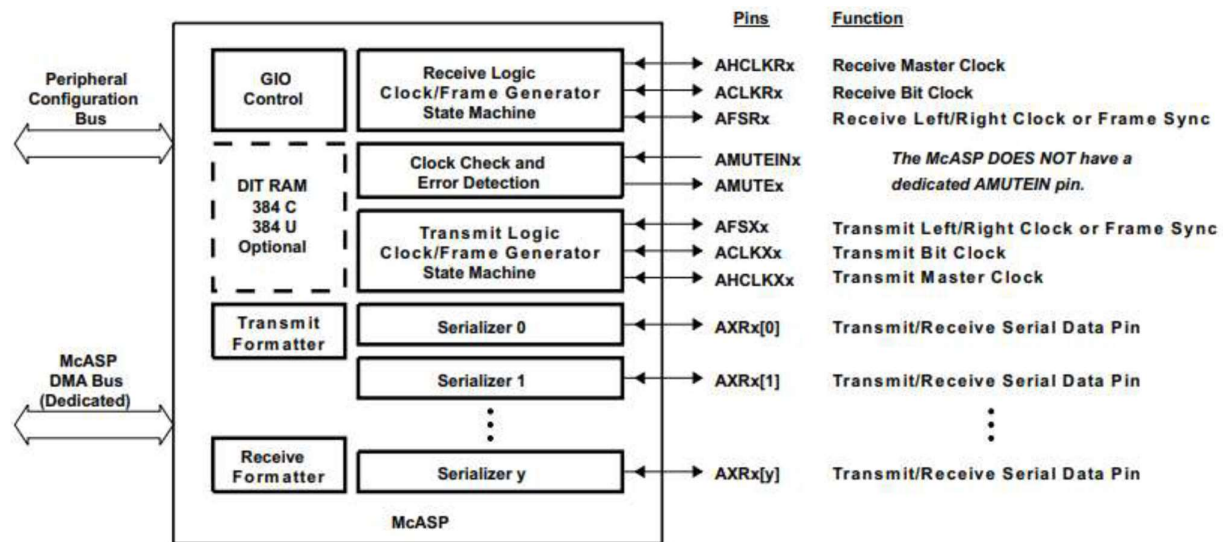The ADC circuitry on the codec converts the input analog signal to a digital representation to be processed by the DSP. The maximum level of the input signal to be converted is determined
by the specific ADC circuitry on the codec, which is 6 V p-p with the onboard codec. After the
captured signal is processed, the result needs.
to be sent to the outside world. DAC, which performs the reverse operation of the ADC. An output filter smooths out or reconstructs the output signal. ADC, DAC, and all required filtering
functions are performed by the single-chip codec AIC23 on board the DSK.

Pins	Function
AHCLKRx	Receive Master Clock
ACLKRx	Receive Bit Clock
AFSRx	Receive Left/Right Clock or Frame Sync
AMUTEINx	*The McASP DOES NOT have a*
AMUTEx	*dedicated AMUTEIN pin.*
AFSXx	Transmit Left/Right Clock or Frame Sync
ACLKXx	Transmit Bit Clock
AHCLKXx	Transmit Master Clock
AXRx[0]	Transmit/Receive Serial Data Pin
AXRx[1]	Transmit/Receive Serial Data Pin
AXRx[y]	Transmit/Receive Serial Data Pin

Result: Familiarized the input and output ports of dsp board.