Lab 05: Simple Arithmetic Logic Unit

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ECEN 248-510
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October 9, 2016

Objectives

The purpose of this lab was to design, implement, and test a simple 4-bit Arithmetic Logic Unit (ALU) that has the ability to perform simple addition and subtraction. This lab also exposes the student to Two's Complement arithmetic and multiplexers.

Design

Experiment 1

This lab had three seperate parts. The first part was modified from the initial lab desing to to the fact that there were not enough AND gates and XOR gates in order to create a 4 bit Ripple Carry Adder. Instead, the 4-bit adder IC was utilizied. Because of this, **Experiment 1** consisted of setting up the 4-bit IC to be connected to a DIP switch to supply the input, operants. Also the CIN was used as a **!Add/Sub** switch. The resulting 4 bit sum was then displayed using four LEDs. The following is a desing of the Circuit that was built.

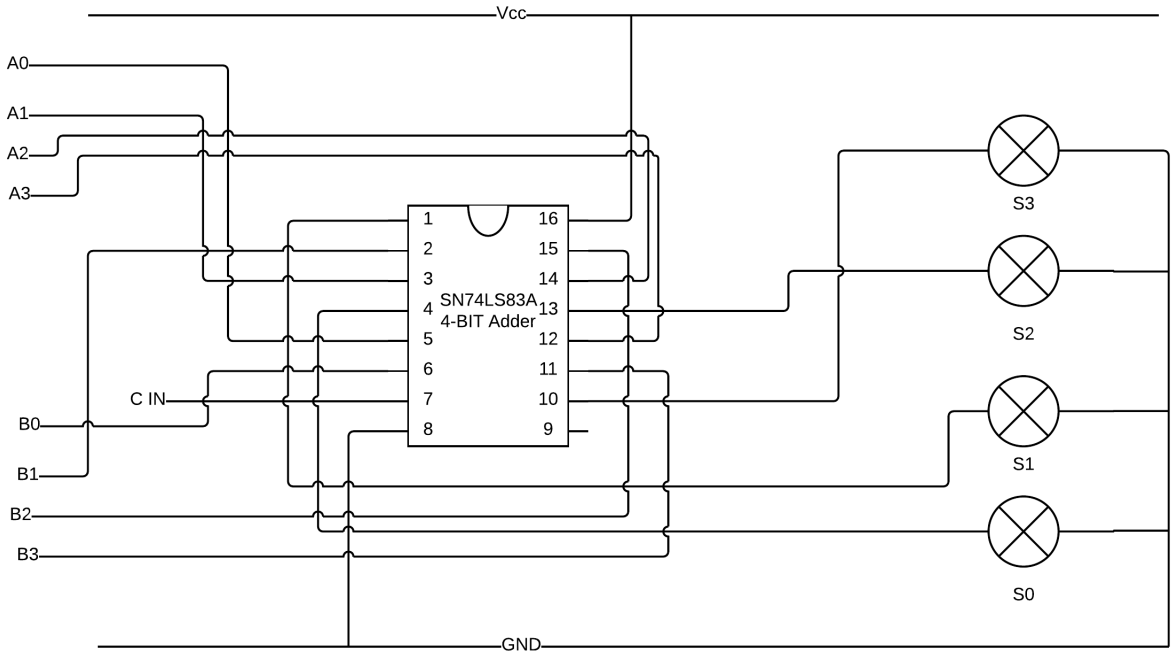


Figure 1: *4-Bit Adder Circuit*

Experiment 2

For the 2nd expirement, on the same breadboard, a 2:1 MUX was used for the first time. The inputs A and B were hardwired for this part. The output was displayed on the LEDs. On the next page is a desing of the Circuit that was built.

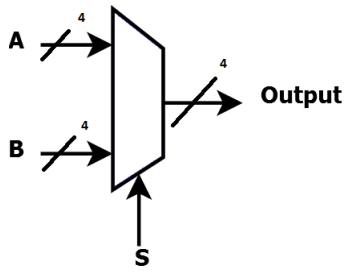


Figure 2: *4-Bit Mux*

Experiment 3

In the 3rd and final part of the lab, the circuits built in **Experiment 1** and **Experiment 2** *(and shown in Fig 1 and Fig 2)* were combined into one circuit. the outputs of **Experiment 1** were the inputs of **Experiment 2**. The outputs of **Experiment 2** were then connected to the LEDs. The inputs were hardwired for this part due to issues with the DIP switch.**c1** and **c0** were also hardwired. The outputs were then connected to 4 LED lights.

Results

Experiment 1

This first part of the lab was able to be comleted rather quickly compared to having to build a 4-bit ripple adder. Due to the fact that we were using a 4-bit adder IC, it was not possible to XOR the values of the last two COUTs. The circuit was able to pass all the test values.

Experiment 2

For the 2nd part, I encountered several issues setting up the None of the LEDs would turn on after the circuit was setup. I first used the multimeter to test to make sure that the power supply was outputing $5V$, which it was. I then checked to make sure the LEDs were recieving $5V$, which it was not. The LEDs were only getting $1.4V$. The issue was then somewhere in between the LEDs and power supply. I then checked the input values *(A and B)* to make sure they were getting the correct voltage, which it was. I was able to find the culprit by testing the output of the MUX. The output was 1.4, the same as the LEDs. I did not see anything wrong with the wiring so decided to replace the MUX IC. After the replacement, the circuit passed all the tests.

Experiment 3

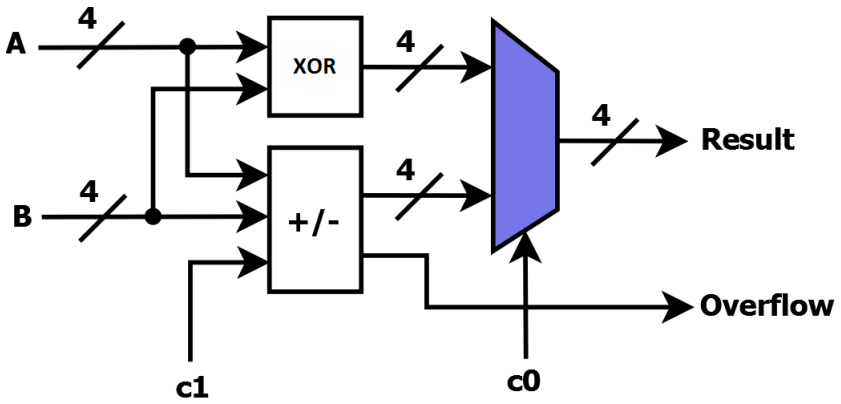
In the final part of the expirement, time became an issue. After constructing the circuit, there was not much time left in lab and it took some time to setup for each test case due to lack of orginaztion when combinging the MUX and the 4-bit adder. I believe that the circiut was setup and functiong properbly because it passed the first three tests but due to time contraints, the final three tests could not be checked.

Conclution

In conclution, this lab taught me a lot on how multiplexors work as well how 4-bit adders functions. I also learned how 2's complement is used in order to have negative numbers in binary. I also learned, yet again, time contraints are a big issue in these labs.

Questions

1. **Provide all design items found in the pre-lab deliverables. If you found that a design needed corrections while executing the lab, supply the updated version of that material.**



2. **Create a table with the following columns: *Control, A, B, Results* and *Overflow.* Fill in sixteen rows of the table with with values from your bread-boaarded circuit, where twelve of the rows show the result of the addition/subtraction unit with at least two rows demonstrate overflow.**

Control	*A*	*B*	*Results*	*Overflow*
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	0	0
1	0	1	1	1
1	1	0	1	0
1	1	1	0	0

Not sure how to make 16 rows with only Control, A, and B

3. **Determine the maximum gate delay through your final ALU circuit assuming each gate has a delay of 1 unit. Highlight the critical path on the gate-level schematic.**
   Using a 4 bit IC and a MUX, the delay would be only 2 units.

4. **Draw a diagram showing how to construct an 8:1 multiplexer from 4:1 and 2:1 multiplexers. Do NOT draw a gate-level schematic.**