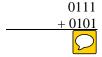
ELEN248 Fall 2015

1st Hour Exam

100points Total

- \*Assume all input variables and their complements are available unless otherwise stated
- \*Answer with minimum complexity (gates, connections, switches) in expression or design expected
- **1. (8pt)** Add the following 2's compliment numbers. Show why there is(not) an overflow.



**3.** (22pt) Given  $f = \Sigma m(0, 1, 7) + d(3)$ 

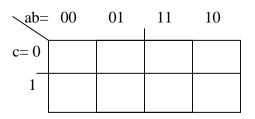
(a 2pt) Fill in the truth table representing the above function

a,b,c		
000		
001		
010		
011		
100		
101		
110		
111		

**2.** (**8pt**) Algebraically reduce /simplify the following function: (hint: x'+y' = (xy)' deMorgan) Z = ((abc+(a'+c')b) + deb)(ab'g + de'f)



(**b 4pt**) Draw **ESSENTIAL** prime implicants (maximal coverings for **minterms**) on the Kernaugh-Map



(c 4pt) Write the minimal SOP expression for the

function f =

(d 4pt) Write the minimal POS(using maxterms) for the

function f=

(e 4pt) Draw AND-OR gate network(diagram)

of the above function		

(f 4pt) Draw the above network using ONLY

NAND gates for function f

**4.** (12pt) A ripple-carry adder design uses a full-adder with unknown internal structure.

Delay values, however, from the inputs to the outputs of the full adder are known and given:

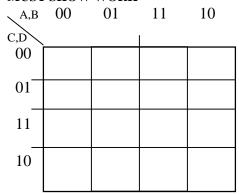
X/Y inputs to Carry-out: 8nS
X/Y inputs to Sum: 4nS

Carry input to Carry-out: 5nS
Carry input to Sum: 3nS

At time=0 all inputs (including carry into the first stage) become simultaneously available for the ripple adder. When (after how man nS) does all the outputs (max of [all sums,carry]) become stable for a 8-bit ripple-carry adder?

**5.** (14pt) A bakery employees Ashley(A), Bud(B), Cortney(C), and Dan(D). We are asked to formulate a logical function for flagging when business possible given the following constraints: Dan can't work with Bud, and Cortney can't work with Ashley. If all of them are missing, obviously we can't open the business. However, when all four of them show up, they just have a party and won't do any work. In terms of A, B, C, D, draw a boolean expression for making the bakery operable.

## MUST SHOW WORK



 $\mathbf{f}(\mathbf{A},\mathbf{B},\mathbf{C},\mathbf{D}) = \underline{\hspace{1cm}}$ 

**6.** (16pt) Draw a circuit diagram that implements the following function f given in the truth table using..

	4pt a) One 8-1 multiplexer	6pt b)One 4-1 multiplexer	6pt c)One 2-1 multiplexer
a b c f 0 0 0 1			
$egin{array}{c ccc} 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \\ \end{array}$			
$egin{array}{c cccc} 0 & 1 & 0 & 1 \\ 0 & 1 & 1 & 1 \\ \end{array}$			
$\begin{bmatrix} 0 & 1 & 1 & 1 \\ 1 & 0 & 0 & 0 \end{bmatrix}$			
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			
1 1 1 1			

7. (15pt) Three functions f, g, and h are shown in the truth table below.

abc	f	g	h
000	1	1	0
001	1	1	1
010	0	0	0
011	1	0	1
100	1	0	1
101	1	1	0
110	1	1	1
111	0	0	0

(a 9pt) Implement(Draw gate-level diagram) f, g, and h using only minimum number of AND, XOR and/or OR gates