

Objective

In this lab, students were introduced to latches and flip-flops. These sequential logic circuits will be described in first structural Verilog and then behavioral Verilog. Synchronous sequential circuits will also be introduced towards the end of the lab. Delays will also be added to logic gates for the first time while implementing a clock signal. Finally, students will design one block of code that will include both flip-flops and combinational logic (full adder) to simulate synchronous logic.

Design

Results

Explain the 2 unit delay to 4 units and explain the results of the simulation (Experiment 1 1.e)

(Experiment 1 3.b) Do the latches behave as expected? Why or why not?

(Experiment 1 4.b) Compare the waveforms you captured from the behavioral Verilog to those captured from the structural. Are they different? If so, how?

Conclutions

Questions

1. Include the source code with comments for all modules you simulated. You do not have to include test bench code that was provided; however, you must supply the test bench code that you wrote! Code without comments will not be accepted.

In the report.

2. Include screenshots of all waveforms captured during simulation in addition to the test bench console output for each test bench simulation.

In the report.

3. Answer all questions throughout the lab manual.

In the report.

4. Compare the behavioral description of the synchronous adder found in the test bench code with the combination of structural and dataflow Verilog you used in the lab assignment. What are the advantages and disadvantages of each? Which do you prefer and why?
5. Based on the clock period you measured for your synchronous adder, what would be the theoretical maximum clock rate? What would be the effect of increasing the width of the adder on the clock rate? How might you improve the clock rate of the design?

Student Feedback

1. What did you like most about the lab assignment and why? What did you like least about it and why?
2. Were there any section of the lab manual that were unclear? If so, what was unclear? Do you have any suggestions for improving the clarity?
3. What suggestions do you have to improve the overall lab assignment?