Lab 09 Questions

1. Measure and record the period of each clock signal using the green and yellow markers. Based on your measurements, what frequency do you think the input (Experiment 1.4.b)

2. Open up the test bench file and try to understand what is going on. You should see that the test bench produces a Clk signal. What is the frequency of that signal? (Exp 2.2.b)

3. You should also see that the test bench holds the counter in reset for a specific interval of time. How long is that interval? (Exp 2.2.c)

4. After reset is de-asserted, the test bench holds the enable LOW for some amount of time before allowing the counter to run. How long is this time period? (Exp 2.2.d)

5. What is this maximum count value and what signal in the waveform could we use to know exactly when the counter is going to roll over? (Exp 2.2.f)

6. If we use a 50MHz clock to drive our frequency divider, what rate will the most significant bit of the divider oscillate at? (Exp 2.3.a)

7. Copy the waveform on the scope into your lab write-up. (Exp 3.1.j)

8. Does the design work as intended? Why or why not? (Exp 3.2.f)