

Prelab

1. Fill in the remaining entries in Table 1. You may find the discussion on Generating Timing Delays in the background section helpful.

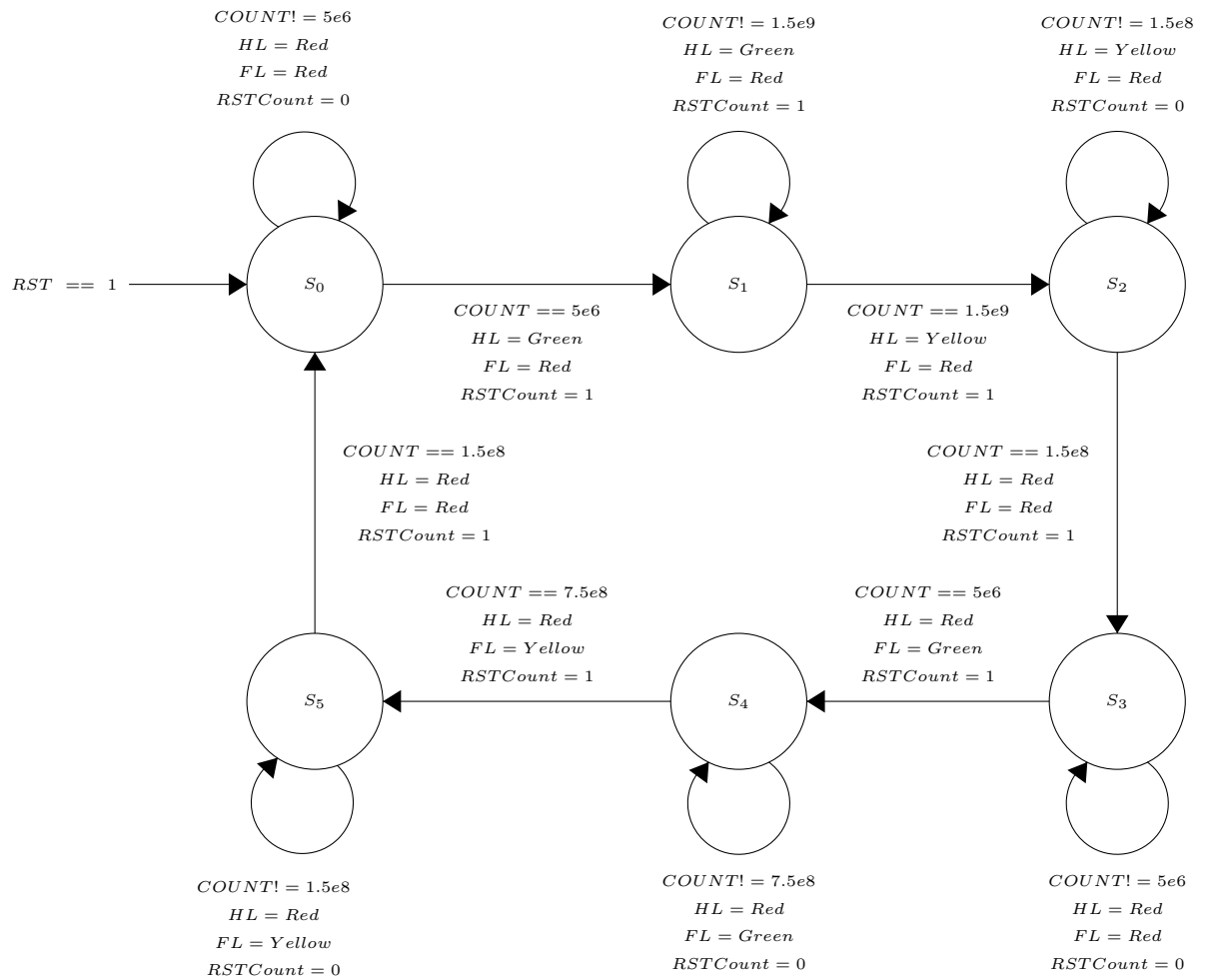
Table 1: Traffic Light Controller States

State	Highway Output	Farm Road Output	Delay (seconds)	Delay (cc)
S0	red	red	1	50,000,000
S1	green	red	30	1,500,000,000
S2	yellow	red	3	150,000,000
S3	red	red	1	50,000,000
S4	red	green	15	750,000,000
S5	red	yellow	3	150,000,000

2. Based on the column entries you just calculated, what is the necessary value of n in Figure 5?

The largest number that will need to be represented in binary is 1,500,000,000. That number in binary is 10110010110100000101111000000000 which consists of 31 bits thus $n = 31$ wires.

3. Given Table 1 and Figure 6, create a state diagram for the traffic light controller FSM. Be sure to include the appropriate input and output labels. Assume S0 is the reset state.



4. Now describe the traffic light controller FSM in Verilog using the following module interface

Code Block 1: TLC FSM Verilog

```

1 module tlc_fsm (
2     output reg [2:0] state, // output for debugging
3     output reg RstCount, // use an always block
4     // another always block for these as well
5     output reg [1:0] highwaySignal, farmSignal,
6     input wire [31:1:0] Count,
7     input wire Clk, Rst // clock and reset
8 );
9
10 parameter S0 = 3'b000,

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```

11         S1 = 3'b001,
12         S2 = 3'b010,
13         S3 = 3'b011,
14         S4 = 3'b100,
15         S5 = 3'b101,
16         GREEN = 2'b00,
17         YELLOW = 2'b01,
18         RED = 2'b10;
19
20     reg [2:0] nextState;
21
22     // Output logic
23     always @ (state or RstCount) begin
24         case (state)
25             S0: begin
26                 if (RstCount) begin
27                     highwaySignal = GREEN;
28                     farmSignal = RED;
29                 end else begin
30                     highwaySignal = RED;
31                     farmSignal = RED;
32                 end
33             end
34             S1: begin
35                 if (RstCount) begin
36                     highwaySignal = YELLOW;
37                     farmSignal = RED;
38                 end else begin
39                     highwaySignal = GREEN;
40                     farmSignal = RED;
41                 end

```

42	end
43	S2: begin
44	if (RstCount) begin
45	highwaySignal = RED;
46	farmSignal = RED;
47	end else begin
48	highwaySignal = YELLOW;
49	farmSignal = RED;
50	end
51	end
52	S3: begin
53	if (RstCount) begin
54	highwaySignal = RED;
55	farmSignal = GREEN;
56	end else begin
57	highwaySignal = RED;
58	farmSignal = RED;
59	end
60	end
61	S4: begin
62	if (RstCount) begin
63	highwaySignal = RED;
64	farmSignal = YELLOW;
65	end else begin
66	highwaySignal = RED;
67	farmSignal = GREEN;
68	end
69	end
70	S5: begin
71	if (RstCount) begin
72	highwaySignal = RED;

```

73             farmSignal = RED;
74         end else begin
75             highwaySignal = GREEN;
76             farmSignal = YELLOW;
77         end
78     end
79
80     default: ;
81 endcase
82 end
83
84
85
86
87 // Next state logic
88 always @ ( * ) begin
89     case (state)
90         S0: begin
91             if (Count == 50000000) begin
92                 nextState = S1;
93             end else begin
94                 nextState = S0;
95             end
96         end
97         S1: begin
98             if (Count == 1500000000) begin
99                 nextState = S2;
100             end else begin
101                 nextState = S1;
102             end
103         end

```

```

104         S2: begin
105             if (Count == 150000000) begin
106                 nextState = S3;
107             end else begin
108                 nextState = S2;
109             end
110         end
111     S3: begin
112         if (Count == 50000000) begin
113             nextState = S4;
114         end else begin
115             nextState = S3;
116         end
117     end
118     S4: begin
119         if (Count == 750000000) begin
120             nextState = S5;
121         end else begin
122             nextState = S4;
123         end
124     end
125     S5: begin
126         if (Count == 150000000) begin
127             nextState = S1;
128         end else begin
129             nextState = S5;
130         end
131     end
132     default: ;
133 endcase
134 end

```

```
135
136     always @ (posedge Clk) begin
137         if (Rst) begin
138             stat <= S0;
139         end else begin
140             state <= nextState;
141         end
142     end
143
144     assign Count = 0;
145
146 endmodule // tlc_fsm
```