Lab 04: Rudimentary Adder Circuits

Joseph Martinsen

ECEN 248 – 510

TA: Michael Bass

Date: October 1, 2016

Objectives:

The objective of this lab was to introduce students to the design and implementation of a simple combinational adder circuit such as a half adder, full adder, and a ripple carry adder. This lab also hopes to further develop one's knowledge and familiarity with Karnaugh maps. Students will also gain more experience with breadboards, IC's, and circuit debugging.

Design:

This lab was separated into three distinct experiments. The first was to construct a half adder, the second to build a full adder, and the final was to implement a ripple carry adder.

Experiment 1: Half Adder

A half adder has two inputs, A and B, as well as two outputs, a Sum (S) and a carry out (COUT).

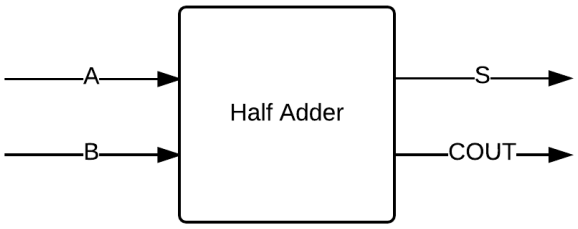


Figure 1

The following is the truth table and Karnaugh map for a half adder

Half Adder Truth Table

A	B	S	COUT
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Table 1

S

$\bar{A}$ \ $\bar{B}$	$\bar{B}$	B
$\bar{A}$	0	1
	1	0

Table 2

COUT

$\bar{A}$ \ $\bar{B}$	$\bar{B}$	B
$\bar{A}$	0	0
	0	1

Table 2

The following is the design used for the half adder. Using one XOR gate and one AND gate.

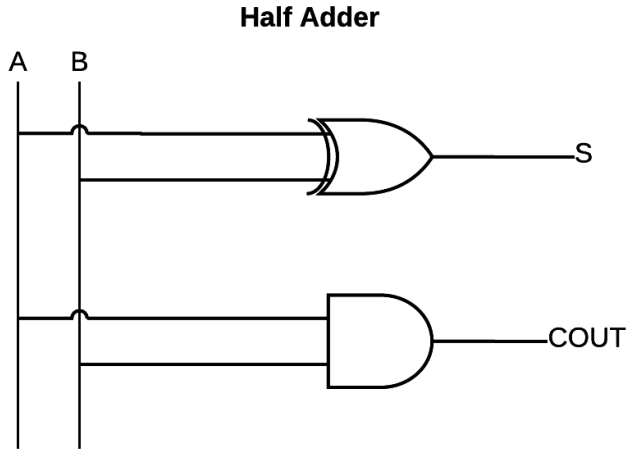


Figure 2

Experiment 2: Full Adder

The full adder is similar to the half adder except the full adder has a carry in (CIN). The other inputs, A and B, are the same. The outputs are the same as well, S and COUT.

Full Adder Truth Table

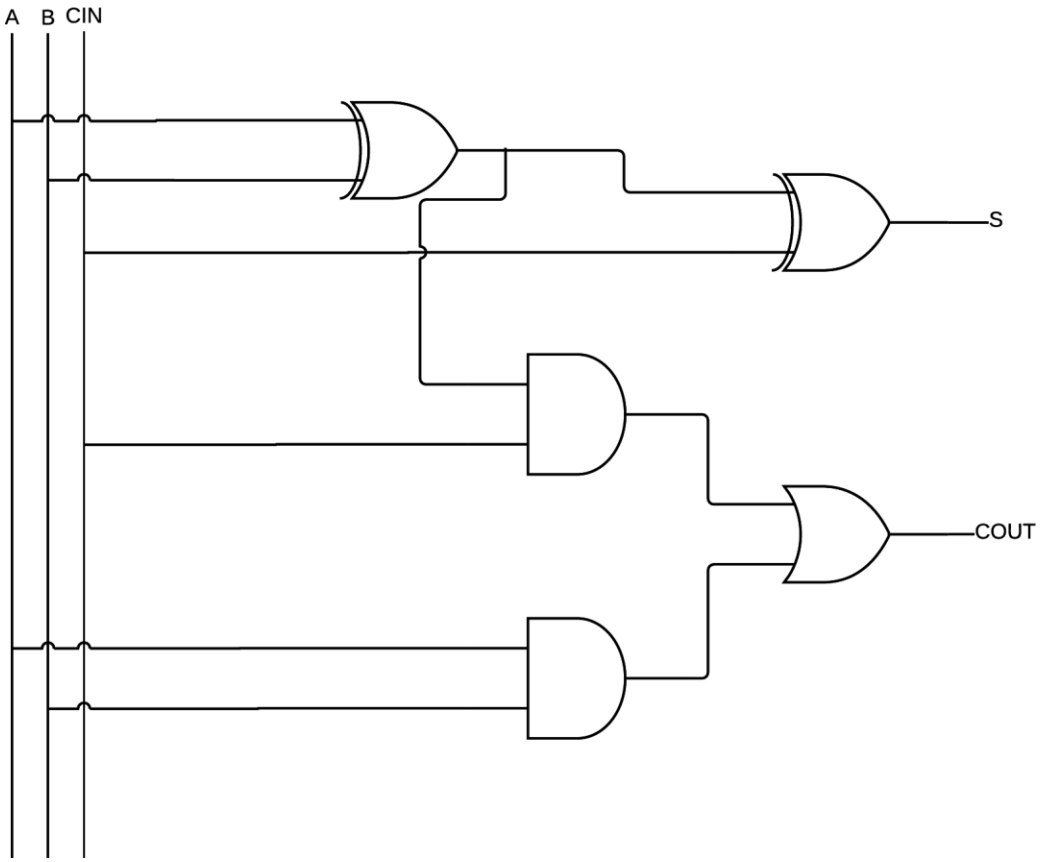
A	B	CIN	S	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1

1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

		A	A	
	B	B		
0	1	0	1	
CIN 1	0	1	0	

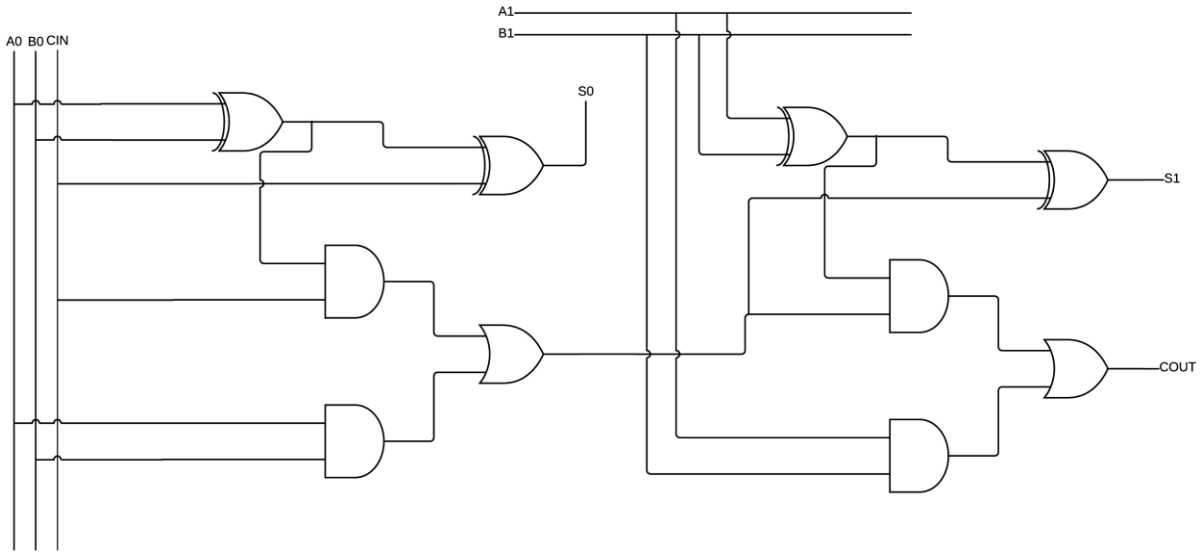
		A	A	
	B	B		
0	1	1	0	
CIN 0	0	1	1	

The following is the diagram for the circuit using one XOR gate, three AND gates, and one OR gate.



Experiment 3: Ripple Carry Adder

A ripple carry adder is simply two full adders in succession. COUT of the first full adder is then inputted into the CIN of the second full adder. The sum is then calculated. Here is the design.



Results:

At first the half adder was not working properly. I was able to find that the issue was with the XOR integrated circuit. The XOR of A and B would also return as 1. After replacing the IC, the half adder circuit functioned properly. The full adder circuit functioned properly on the first try for all values of A, B and CIN.

For the ripple carry adder, CIN was not properly integrated into my circuit. The circuit was set up without a CIN. After modifying my circuit drastically, I was able to get all the values to function properly for values of CIN = 0. I was able to confirm that CIN value was correct after passing through the first ripple carry adder. Due to the mistake of not having a CIN in the first circuit, I was not to find where the exact issue was.

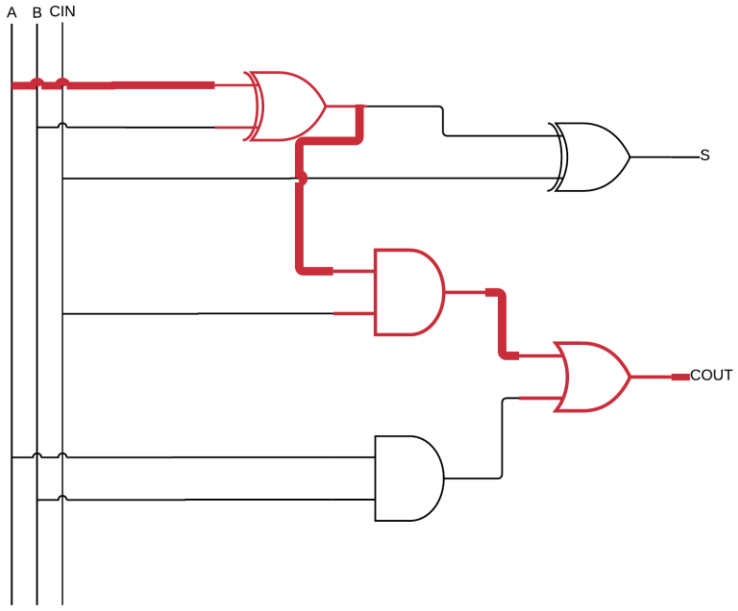
Conclusion:

In conclusion, this lab consisted of designing a half adder, full adder, and a ripple carry adder. Each case required the construction of a truth table and Karnaugh map. Do to the increased complexity of the ripple carry adder, debugging skills were utilized.

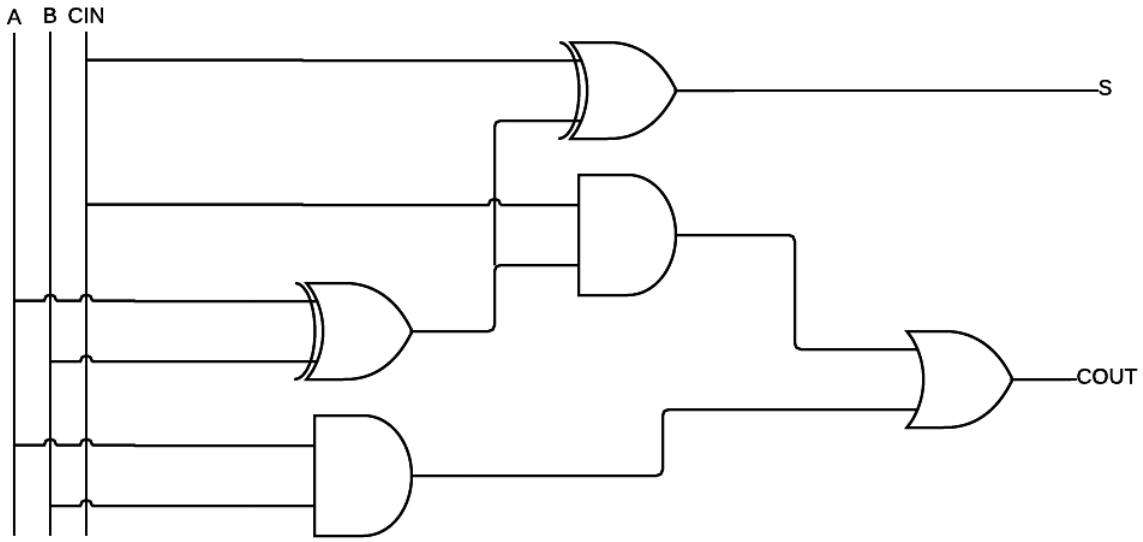
Questions:

1. **Provide all design items found in the pre-lab deliverables. If you found that a design needed corrections while executing the lab, supply the updated version of that material.**

2. **Determine the worst case propagation delay for your full adder design. Assume each gate has the same delay of 1 unit. Show the maximum delay path in your schematic. The maximum delay path is known as the critical path for that particular combinational block.**
   The worse case propagation is three units. One for the XOR, one for the AND, and another for OR.



3. **Design a 2-bit carry ripple adder assuming you only have half adder circuits and OR gates to work with. Draw up a schematic for your design using half adder building blocks and OR gates. Be sure the clearly label all inputs and outputs of your blocks.**



Feedback

1. **What did you like most about the lab assignment and why? What did you like least about it and why?**
   I enjoyed creating my circuits. I did not enjoy correcting my mistake of not having a CIN on my first design of the ripple carry adder.

2. **Were there any section of the lab manual that were unclear? If so, what was unclear? Do you have any suggestions for improving the clarity?**
   No. Can't help someone who misreads the lab manual.

3. **What suggestions do you have to improve the overall lab assignment?**
   Lab should have been rather easy