Objective

In the last lab, two different methods to create digital circuits in Verilog was introduced. One was structural method and the other was dataflow modeling. In this lab, a 3^{rd} method will be used, behavioral modeling.

This lab consisted of three separate experiments. For **Experiment 1**, the multiplexers created last lab will be converted into behavioral Verilog. In **Experiment 2**, students will describe, using behavioral Verilog, binary encoders and decoders. Finally, **Experiment 3** will introduce logic synthesis, as well as translating HDL code into implementable digital logic. The code written in Experiment 2 will be synthesized and programed onto a Spartan 3E in order to further verify that the encoder and decoder described is in fact correct.

Design

Experiment 1

Code Block 1: 4-Bit ALU

```
1  `timescale 1ns / 1ps
2  //////////////////////////////////////////////////////////////////
3  // Design Name:
4  // Module Name: four_bit_mux_behavioral
5  // Author:
6  //
7  //////////////////////////////////////////////////////////////////
8  module four_bit_mux(Y, A, B, S);
9      /*output and input ports*/
10     output reg [3:0]Y;
11
12     input wire [3:0]A;
13     input wire [3:0]B;
14     input wire S;
```

```
15
16
17      always@(A or B or S)
18              begin
19                      if(S == 1'b0)
20                              Y = A;
21                      else
22                              Y = B;
23              end
24  endmodule
```

Experiment 2

Experiment 3

Results

Experiment 1

Experiment 3

Conclutions

Questions

1. **Include the source code with comments for all modules you simulated. You do not have to include test bench code. Code without comments will not be accepted!**

   In Report

2. **Include screenshots of all waveforms captured during simulation in addition to the test bench console output for each test bench simulation.**

   In Report

3. **Provide a comparison between behavioral Verilog used in this weeks lab and the structural and dataflow Verilog used in last weeks lab. What might be the advantages and disadvantages of each.**

4. **Compare the process of bread-boarding digital circuit to implementing a digital circuit on an FPGA. State some advantages and disadvantages of each. Which process do you prefer?**

Student Feedback

1. **What did you like most about the lab assignment and why? What did you like least aboub it and why?**

2. **Were there any section of the lab manual that were unclear? If so, what was unclear? Do you have any suggetions for improving the clarity?**

3. **What suggestions do you have to improve the overall lab assignment?**