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CPE 439
Final Project Proposal

Logic Analyzer on the Zynq-7000 SoC

Overview

The goal of this project is to implement a usable logic analyzer on a Zybo board featuring the Zynq-7000 Soc. This project will mainly serve as an educational exercise in SoC development but may prove to be a useful tool in the development of future projects due to its (hopeful) applicability towards diagnosing problems in digital projects.

Features

8 or 16 Inputs	Either one or two pmod ports will be used, each pmod will provide 8 input channels. (FPGA)
Variable Sample Rate	Users should be able to set sampling rate to any rate they deem necessary. Research is needed to determine the max sampling rate possible. The PL portion of the SoC is clocked at a max of 450 MHZ. (Implemented on FPGA, controlled by CPU)
Graphical Display	This project will feature some sort of graphical output to an external monitor. VGA or HDMI will be targeted based on the whether the old Zybo or new Zybo is used. (FPGA)
Keyboard Based CLI	This will be the main way that the user will configure the logic analyzer. Targeting very simple command syntax. (CPU)
Protocol Decoding	This is the first big feature goal for this project after basic functionality as it will make the analyzer possibly useful. (CPU)
Simple & Protocol Triggering	Further addition to protocol decoding is the ability to trigger data capture on a certain protocol event or pin rise/fall. (CPU)

Stretch Features

Graphics Acceleration	At high sampling rates, the CPU will likely be unable to handle both the data decode task and the video output task. Add a graphics accelerator on the FPGA to reduce CPU load. (FPGA)
Support for Burst Data Acquisition	If DMA through the AMBA interconnect does not provide a stable enough bandwidth to support high sample rates then create a block to handle more complex buffering of incoming data. (FPGA)
Protocol Generator	To add to analyzer feature set, provide a way to spoof protocols for greater in circuit debugging usefulness. (CPU)
Mouse UI	Add a mouse to make the UI more intuitive, (CPU)
USB Trace Storage	Add the ability to save buffers of trace data to a usb mass storage device (CPU)