

Revision History:



Date:	Revision:	Comments:
		Initial Revision
		Additional Notes:

Important Notes about this Schematic:

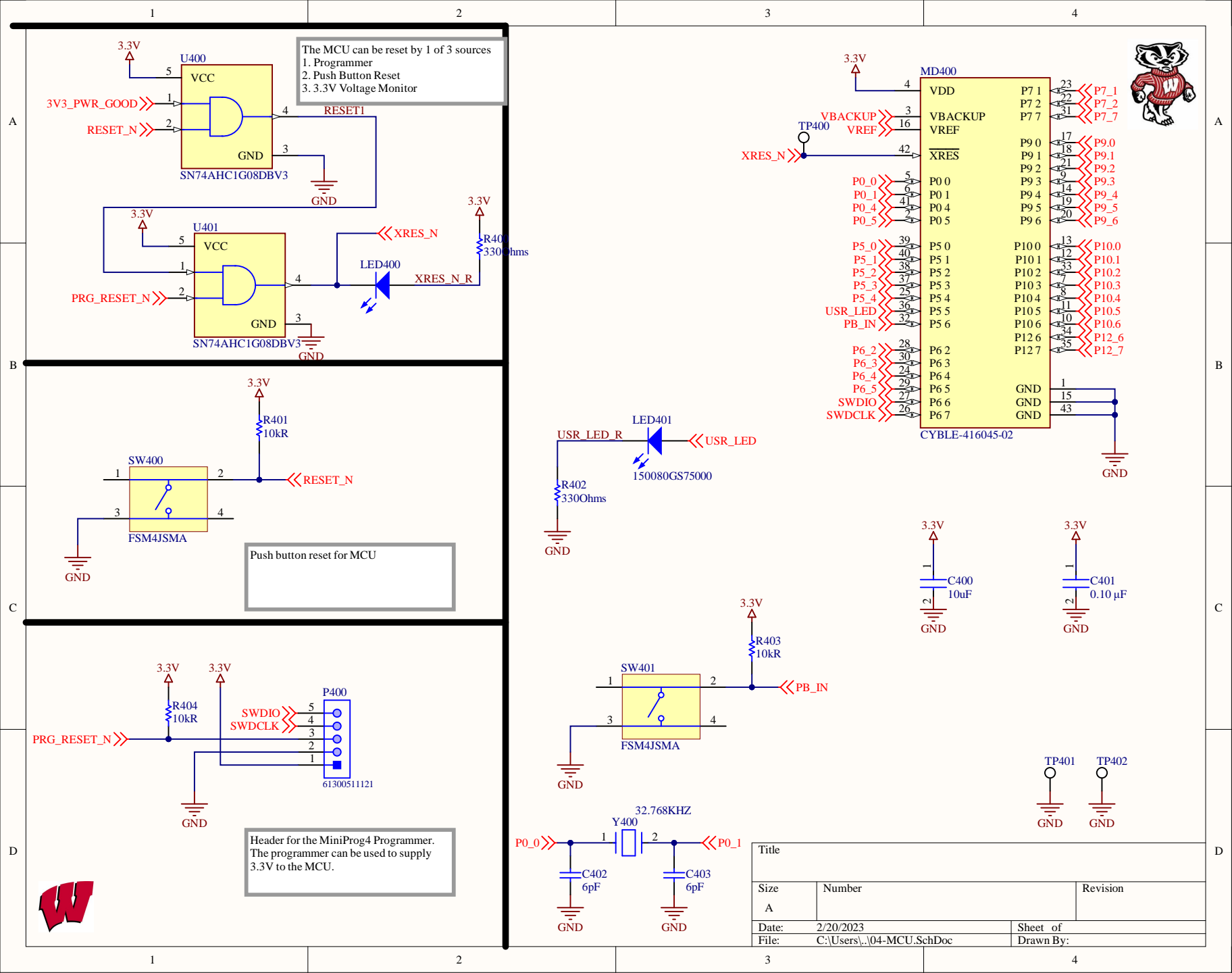
DESIGN NOTE:
Design notes in gray text boxes give information about design requirements and descisions.

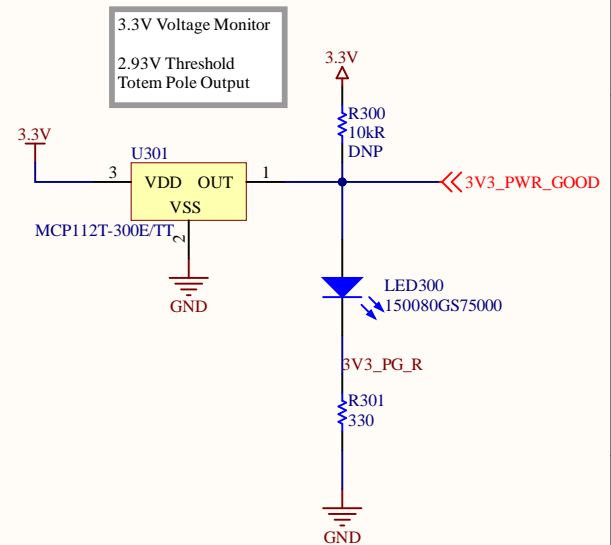
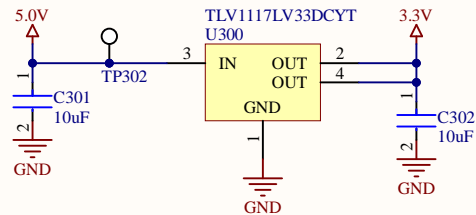
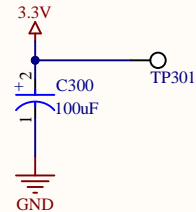
LAYOUT NOTE:
Layout notes in red text boxes give information regarding layout requirements.

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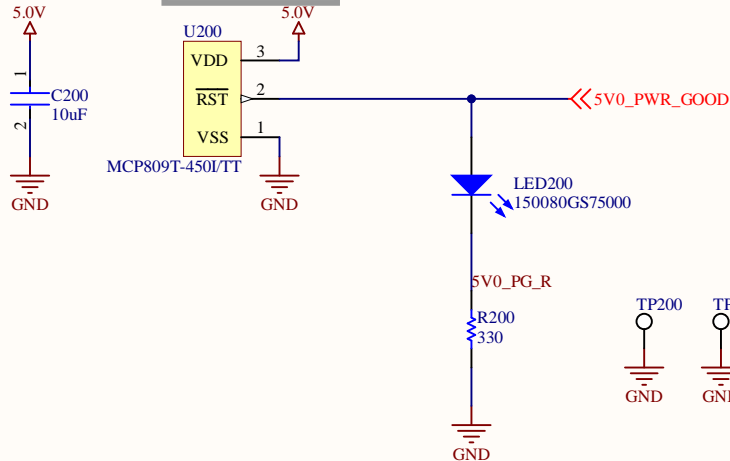




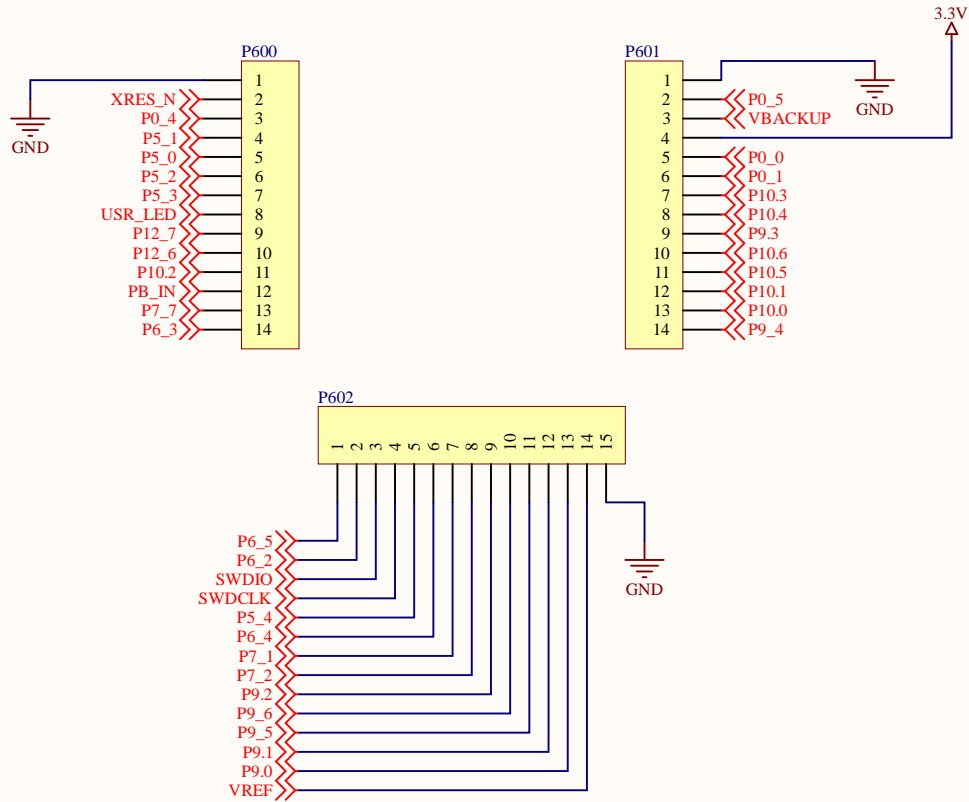
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5.0V Voltage Monitor
4.375V Threshold
Totem Pole Output



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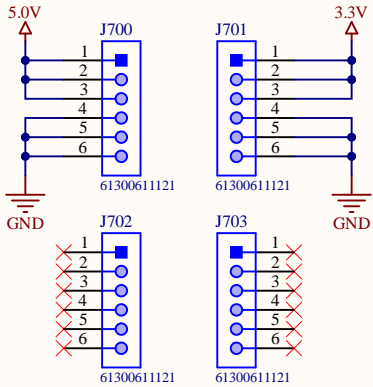


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A

A



B

B

C

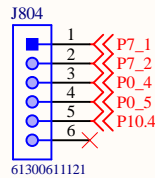
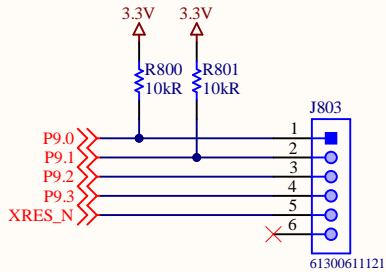
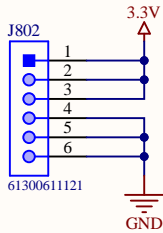
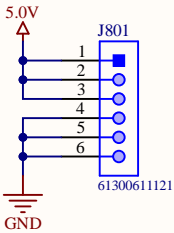
C

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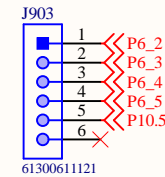
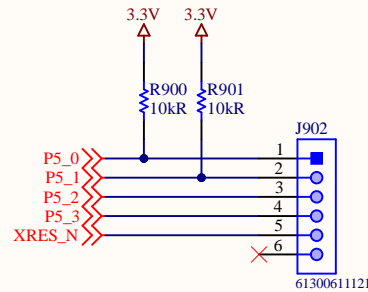
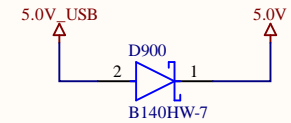
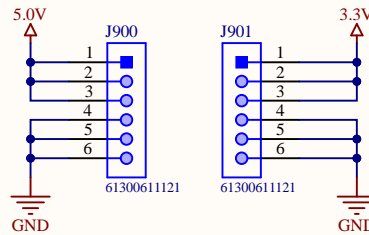
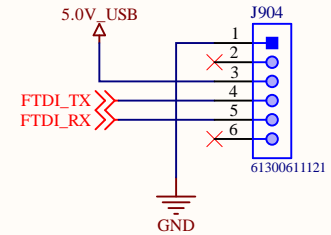


Pin	UART	SPI	I2C	PWM
P9.0	SCB2_RX	SCB2_MOSI	SCB2_SCL	tcpwm_0[4]
P9.1	SCB2_TX	SCB2_MISO	SCB2_SDA	!tcpwm_0[4]
P9.2		SCB2_SCLK		tcpwm_0[5]
P9.3		SCB2_SS0		!tcpwm_0[5]

Pin	PWM	Analog
P7.1	!tcpwm_0[4]	
P7.2	tcpwm_0[5]	
P0.4	tcpwm_0[2]	
P0.5	!tcpwm_0[2]	
P10.4	tcpwm_0[0]	SAMUX[4]

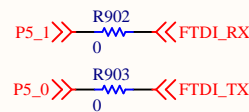


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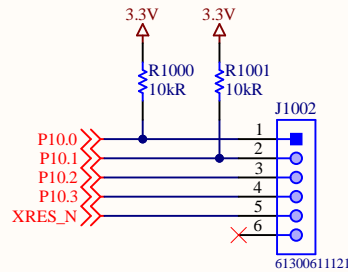
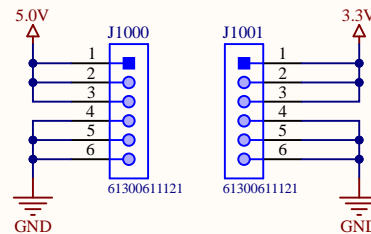
Pin	PWM	Analogs
P6.2	tcpwm_1[9]	
P6.3	!tcpwm_1[9]	
P6.4	tcpwm_1[10]	
P6.5	!tcpwm_1[10]	
P10.5	tcpwm_0[0]	SAMUX[5]

Pin	UART	SPI	I2C	PWM
P5.0	SCB5_RX	SCB5_MOSI	SCB5_SCL	tcpwm_1[4]
P5.1	SCB5_TX	SCB5_MISO	SCB5_SDA	!tcpwm_1[4]
P5.2		SCB5_SCLK		tcpwm_1[5]
P5.3		SCB5_SS0		!tcpwm_1[5]



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Pin	UART	SPI	I2C	PWM
P10.0	SCB6_RX	SCB6_MOSI	SCB6_SCL	tcpwm_0[6]
P10.1	SCB6_TX	SCB6_MISO	SCB6_SDA	!tcpwm_0[6]
P10.2		SCB6_SCLK		tcpwm_0[7]
P10.3		SCB6_SS0		!tcpwm_0[7]

Pin	PWM	Analog
P9.4	tcpwm_1[0]	
P9.5	!tcpwm_1[0]	
P12.6	tcpwm_1[7]	
P12.7	!tcpwm_1[7]	
P10.6	tcpwm_1[2]	SAMUX[6]



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