

Quiz 2

● Graded

Student


Total Points

100 / 100 pts

Question 1

1a

4 / 4 pts

+ 4 pts Correct (D)

+ 0 pts incorrect

Question 2

1b

4 / 4 pts

+ 4 pts Correct (B)

+ 0 pts incorrect

Question 3

1c

6 / 6 pts

Addressability

+ 2 pts 16

+ 1 pt 2 bytes

Address Space

+ 2 pts 512

+ 1 pt 2^9

Total Memory

+ 2 pts 1024 bytes

+ 1 pt 2^{10} bytes, 2^{13} bits, 8192 bits

+ 0 pts incorrect

Question 4

1d

4 / 4 pts

✓ + 4 pts Correct (all x's)

+ 0 pts incorrect

Question 5

1e

8 / 8 pts

5.1 1ei

4 / 4 pts

✓ + 2 pts Correct (No)

✓ + 2 pts Explanation **must** state that a larger grouping can be made or writing down the simplified boolean expression.

+ 0 pts incorrect

5.2 1eii

4 / 4 pts

✓ + 2 pts Correct (No)

✓ + 2 pts Explanation **must** state that a larger grouping can be made or writing down the simplified boolean expression.

+ 0 pts incorrect

Question 6

1f

24 / 24 pts

6.1 1fi

4 / 4 pts

✓ + 2 pts Correct (False)

✓ + 2 pts Explanation states at least one of the following:

- › The given statement describes sequential logic
- › Combinational logic depends only on current inputs

+ 0 pts incorrect

6.2 1fii

4 / 4 pts

✓ + 2 pts Correct (False)

✓ + 2 pts Explanation must state that a gated d-latch only has two inputs: WE and data (**must include what the two inputs are**)

+ 0 pts incorrect

6.3 1fiii

4 / 4 pts

✓ + 2 pts Correct (False)

✓ + 2 pts Explanation must state one of the following:

- › We need 5 bits to represent 17 states
- › 4 bits can only represent 16 states at most
- › or any other valid reasoning

+ 0 pts incorrect

6.4 1fiv

4 / 4 pts

✓ + 2 pts Correct (False)

✓ + 2 pts Explanation must state one of the following:

- › Flip flops are edge triggered
- › Only updates on a clock edge
- › Any other valid reasoning

+ 0 pts incorrect

6.5

1fv

4 / 4 pts

✓ + 2 pts Correct (True)

✓ + 2 pts Explanation describes the correct components that are used to build a flip-flop in any reasonable way.
(Also give full points if they state False and we can use one less NOT gate by using Q' as input to second latch).

+ 0 pts Incorrect

6.6

1fvi

4 / 4 pts

✓ + 2 pts Correct (True)

✓ + 2 pts Explanation mentions one of the following:

- › Synchronization
- › Ensure we do not skip through states
- › Any other valid reasoning related to edge triggered logic

+ 0 pts incorrect

Question 7

2a

6 / 6 pts

✓ + 6 pts Fully Correct (by row)

- › 0 0 1
- › 0 1 1
- › 1 0 0
- › 0 1 0
- › 1 0 1
- › 1 1 1
- › 1 0 0
- › 0 1 0

+ 5.25 pts 1 incorrect row

+ 4.5 pts 2 incorrect rows

+ 3.75 pts 3 incorrect rows

+ 0 pts 4 or more rows incorrect

Question 8

2b

9 / 9 pts

KMAP (N1)

✓ + 3 pts Fully correct (by row)

- › 0 1 0 1
- › 0 0 1 1

+ 2 pts one cell incorrect

+ 1 pt two cells incorrect

+ 0 pts 2+ incorrect

KMAP (N2)

✓ + 3 pts Fully correct

- › 1 0 1 1
- › 0 1 0 0

+ 2 pts one cell incorrect

+ 1 pt two cells incorrect

+ 0 pts 2+ incorrect

KMAP (Output)

✓ + 3 pts Fully correct

- › 0 0 1 0
- › 0 1 1 1

+ 2 pts one cell incorrect

+ 1 pt two cells incorrect

+ 0 pts 2+ incorrect

+ 0 pts incorrect

Question 9

2c

10 / 10 pts

Sum of products

✓ + 5 pts Fully correct ($A'B' + A'CD + ACD' + ABC'D$)

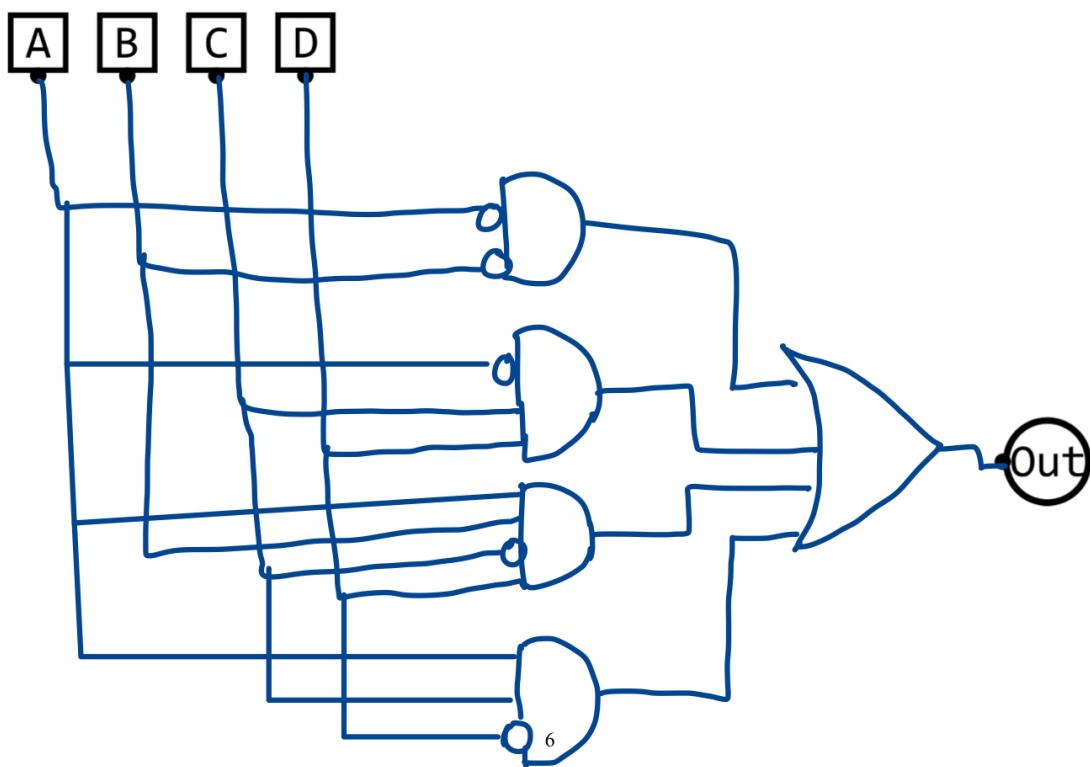
+ 2.5 pts one mistake

+ 0 pts incorrect

Circuit

✓ + 5 pts Fully correct (matches SOP, propagate errors)

Circuit:



+ 1 pt OR4 gate

+ 4 pts All AND gates match SOP

+ 3 pts 3 AND gates match SOP

+ 2 pts 2 AND gates match SOP

+ 1 pt 1 AND gate matches SOP

+ 0 pts incorrect

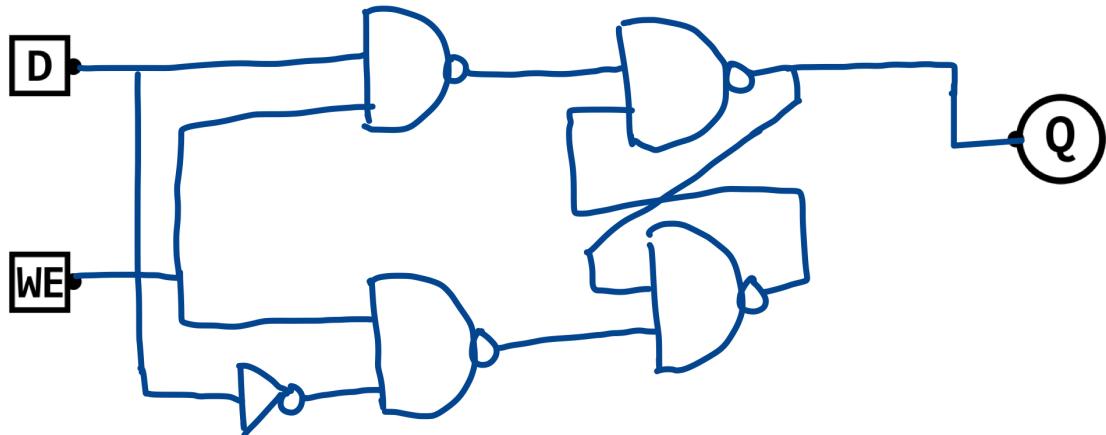
+ 0 pts incorrect

Question 10

3a

5 / 5 pts

✓ + 5 pts Correct (Fully correct)



- 1 pt Uses bubbles instead of inverters

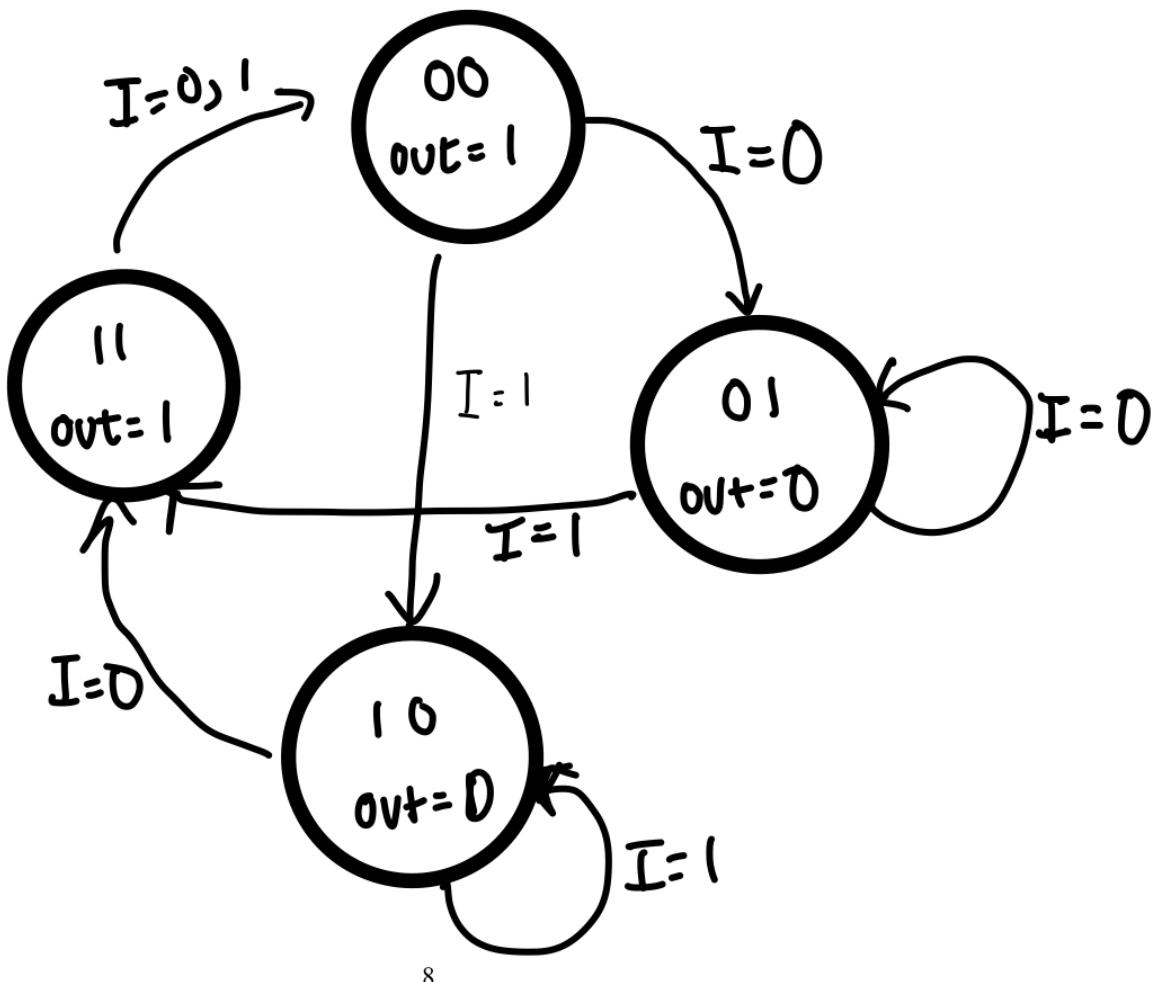
- 1 pt connects Q' instead of Q to output

- 2 pts forgets NOT gate

- 2 pts negates WE

+ 0 pts very incorrect or use gates other than NAND2 and NOT

✓ + 7 pts Correct



8

+ 6 pts one error

+ 5 pts two errors

+ 4 pts three errors

+ 0 pts 3+ errors

Question 12

3c

6 / 6 pts

Groupings

✓ + 3 pts Fully correct

...

	C'D'	C'D	CD	CD'
A'B'	0	0	0	1
A'B	1	1	0	1
AB	0	0	1	1
AB'	1	0	1	1

+ 2 pts one incorrect/extraneous grouping

+ 1 pt two incorrect/extraneous groupings

SOP

✓ + 3 pts correct ($CD' + AC + A'BC' + AB'D'$) or correct translation based on groupings

+ 0 pts incorrect translation from kmap groupings

+ 0 pts incorrect

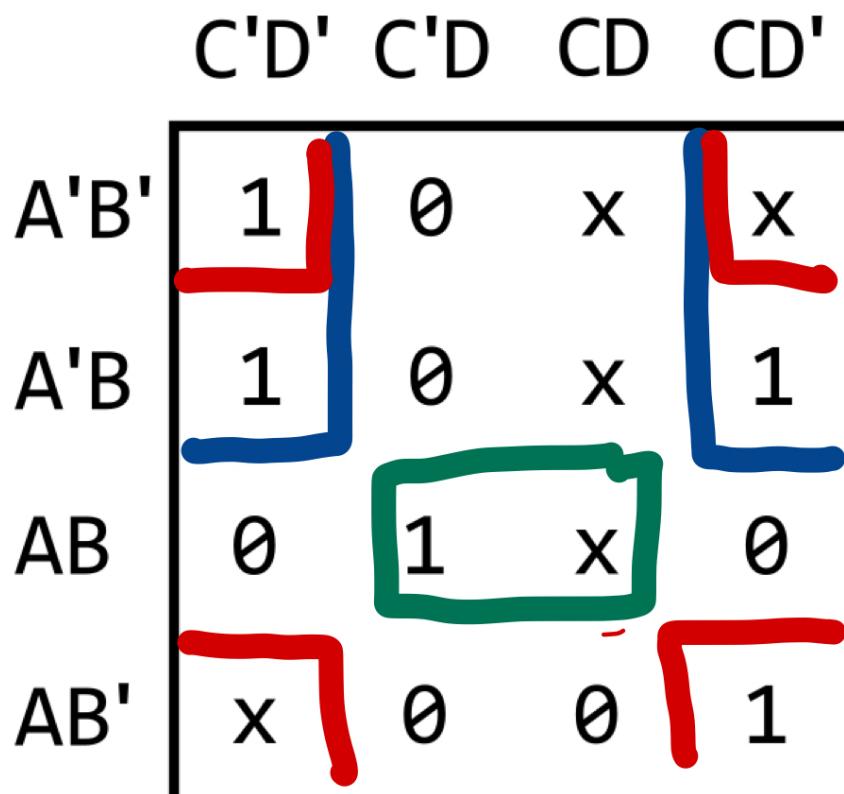
Question 13

3d

7 / 7 pts

Groupings

✓ + 4 pts Fully correct



+ 3 pts one incorrect/extraneous grouping

+ 2 pts two incorrect/extraneous groupings

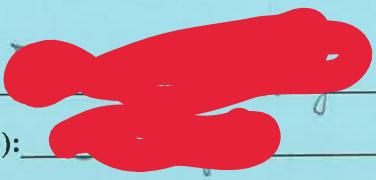
SOP

✓ + 3 pts correct ($B'D' + A'D' + ABD$) or correct translation based on groupings

+ 0 pts incorrect translation from kmap groupings

+ 0 pts incorrect

Your Initials: DB

Name [PRINT CLEARLY]: 

GT username (e.g. gburdell3): 

CS 2110: Computer Organization and Programming
Gupta/Conte/Adams Fall 2023

QUIZ 2
VERSION A

This exam is given under the Georgia Tech Honor Code System.
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work will be dealt with in full accordance with Institute policies.

Georgia Tech Honor Pledge: *"I commit to uphold the ideals
of honor and integrity by refusing to betray the trust bestowed
upon me as a member of the Georgia Tech community."*

[MUST sign:] 

- THIS IS A CLOSED BOOK, CLOSED NOTES EXAM
- NO CALCULATORS
- This examination handout has **9** pages.
- Do all your work in this examination handout.
- Only the front of exams sheets will be scanned. Do **not** write your answer on the back of the exam sheets.
- Please write your initials at the top of each page
- WHERE NEEDED, SHOW ALL YOUR INTERMEDIATE RESULTS TO RECEIVE FULL CREDIT

*In case you forgot, here
are some good facts to
know:*

Hex	Dec
0x1	1
0x2	2
0x3	3
0x4	4
0x5	5
0x6	6
0x7	7
0x8	8
0x9	9
0xA	10
0xB	11
0xC	12
0xD	13
0xE	14
0xF	15

x	2^x
1	2
2	4
3	8
4	16
5	32
6	64
7	128
8	256
9	512
10	1024
11	2048
12	4096
13	8192
14	16,384
15	32,768
16	65,536

Problem	Points	Score
1	50	
2	25	
3	25	
TOTAL	100	

GOOD LUCK!

*More good facts to
know:*

$$1K = 2^{10}$$

$$1M = 2^{20}$$

$$1G = 2^{30}$$

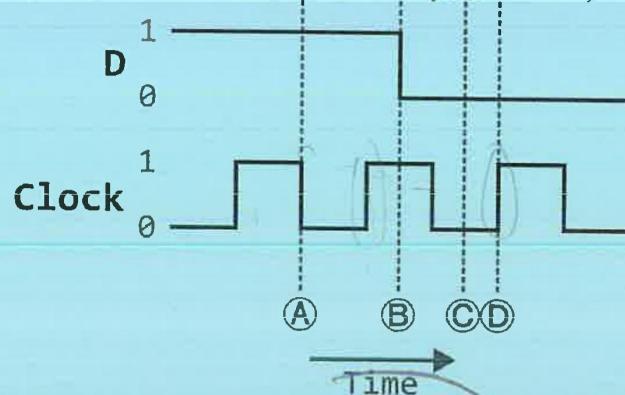
$$1T = 2^{40}$$

$$1P = 2^{50}$$

$$1E = 2^{60}$$

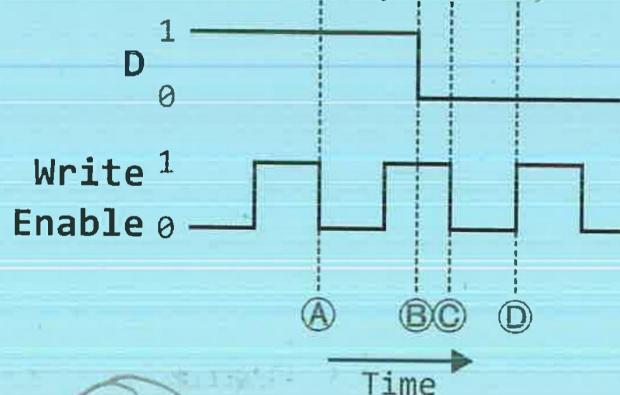
1. [50 pts] Answer the following short questions. Show your work (where needed) to receive full credit.

(a) At approximately which of the times below would a **D Flip-Flop's** output change to the value 0? Assume the flip-flop initially stores a 1. (Circle your answer)



Circle one: Time=(A), Time=(B), Time=(C), or Time=(D)

(b) At approximately which of the times below would a **Gated D Latch's** output change to the value 0? Assume the latch initially stores a 1. (Circle your answer)



Circle one: Time=(A), Time=(B), Time=(C), or Time=(D)

(c) You have acquired a new laptop for college. Your new computer uses **9-bit addresses**, and each address points to **2 bytes**. Please answer the following about the memory in your new computer (write a decimal number): (Please pay attention to units)

Addressability: 16 bits

$$2^9 \cdot 16$$

Address space: 512 locations

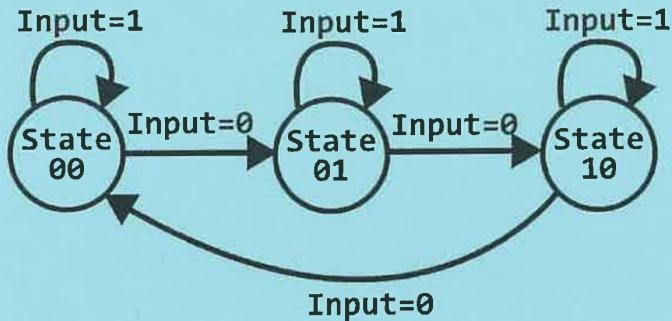
$$2^9 \cdot 2^4$$

Total Memory: 1024 bytes

$$2^{13} \text{ bits} \cdot 1 \text{ byte} = 2^{13} \text{ bytes}$$

Your Initials: _____

(d) Fill in the missing last 4 cells of the truth table for the following state machine to ensure a minimal logical expression *could* be found with a K-map. N1 and N0 are the next state bits.



S1	S0	Input	N1	N0
0	0	0	0	1
0	0	1	0	0
0	1	0	1	0
0	1	1	0	1
1	0	0	0	0
1	0	1	1	0
1	1	0	X	X
1	1	1	X	X

Hint: You do NOT need to solve a K-map to answer this question.

(e) Will the following K-map groupings produce a minimal logical expression? Why or why not?

(1) Will these **two** groupings produce a minimal logical expression? Why or why not?

	B'C'	B'C	BC	BC'
A'	1	0	0	1
A	1	0	0	1

Your answer:

No because the sum of products will have 2 terms. Meanwhile, the equivalent expression C' has one term. This can be one group.

(2) Will these **two** groupings produce a minimal logical expression? Why or why not?

	B'C'	B'C	BC	BC'
A'	0	1	1	0
A	1	1	1	1

Your answer:

No because the sum of products will have 3 variables. Meanwhile, the equivalent expression $A + C$ uses just two variables. One group can be bigger.

$$C + AC'$$

$$a + \bar{a}b = a + b$$

(f) Answer the following true/false questions by circling "true" or "false," and then give a reason for each answer:

TRUE or FALSE	The output of combinational logic depends on past inputs in addition to current inputs. Why or why not? False because combinational logic does not depend on the past inputs. Sequential logic, though, depends on current and past inputs.
TRUE or FALSE	A Gated D Latch has 3 inputs: Write-Enable, S, and R. Why or why not? False because a gated D Latch has only the Write-Enable Input and D input.
TRUE or FALSE	To implement a finite state machine with 17 states, I only need 4 bits of memory. Why or why not? False because 4 bits at most allows 16 states of memory. 5 bits are needed to allow 17 states.
TRUE or FALSE	Flip-flops are level-triggered. Why or why not? False because flip-flops use clocks for synchronization, allowing them to be edge-triggered
TRUE or FALSE	I can build a flip-flop with 2 RS latches along with 3 NOT gates and 4 NAND gates. Why or why not? Yes because a flip-flop is just a gated D latch with an extra NOT. Since 1 Gated D uses 1 RS latch, 1 not and 2 Nands, a flip-flop uses 2 latches, 4 Nands, and 3 NOTS
TRUE or FALSE	The clock signal and edge-triggered logic are useful for building state machines. Why or why not? Yes, because it synchronizes the state changes. All memory can be in one state according to the clock cycle.



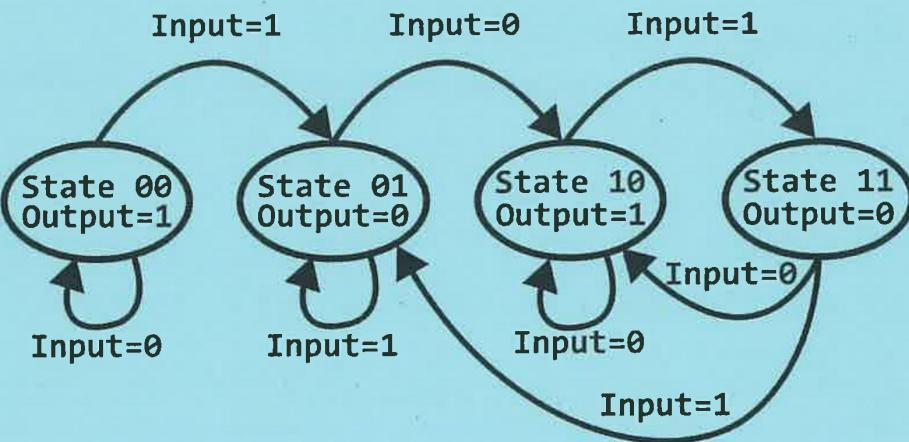
2 NMOS

2 NMOS

4

2. [25 pts] Answer the following questions about sequential logic. **Show your work.**

- (a) Complete the truth table for the following state machine diagram (note that output in the diagram refers to the current output for that state):



S1	S0	Input	N1	N0	Output
0	0	0	0	0	1
0	0	1	0	1	1
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	1	0	1
1	0	1	1	1	1
1	1	0	1	0	0
1	1	1	0	1	0

- (b) Convert the following truth table to a K-map. **You do not need to find K-map groupings!** The top-left cell of the K-maps below corresponds to the truth table column for that output.

S1	S0	I	N1	N0	Output
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	1	0	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	0	1	1

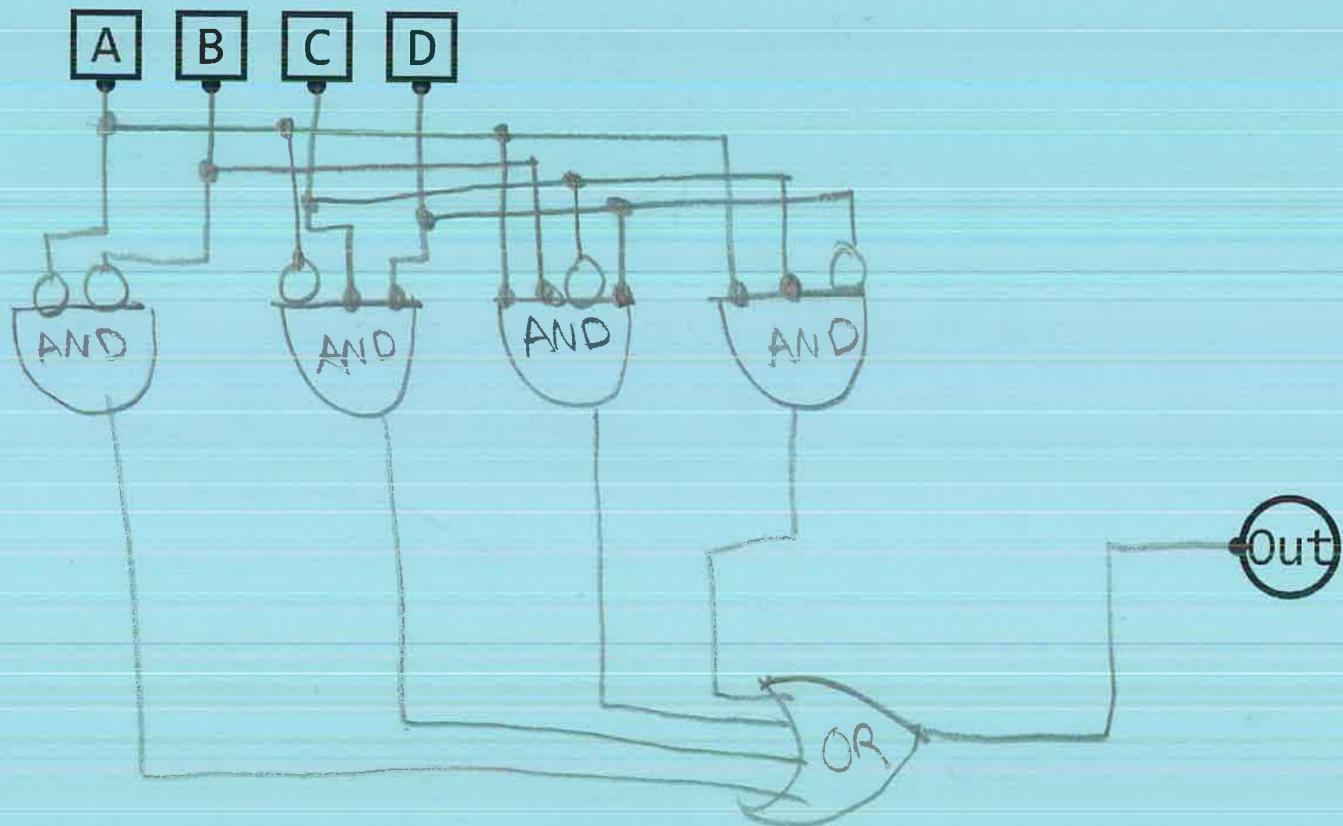
N1	S1'S0'	S1'S0	S1S0	S1S0'
I	0	1	0	1
I'	0	0	1	1
N0	S1'S0'	S1'S0	S1S0	S1S0'
I	1	0	1	1
I'	0	1	0	0
Output	S1'S0'	S1'S0	S1S0	S1S0'
I	0	0	1	0
I'	0	1	1	1

- (c) Convert the following K-map groupings to a Sum-of-Products (SOP) equation. Then draw a circuit using only AND and OR gates (possibly with bubbled inputs) that performs your equation:

	C'D'	C'D	CD	CD'
A'B'	1	1	X	1
A'B	0	0	1	0
AB	0	1	0	1
AB'	0	0	0	X

SOP Expression: $A'B' + A'CD + ABC'D + ACD'$

Circuit:

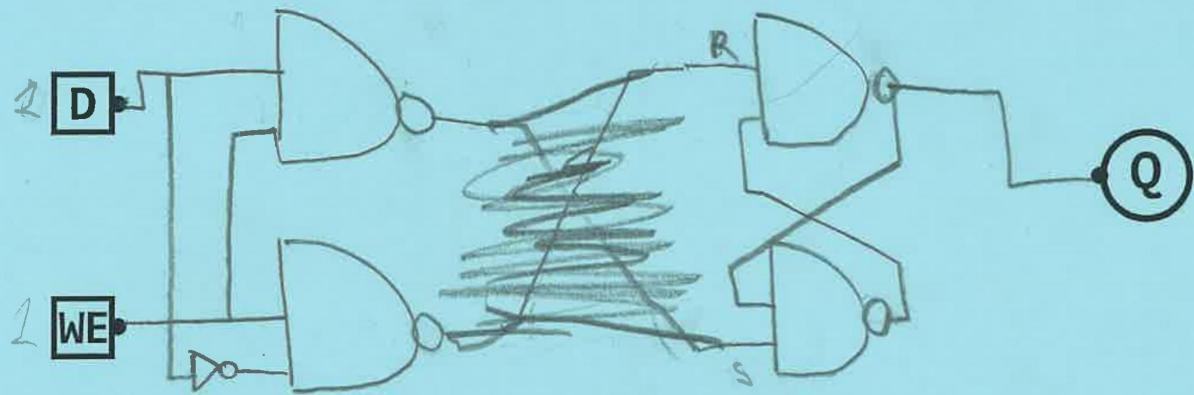


Your Initials: _____

3. [25 pts] Answer the following questions about sequential logic. **Show your work.**

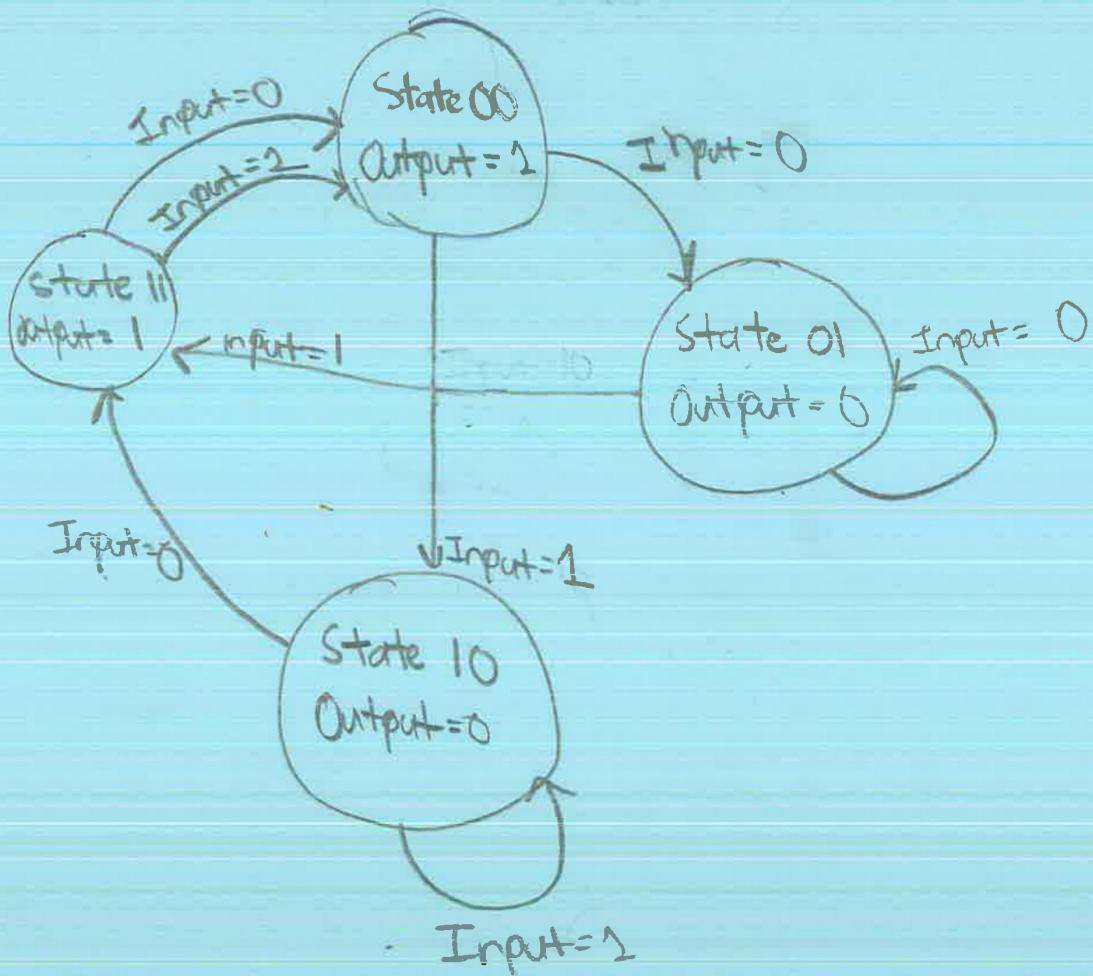
- (a) Draw a Gated D-Latch using only NAND2 gates and NOT gates. Do **not** use bubbles on the inputs of gates.

If $WE=1$ and $D=0$
 $WE=1$ and $D=1$, set R



- (b) Based on the following truth table, re-draw the finite state machine diagram. Follow a format similar to the state transition diagram in Q2(a): Represent each state with a circle containing the state number. Draw state transitions as arrows, clearly labeling them with the respective inputs. Write the output as "Output=0" or "Output=1" inside the circle for the corresponding state.

S1	S0	I	N1	N0	Output
0	0	0	0	1	1
0	0	1	1	0	1
0	1	0	0	1	0
0	1	1	1	1	0
1	0	0	1	1	0
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	0	0	1



- (c) Find and draw the ideal groupings for the following K-map and write a Sum-of-Products (SOP) formula:

	$C'D'$	$C'D$	CD	CD'
$A'B'$	0	0	0	1
$A'B$	1	1	0	1
AB	0	0	1	1
AB'	1	0	1	1

SOP Expression: $A'B'C' + AB'D' + CD' + AC$

- (d) Find and draw the ideal groupings for the following K-map and write a Sum-of-Products (SOP) formula:

	$C'D'$	$C'D$	CD	CD'
$A'B'$	1	0	x	x
$A'B$	1	0	x	1
AB	0	1	x	0
AB'	x	0	0	1

SOP Expression: $A'D' + B'D' + ABD$

