Homework 4

Graded

Student

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Total Points

92 / 100 pts

Question 1

Overview

0 / 0 pts

✔ **+ 0 pts** Correct

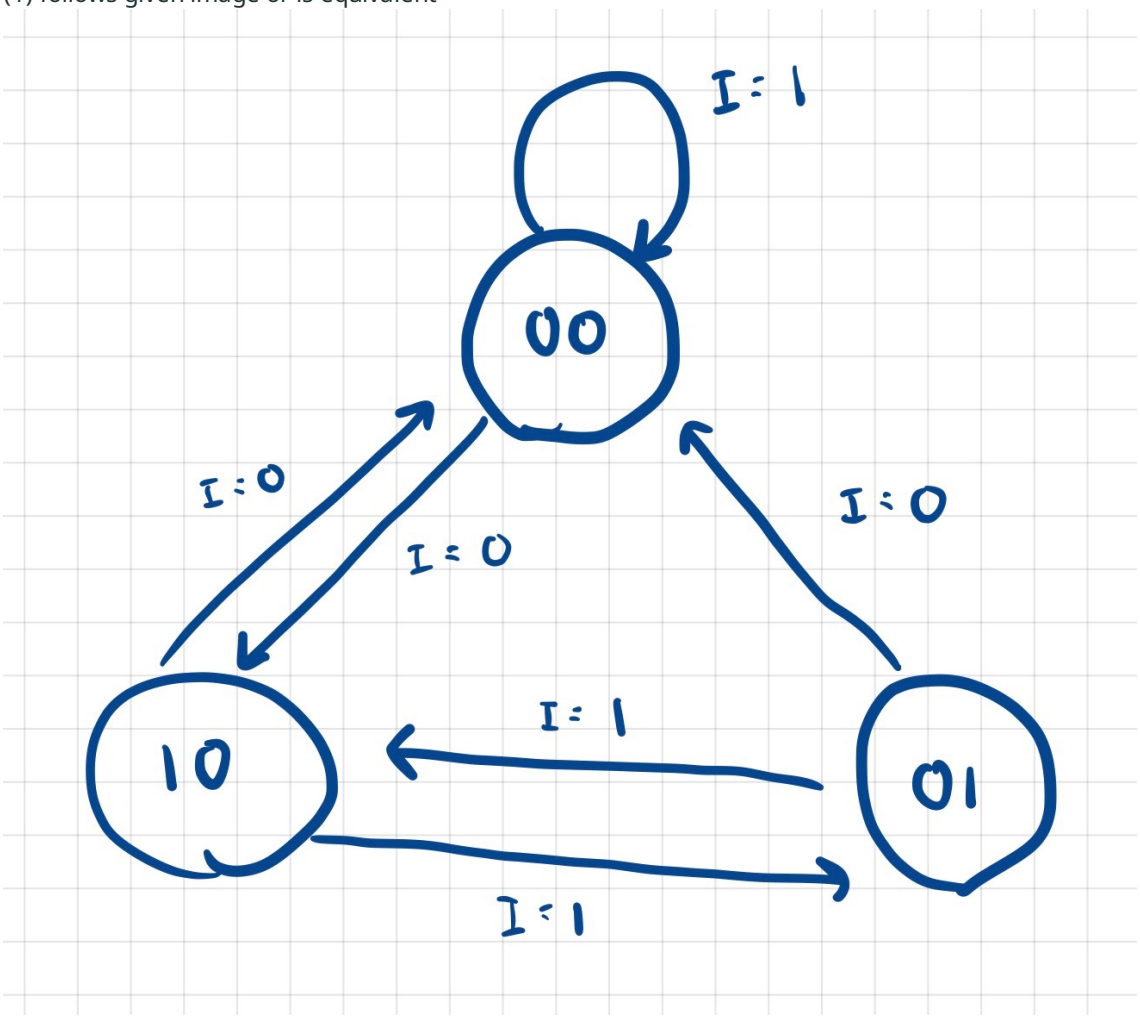
+ 0 pts Incorrect

Question 2

State Machines **10** / 10 pts

2.1 **State Machines** **10** / 10 pts

✔ **+ 10 pts** Correct:
(1) follows given image or is equivalent



+ 9 pts Partially correct - does ONE of the following:
(1) Incorrect SINGLE input for ONE state (ex. having two 0s from one state)
(2) Flips a single arrow from ONE state to another (ex. having two I = 1 arrows pointing to state 01 from state 10)

+ 8 pts Partially correct - does ONE of the following:
(1) Incorrect for BOTH of the inputs for ONE state (ex. in state 01, has I = 0 to state 10 and I=1 to state 00 instead of correct transition)
(2) Incorrect for ONE of the inputs for TWO states (ex. in state 01, has I = 0 to state 10 and in state 00 has I=1 to state 00 instead of correct transition)

+ 4 pts Partially correct - does ONE of the following
(1) Incorrect for BOTH of the inputs for TWO states (ex. in state 01, has I = 0 to state 10 and I=1 to state 00 instead of correct transition + one more similar error)

+ 1 pt Partially correct - does ONE of the following:
(1) Correct states but COMPLETELY incorrect inputs (ex. has 3 state bubbles labelled correctly but arrows are all incorrect)

+ 0 pts Incorrect

Question 3

Sequential Logic **14** / 14 pts

3.1 **Circuit Identification** **3** / 3 pts

✔ **+ 3 pts** Correct: Gated D-Latch, level-triggered (there is no partial credit on this question - it is all or nothing)

+ 3 pts Correct

+ 0 pts Incorrect

3.2 **Combinational vs. Sequential** **3** / 3 pts

✔ **+ 3 pts** Correct (sequential)

+ 3 pts Correct

+ 0 pts Incorrect

3.3 **Level/Edge Triggered Logic** **4** / 4 pts

✔ **+ 4 pts** Correct (Level-Triggered)

+ 4 pts Correct

+ 0 pts Incorrect

3.4 **(no title)** **4** / 4 pts

+ 0 pts Incorrect

✔ **+ 4 pts** Correct: 16 (all or nothing, no partial credit)

+ 4 pts Correct

Question 4

Memory **12** / 12 pts

4.1 **MAR** **6** / 6 pts

✔ **+ 6 pts** Correct: 10 (no partial credit)

+ 6 pts Correct

+ 0 pts Incorrect

4.2 **MDR** **6** / 6 pts

✔ **+ 6 pts** Correct: 16 (no partial credit)

+ 6 pts Correct

+ 0 pts Incorrect

Question 5

LC-3 Instruction Cycle **13** / 21 pts

5.1 **Fetch** **0** / 8 pts

+ 8 pts Correctly mentions ALL three of the following steps:
(1) Puts the PC value into the MAR and increments PC
(2) Reads from memory at the value of the PC
(3) Loads the Instruction Register with the next instruction
NOTE: do not subtract points for incrementing the PC in different steps - this could occur in any step technically without causing errors

+ 6 pts Partially correct - does ONE of the following:
(1) only provides 2 of the steps above
(2) Provides all three steps in correct order but one is incorrectly explained

+ 3 pts Partially correct:
(1) only provides 1 of the steps above
(2) attempts to provide all three steps but two are incorrectly explained
(3) condenses one of the steps such that there would be an error (ex. putting PC value into MAR AND reading from MEM in same cycle)
(4) Provides steps out of order such that it would cause an error (ex. reading from memory before putting PC value in MAR)

✔ **+ 0 pts** Incorrect

5.2 **Execute** **8** / 8 pts

✔ **+ 8 pts** Correct, provides the following detail:
(1) Signals are asserted on the datapath, which signals depend on instruction
(2) Gives DETAILED descriptions of different examples of instruction execution
(3) Optional: variable amount of clock cycles depending on the instruction

+ 4 pts Partially correct - does ONE of the following (if does multiple of the following, mark fully incorrect):
(1) Attempts to explain that signals are asserted but has slightly incorrect explanation
(2) Makes incorrect statement that execute takes X clock cycles (where X is a constant integer)
(3) Talks about decoding the instruction and does not explicitly state that this phase occurs before EXECUTE
(4) Just states that instruction execution differs by instruction but DOES NOT specify that different SIGNALS are activated

+ 0 pts Incorrect

5.3 **Clock Cycles** **5** / 5 pts

✔ **+ 5 pts** Correct - has BOTH of the below points in explanation:
(1) States that the LC-3 instruction cycle takes a variable amount of clock cycles
(2) States that it is a variable amount clock cycles because different instructions take different amounts of time to execute

+ 2.5 pts Partially correct - does ONE of the following:
(1) States that is is a variable number of clock cycles, but does not have explanation
(2) States that it is a variable number of clock cycles, but gives an incorrect explanation (doesn't follow rubric above)

+ 0 pts Incorrect:
(1) Claims constant amount of clock cycles
(2) No answer

Question 6

Macrostates and Von Neumann Model **15** / 15 pts

6.1 **Clock** **6** / 6 pts

✔ **+ 6 pts** Correct - answers YES and mentions ONE of the following:
(1) Ensures components are synchronized and are working together
(2) If not synchronized, causes short circuits

+ 3 pts Partially correct - does one of the following:
(1) Answers YES, but with no explanation
(2) Answers YES, but with incorrect explanation (does not provide one of above reasons)

+ 0 pts Incorrect

6.2 **(no title)** **6** / 6 pts

✔ **+ 6 pts** Correct, provides one of the following:
(1) It will cause short circuits since multiple values could be on the bus

+ 3 pts Partially correct:
(1) Explains that causes short circuits, but incorrect explanation
(2) Explains that there could be multiple values on the bus, but does not say that this causes short circuits

+ 0 pts Incorrect

6.3 **(no title)** **3** / 3 pts

✔ **+ 3 pts** Correct - Data and Instructions/Program

+ 1.5 pts Partially correct - 1 out of 2 correct answers selected

+ 0 pts Incorrect

Question 7

LC-3 Datapath **24** / 24 pts

7.1 **FETCH** **12** / 12 pts

✔ **+ 12 pts** Correct: 3 clock cycles, LD.MDR and MEM.EN selected

+ 8 pts Partially correct - does one of the following:
(1) Provides correct clock cycles, only one correct control signal (no extras)
(2) Provides correct clock cycles, two correct control signals and one incorrect control signal
(3) Provides incorrect clock cycles, two correct control signals (only provides correct ones, no extras)

+ 4 pts Partially correct - does one of the following:
(1) Provides correct clock cycles, neither correct control signal
(2) Provides correct clock cycles, two correct control signals and two incorrect control signals
(3) Provides incorrect clock cycles, one correct control signal (no extras)

+ 2 pts Partially correct - does the following:
(1) Incorrect clock cycles, all control signals selected

+ 0 pts Incorrect:
(1) Incorrect clock cycles and no control signals selected
(2) Incorrect clock cycles and only incorrect control signals selected

7.2 **(no title)** **12** / 12 pts

✔ **+ 12 pts** Correct: 1 clock cycle, ALUK = NOT, LD.REG, and GateALU selected

+ 9 pts Partially correct - does one of the following:
(1) Incorrect clock cycles, selects three correct signals
(2) Correct clock cycles, selects two correct signals
(3) Correct clock cycles, selects three correct signals and one incorrect signal

+ 6 pts Partially correct - does one of the following:
(1) Correct clock cycles, selects one correct signal
(2) Incorrect clock cycles, selects two correct signals
(3) Incorrect clock cycles, selects three correct signals and one incorrect signal

+ 3 pts (1) Correct clock cycles, no correct control signals selected
(2) Incorrect clock cycles, one correct control signal selected (no extras)
(3) Incorrect clock cycles, two correct control signals and one incorrect control signal selected
(4) Correct clock cycles, all control signals selected

+ 1 pt Partially correct - does the following:
(1) Incorrect clock cycles, all control signals selected (three correct, 2 incorrect)

+ 0 pts Incorrect:
(1) Incorrect clock cycles and no control signals selected
(2) Incorrect clock cycles and only incorrect control signals selected

Question 8

LC-3 Components **4** / 4 pts

8.1 **(no title)** **2** / 2 pts

+ 0 pts Incorrect

✔ **+ 2 pts** Correct (IR)

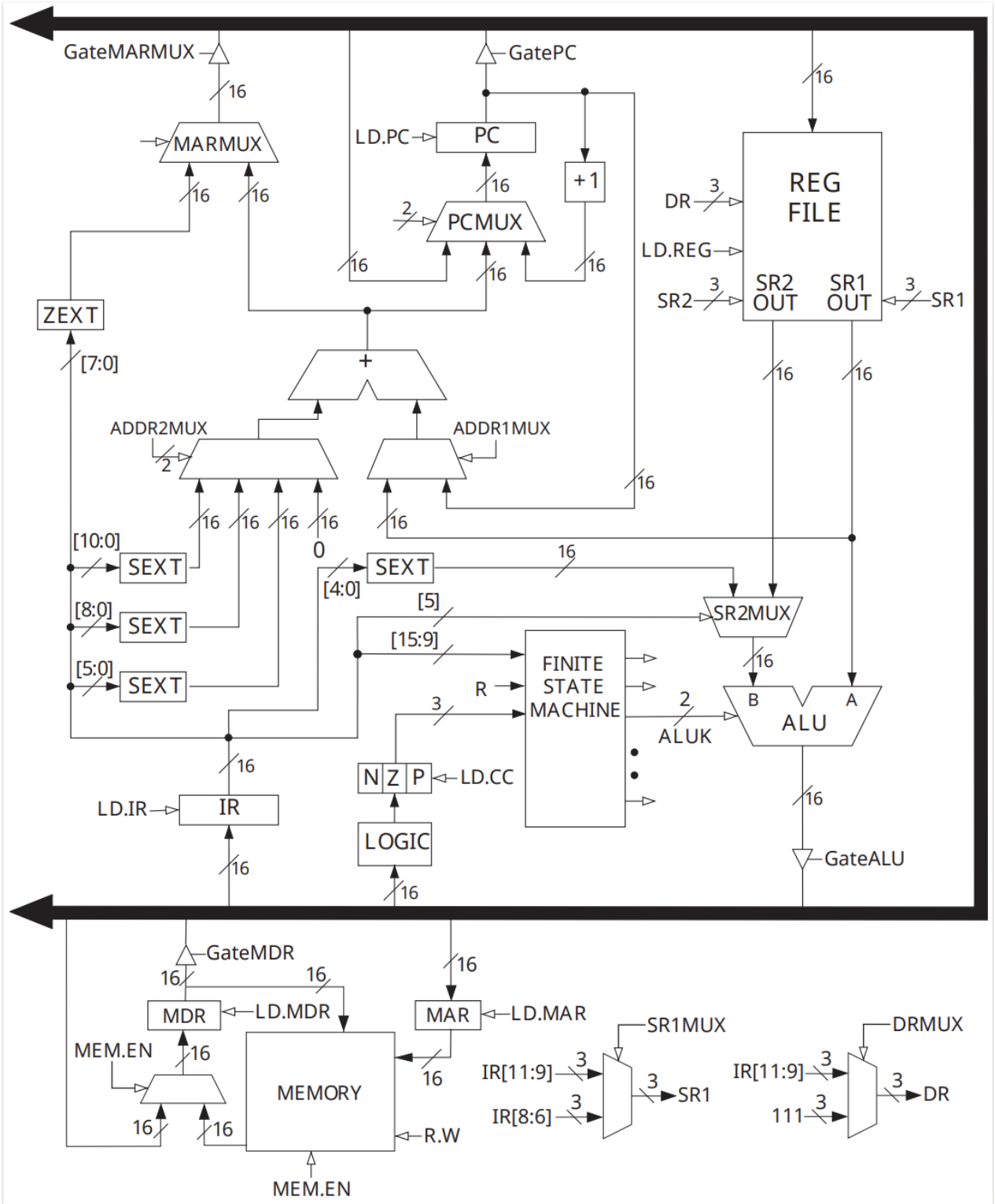
8.2 **(no title)** **2** / 2 pts

+ 0 pts Incorrect

✔ **+ 2 pts** Correct (PC)

Q1 Overview

0 Points



This homework is worth a total of 100 points.

This question (`Q1`) cannot be answered. It's used for formatting instructions. Do not worry about Gradescope saying you haven't answered one question. It's this one!

Try not to use calculators or any other computer aids in working on these problems, except to double-check your responses. Why? The exam will not allow calculators.

Please complete the following problems. The collaboration policy for the course still applies. Refer to the syllabus for details regarding this policy.

Q2 State Machines

10 Points

Q2.1 State Machines
10 Points

Draw a **binary-encoded state machine diagram** that represents the logic from the truth table provided below.

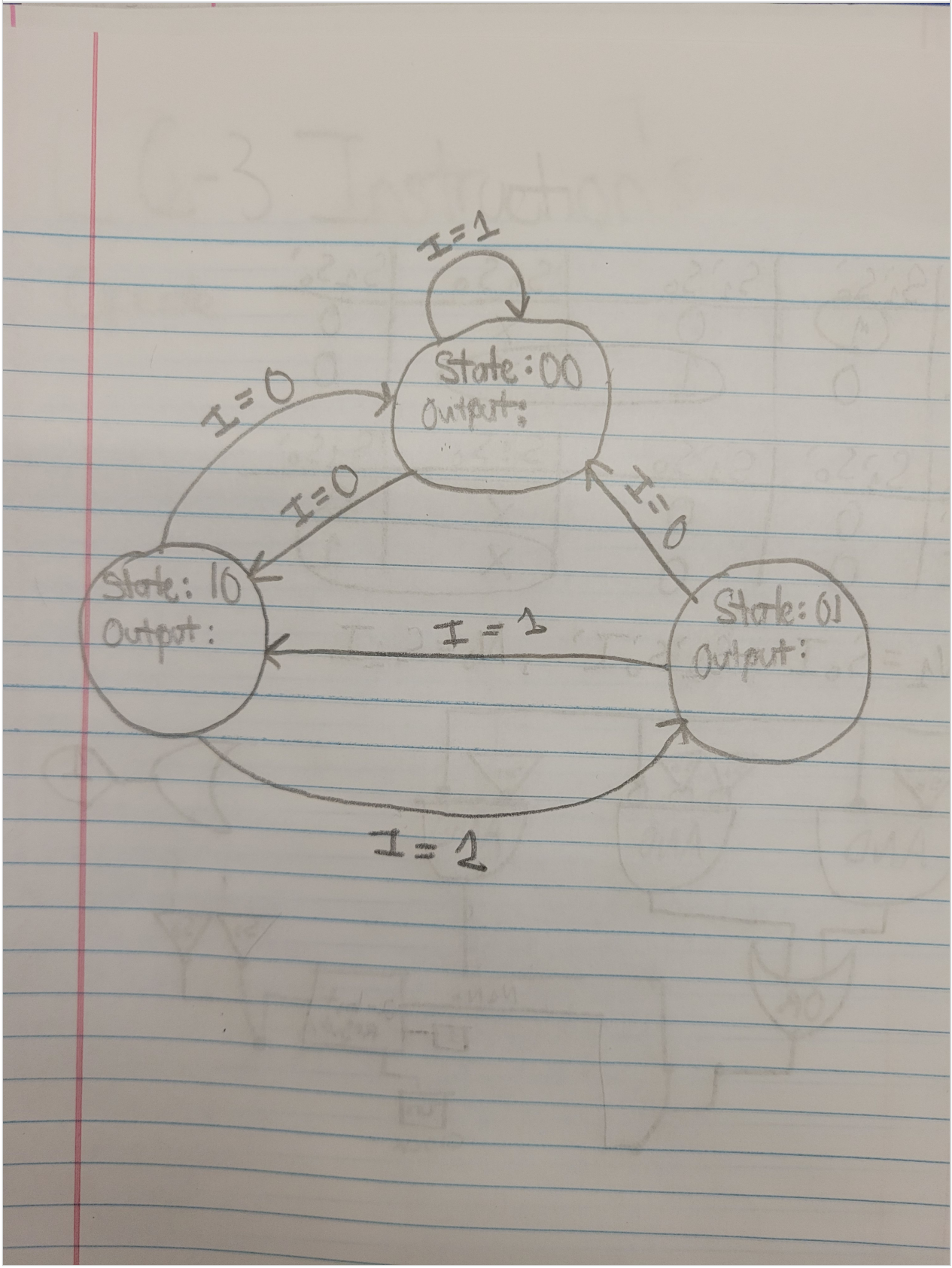
S1	S0	I	N1	N0
0	0	0	1	0
0	0	1	0	0
0	1	0	0	0
0	1	1	1	0
1	0	0	0	0
1	0	1	0	1

Formatting Notes:

- In the table above, `S1` and `S0` represent bits 1 and 0 of the current state (ex. if we are in state `01`, `S0` = 1, and `S1` = 0)
- In the table above, `N1` and `N0` represent bits 1 and 0 of the next state (ex. if the next state is `10`, `N0` = 0, and `N1` = 1)
- `I` represents the input to the state machine

Label the states with their `S0` and `S1` bits (ex. `S0` = 0, `S1` = 1, label the state as `10`)

Please draw the state machine diagram clearly on a piece of paper and upload it below.

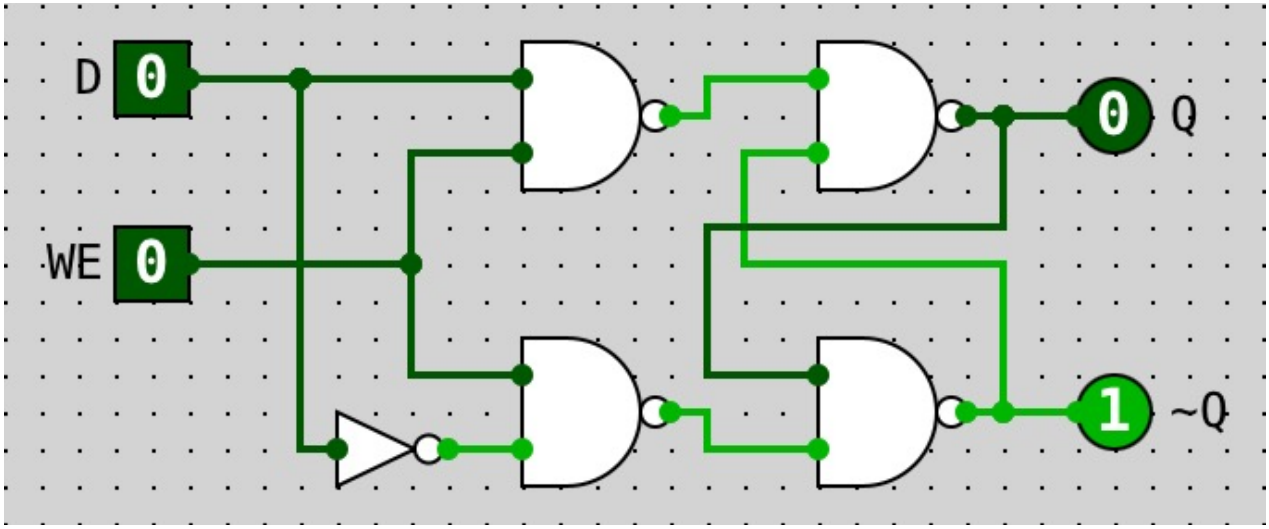


Q3 Sequential Logic

14 Points

Q3.1 Circuit Identification

3 Points



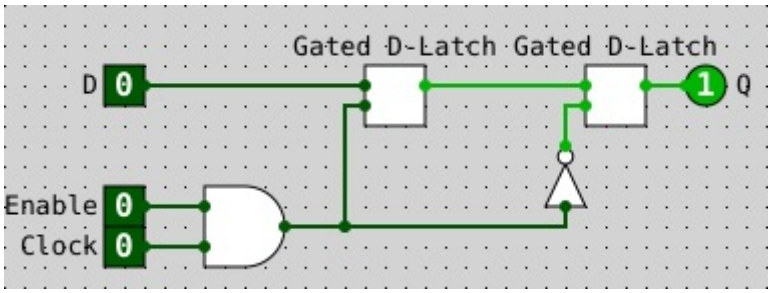
Which sequential logic circuit is the above showing?

- ○ R-S Latch
- ◉ Gated D-Latch
- ○ D Flip-Flop

Is this component level-triggered, edge-triggered, or neither?

- ◉ Level-triggered
- ○ Edge-triggered
- ○ Neither

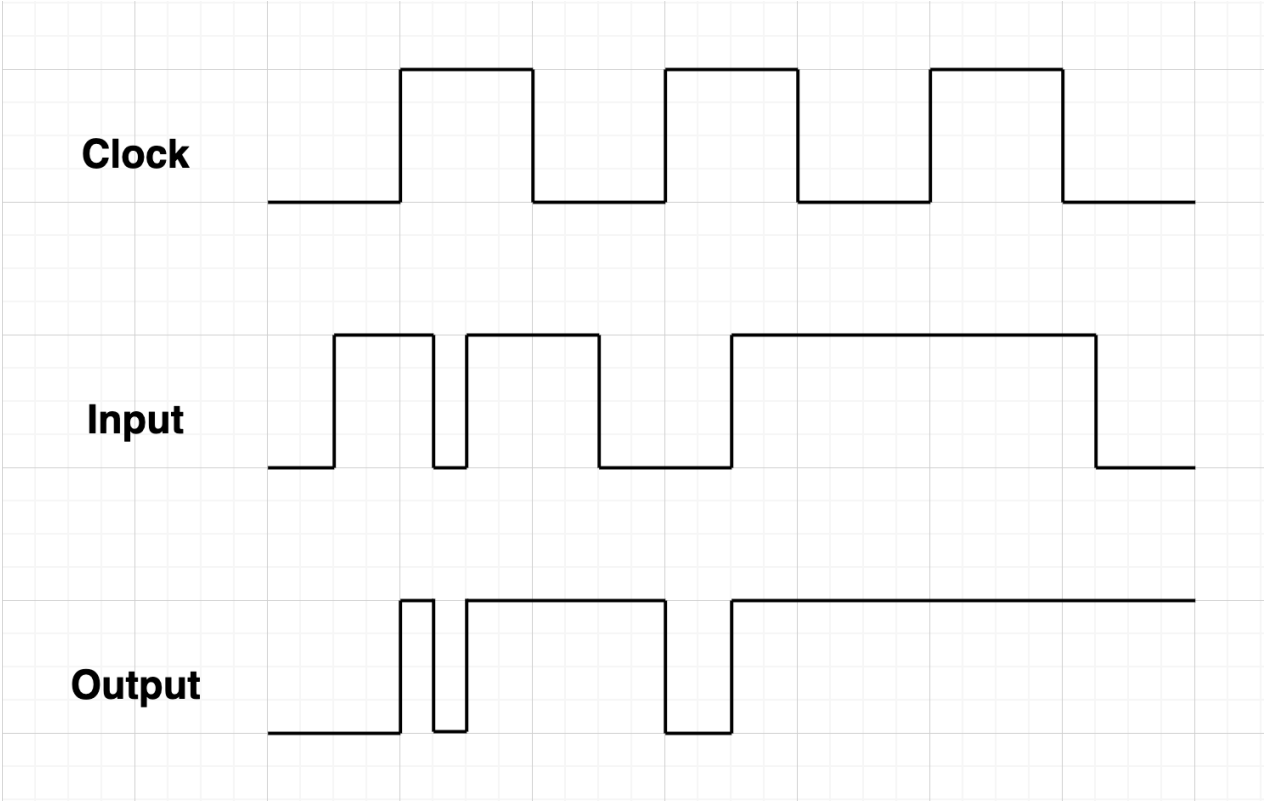
Q3.2 Combinational vs. Sequential
3 Points



Is the above circuit an example of combinational logic, sequential logic, or neither?

- ○ Combinational
- ◉ Sequential
- ○ Neither

Q3.3 Level/Edge Triggered Logic
4 Points



Assume there is a circuit that connects input to output and depends on the clock. The above diagram shows all three of these signals. Based on the diagram, what type of logic is this circuit using?

- (●) Level-Triggered
- ( ) Edge-Triggered
- ( ) Neither

Q3.4
4 Points

A computer scientist wants to build a register for their computer. This register should be able to store **8 bits**. How many **Gated D-Latches** does she need to build this register?

16

Q4 Memory
12 Points

Given a computer with **1024** memory addresses and an addressability of **16 bits**, answer the following questions as a **decimal** number (e.g. `8` not `2^3`).

This computer has a **MAR** and a **MDR**.

Do **not** include commas, spaces, or any other formatting in your answer (e.g. `4365` not `4,365` nor `4 365`).

Q4.1 MAR
6 Points

Based on the information given above, how many bits should the **MAR** be able to hold?

10

Q4.2 MDR
6 Points

Based on the information given above, how many bits should the **MDR** be able to hold?

16

Q5 LC-3 Instruction Cycle
21 Points

Q5.1 Fetch
8 Points

Describe the process of **instruction fetch** in the LC-3.

Please use *4 sentences or less.*

During the fet

Q5.2 Execute
8 Points

Describe the process of **instruction execute** in the LC-3.

Please use *4 sentences or less*.

The execute phase is when the FSM uses its given operands to assert the control signals that perform the proper operation along the LC-3. Different instructions have different execute phases which uses different control signal.

Q5.3 Clock Cycles
5 Points

How many clock cycles does an **entire** LC-3 instruction cycle take? Is it a constant number of cycles?

Explain your reasoning in three sentences or less.

It is variable because it depends on the instruction during the execute cycle. For example, LD takes 3 meanwhile LDA takes 5.

Q6 Macrostates and Von Neumann Model
15 Points

Q6.1 Clock
6 Points

Does every component in the LC-3 have to be connected to the same clock? Provide **one** reason as to why or why not.

Explain your answer in *three sentences or less*.

Yes because all the registers need to be responsive to the same clock cycle and always be in one state. In fact, memory must be synchronized together so that the FSM can function properly.

Q6.2
6 Points

What is the purpose of tri-state buffers in the LC-3? In other words, what would happen to the bus if we had no tri-state buffers?

Explain your answer in *three sentences or less*.

The purpose of the tri-state buffers is to ensure that only one gate is asserted at a time on the bus. Otherwise, the LC-3 will experience a short circuit.

Q6.3
3 Points

According to the **Von Neumann model**, what type of information is stored in the **memory unit**?

- [x] Data
- [x] Instructions/Program
- [ ] Neither

Q7 LC-3 Datapath
24 Points

The following questions will provide you with a **LC-3 macrostate or instruction**, and ask questions about its execution.

Some signals may be asserted that are not listed below. Ignore them.

Q7.1 FETCH
12 Points

How many clock cycles does the **instruction FETCH** phase take?

3

Which of the following signals **must** be asserted on the **SECOND** clock cycle of the **FETCH** macrostate?

***Hint**: In the second clock cycle of the FETCH macrostate, we would be in memory trying to find the data contained in the given address.*

- [ ] LD.MAR
- [x] LD.MDR
- [ ] MARMUX = ADDER
- [x] MEM.EN
- [ ] GateMDR

Q7.2
12 Points

How many clock cycles does it take to **execute** a **NOT** instruction?

1

Which of the following signals **must** be asserted on the **first** clock cycle of a **NOT** instruction?

Hint: `ALUK` *are the selector bits of the ALU Multiplexer, which selects which operation to perform.*

- [x] ALUK = NOT
- [ ] LD.MAR
- [ ] MARMUX = ADDER
- [x] LD.REG
- [x] GateALU

Q8 LC-3 Components

4 Points

Q8.1

2 Points

What component of the LC-3 datapath holds the **currently executing instruction**?

- ○ PC
- ◉ IR
- ○ Other

Q8.2

2 Points

What component of the LC-3 datapath holds the **address** of the **next instruction** during instruction execution?

- ◉ PC
- ○ IR
- ○ Other