

Homework 2

● Graded

Student

Devonte Dane Billings

Total Points

89 / 100 pts

Question 1

Overview

0 / 0 pts

+ 0 pts Incorrect

✓ + 0 pts Correct

Question 2

Transistors

13 / 13 pts

2.1 (no title)

2 / 2 pts

✓ + 2 pts Correct (N-type)

+ 0 pts Incorrect

+ 2 pts Correct

2.2 (no title)

3 / 3 pts

✓ + 3 pts Correct (2 P-Type and 2 N-Type)

+ 0 pts Incorrect

+ 3 pts Correct

2.3 (no title)

5 / 5 pts

✓ + 5 pts Correct:

- › Gives formula $2n$
- › Explains reasoning correctly

+ 2.5 pts Gives formula $2n$, but does not explain reasoning correctly

+ 0 pts Incorrect

2.4 (no title)

3 / 3 pts

+ 0 pts Incorrect

+ 3 pts Correct

✓ + 3 pts Correct (A)

Question 3

Combinational Logic

18 / 18 pts

3.1 (no title)

8 / 8 pts

- ✓ + 8 pts Correct: $A'B'C' + A'BC' + AB'C$ (or equivalent terms in different order)

+ 8 pts Correct

+ 5 pts provides 2 out of 3 terms correctly

+ 3 pts provides 1 out of 3 terms correctly

+ 0 pts Incorrect

3.2 (no title)

10 / 10 pts

- ✓ + 10 pts Correct

+ 8 pts Partial credit - Correct AND gates, does not use OR gate to combine outputs of AND gates (or logical equivalent)

+ 6 pts Partial credit - two correct AND gate representations of terms out of 3

+ 3 pts Partial credit - one correct AND gate representation of term out of 3

+ 0 pts Incorrect

Question 4

NOR3

16 / 16 pts

4.1 Transistors

6 / 6 pts

✓ + 6 pts Correct

+ 0 pts Incorrect

+ 5 pts Minor mistake such as:

- › missing inputs
- › missing output
- › missing power/ground
- › missing line above transistor

4.2 Cascading

6 / 6 pts

✓ + 6 pts Correct

+ 3 pts Partial credit:

- (1) only uses two cascading NOR gates and a NOT gate (bubble or actual gate both count)
- (2) Unclear gate drawings

+ 0 pts Incorrect

- (1) Just 2 cascading NORs
- (2) Uses other gates
- (3) Drawn with transistors
- (4) Not equivalent to NOR3

4.3 Comparison

4 / 4 pts

✓ + 4 pts Correct, provides at least one of the facts below:

- › NOR3 has 6 transistors, which is less than NOR3 with cascading NOR2 gates.
- › NOR3 built with cascading NOR2 gates has 12 transistors.
- › More efficient to build NOR3 itself with transistors instead of cascading NOR2 gates as it requires less transistors. (Wiring is negligible compared to transistors).

+ 1.5 pts Correct conclusion (build w/ transistors), but does not explain reasoning

+ 0 pts Incorrect

Question 5

Multiplexers and Decoders	14 / 14 pts
5.1 (no title)	2 / 2 pts
+ 2 pts Correct	
✓ + 2 pts Correct (4)	
+ 0 pts Incorrect	
5.2 (no title)	2 / 2 pts
+ 2 pts Correct	
✓ + 2 pts Correct (32)	
+ 0 pts Incorrect	
5.3 (no title)	2 / 2 pts
+ 2 pts Correct	
✓ + 2 pts Correct (1)	
+ 0 pts Incorrect	
5.4 (no title)	2 / 2 pts
+ 2 pts Correct	
✓ + 2 pts Correct (8)	
+ 0 pts Incorrect	
5.5 (no title)	6 / 6 pts
✓ + 6 pts Correct	
+ 2 pts Partial credit - incorrect, but ATTEMPTS to use decoder and AND gates to select between inputs	
+ 0 pts Incorrect	

Question 6

Circuit Tracing	10 / 10 pts
✓ + 10 pts Correct (0, 1, 1, 1)	
+ 10 pts Correct	
+ 6 pts 3 out of 4 correct	
+ 4 pts 2 out of 4 correct	
+ 2 pts 1 out of 4 correct	
+ 0 pts Incorrect	

Question 7

DeMorgan's Law/Bubble Theorem

0 / 11 pts

7.1 (no title)

0 / 6 pts

+ 6 pts Correct: $\sim A \mid (B \mid C) \mid \sim(\sim A \mid \sim C)$

+ 6 pts Correct

✓ + 0 pts Incorrect

7.2 (no title)

Resolved 0 / 5 pts

+ 5 pts Correct

✓ + 0 pts Incorrect

C Regrade Request

Submitted on: Sep 24

My answer was correct.

No it is not, because your last NAND gate has 2 outputs coming from the same NAND gate with one of them being inverted, this means the circuit will always output a value of 1, because if there is a 0 in any of a NAND's inputs, it will be a 1.

Reviewed on: Sep 24

Question 8

K-Maps

18 / 18 pts

8.1 (no title)

6 / 6 pts

+ 6 pts Correct: $BD + BC + A'CD + B'C'D'$

✓ + 6 pts Correct

+ 4.5 pts 3 out of 4 terms correct

+ 3 pts 2 out of 4 terms correct

+ 1.5 pts 1 out of 4 terms correct

+ 0 pts Incorrect

8.2 (no title)

6 / 6 pts

+ 6 pts Correct: $AC + A'B'C'$

✓ + 6 pts Correct

+ 3 pts provides 1 out of 2 correct terms

+ 0 pts Incorrect

8.3 (no title)

6 / 6 pts

+ 6 pts Correct: $A'BC'D$ (or equivalent)

✓ + 6 pts Correct

+ 0 pts Incorrect

+ 2 pts Typo

Q1 Overview**0 Points**

Please complete the following problems.

The collaboration policy for the course still applies. Refer to the syllabus for details regarding this policy.

Q2 Transistors

13 Points

Q2.1

2 Points

This type of transistor is closed when a 1 is applied to the gate and connects to ground.

- P-type
- N-type

Q2.2

3 Points

In CMOS design, what is the **minimum** number of each transistor required to build a **2-input NAND gate**?

P-type:

2

N-type:

2

Q2.3

5 Points

Write a general formula for the **total** (N-type and P-type) **minimum** number of transistors required to build a **NAND_n** gate where **n** is the number of **inputs** to the **NAND** gate.

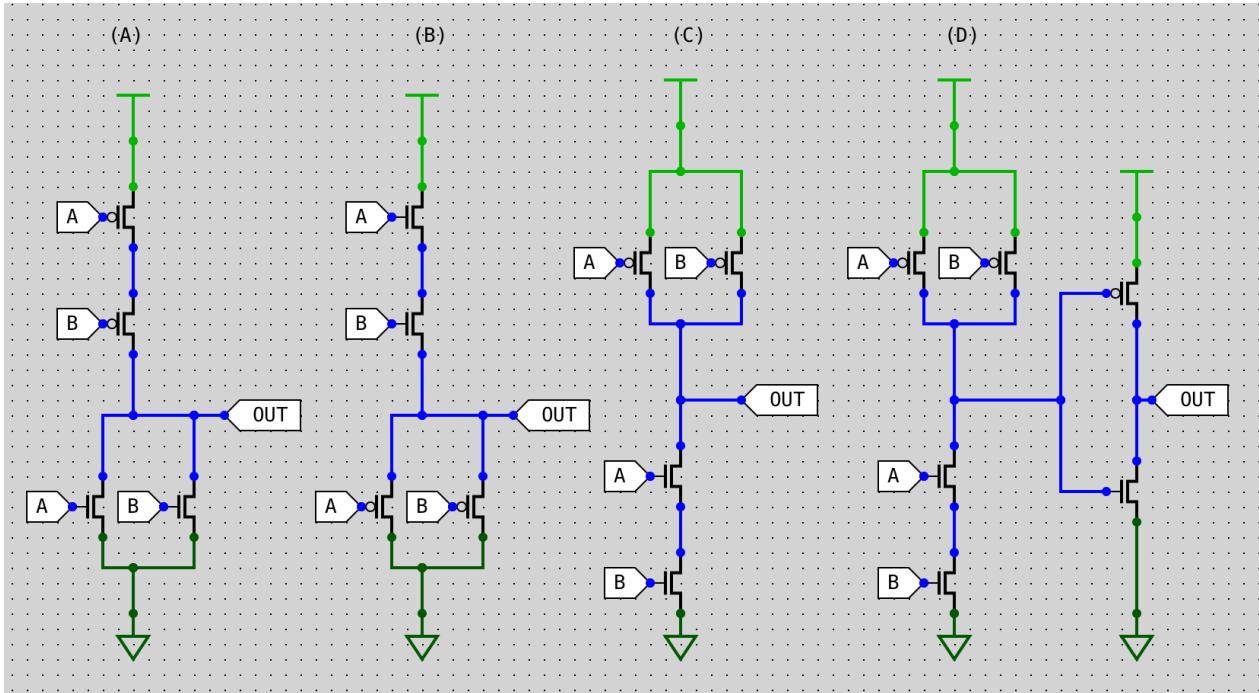
Explain your answer in 1-2 sentences.

To build a NAND gate, n P-type transistors are required to be in series and n N-type transistors are required to be parallel. In total, $2n$ transistors are required.

Q2.4

3 Points

Which of the following transistor diagrams represents a valid, functioning NOR2 gate? The inputs are represented by A and B and the output is represented by OUT.



A

B

C

D

Q3 Combinational Logic

18 Points

Q3.1

8 Points

Given the following truth table, please generate a boolean expression which describes the variable O using A, B, and C. Write your answer in the sum of products format. Do not simplify your answer.

You should use **'** for **NOT** (no spaces) and **+** for **OR** (use spaces in between).

For **AND**, put the inputs together with no space.

Example (NOT THE ANSWER): $AB + A'B'C'$

A	B	C	O
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

A'B'C' + A'BC' + AB'C

Q3.2

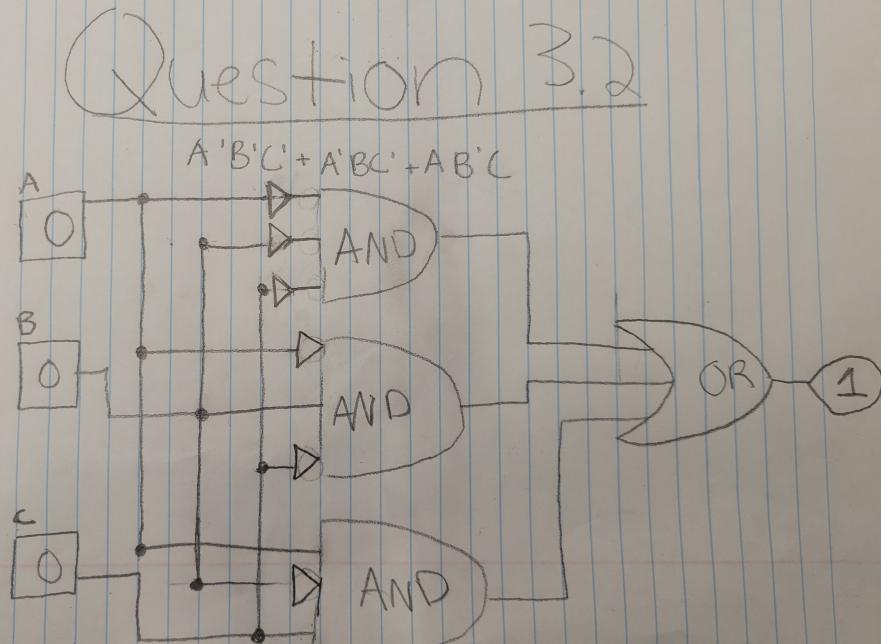
10 Points

Create a circuit representation of the boolean expression created in 3.1. You do **not** need to draw the gates with transistors.

Please draw the circuit clearly on a piece of paper and upload it below.

▼ 16945485779892258814290708283938.jpg

Download



Q4 NOR3

16 Points

Q4.1 Transistors

6 Points

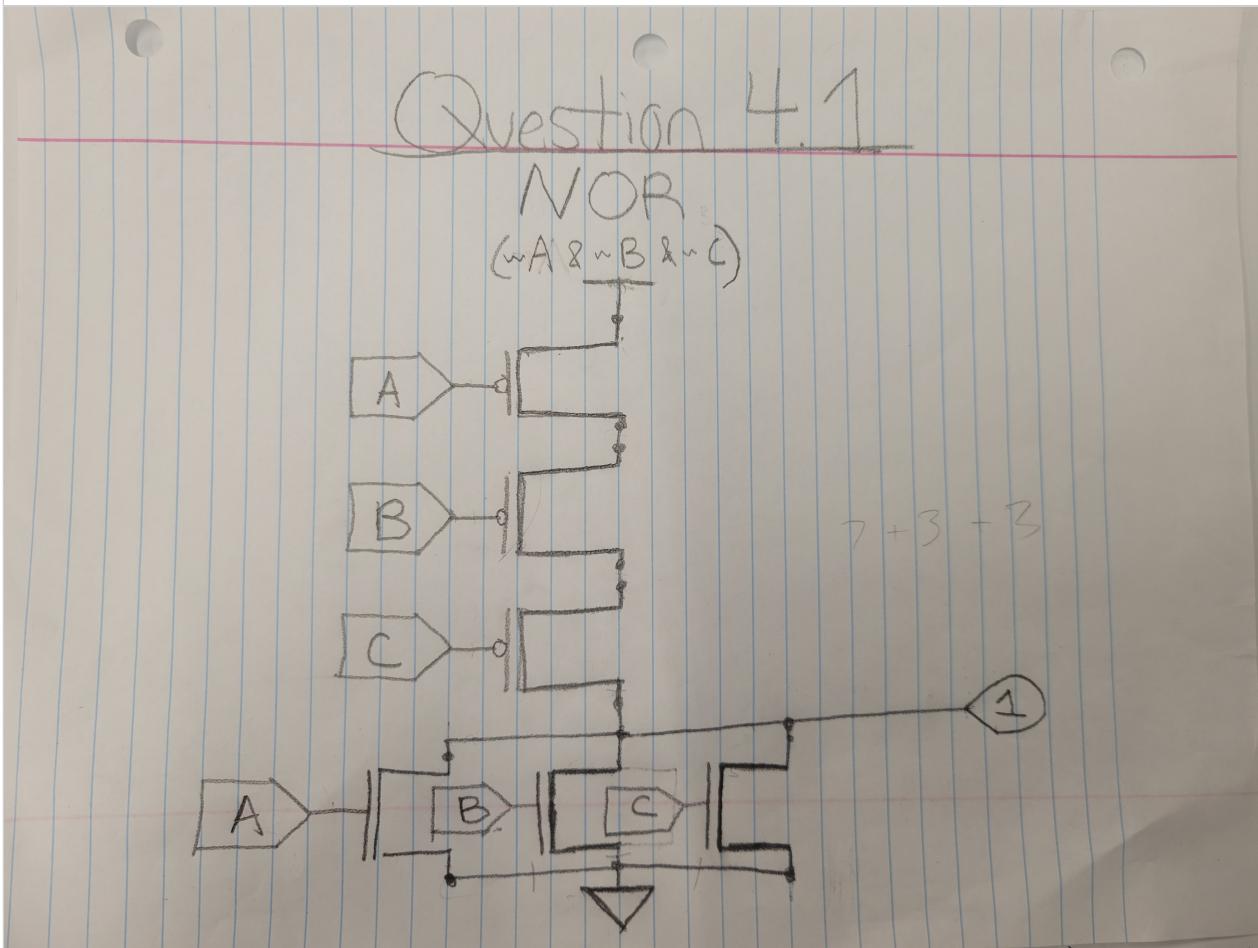
Using only P-type and N-type transistors, 3 inputs, and basic wiring, create an NOR3 gate.

A NOR3 gate is an NOR gate with 3 inputs.

Please draw the circuit clearly on a piece of paper and upload it below.

▼ 16945486495204535310960446008202.jpg

 Download



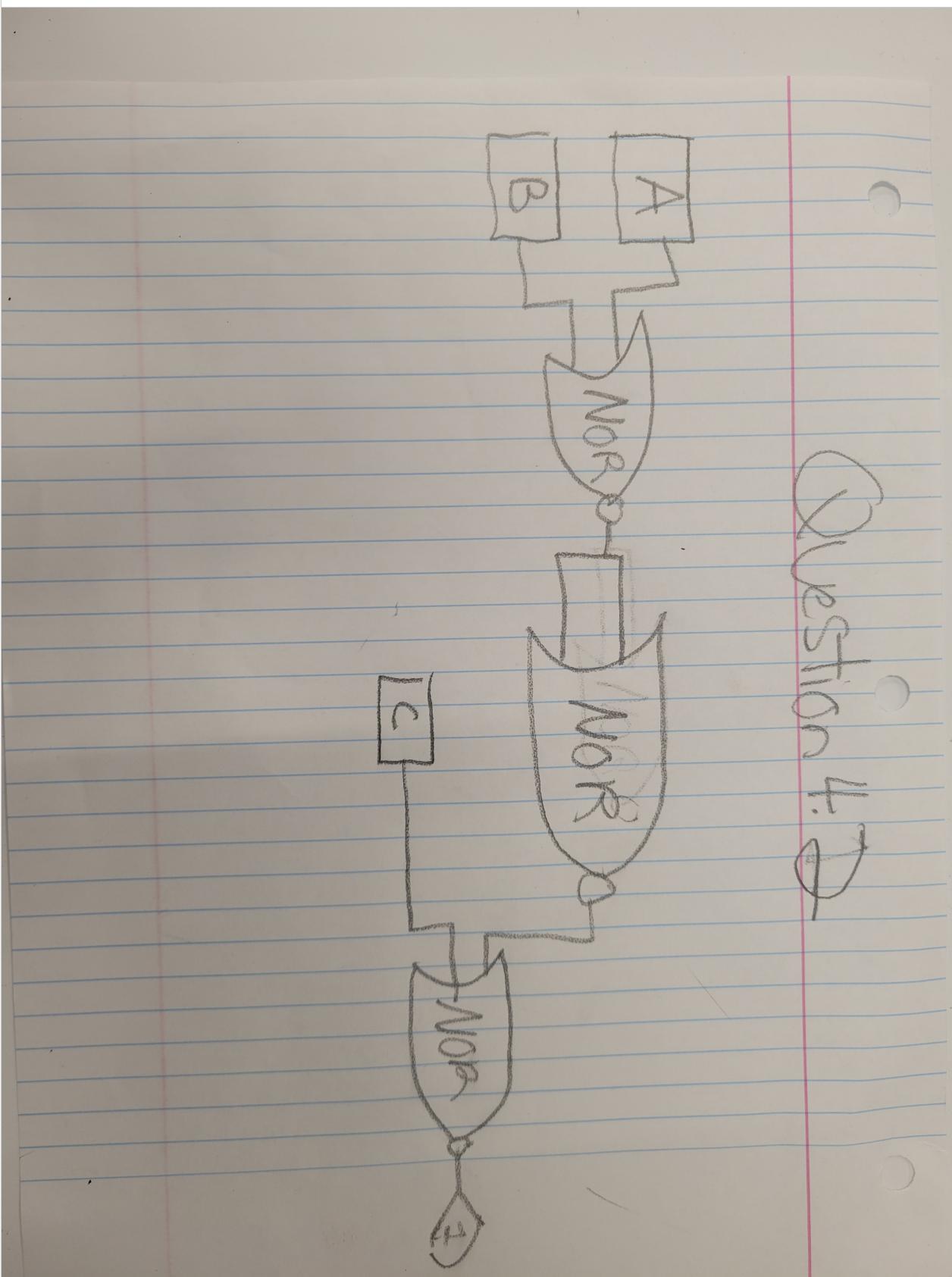
Q4.2 Cascading

6 Points

Using **only** NOR2 gates, the 3 inputs, and basic wiring, create an NOR3 gate.

A NOR2 gate is an NOR gate with 2 inputs. You do **not** need to draw the NOR2 gates out of transistors.

Please draw the circuit clearly on a piece of paper and upload it below.



Q4.3 Comparison

4 Points

Compare your implementation of the NOR3 gate with transistors and with NOR2 gates. If you were deciding which to use, which would be the better choice? Think about the total hardware (transistors and wires) cost of the circuit.

Let's compare the number of transistors and wires required in Q4.1 vs Q4.2.

In Q4.1, the number of transistors required are 3 P-type transistors + 3 N-type transistors = 6 transistors. Additionally, at least 16 wires are used to connect the circuit.

In Q4.2, there are 3 individual NOR gates, already equating to 18 transistors and 48 wires. Additionally, to connect each NOR gate and run the circuit, there are 9 wires used. Therefore, this question requires 18 transistors and 57 wires.

The obvious better choice would be the solution to Q4.1 that uses transistors to create a NOR3 gate because it uses less transistors and less wires than the remaining gates. Less hardware required means less money to spend, and less money to spend means more happiness.

Q5 Multiplexers and Decoders

14 Points

Please give all answers as **integers**, not as an expression (eg. 1024 instead of 2^{10}).

Q5.1

2 Points

Given a decoder with 16 outputs, what is the **minimum** number of input/selector bits it must have?

4

Q5.2

2 Points

Given a decoder with 5 input/selector bits, what is the **maximum** number of outputs it can have?

32

Q5.3

2 Points

Given a multiplexer with 8 selector bits, up to **how many outputs can it have?**

1

Q5.4

2 Points

Given a multiplexer with 3 selector bits, what is the **maximum** number of inputs it can have?

8

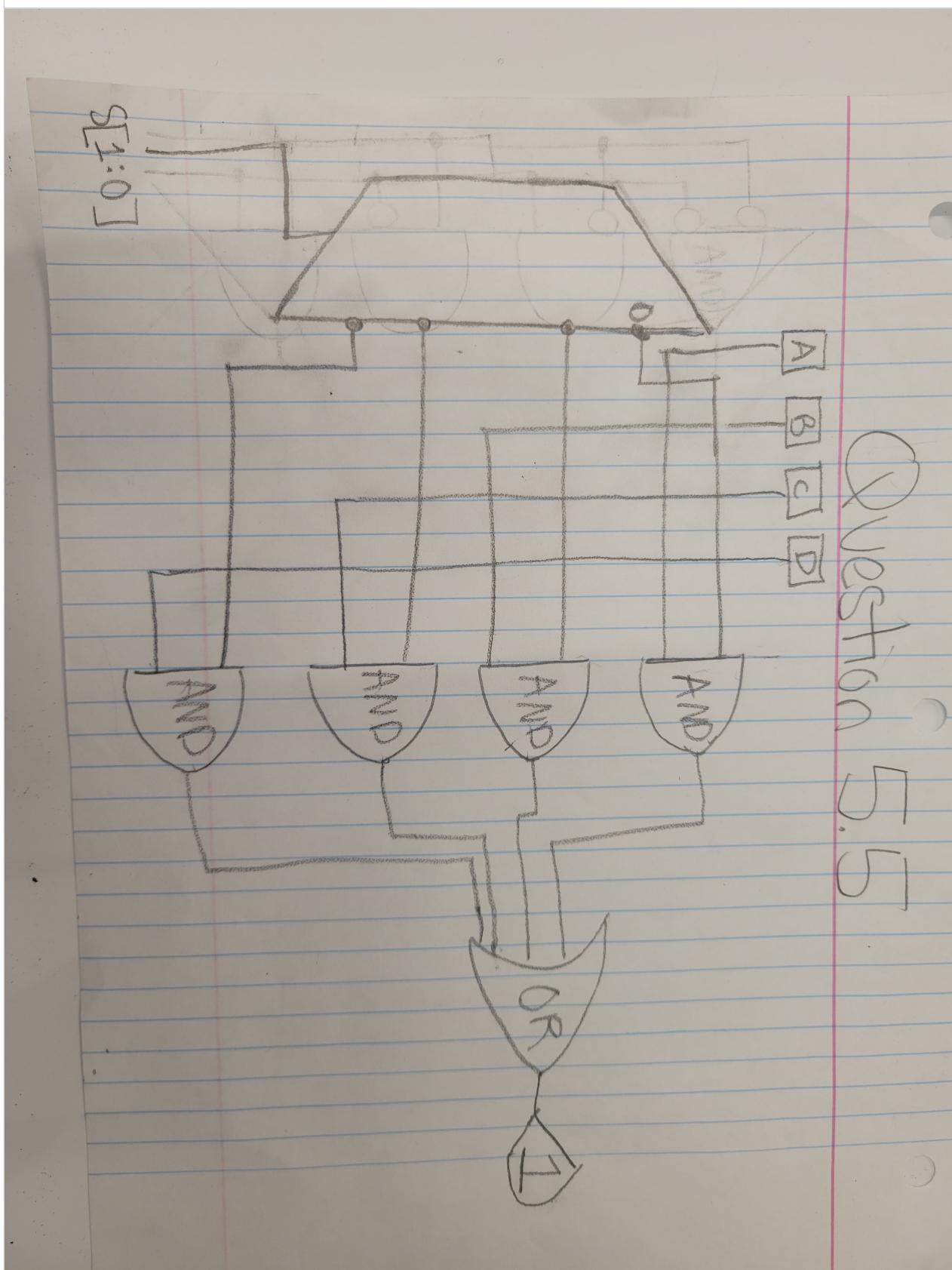
Q5.5

6 Points

You want to build an **4-to-1 mux**, but all you have is a **2-to-4 decoder** plus a supply of **AND** and **ORs** of various fan-ins (e.g., AND2, AND3, etc.)!

Show how you can construct the **4-1 mux** out of the **decoder** using these **extra gates**. You **may** use the simplified symbol for a decoder in your drawing.

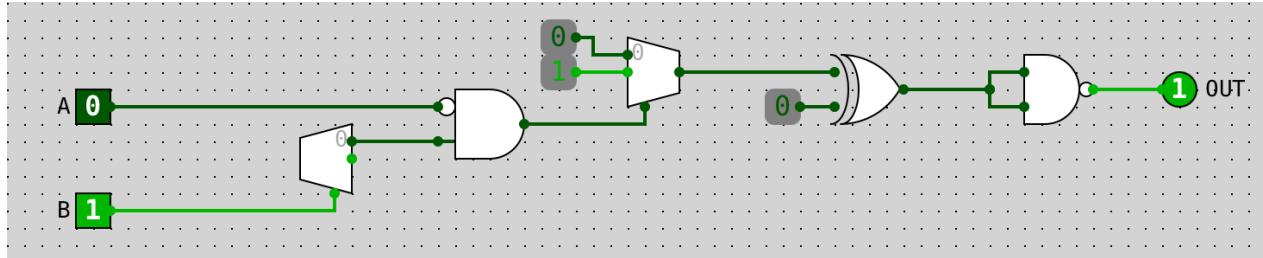
Please draw the circuit clearly on a piece of paper and upload it below.



Q6 Circuit Tracing

10 Points

Fill out the truth table below for the following circuit. The output should be either a **1** or a **0**. Fill in the corresponding short answer questions to the entries in the table below numbered 1-4.



A	B	OUT
<input type="text" value="0"/>	<input type="text" value="0"/>	(1)
<input type="text" value="0"/>	<input type="text" value="1"/>	(2)
<input type="text" value="1"/>	<input type="text" value="0"/>	(3)
<input type="text" value="1"/>	<input type="text" value="1"/>	(4)

(1)

(2)

(3)

(4)

1

Q7 DeMorgan's Law/Bubble Theorem

11 Points

Q7.1

6 Points

Convert the following Boolean expression to one that only uses ORs and NOTs

Do not simplify

$$\sim(A \& (\sim B \& \sim C) \& \sim(A \& C))$$

$$\sim(\sim A + \sim(B+C) + \sim\sim(\sim A + \sim C))$$

Q7.2

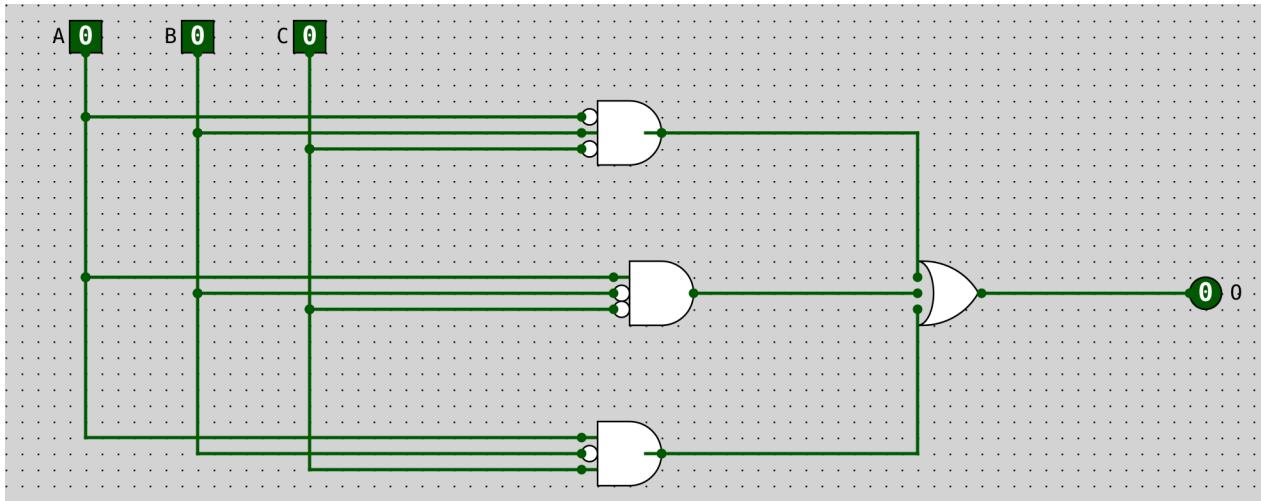
5 Points

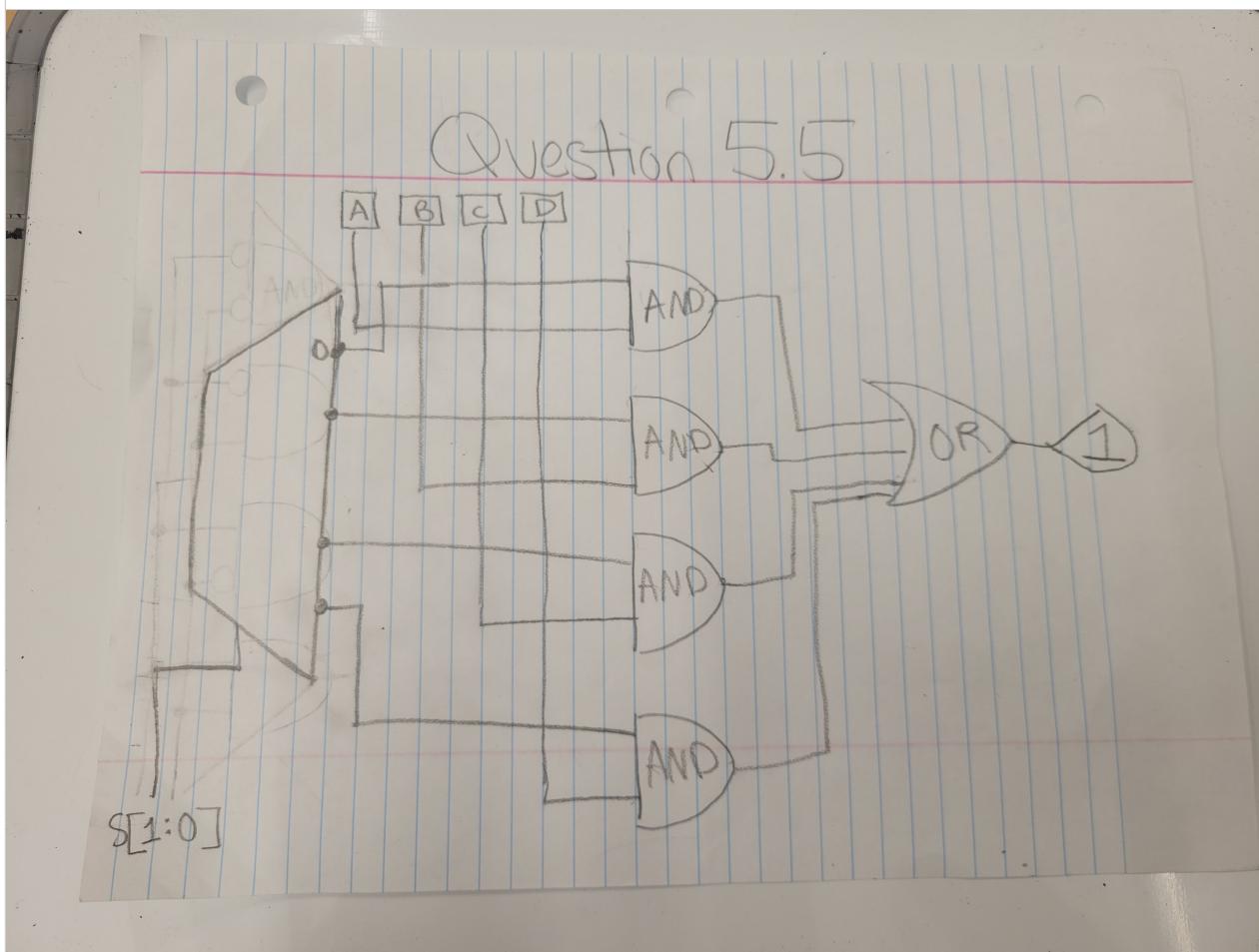
The following sum of products circuit currently uses 3 **AND3** gates, 1 **OR3** gate, and 5 **NOT** gates.

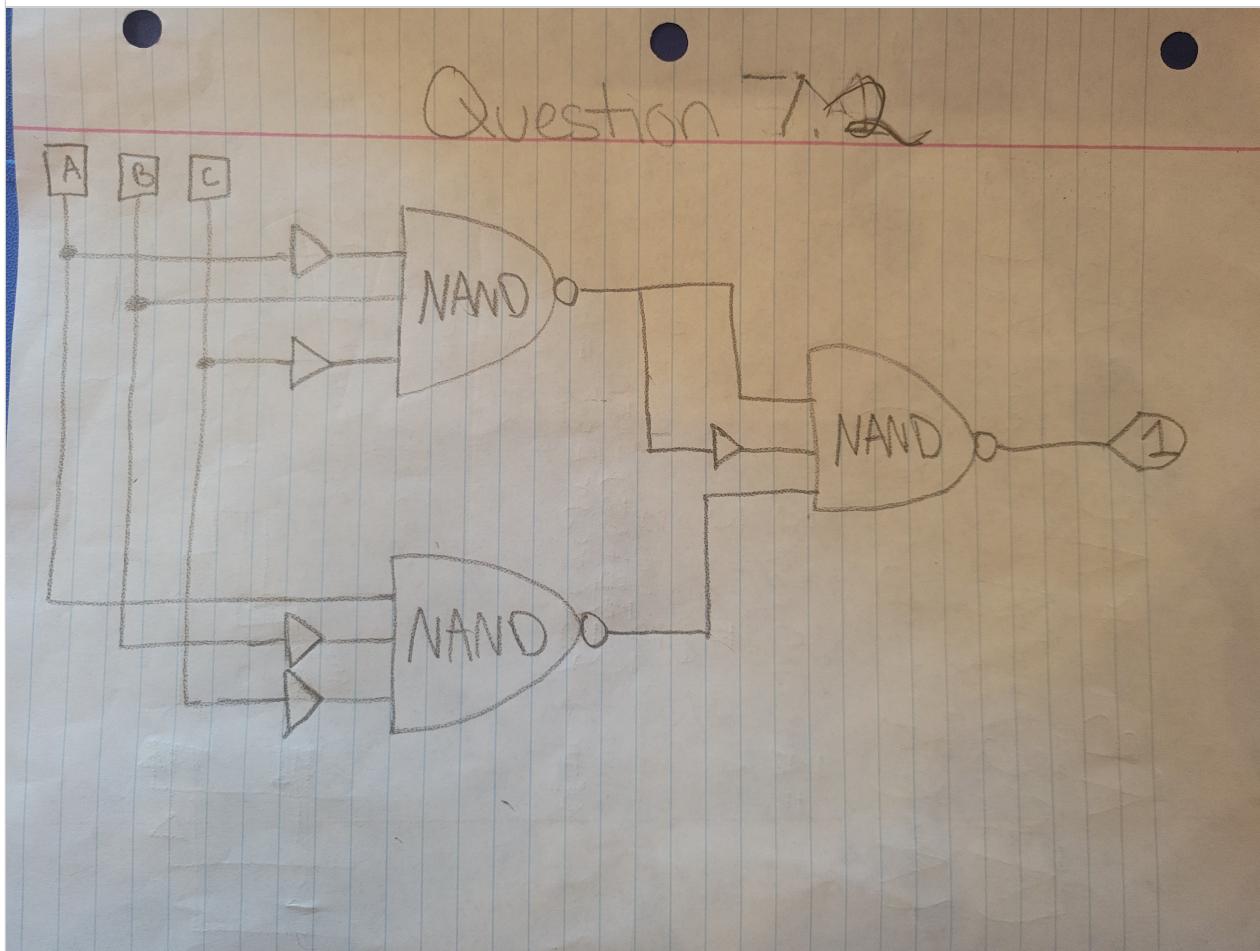
Build a logically equivalent circuit with **only** **NAND3** and **NOT** gates. Use the **minimum** number of gates as possible.

You can assume that the 3-input gates are built in the most efficient transistor implementation.

Please draw the circuit clearly on a piece of paper and upload it below.







Q8 K-Maps

18 Points

Simplify the following K-Maps. Write the corresponding boolean expression with
as few terms as possible.

Q8.1
6 Points

	CD	C'D	C'D'	CD'
AB	1	1	0	1
A'B	1	1	0	1
A'B'	1	0	X	0
AB'	0	0	1	0

Simplify the K-Map above. Write the corresponding boolean expression with **as few terms as possible.**

- Use a single quote ' to denote the complement of a variable.
- Only use the variables A, B, C and D.
- Do not include spaces for AND (e.g. use AB, instead of A AND B, A * B, or A • B)
- Use + for OR (e.g. C+D)
- Within terms that are AND-ed together, place variables alphabetically (e.g. use ACD + BC, not CAD+CB)
- Example of an answer in the correct format: A'B+CD'
- **Do not use spaces in your answer.**

BD+A'CD+B'C'D'+BC

Q8.2

6 Points

	CD	C'D	C'D'	CD'
AB	1	0	0	1
A'B	0	0	0	0
A'B'	0	1	X	0
AB'	1	0	0	1

Simplify the K-Map above. Write the corresponding boolean expression with **as few terms as possible.**

- Use a single quote ' to denote the complement of a variable.
- Only use the variables A, B, C and D.
- Do not include spaces for AND (e.g. use AB, instead of A AND B, A * B, or A • B)
- Use + for OR (e.g. C+D)
- Within terms that are AND-ed together, place variables alphabetically (e.g. use ACD + BC, not CAD+CB)
- Example of an answer in the correct format: A'B+CD'
- **Do not use spaces in your answer.**

AC+A'B'C'

Q8.3

6 Points

	CD	C'D	C'D'	CD'
AB	0	0	0	0
A'B	0	1	0	0
A'B'	0	0	X	0
AB'	0	0	0	0

Simplify the K-Map above. Write the corresponding boolean expression with **as few terms as possible.**

- Use a single quote ' to denote the complement of a variable.
- Only use the variables A, B, C and D.
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- Within terms that are AND-ed together, place variables alphabetically (e.g. use ACD + BC, not CAD+CB)
- Example of an answer in the correct format: A'B+CD'
- **Do not use spaces in your answer.**

A'BC'D