CS-2110 A/B/C Quiz 1 (B)

[redacted]

TOTAL POINTS

86 / 100

QUESTION 1

1 1A **4 / 4**

✓ **+ 4 pts** *Correct (1011 1000, no overflow)*

+ 2 pts Answer or overflow incorrect

+ 0 pts Incorrect

QUESTION 2

2 1B **4 / 4**

✓ **+ 4 pts** *Correct (1101 1001, yes overflow)*

+ 2 pts Answer or overflow incorrect

+ 0 pts Incorrect

QUESTION 3

3 1C **6 / 6**

✓ **+ 6 pts** *Correct (255)*

+ 2 pts incorrect base (1111 1111 or 0xFF)

+ 0 pts Incorrect

QUESTION 4

4 1D **6 / 6**

✓ **+ 6 pts** *Correct:*

(1) 4

(2) 8

+ 3 pts Partially correct - one answer correct

+ 0 pts Incorrect

QUESTION 5

5 1E **2 / 6**

+ 6 pts Correct (0x005E, 0xFFC4)

+ 3 pts Partially Correct - one answer correct

✓ **+ 2 pts** *Partial credit: Both correct in binary*

+ 0 pts Incorrect

QUESTION 6

1F 24 pts

6.1 i **4 / 4**

✓ **+ 4 pts** *Correct (False + Correct Explanation (3 selector bits))*

+ 2 pts Partially correct (False + wrong or incomplete explanation)

+ 0 pts incorrect

6.2 ii **4 / 4**

✓ **+ 4 pts** *Correct (False + Correct Explanation - MSB is the signed bit so there is are two representations of 0)*

+ 2 pts Partially Correct (False + Wrong explanation)

+ 0 pts incorrect

6.3 iii **4 / 4**

✓ **+ 4 pts** *Correct (True + Correct Explanation - n selector bits for 2^n input bits, alternatively: for n inputs, $$log_2$$n selector bits)*

+ 2 pts Partially correct (True + Wrong explanation)

An example of a wrong explanation is $\sqrt{n}$

+ 0 pts incorrect

6.4 iv **2 / 4**

+ 4 pts Correct (True + Correct explanation - You can examine bit by bit left to right from the MSB to determine which one is bigger just like signed magnitude)

+ 4 pts Correct (False + mentions edge cases of IEEE 754 like NaN)

✓ **+ 2 pts** *Partially Correct (True + Mentions that the first bit is the sign bit)*

+ 2 pts Partially Correct (True + Wrong explanation, like comparing only positive vs. negative numbers)

+ 0 pts incorrect

6.5 v **4 / 4**

✓ **+ 4 pts** *Correct (False + Correct explanation - range of 5 bit 2s complement [-16,15] or [-2^n-1, 2^n-1 - 1])*

+ 2 pts Partially Correct (False + Wrong explanation)

+ 0 pts incorrect

6.6 vi **4 / 4**

✓ **+ 4 pts** *Correct (True + Correct explanation - A turing machine is "a mathematical model of a hypothetical computing machine which can use a predefined set of rules to determine a result from a set of input variables" or something similar)*

+ 2 pts Partially Correct (True + Wrong explanation)

+ 0 pts incorrect

QUESTION 7

7 2A **8 / 8**

✓ **+ 8 pts** *Fully Correct (1,1,1,1,1,1,1,1)*

+ 4 pts Inverse

+ 6 pts 1 row incorrect

+ 4 pts 2 rows incorrect

+ 2 pts 3 rows incorrect

+ 0 pts 4 or more row incorrect

QUESTION 8

8 2B **0 / 8**

+ 8 pts Correct (NOT)

+ 4 pts Incorrect (NAND)

✓ **+ 0 pts** *incorrect*

QUESTION 9

9 2C **9 / 9**

✓ **+ 9 pts** *Correct*

![Screenshot_2023-09-13_at_8.37.56_PM.png](/files/18c5ace5-3e26-4e0a-92dd-d6b9cfc1a6ef)

+ 0 pts incorrect

+ 6 pts Mostly correct (e.g. no output wire, switched n/p types). Drawing a NAND doesn't count (wrong)

QUESTION 10

10 3A **8 / 8**

✓ **+ 8 pts** *Fully Correct (0,1,1,0,1,0,1,0)*

+ 4 pts Inverse

+ 6 pts 1 row incorrect

+ 4 pts 2 rows incorrect

+ 2 pts 3 rows incorrect

+ 0 pts 4 or more row incorrect

QUESTION 11

11 3B **8 / 8**

✓ **+ 8 pts** *Correct (Example below or equivalent)*

![Screenshot_2023-09-13_at_8.17.40_PM.png](/files/f64f7dbc-4f27-4ceb-bf2a-1c30f2d48842)

+ 0 pts incorrect

QUESTION 12

12 3C **9 / 9**

✓ **+ 9 pts** *Correct (Example below or equivalent)*

![Image_9-13-23_at_8.24_PM.png](/files/750450fe-4492-4c7a-889a-7d7bfcaf3670)

+ 5 pts Structure (2 muxes feeding into a 3rd) is correct but one or more inputs were wrong

+ 0 pts incorrect

Name [PRINT CLEARLY]: [redacted]

GT username (e.g. gburdell3): [redacted]

CS 2110: Computer Organization and Programming
Gupta/Conte/Adams Fall 2023

QUIZ 1
VERSION B

This exam is given under the Georgia Tech Honor Code System. Anyone found to have submitted copied work instead of original work will be dealt with in full accordance with Institute policies.

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[MUST sign:] [redacted]

(a) THIS IS A CLOSED BOOK, CLOSED NOTES EXAM
(b) NO CALCULATORS
(c) This examination handout has **5** pages.
(d) Do all your work in this examination handout.
(e) Use the back of the exam sheets if necessary.
(f) WHERE NEEDED, SHOW ALL YOUR INTERMEDIATE RESULTS TO RECEIVE FULL CREDIT

In case you forgot, here are some good facts to know:

Hex	Dec
0x1	1
0x2	2
0x3	3
0x4	4
0x5	5
0x6	6
0x7	7
0x8	8
0x9	9
0xA	10
0xB	11
0xC	12
0xD	13
0xE	14
0xF	15

x	2^x
1	2
2	4
3	8
4	16
5	32
6	64
7	128
8	256
9	512
10	1024
11	2048
12	4096
13	8192
14	16,384
15	32,768
16	65,536

Problem	Points	Score
1	50	
2	25	
3	25	
TOTAL	100	

GOOD LUCK!

More good facts to know:

1K = 2^{10}
1M = 2^{20}
1G = 2^{30}
1T = 2^{40}
1P = 2^{50}
1E = 2^{60}

1. [50 pts] Answer the following short questions. Show your work (where needed) to receive full credit.

(a) Compute the following operation on two **2's complement 8-bit binary numbers**. Write your answer as a **2's complement 8-bit binary number**. Then circle "Yes" if the calculation results in overflow, otherwise circle "No." The word size is **8 bits**.

```
 1111111
  1011 1010
+ 1111 1110
 1 011 1000
```

ANS: 1011 1000

Overflow (circle): Yes (No)

(b) Compute the following operation on two **2's complement 8-bit binary numbers**. Write your answer as a **2's complement 8-bit binary number**. Then circle "Yes" if the calculation results in overflow, otherwise circle "No." The word size is **8 bits**.

```
 0 1111 11
  0101 1011
+ 0111 1110
 1101 1001
```

ANS: 1101 1001

Overflow (circle): (Yes) No

(c) Compute the following operation that uses bitwise operators on **unsigned 8-bit hex numbers**. Write your answer as an **unsigned decimal number**.

(0x9C & 0x3D) | 0xE3

ANS: 255

1001 1200 => 0001 1100 +
0011 1101 1110 0011

1111 1111

12 8+

(d) In CMOS design, what is the **minimum** number of transistors needed to build:

(1) NAND2: 4

(2) OR3: 8

(e) Sign-extend the following **2's complement 8-bit hexadecimal numbers** to **16** bits. Write your answer as a **2's complement 16-bit hexadecimal number**. We have already written the conventional hexadecimal prefix (0x) for you.

0x5E ANS: 0x 0000 0000 0101 1110

0xC4 ANS: 0x 1111 1111 1100 0100

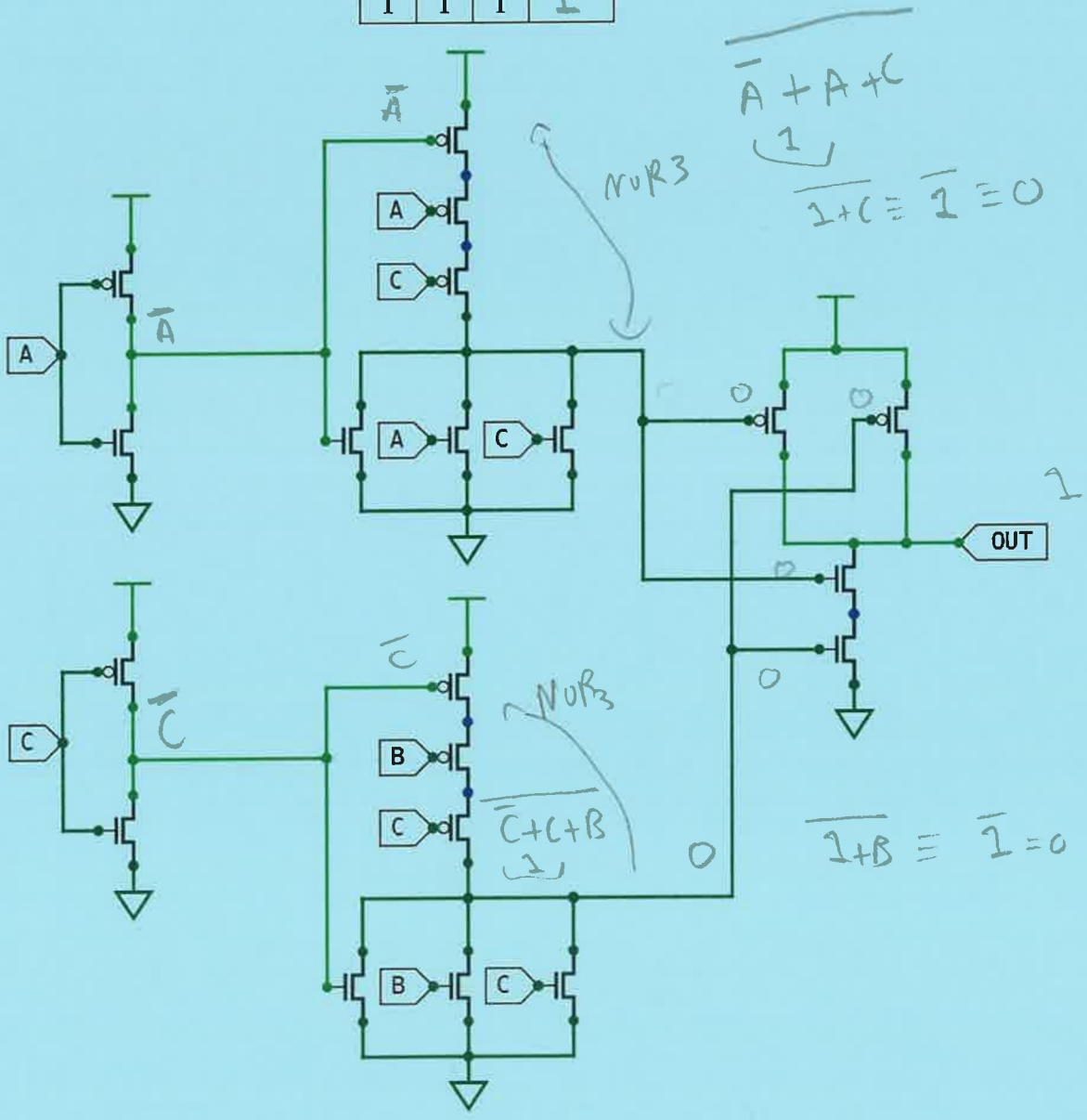
(f) Answer the following true/false questions by circling "true" or "false," and then give a reason for each answer:

TRUE or (FALSE)	A 3-to-8 decoder has 6 selector bit lines. Why or why not? It has 3 selector bit lines.
TRUE or (FALSE)	Signed magnitude defines an encoding for +0, but not -0. Why or why not? Signed magnitude has encoding 0000 for 4bit (+0), and 1000 for 4-bit (-0)
(TRUE) or FALSE	A 16-to-1 mux has 4 selector bit lines. Why or why not? 2^n where n is the selector bit lines and 2^n is the input
(TRUE) or FALSE	A and B are numbers encoded in IEEE floating point. Because of the ordering of the sign bit, encoded-exponent and fraction fields in IEEE floating point, testing "is A is greater than B?" can be done by assuming A and B are already encoded as sign-magnitude integers. Why or why not? Because the leftmost bit in IEEE indicates whether or not a number is positive or negative by 0, or 1 respectively. Then the exponent can provide which if they were the same, is bigger
TRUE or (FALSE)	I can represent 16 with two's complement and a word size of 5 bits. Why or why not? because if we were to write 10000 = -16, we need to have a bigger word size
(TRUE) or FALSE	"Turing Machine" does not refer to a physical contraption that Alan Turing built. You cannot buy it at your local electronics store. Why or why not? Turing machine allows for computations in our computer that take in input, such as adding subtracting etc.

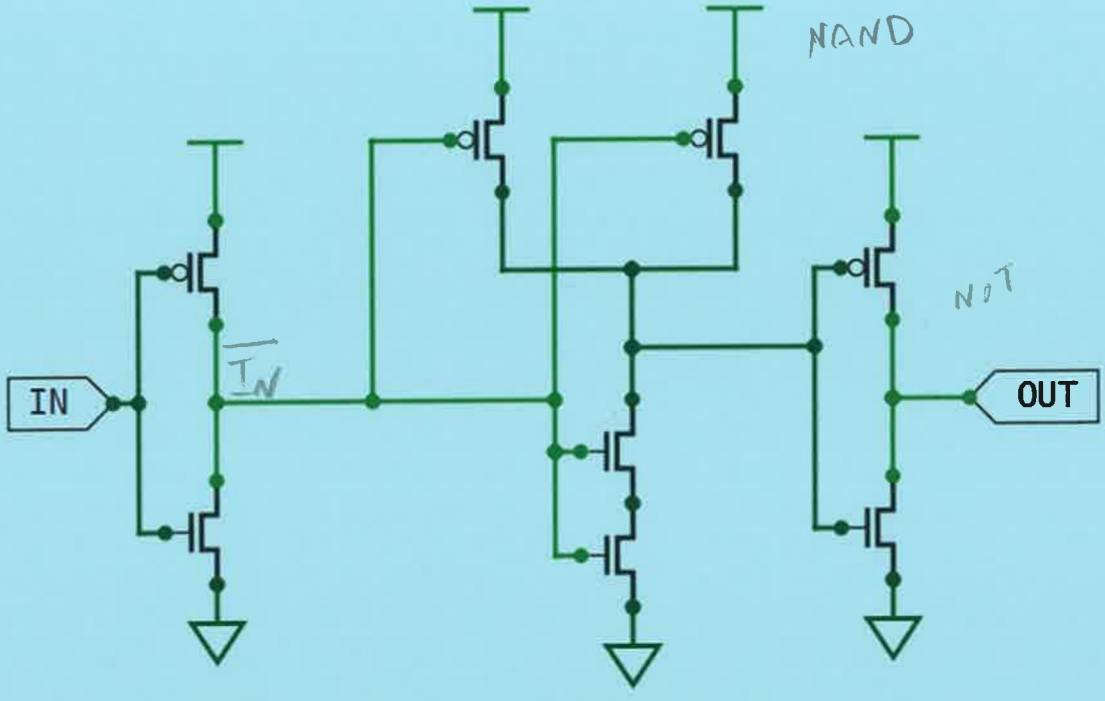
2. [25 pts] Answer the following questions about transistors. **Show your work.**

(a) Complete the truth table for the following CMOS transistor diagram:

A	B	C	OUT
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1



(b) Which logic gate does the following circuit correspond to? Your answer should be the name of a gate we covered in class (XOR, AND, OR, NOT, NAND, or NOR).

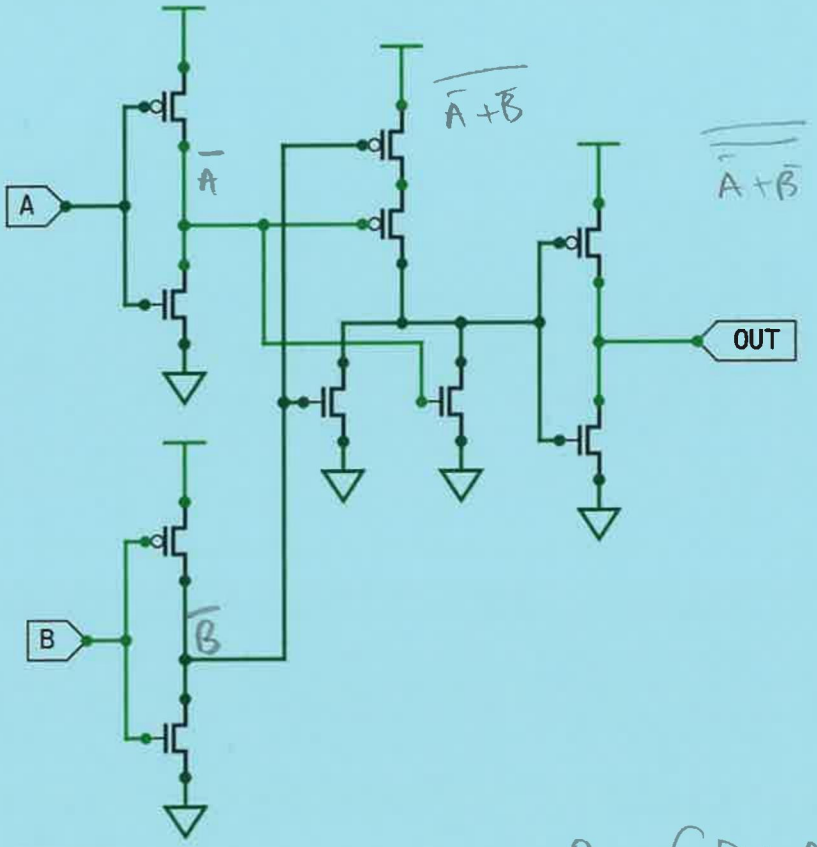


Name of the gate this circuit performs: NOR

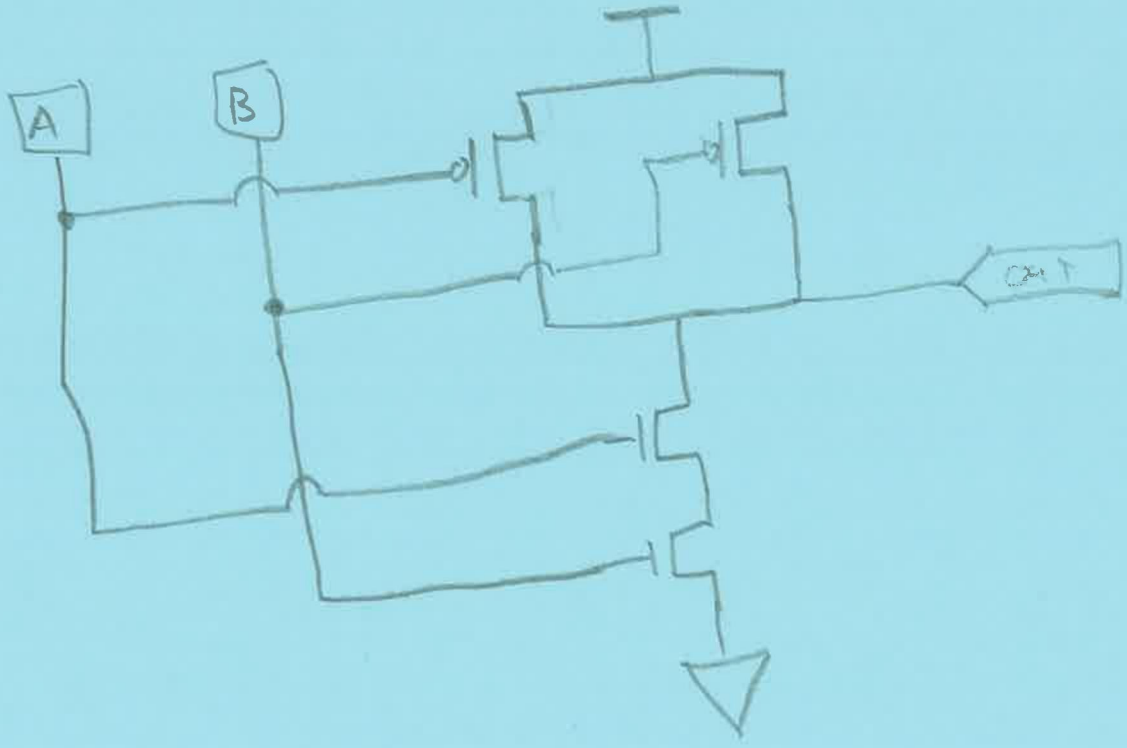
$IN \rightarrow \overline{IN} \rightarrow \overline{IN} \cdot \overline{IN} \rightarrow \overline{IN \cdot IN}$

$\overline{IN} \cdot \overline{IN} = \overline{IN + IN}$ De Morgan's

(c) Re-draw the following circuit using only 4 transistors by applying DeMorgan's Laws.



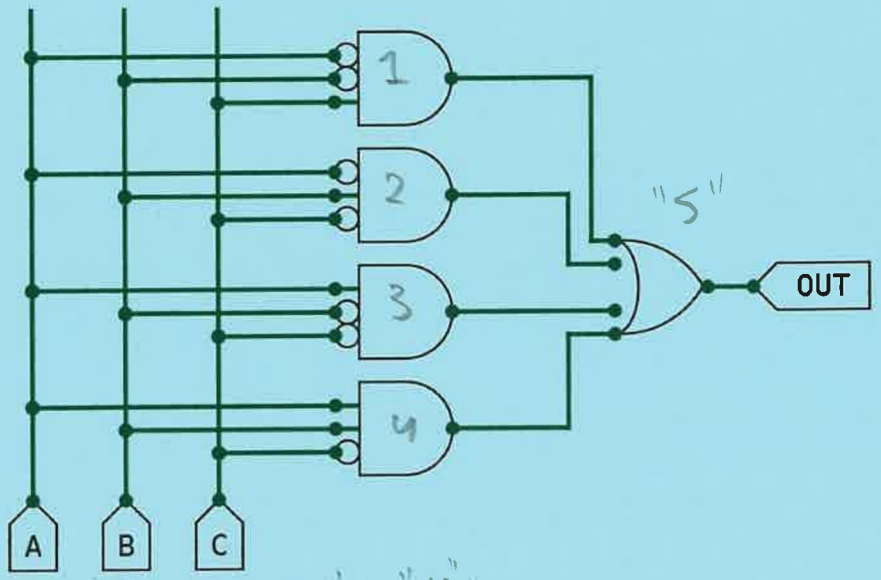
$\overline{A}+\overline{B} \equiv \overline{A \cdot B} \Rightarrow$ A NAND B (De Morgan's)



3. [25 pts] Answer the following questions about gates. **Show your work.**

(a) Complete the truth table for the logic diagram as shown.

A	B	C	OUT
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0



Situations in which output = "1"; otherwise "0":

1: A=0, B=0, C=1, because of the not bubble on A and B.

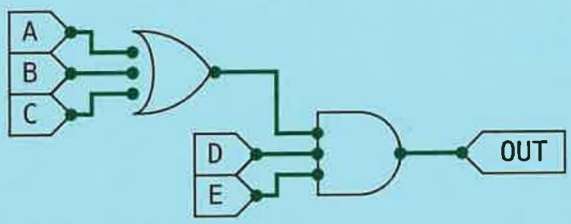
2: A=0, B=1, C=0, because of the not bubble on A and C

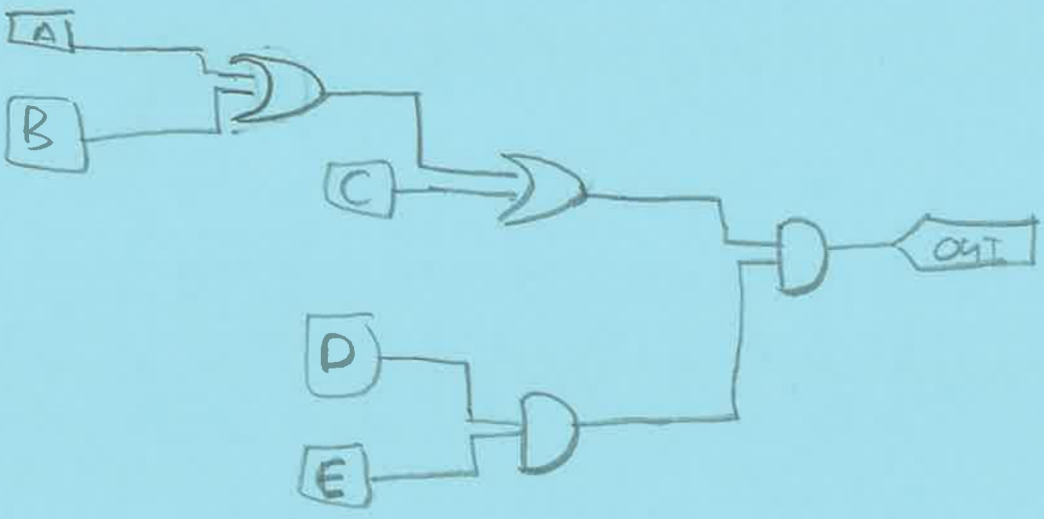
3: A=1, B=0, C=0, because of the not bubble on B and C

4: A=1, B=1, C=0, because of the not bubble on C that flips the zero to one.

Seeing there's an OR gate (number 5) for all the 4 AND gates it is sufficient for one of them to output a "1" for the final OUT to be 1.

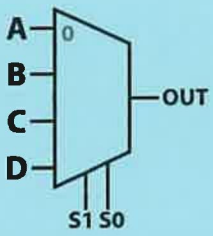
(b) Re-draw the following circuit using **only** AND and OR gates with two inputs (AND2 and OR2 gates). Do ***not*** attempt to minimize the logic or simplify it.





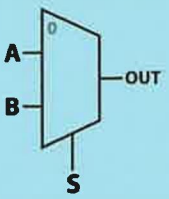
(c) Consider a 4-to-1 mux with 4 input signals for A, B, C, and D, and 2 selector signals S0 and S1. The symbol and a table that describes the behavior of a 4-to-1 mux follow:

S1	S0	Output
0	0	A
0	1	B
1	0	C
1	1	D



However, you only have 2-to-1 muxes and wires that you can use to build this 4-to-1 mux. The symbol and a table that describes the behavior of a 2-to-1 mux follow:

S	Output
0	A
1	B



Construct a 4-to-1 mux using only 2-to-1 muxes and wires: