Caravel SOC Introduction
- Reset and management protect

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Reference code
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- main repo in tag=mpw-8c
  - https://github.com/efabless/caravel_user_project/tree/mpw-8c
- sub-module in tag=mpw-8c
  - https://github.com/efabless/caravel-lite/tree/mpw-8c
  - https://github.com/efabless/caravel_mgmt_soc_litex/tree/mpw-8c
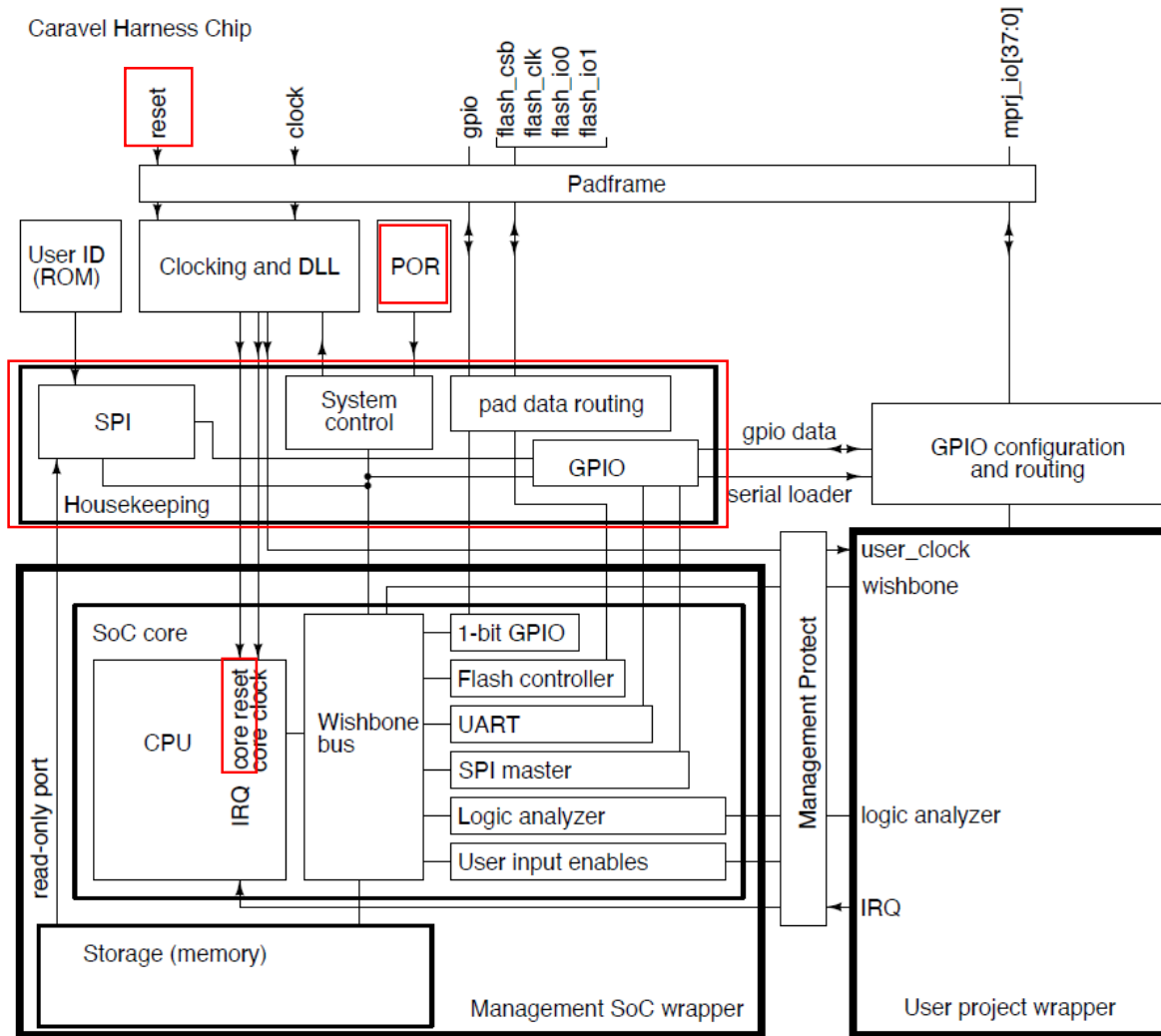- Lab
  - https://github.com/bol-edu/caravel-lab

```
Setup caravel_user_project
$ git clone -b mpw-8c https://github.com/efabless/caravel_user_project ~/caravel_user_project
$ cd ~/caravel_user_project
$ mkdir dependencies
$ export OPENLANE_ROOT=$(pwd)/dependencies/openlane_src
$ export PDK_ROOT=$(pwd)/dependencies/pdks
$ export PDK=sky130A
$ make setup
```

Reset

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- source
  - por(simple_por module)
  - reset pin (resetb)
  - ext_reset (reset_reg or pass_thru_mgmt_reset) from housekeeping
- Signal
  - Por
    - porb_h
    - porb_l
    - por_l -> por_l_buf
  - resetb
    - come from reset pin
    - resetb -> [padframe]-> rstb_h in caravel.v
      - resetb -> [resetb_pad]-> resetb_core_h in chip_io.v
    - rstb_h -> [rstb_level] -> rstb_l in caravel.v
    - rstb_l -> [soc] -> rstb_l_buf in caravel.v
    - rstb_l_buf -> [clock_ctrl] in caravel.v
  - caravel_rstn (generated by caravel_clocking module)
    - come from prob or resetb or ext_reset
      - resetb ->> rstb_l_buf -> [clock_ctrl] -> caravel_rstn

- Code trace reference
  - **Trace code for caravel_user_project mpw-8c**

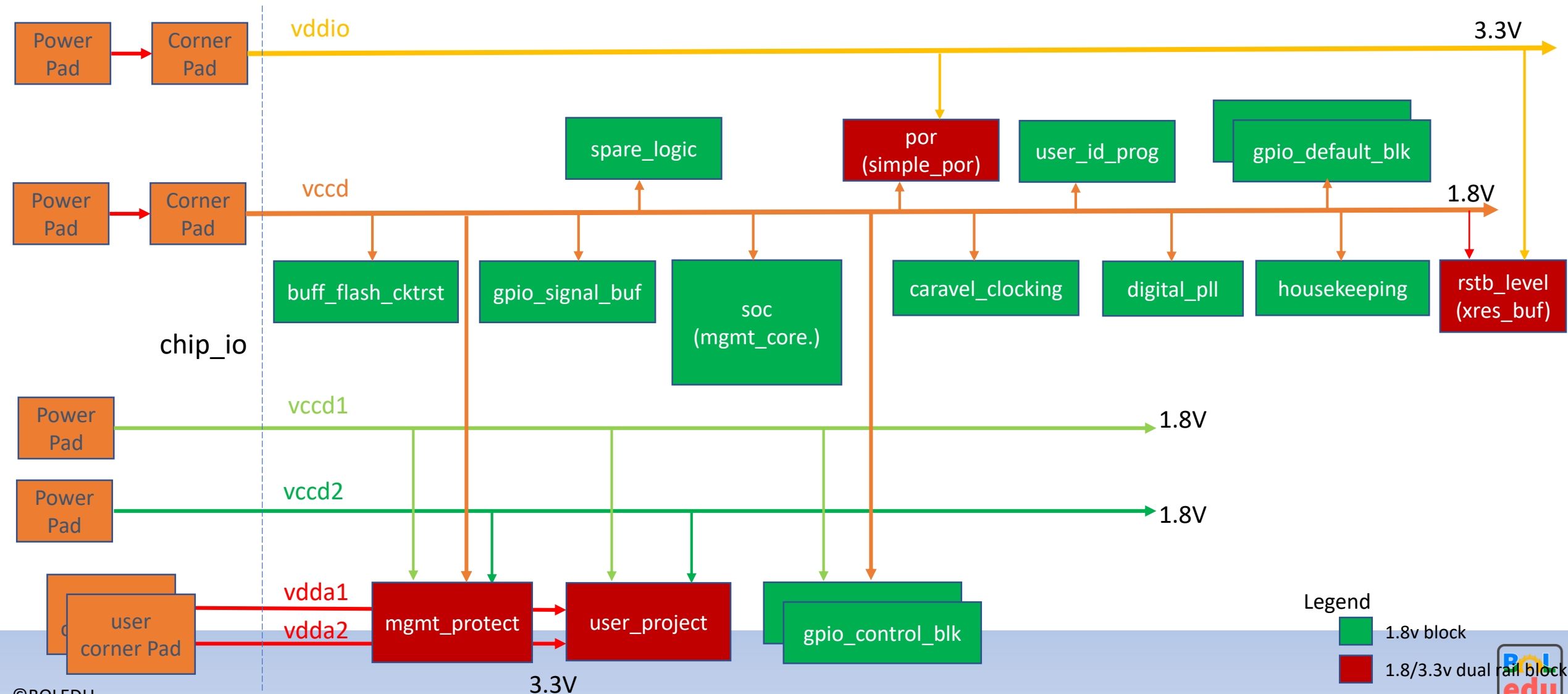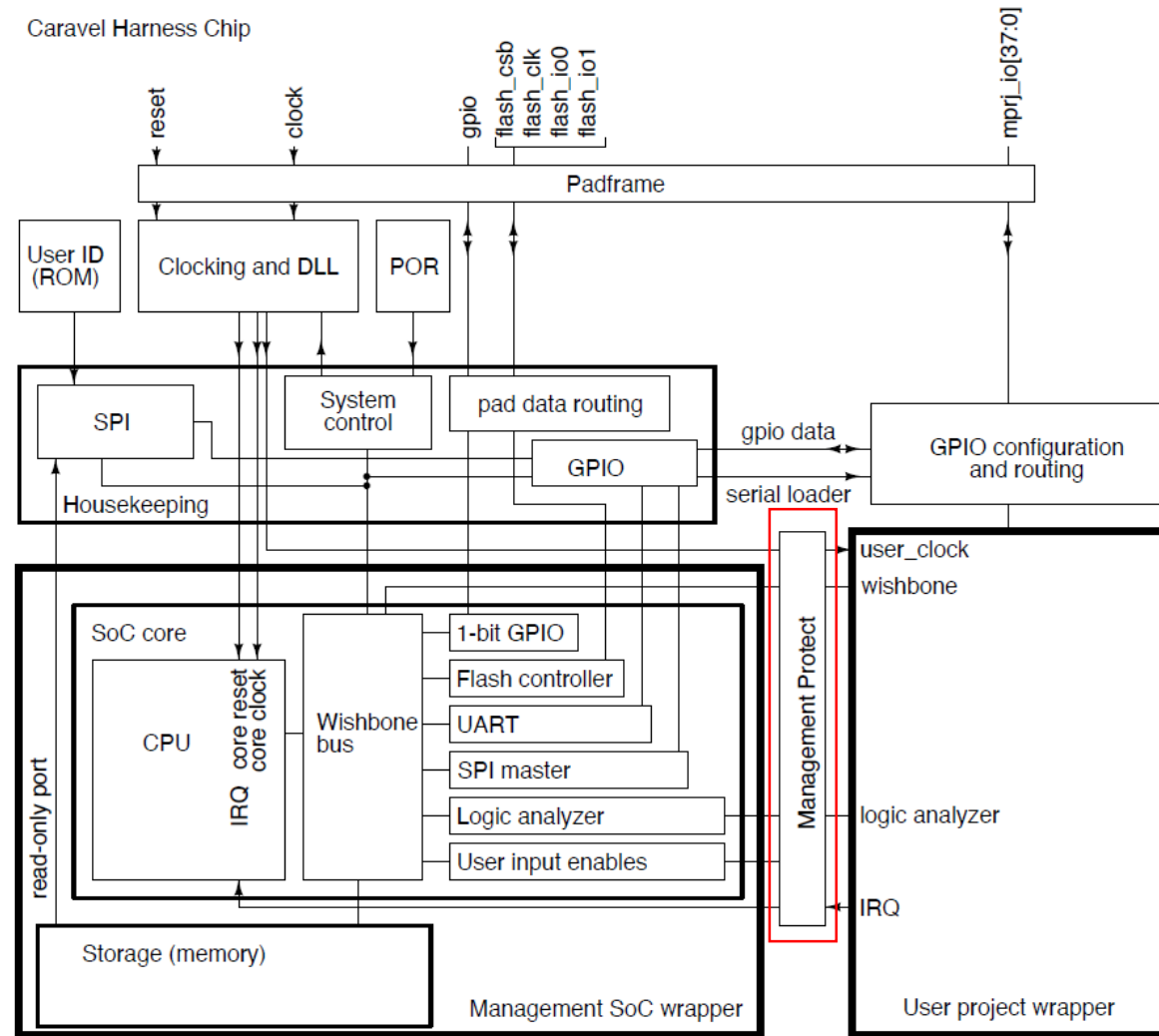# System Block Diagram – for reset part

- por(simple_por)
- reset pin (resetb)
- ext_reset (reset_reg or pass_thru_mgmt_reset) from housekeeping

- caravel_rstn -> core reset -> wb_rst

SOC PDN (Power Distributed Network)

Ref: https://github.com/bol-edu/caravel-soc/discussions/38

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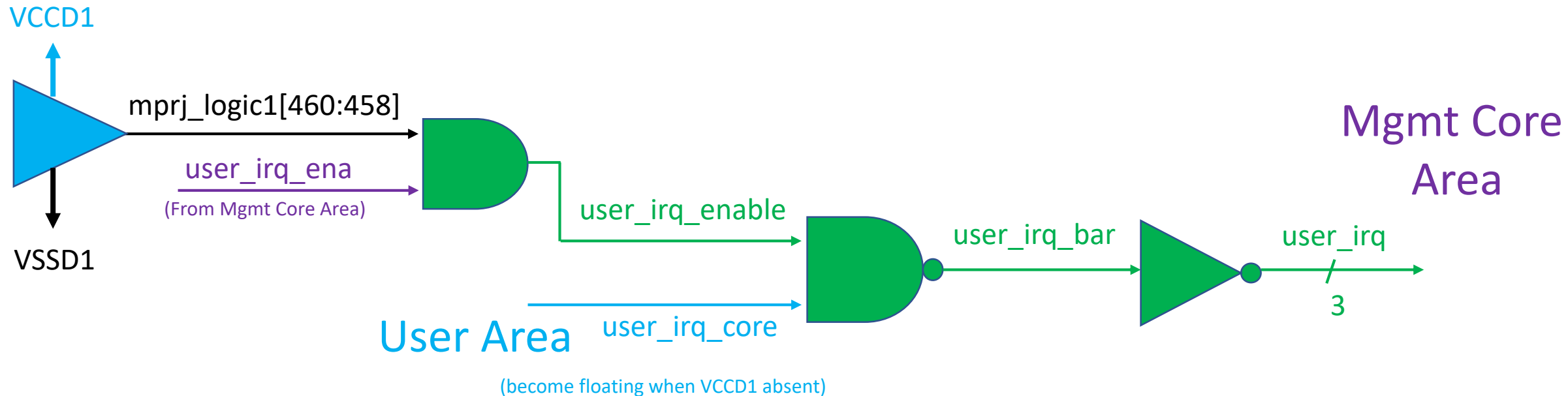# System Block Diagram – for management protect

Isolation (module mgmt_protect)

- Protect floating input from user area to management core

3X instances

End