Jing-Hua (Joseph) Chang

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Education

University of California, San Diego (UCSD) *Sep.2025 - Jan.2027 (Anticipated)*

M.S. in Electrical and Computer Engineering | Track: Computer Engineering

- **Relevant coursework:** Principles in Computer Architecture, Low-power VLSI Implementation for Machine Learning, Modern Communication Networks

National Taiwan University (NTU) *Sep.2020 - Jun.2024*

B.S. in Engineering Science and Ocean Engineering | Track: Optoelectronics and Information Engineering

- Ranked **2nd place** among 58 students in the 2023 academic year
- **Relevant coursework:** SoC Design Laboratory, Computer-aided VLSI System Design, Digital Signal Processing in VLSI Design, Logic Design, Circuit and Electronics (I & II), Natural Language Processing, Data Structure

Skills

- **Coding:** Verilog, Python, C / C++, MATLAB, Java
- **Domain Knowledge:** ASIC, FPGA, RTL, STA, SYN, APR, CDC/RDC, SoC, Digital Systems, Computer Architecture, Automation, VLSI Design, CMOS Digital Circuits, Acclerator, LLM, ML, SerDes.
- **Tools:** Synopsys Design Compiler / Spyglass / Prime Time / Verdi, Cadence Virtuoso, Xilinx Vivado, Intel Quartus, Git, Linux, Vim, Lint, PyTorch.
- **Language:** English (fluent) GRE 324/340, TOEFL 101/120 Chinese (native) Korean (beginner) TOPIK I 134/200

Internships

Marvell, Digital Design Engineer - SerDes Team, Hsinchu *Jun.2025 - Aug.2025*

- Designed a high-speed (DDR) descrambler for a die-to-die SerDes test chip using Verilog, contributing to networking PHY functionality.
- Conduct Clock/Reset-Domain Crossing (CDC/RDC) analysis, ensuring robust multi-clock data transfer for high bandwidth links.

Lumentum, Software Developer - Product Team, New Taipei *Nov.2023 - Jun.2024*

- Developed a portable software program for VCSELs die crack detection that expedited the testing process by 48x, and supported wafer mask generation & visualization for failure analysis. (OpenCV, Python, Docker)
- Utilized OpenCV to preprocess microscopic VCSEL .bmp images and calculate their die eye area, width, and length. (C++, Qt)

Samsung Electronics, Field Application Engineer - SSD Memory Team, Taipei *July.2023 - Nov.2023*

- Performed SSD testing on the servers (performance, stress, power cycle, chamber temperature test) and composed testing scripts
- Designed an automation program streamlining the SSD FIO golden test on joint qualification requests, saving up to 72 hours. (Python)

Research

High Efficiency Circuit and System Laboratory *Jul.2022 - Feb.2024*

Undergraduate Research: MOS Current-Mode Logic Applied to VLSI Digital Design *Advisor: Professor Jau-Horng, Chen*

- Designed MCML XORs schematics/layout that reduces 37% area & 33% power consumption of a sigma-delta modulation DAC.
- Deviced new structure for high-speed D flip-flop (fine-tuned & realized with UMC 0.18 um CMOS 1.8V process) using Cadence Virtuoso
- Integrated the PEX netlist into the algorithm which converts an ASIC design from a single-ended to a differential source-coupled circuit

Robot Learning Lab *Feb.2024 - July.2024*

Undergraduate Research: Reinforcement Learning & Machine Learning *Advisor: Professor Shao-Hua, Sun*

Capstone Topics of Engineering Science and Ocean Engineering *Instructor: Professor Chao-Nan, Wang*

- Designed a class-D audio signal amplifier, configured Pulse-Width Modulation, ADC, and GPIO protocol on STM32 microcontroller.