Jing-Hua (Joseph) Chang

Taipei, Taiwan

☐ (+886) 912-873-887   ✉ dong.joseph7@gmail.com   in LinkedIn   ⓞ GitHub   </> LeetCode

EDUCATION

National Taiwan University (NTU)   *Sep.2020 - Present*

B.S. in Engineering Science and Ocean Engineering (track: Optoelectronics and Informaion Engineering) 🎓
- *Overall GPA: 3.5/4.0*

M.S. in Engineering Science and Ocean Engineering (track: Informaion Engineering) - Admitted

RESEARCH EXPERIENCE

High Efficiency Circuit and System Laboratory   *Jul.2022 - Feb.2024*
Advisor: Professor Jau-Horng, Chen

- Constructing MCML cell library (Analog schematic & layout design) for VLSI digital design flow, EDA optimization

- High-speed DFF research & implementation

Robot Learning Lab   *Feb.2024 - Present*
Advisor: Professor Shao-Hua, Sun

- Reinforcement Learning paper research 📕

INTERNSHIPS

Lumentum   *Nov.2023 - June.2024*
Software Developer - Product Team

- Develop a portable software program for VCSEL die crack detection, decode & decrypt XY-coordinates, wafer mask generation & visualization. (OpenCV, Python, Docker) 📄

- Use OpenCV to preprocess microscopic VCSEL .bmp images and calculate its die eye area, width, and length. (C++) ⓞ

- Experienced in VCSEL wafer testing using VNA probing and laser beam profiler to collect S-parameter & Smith chart.

Samsung Electronics   *July.2023 - Nov.2023*
Field Application Engineer - SSD Memory Team

- SSD FIO Testing Automation on Linux-Based Multi-Server (Python & Bash) 📄 ✅

- Perform solid state drive testing on server (performance, OS installation, stress, power cycle, chamber temperature test)

- Participate in Korean classes.

COMPETITIONS

Programming Design and Optimization - Hackathon   *May.2024*
Group leader

- C++ coding competition. Ranking 7th place. ✅

Genius for home - MediaTek   *May.2023*
Group leader

- Propose net-zero food carbon footprint App. 📄 ✅

COURSEWORK

SoC Design Laboratory
- Caravel SoC architecture workload optimization (RTL, firmware, software, HLS) ⓞ
- Hardware accelerator, UART, SDRAM banking, AXI bus, Wishbone.

Logic Design
- Labs: FPGA

Digital Signal Processing in VLSI Design

Circuit and Electronics (I & II)
- Project: OP-AMP Schematics Structure Design
- Labs: Circuit Analysis, Filters, OP-AMP, Rectifier

Capstone topics of Engineering Science and Ocean Engineering
- Design an FIR filter using a C language-based embedded program on ARM® Cortex™-M4 MCUs. 📄
- Design a class-D Audio signal amplifier & ADC and configure via Pulse-Wide Modulation & GPIO protocol on STM32 microcontroller.
- Make a high-quality vented box speaker out of daily necessities. (elected as the best speaker of the class) ▶

Natural Language Processing
- Fine-tune & prompt tune llama2 & 3 for argument classification

Naval Architecture
- Designed a boat hull prototype that meets the specification of hydrostatic stability & coefficients using Rhino. 📄
- Import Rhino in a Python script to compute the center of buoyancy and draw the cross-curve stability. 📄

Electroacoustics
- Design a vented box loudspeaker using AutoCAD & 3D printer. 📄
- Frequency response testing of the loudspeaker in an anechoic/reverberation chamber of the acoustic laboratory. 📄

Electromagnetics, Computer Organization, Signal and Systems

LANGUAGE

English
- TOEIC 920 📄

EXTRACURRICULAR EXPERIENCE

Varsity Men's Soccer Team *Jun.2021 - Jun.2022*
Striker
- Champion of Taiwan University Football Association challenge 1st division (UFA). 🏆 ⊚ ⊚

ESOE Soccer Team *Sep.2020 - July.2022*
Founder & Captain
- NTU Cup champion (2021), NTU League 2nd place (2022), freshmen cup 3rd place (2020). ⊚

ESOE Student Association *July.2021, Jun.2023*
Academic affairs officer & IT officer
- Organize study materials using the Box platform and share solutions on a personal blog.

Fingerstyle Guitar Club *Feb.2021 - Jun.2022*
Guitarist & Design officer
- Fingerstyle guitar solo, sing guitar. ▶ ▶ 🖼 ✅

Kind Kids Friends Group *Sep.2022, Apr.2023*
Volunteer
- Participate in the volunteer work at Ruibei Elementary School in Hualien county