EC580-HOMEWORK 2

Due Date: October 10, 2025, 11:59pm ET

Describe your reasoning for your design and calculations. Provide the simulation setups you used for this problem set and provide the necessary simulation results (operating point, plots, etc.) to document your findings. Make sure you provide sufficient information, but not too much information either. The grade will depend on both the quality of the results and the quality of the succinct but insightful description of your reasoning and calculations.

Problem 1

For this problem, choose a 120nm/50nm device. Plot one of each of the following plots for the nMOS and pMOS devices.

- I_{DS} vs. V_{GS} for a $V_{DS} = 0.8V$.
- $log(I_{DS})$ vs. V_{GS} for a $V_{DS} = 0.8V$.
- I_{DS} vs. V_{DS}, sweeping V_{GS} from 0 to V_{DD} in steps of 0.1 V.
- $log(I_{DS})$ vs. V_{DS}, sweeping V_{GS} from 0 to V_{DD} in steps of 0.1 V.

Problem 2

Estimate the following parameters for a 120nm/50nm device. Do this only for the nMOS transistor.

- α, which models the inversion layer's variation across the channel. I_{DS} is proportional to $(V_{GS}-V_{th})V_{DS}-\frac{\alpha V_{DS}^2}{2}$ in triode region.
- The sub-threshold slope n in I_{DS} proportional to $e^{\frac{V_{GS}}{n\phi_t}}$.
- γ, the body effect coefficient.
- The Early voltage, V_A.
- Specific current for teaching model. This is the current where the two asymptotes in a log-log plot of g_m/I_{DS} vs. I_{DS} meet, scaled by the size of the device.
- Plot f_T (transition frequency) vs. V_{DS}.