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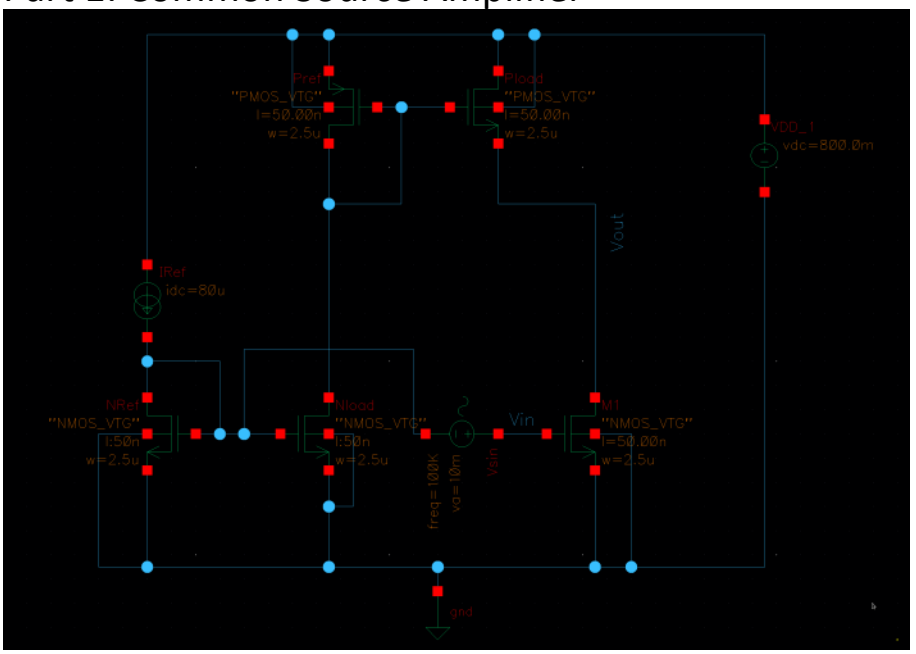
Assignment 3
EC580 Fall 2025

Part 1: Common Source Amplifier



For this circuit I biased the common-source (CS) amplifier by designing an NMOS current mirror which would copy the current from the reference current source. This is then fed to a PMOS current mirror connected to M1. All devices are sized to 2.5um.

The DC voltage bias to the amplifier is achieved by connecting the NMOS current mirror directly to Vin and subsequently the gate of M1.

Figure 1. Common Source Amplifier Schematic

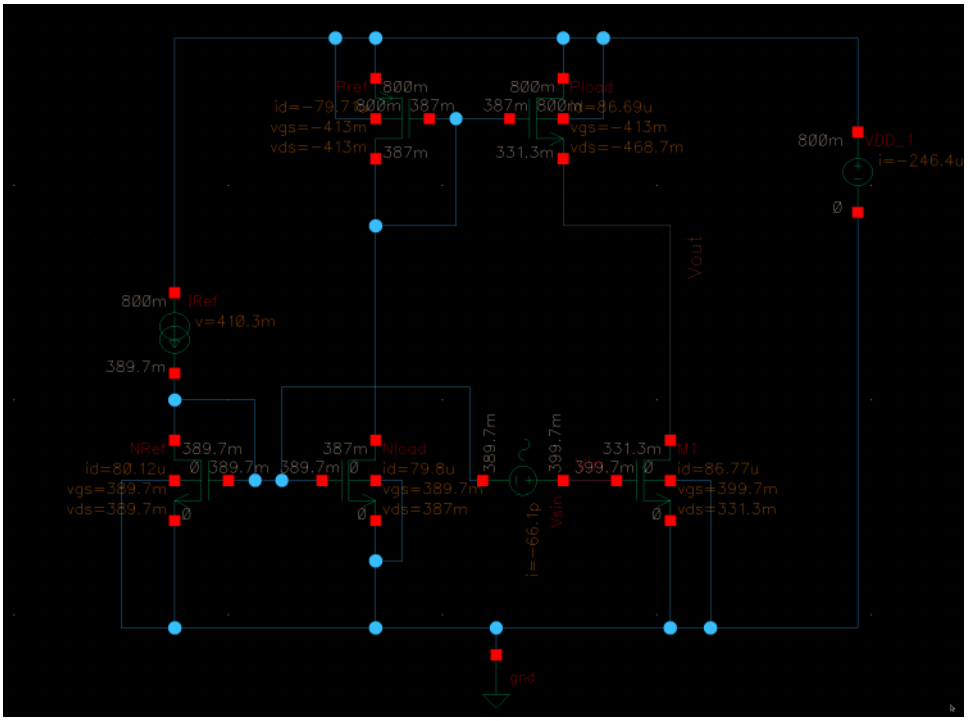


Figure 2. Common Source Amplifier Bias Points

The gain and thew swing of the amplifier are shown in the figures and table below. Across all PCT corners the gain consistently maintains at 5.2-5.5 (14.4-15dB).

PVT	Temperature/C	dB Gain	Linear Gain
TT	27	14.9	5.56036
SS	85	15.46	5.5.93008
FF	20	14.433	5.26822

Table 1. Gain of the CS Amplifier across PVT Corners

The voltage swing range is defined by: Vgs, M1 - Vth, M1 < Vout < VDD - (Vsg - |Vth, Pload|).

Based on the operating point analysis, Vgs, M1 - Vth, M1 = 14.07mV, VDD - (Vsg - |Vth, Pload|) = 728.184mV. While the theoretical VPP is 357.06mV, our biasing has limited our achieved VPP to 342.8187mV

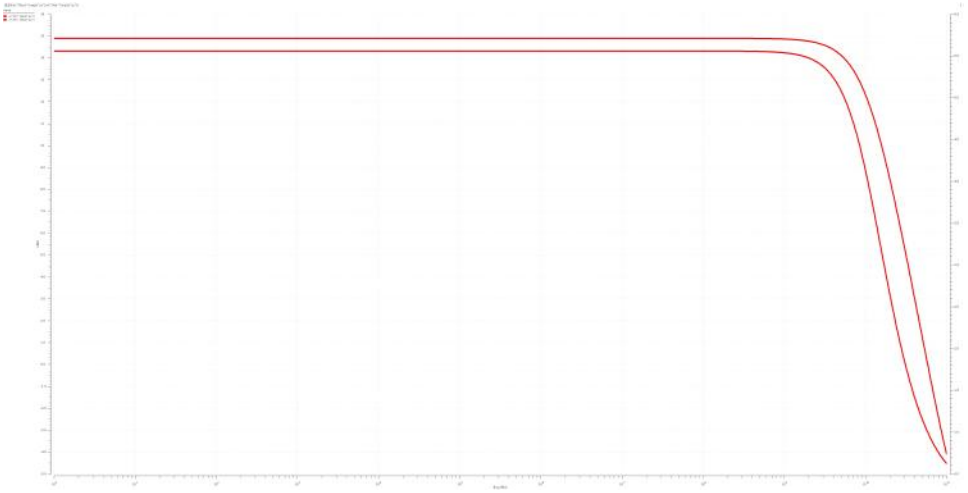


Figure 3. Gain of the CS Amplifier at the Nominal (TT) PVT Corner

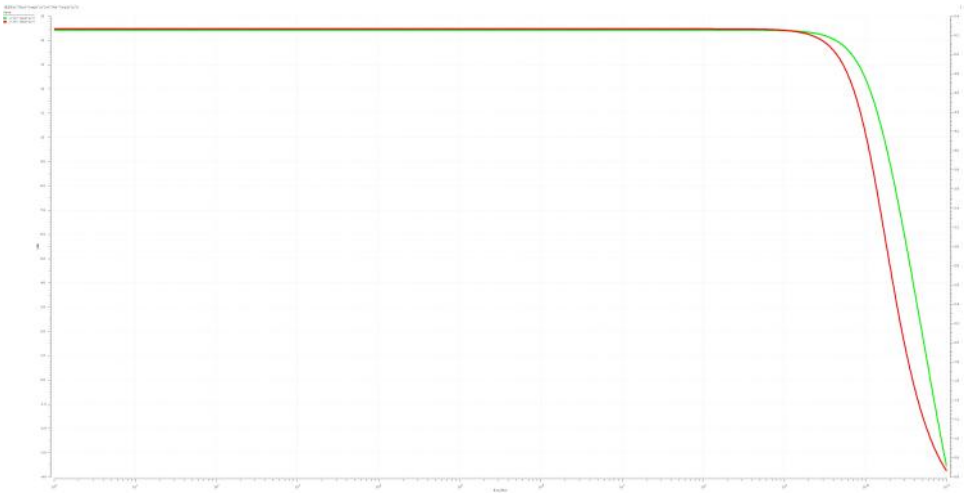


Figure 4. Gain of the CS Amplifier at the Fast-Fast (FF) PVT Corner

Figure 5. Gain of the CS Amplifier at the Slow-Slow (SS) PVT Corner

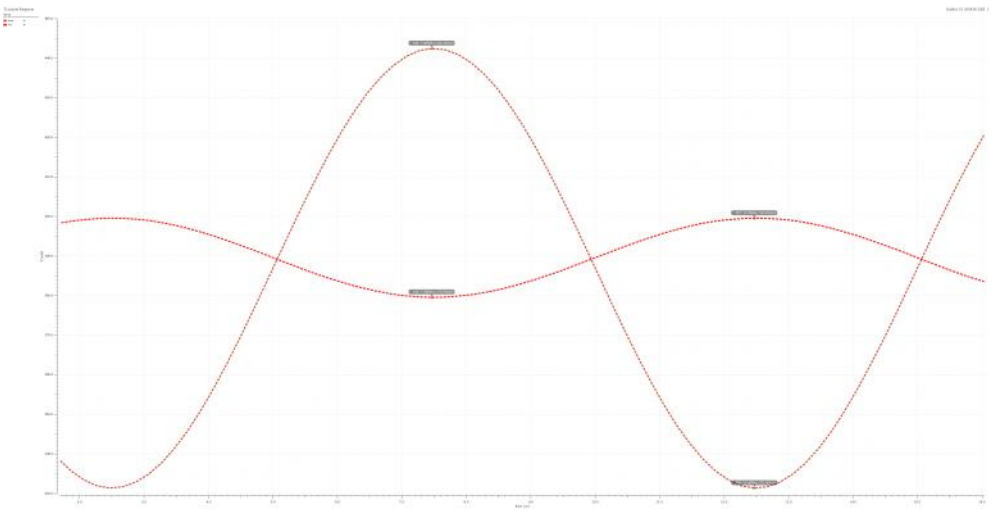


Figure 6. Voltage swing of the CS Amplifier at the Nominal PVT Corner

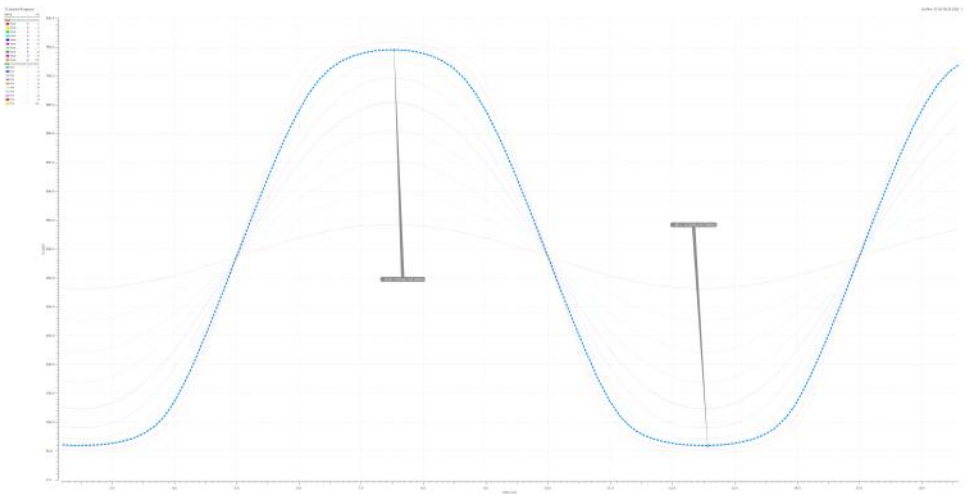


Figure 7. Maximum Swing of the CS Amplifier via Parametric Sweep

Part 2: Common Source Amplifier

For this circuit I biased the common-drain (CD) amplifier by designing an NMOS current mirror with a diode-connected transistor as the for biasing. For source follower amplifier the gain can at most be. The NMOS current mirror generates a stable current load to the diode load making Vgs stable across the different PVT corners.

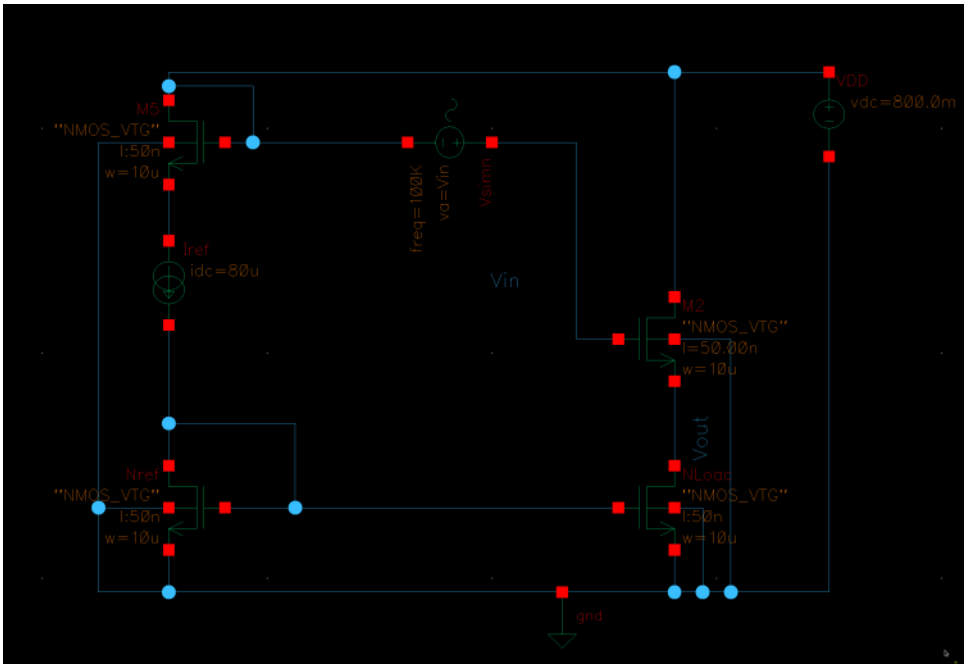


Figure 8. Common Drain Amplifier Schematic

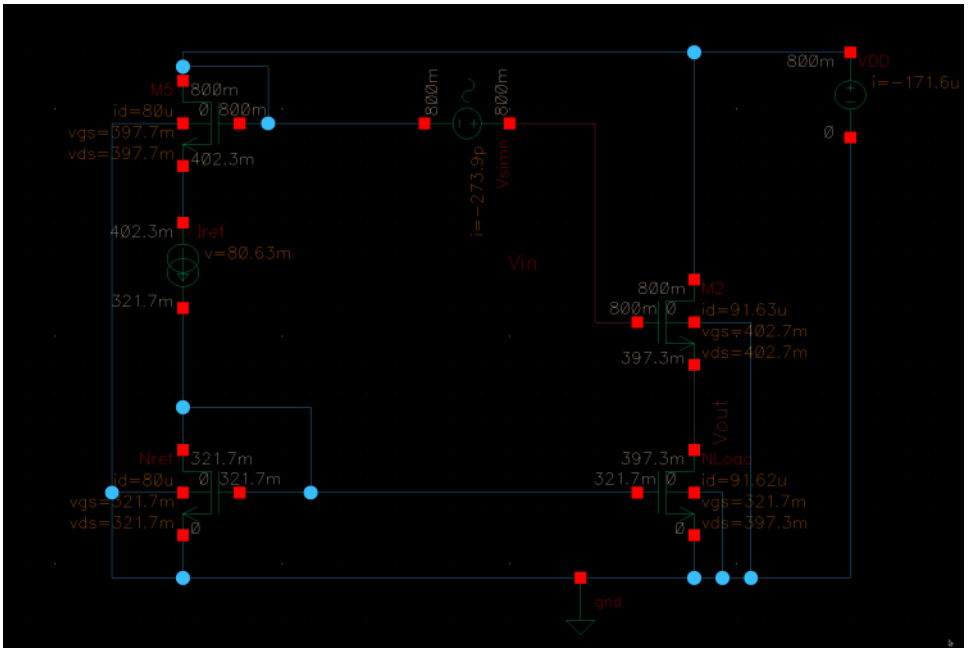


Figure 9. Common Drain Amplifier Bias Points

The gain and thew swing of the amplifier are shown in the figures and table below. Across all PCT corners the gain consistently maintains at 0.73 to 0.74.

Case	Temperature/C	dB Gain	Linear Gain
TT	27	-2.6671	0.735
SS	85	-2.59025	0.742143
FF	20	-2.71753	0.731347

Table 2. Gain of the CD Amplifier across PVT Corners

The voltage swing range is defined by: (Vgs, M3) - Vth, M2 < Vout < VDD - (Vgs, Nload - Vth, Nload).

Based on the operating point analysis, Vgs,m1 - Vth,m1 = 58.362mV, VDD - (Vgs, Nload - Vth, Nload) = 736.266mV. While the theoretical VPP is 368.133mV, our biasing has achieved VPP to 368.6588mV, over our theoretical estimations.

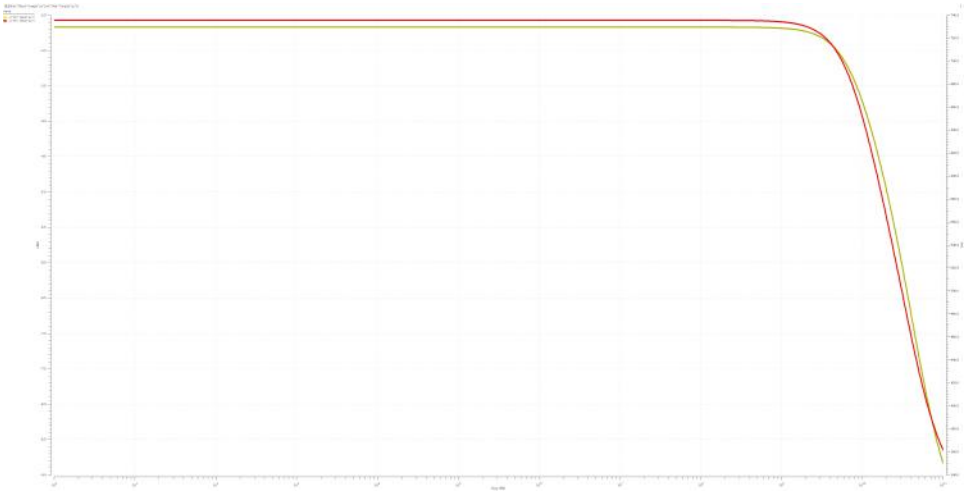


Figure 10. Gain of the CD Amplifier at the Nominal (TT) PVT Corner

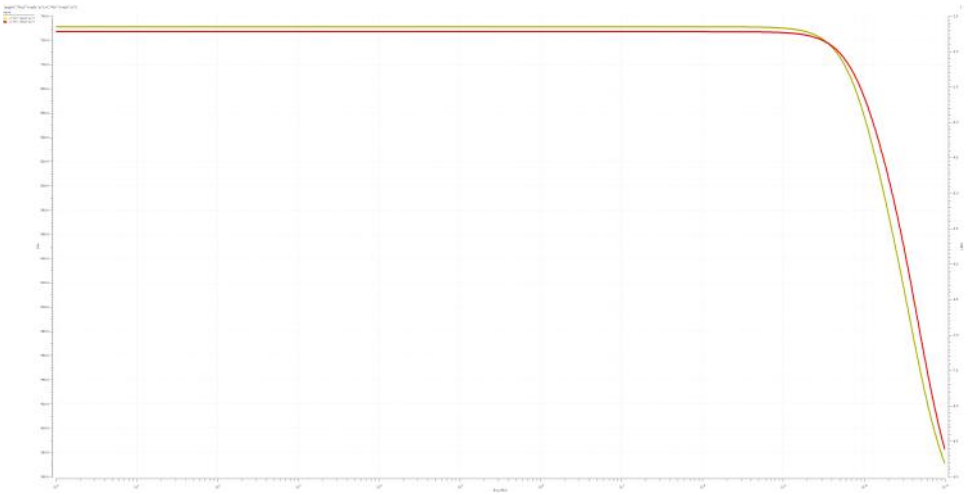


Figure 11. Gain of the CD Amplifier at the Fast-Fast (FF) PVT Corner

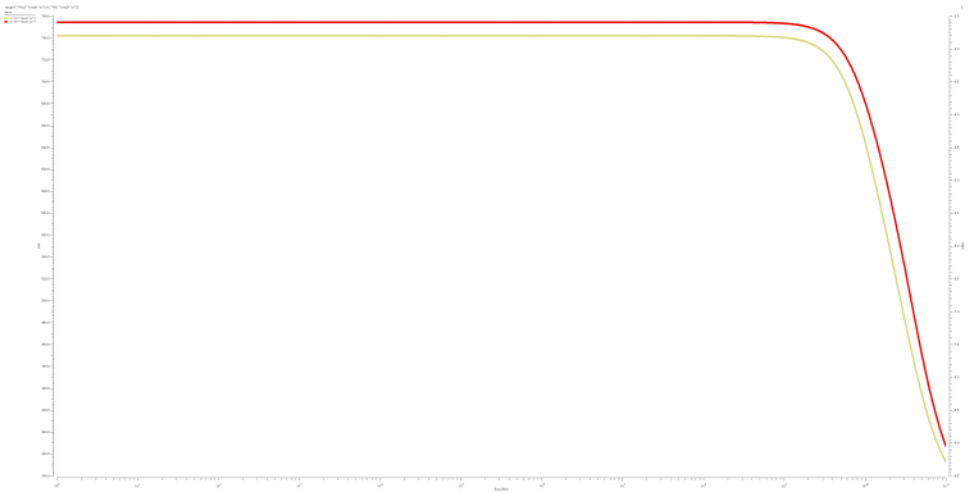


Figure 12. Gain of the CD Amplifier at the Slow-Slow (SS) PVT Corner

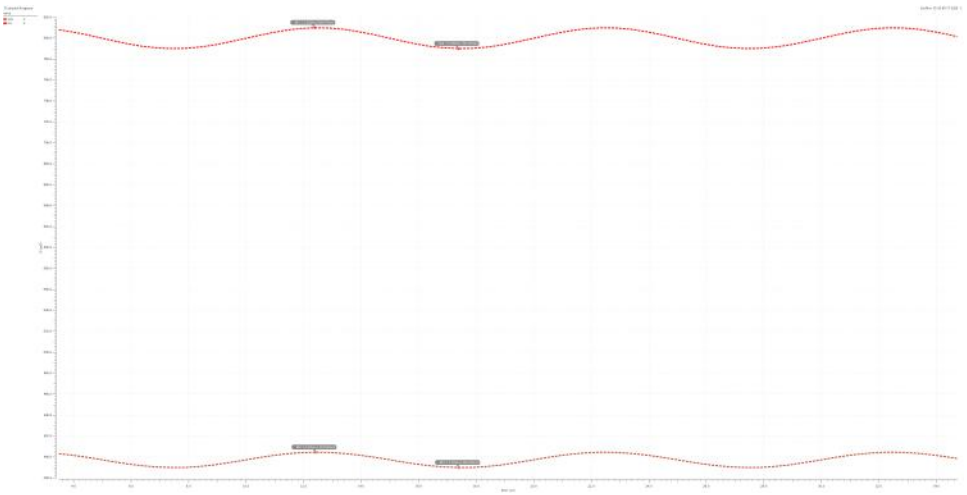


Figure 13. Voltage swing of the CD Amplifier at the Nominal PVT Corner

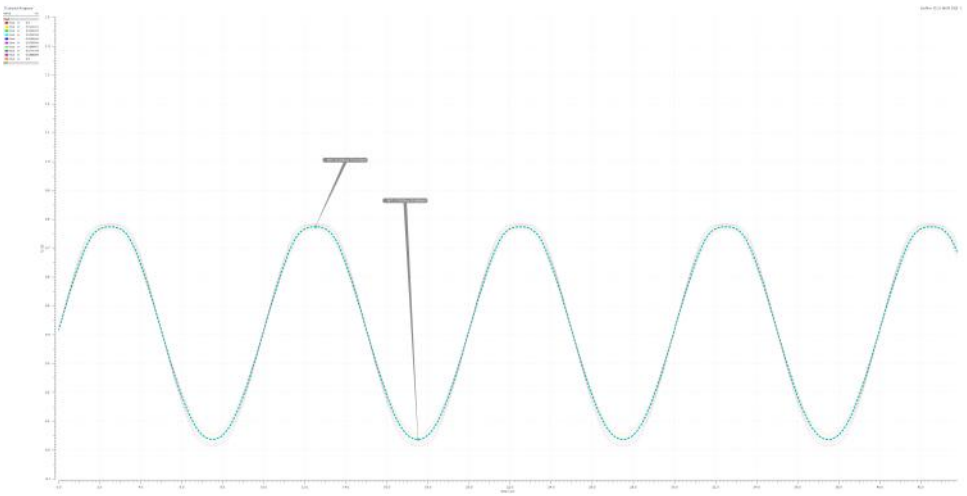


Figure 14. Maximum Swing of the CD Amplifier via Parametric Sweep

Part 3: Common Source Amplifier with Cascode

For this circuit I biased the common-source cascoded amplifier (CS-CAS) by designing an NMOS current mirror connected to Iref which would subsequently lead to the current be copied by a PMOS current mirror to the amplifier. There is no need to for DC voltage biasing since the amplifier design is self-biased.

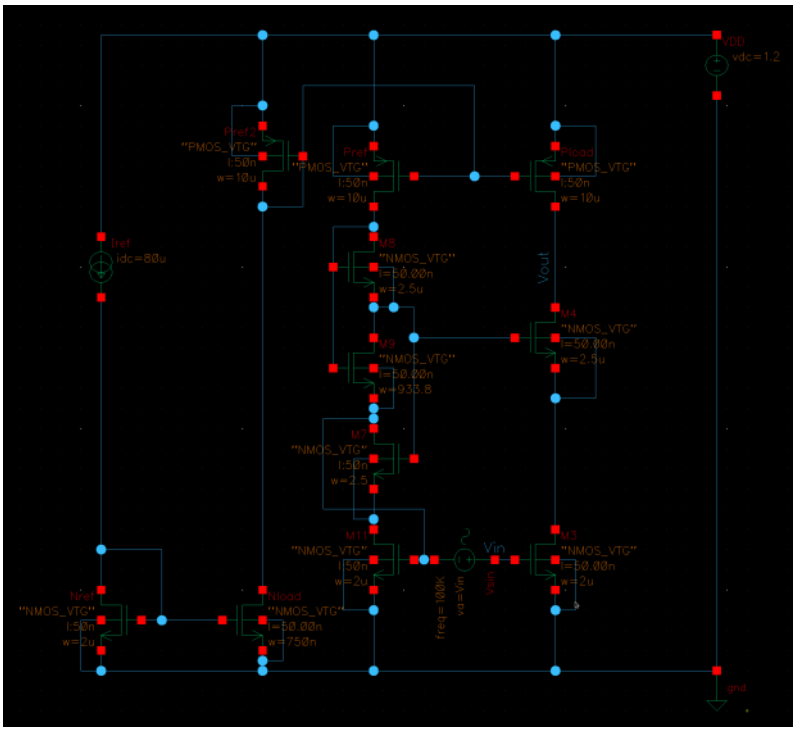


Figure 15. Cascoded CS Amplifier Schematic

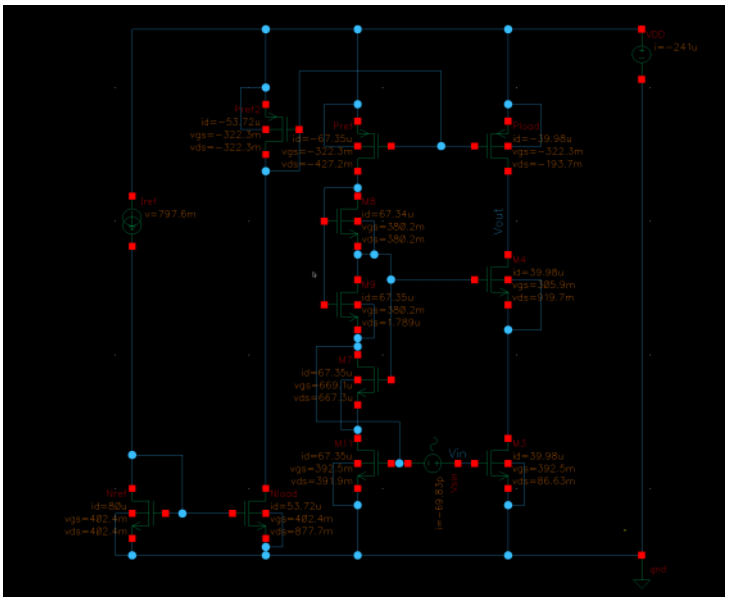


Figure 16. CS-CAS Schematic w Bias Points

The gain and thew swing of the amplifier are shown in the figures and table below. Across all PCT corners the gain consistently maintains at 5.3 to 5.7.

Case	Temperature/C	dB Gain	Linear Gain
TT	27	15.0733	5.671
SS	85	15.246	5.78505
FF	20	14.481	5.29708

Table 3. Gain of the CS-CAS Amplifier across PVT Corners

The voltage swing range is defined by: [(Vgs, M3 - Vth, M3) + (Vgs, M4 - Vth, M4)] < Vout < VDD - (Vgs, Pload - Vth, Pload).

Based on the operating point analysis, Vout, min = 27.4573mV,

The voltage swing range is defined by: [(Vgs, M3 - Vth, M3) + (Vgs, M4 - Vth, M4)] < Vout < VDD - (Vsg, Pload - |Vth, Pload|).

Based on the operating point analysis, Vout, min = 27.4573mV; Vout, max = 769.0345mV. The theoretical voltage swing by analysis is 370.7886mV, while our achieved simulated maximum voltage is 193.7015.

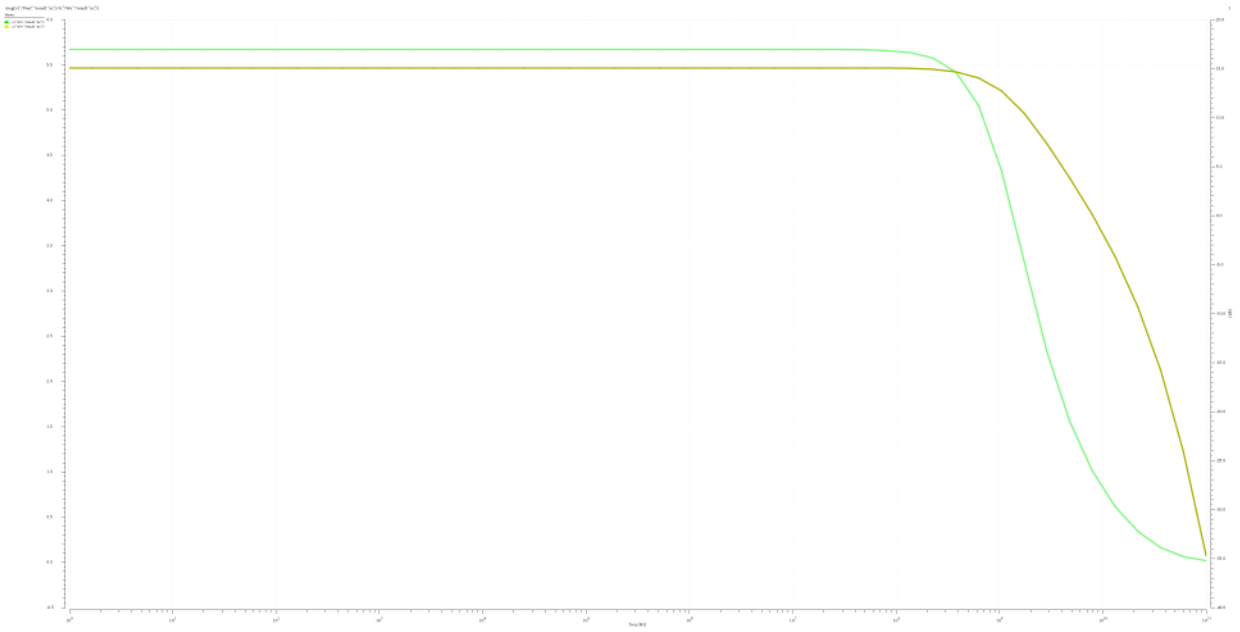


Figure 17. Gain of the CAS-CS Amplifier at the Nominal (TT) PVT Corner

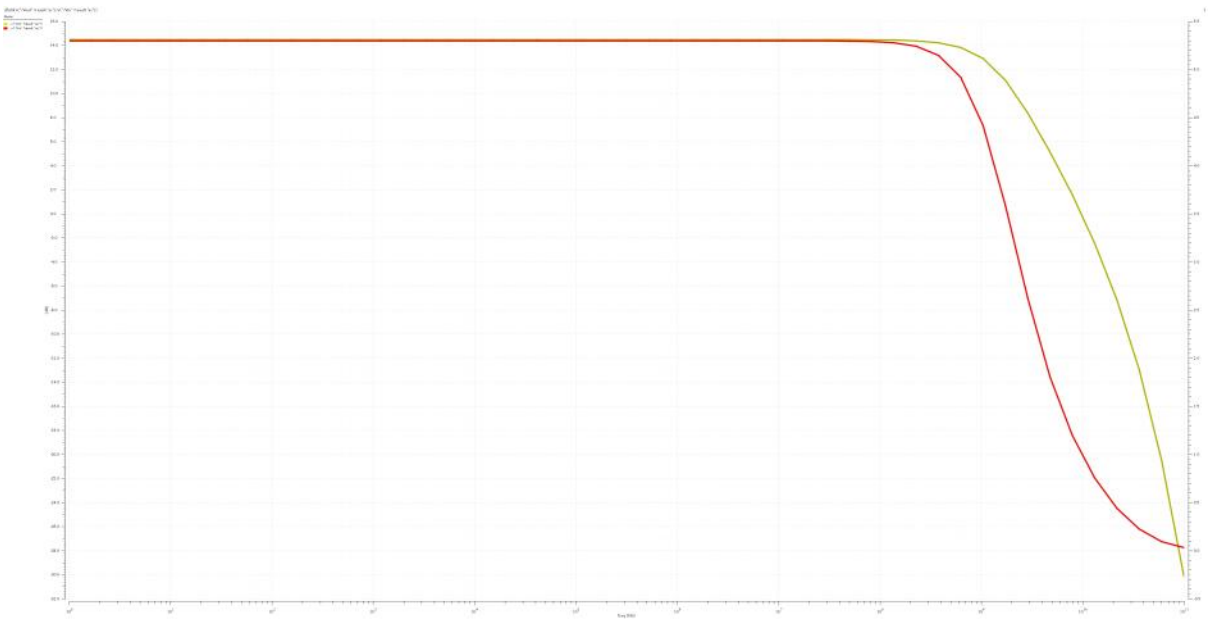


Figure 18. Gain of the CAS-CS Amplifier at the Fast-Fast (FF) PVT Corner

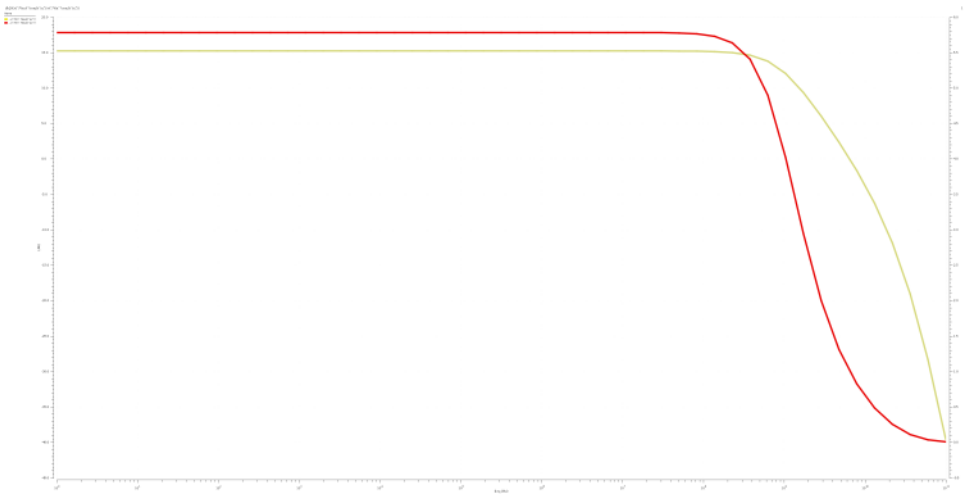


Figure 19. Gain of the CS-CAS Amplifier at the Slow-Slow (SS) PVT Corner

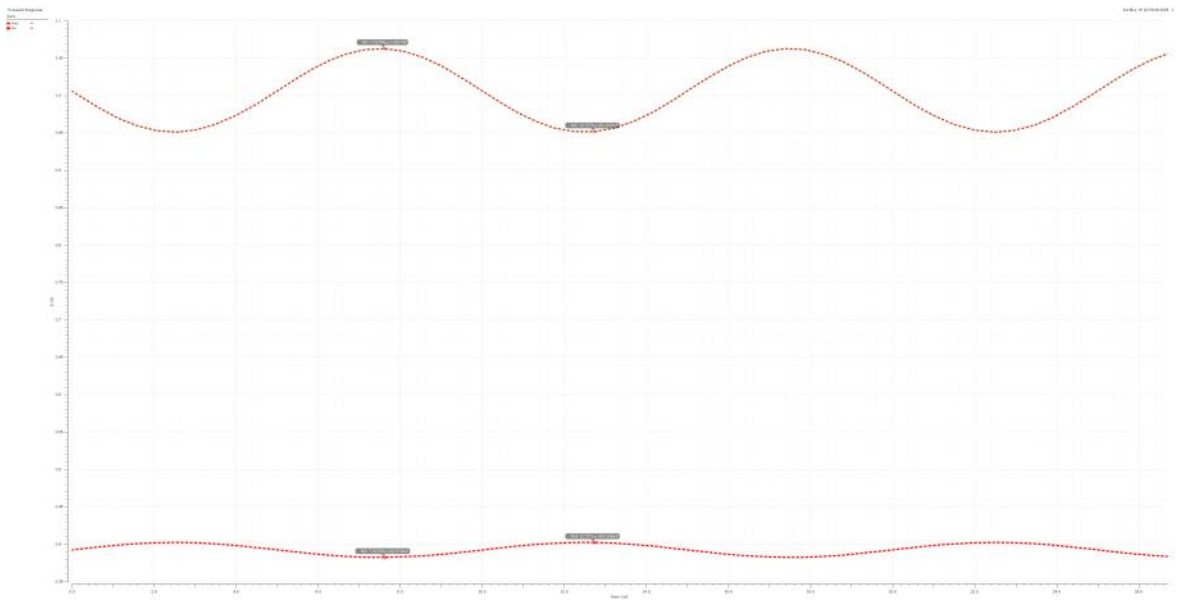


Figure 20. Voltage swing of the CS-CAS Amplifier at the Nominal PVT Corner

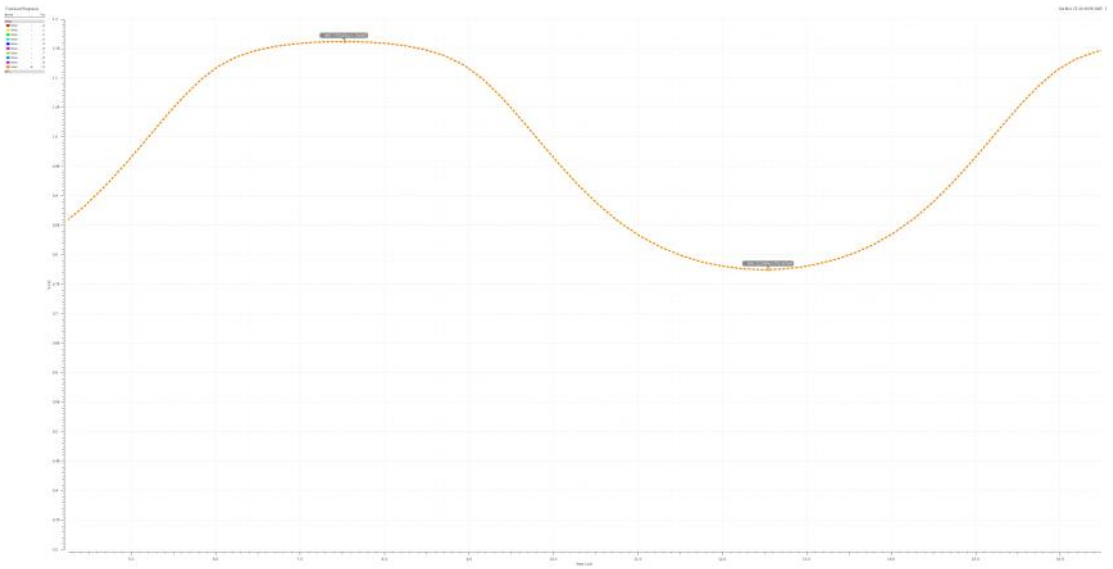


Figure 21. Maximum Swing of the CS-CAS Amplifier via Parametric Sweep