A Low Power Preamplifier Latch based Comparator Using 180nm CMOS Technology

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***Abstract*-Design of high speed low power comparators are required to build an efficient analog to digital converters (ADCs). This paper mainly focuses on the preamplifier positive feedback latch based comparator for Asynchronous Successive Approximation Register ADC (ASAR ADC). The main components of such comparator are the preamplifier and latch circuit. Preamplifier is used for removing the kickback noise and the dc offset voltage while the latch is required for the comparison. The proposed architecture operates on three phases which are non overlapping and dissipates 70µW power when operated on a single 1V supply voltage. The latch is basically a back to back connected inverter circuit which is activated only during the second phase. This specialty credits to the least power dissipation in the circuitry which was designed in 180nm CMOS technology.**

***Keywords:* analog to digital convertor (ADC), asynchronous successive approximation register (ASAR).**

I. INTRODUCTION

High speed and high resolution ADCs are widely used in many applications such as data storage systems, fast serial links, high speed measurement systems etc [1]. In such ADC's comparators plays a crucial role and designing such a circuit with high accuracy and speed is a challenging task. Comparator is a circuit which is used to compare the difference between two analog signals and gives the saturated values. It is also called as one bit ADC. There are several popular structures of high speed comparators like multistage open loop comparator, regenerative latch comparator, preamplifier positive feedback latch based comparator etc [1].However all latch based comparator except preamplifier based one suffers from kickback noise [2] produced by high transmission currents which induces spikes at the differential input voltage signal and the offset error caused due to the device mismatch.

With respect to the previous work done which was proposed by HeungJunJeon and Yong-Bin Kim [3] attained a power dissipation of 162µW after offset calibration. Another approach which was proposed by Kandpal, Varshney and Goswami [4] attained a power dissipation of 71.61µW. Also a design proposed by Schinkel et.al [5] attained a power dissipation of 127.9µW. Attempts have been done by Miyahara et.al [6] for attaining low power dissipation

This paper is organized as follows. Section II describes the theory and principle of the comparator. Section III describes the new architecture for the proposed comparator. Section IV discusses the simulation results of the comparator while, section V concludes the paper.

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II. THEORY AND PRINCIPLE OF COMPARATOR

Preamplifier latch based comparator circuit consists of a preamplifier followed by a latch. The major drawback of the latch comparator is the offset error caused by transistor mismatch [7] and unbalanced charge residues .To overcome this a preamplifier circuit is used. The basic principle of the preamplifiers is that it amplifies the input signal and feeds it to the input of latch which is designed by using back to back inverter [8]. Fig.1 shows the block diagram of a comparator

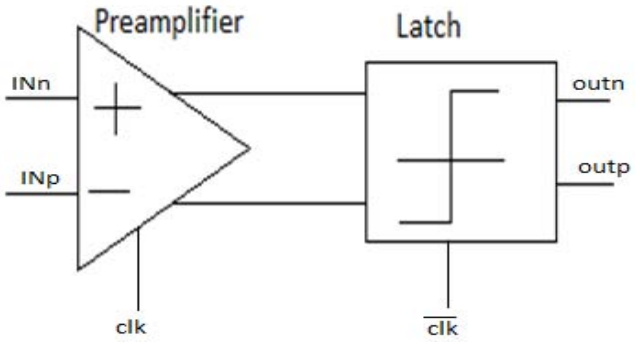

Fig.1.Block Diagram of comparator [1]

High performance comparators are needed to amplify a small input (or the difference between the input voltage and a reference voltage) to a level large enough to be detected by digital logic circuits within a very short time.

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.III. PROPOSED COMPARATOR

A. Comparator

The proposed comparator has two stages. One is the preamplifier stage and second is the positive feedback latch.

A.1.First Stage: Preamplifier Circuit

Preamplifier is used to avoid kickback noise. It is implemented using differential pairs shown in Fig. 2. Its inputs are applied at transistors PM5 and PM6. The transistors PM7 and PM4 form the tail current source to provide high CMRR. The transistors NM7 and NM10 are connected to increase gain of preamplifier circuit. The aspect ratio of preamplifier circuit is presented in Table. I

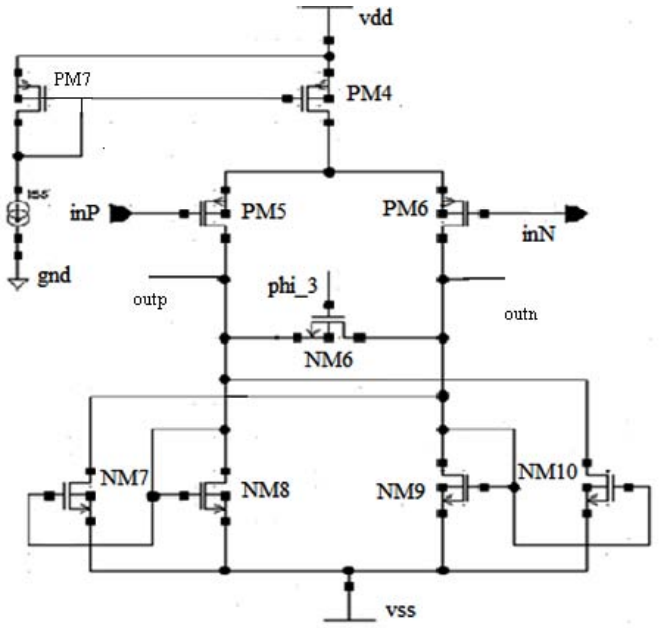

Fig.2. Preamplifier schematic [6]

TABLE.IASPECT RATIO OF PREAMPLIFIER CIRCUIT

Transistor	W	L
PM0,PM1	2µ	0.18µ
PM10,PM11	5µ	0.18µ
NM0,NM3	20µ	0.18µ
NM1,NM2	18µ	0.18µ
NM4	2µ	0.18µ

A.2. Second Stage: Latch

Latch is implemented using transistors pair PM1, NM1 and PM2, NM2. They act as inverter circuits which are connected in back to back configuration. This positive feedback latch has three phases. During the phase phi1 input voltage is sampled or tracked. During the phase phi2 output gets toggled by positive feedback and input voltage is passed. Finally during the phase phi3 the output is reset and both input voltages inP and inN reach on the same voltage level. All the phases are non overlapping phase. Fig. 3 shows a positive feedback latch circuit.

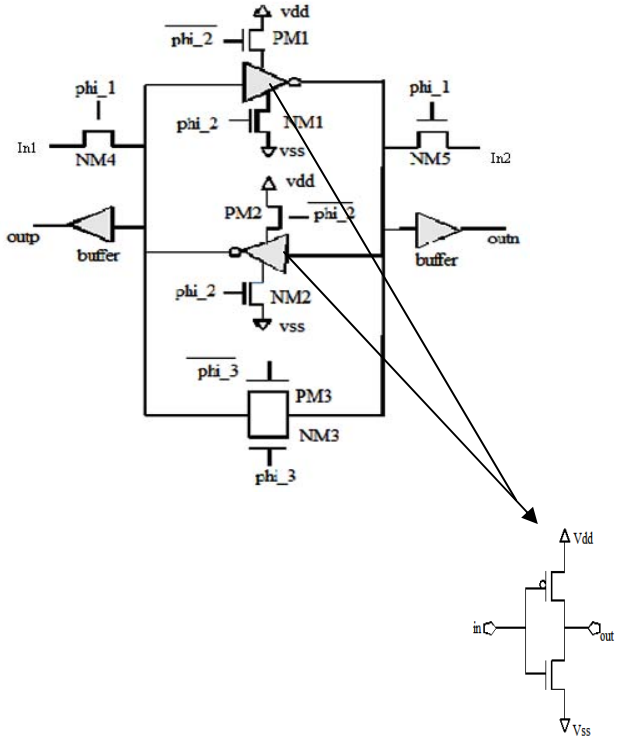

Fig.3.Schematic of Latch

Based on the circuit design of preamplifier and latch, the proposed schematic of comparator is shown in Fig. 4. Here the output of preamplifier (first stage) is connected to the inputs of positive feedback latch circuit (second stage). The circuit works under three phases.

- During the phasephi1, transistors NM4 and NM5 are 'ON' and the output of the pre-amplifier is fed to the back to back inverter pair. During the phasephi1 ,it must be noted that phases phi2and phi3are 'OFF'

- At the end of phase phi1, phase phi2 is 'ON'. At this point of time both the inverters which are connected in back to back pair are activated since the PMOS

PM1,PM2 are connected to VDD and the NMOS NM1,NM2 are connected to the VSS .This makes the inputs pass through the inverter and makes it available for comparison

- At end of phase phi2 ,phase phi3 is 'ON' which will make the voltages of p side and n side to the same potential

It must be noted that all the phases are nonoverlapping. Only during the phase phi2,an inverter circuit trigger which is an approach that reduces power dissipation in the overall circuit.

Reset phase (phi3) in transistor NM3 is given directly while reset phase in transistor PM3 is given through an inverter circuit. The aspect ratio of latch circuit is shown in Table II.

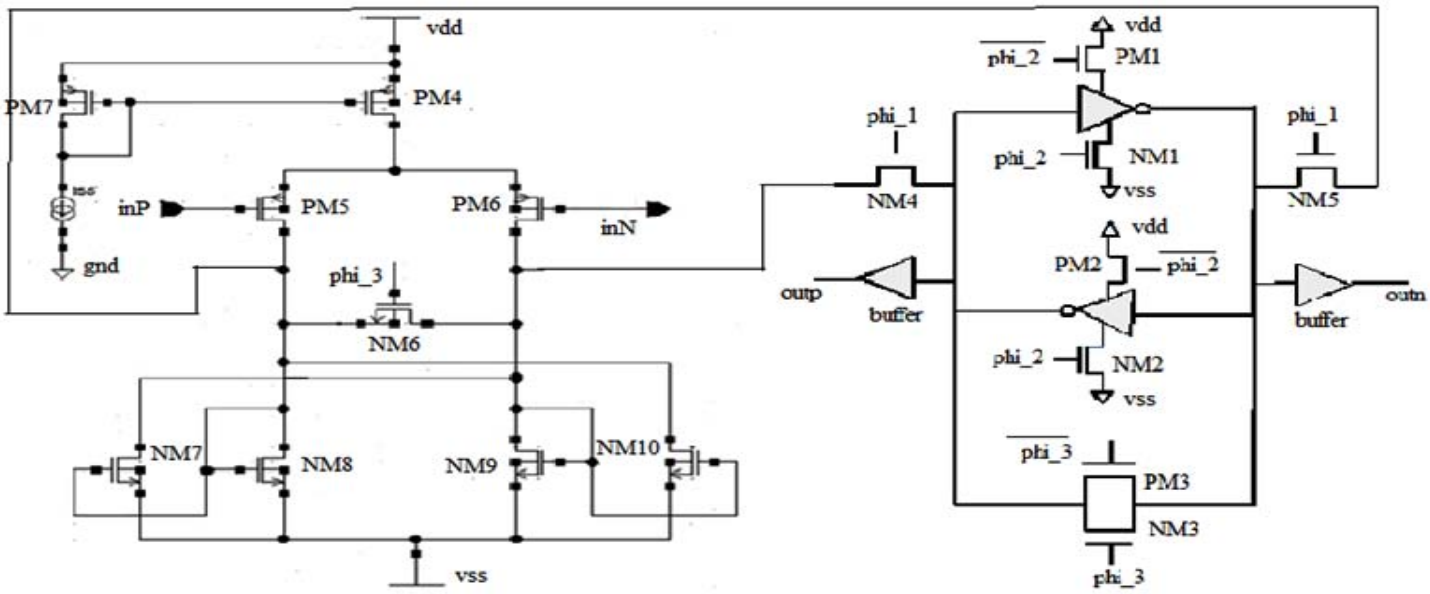

Fig.4. Complete Schematic of comparator

TABLE.IIASPECT RATIO OF LATCH

Transistor	W	L
PM0,PM1	15µ	0.18µ
NM0,NM1,NM9,NM10	5µ	0.18µ
NM6,NM7,PM6,PM7	35µ	0.18µ
PM2,NM2	40µ	0.18µ
Inverter		
PM0	5µ	0.18µ
NM0	2µ	0.18µ
Buffer		
PM0	15µ	0.18µ
PM1	10µ	0.18µ
NM0	5µ	0.18µ
NM1	3µ	0.18µ

IV. SIMULATION RESULTS OF COMPARATOR

Fig.5 shows the transient response of preamplifier architecture. Here one input voltage is applied as a 0V DC signal while the other input is sinusoidal. When the amplitude of sinusoidal wave is greater than0V, output at n side which is denoted as 'on' gives a higher voltage value and when the amplitude of sinusoidal wave gets lower than DC 0Vthe output 'on' gives lower value and viceversa for output at p side which is denoted as 'op'.

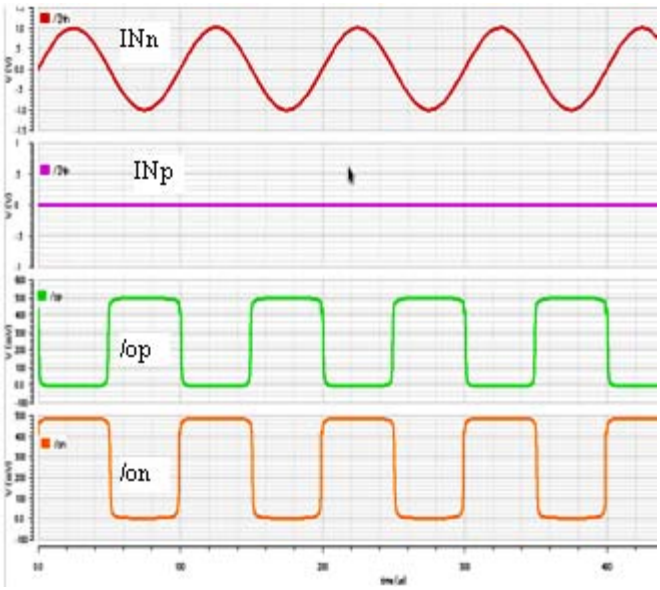

Fig.5.Transient Response of preamplifier

Fig.6 presents the transient response of phases of comparator circuit. All the phases are non overlapping phases.

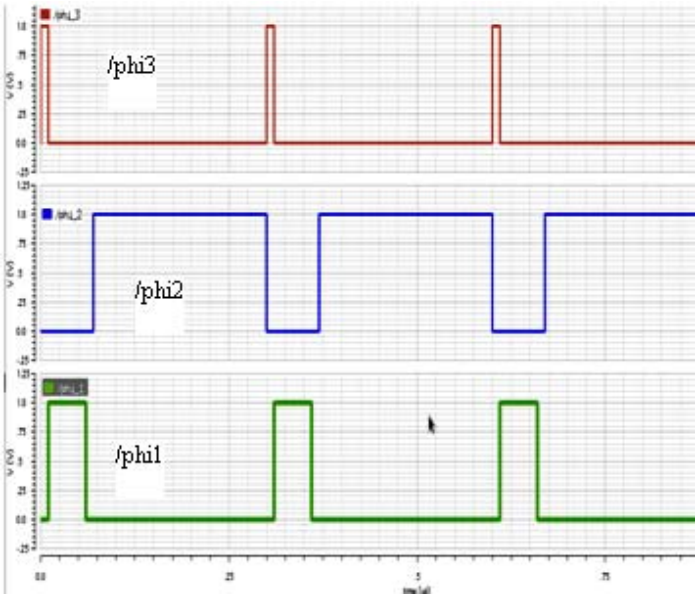

Fig.6. Non-Overlapping Phases (phi1, phi2and phi3) of positive feedback latch

Fig. 7 shows the transient analysis of proposed comparator architecture, in which input voltage at n side i.e.'INn' is given as a ramp signal from 0V to 400mV, while input voltage at p side i.e.'INp' is given as a 200mVDC signal.

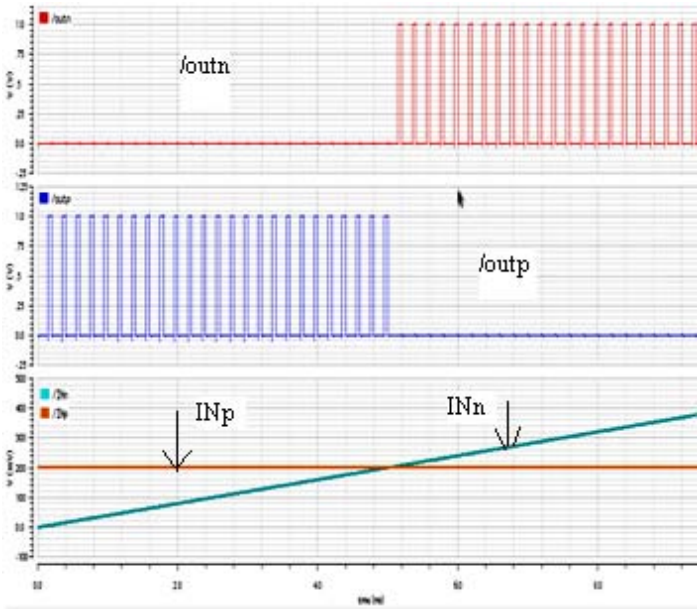

Fig.7. Transient response of comparator

Table IV represents the comparison of previous reported latch based comparator.

TABLE IV PERFORMANCE COMPARISON

Parameters	Ref [10]	Ref [11]	Ref [8]	Ref [12]	This Work
Technology (nm)	35	35	35	35	180
Supply (V)	3.3	3.3	3.3	3.3	1.0
Power consumption (µW)	3300	600	2000	1000	70

Even though the proposed is done on higher process technology (180nm CMOS Technology) it dissipates 70µW power, which is less when compared with other state of art IC's at lower process technologies.

V. CONCLUSION

This paper concludes the preamplifier positive feedback latch based comparator design. The proposed design is implemented using 180nm CMOS technology, dissipates 70µWpower when applied single 1V power supply. The comparison between the previous reported work and proposed work shows the superiority when done using 3 phases which is shown in TableIV.

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