

## Proposal by

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# Building an 8-bit computer

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## End Goal

We are aiming to build a turing complete, gate level 8-bit computer, so it can be used as a learning tool by lecturers in UCD. The computer will be built in such a way that it is easy to see what each component does, and how they interact with each other. The architecture will be a simplified version of modern CPUs, so that students will be able to better understand the architecture of modern CPUs through our model.

## Key Design Specifications

1. **Modular design board:** The computer is designed in a modular form so each part of the computer can be easily identified and its function determined. Each module will also be built on a separate piece of perfboard. This allows different modules to be connected and modules replaced if damaged. This will also enable us to separately connect the different button inputs.
2. **Labels and mounting:** Each module and display will be labeled and include a short description. Each bus and enable pin will be colour coded. The board will be mounted in a frame with a piece of plexiglass covering everything that doesn't need to be directly accessed. This will protect the computer while still allowing complete functionality.

3. **Programming:** The computer can be programmed using two DIP switches, one setting the ROM address and the other setting the value to be stored. This process will also be automated using an Arduino, which will take an assembly file and compile it into binary outputs to program the ROM.
4. **Primary Display:** The main display will be a 8x16, persistent, mono colour led display. It will read directly from the first 16, 8 bit addresses in the RAM. Each address will correspond to one column of the display. In this way writing to these addresses will automatically update the display. The last 2, 8 bit addresses of RAM will be reserved for enabling each column of the display. This will allow a portion of the display to be disabled freeing the corresponding memory addresses, allowing them to but used for other purposes.
5. **Secondary Displays:** The computer will have 3 types of secondary displays. Each register will have a decimal output of 7 segment displays to show the value held in the register. Each enable line will have an led to show which modules are enabled. There will also be a removable decimal output that can be connected to each of the RAM registers to display the value contained in each memory address.
6. **Button Inputs:** The computer will have two different button modules. One where the output bit of the module is set high only while the button is pressed and goes low on release and another where the output remains high until it is read and then is set low.

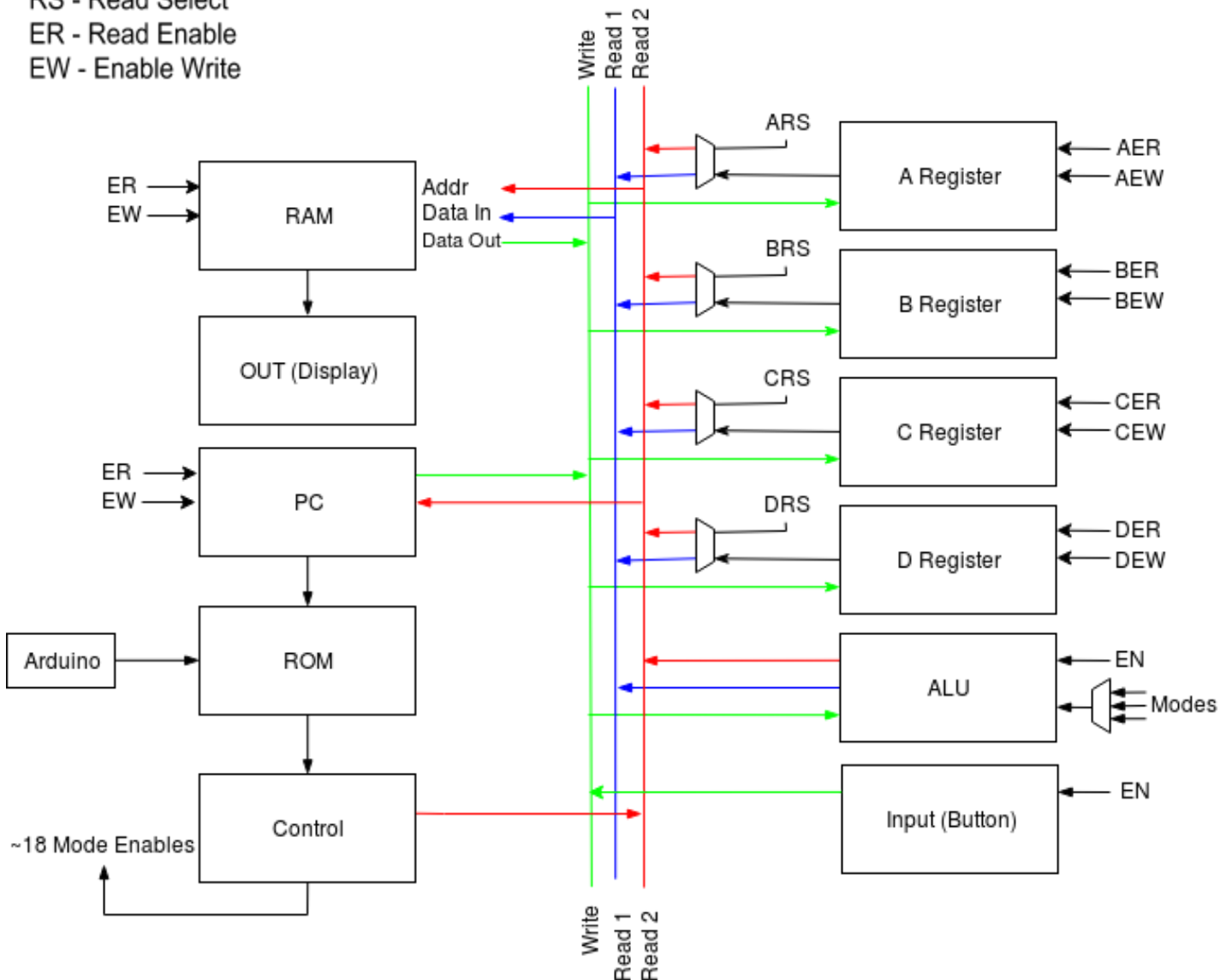
## Proposed specification

Key:

RS - Read Select

ER - Read Enable

EW - Enable Write



## Timeline

### 1. Meeting with Lecturers - 1 week

We will be contacting a lecturer in either the school of computer science or electronic engineering for advice as well as an endorsement, to ensure that the resulting product will be used as a learning tool in UCD.

### 2. Agree on a design - 1 week

Working with the lecturer, we will agree on a design of the architecture, taking into consideration what design choices the lecturer requests for us to incorporate.

### 3. Detail the Instruction set - 1 week

We will then agree on an instruction set, and make a list of instructions that will be implemented in the design. Agreeing on this lets us work on the programming and the hardware design in parallel.

### 4. Write Program - 4 weeks

One person will write a program in Assembly language based on the agreed instruction set. We will also write software for the Arduino to be able to process the Assembly program, and program it directly into the ROM module.

### 5. Initial design on Logisim - 4 weeks

Concurrently, two people will construct and test a gate level design in Logisim. By using Logisim, we will be able to fine tune our design before we actually use parts, and we can error check our hardware design against a working copy of the architecture in Logisim

## 6. Construction - 3 weeks

Finally, we will construct the physical device out of ordered parts.

## Cost Estimate

| Part             | Link                 | Quantity | Price/Part | Total Cost | Used Module |
|------------------|----------------------|----------|------------|------------|-------------|
| Perf Board       | <a href="#">eBay</a> | 100pc    | 0.2        | 19         | All         |
| Ribbon cable     | <a href="#">eBay</a> | 10m      | 17         | 17         | All         |
| 4 Bit register   | <a href="#">eBay</a> | 100pc    | 0.3        | 30         | Registers   |
| Quad and gate    | <a href="#">eBay</a> | 30pc     | 0.15       | 4.50       | All         |
| Quad or gate     | <a href="#">ebay</a> | 30pc     | 0.33       | 9.90       | All         |
| Hex inverter     | <a href="#">eBay</a> | 30pc     | 0.25       | 7.5        | ALU         |
| Dip 16 socket    | <a href="#">eBay</a> | 100pc    | 0.03       | 3.2        | ROM/RAM     |
| Dip 14 socket    | <a href="#">eBay</a> | 100pc    | 0.03       | 2.8        | ROM/RAM     |
| LED's            | <a href="#">ebay</a> | 300pc    | 0.01       | 3.36       | Bus display |
| 7 segment        | <a href="#">ebay</a> | 100pc    | 0.29       | 29         | All         |
| 330R resistor    | <a href="#">ebay</a> | 400pc    | 0.04       | 18.40      | All         |
| 8 pin dip switch | <a href="#">ebay</a> | 10p      | 0.27       | 2.75       |             |
| Total            |                      |          |            | 147.41     |             |