Welcome to The Logic Design Lab!

Fall 2021

Lab 4: Finite State Machines

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Agenda

- Lab 4 Outline
- Lab 4 Basic Questions
- Lab 4 Advanced Questions

Lab 4 Outline

- Basic questions (1.5%)
  - Individual assignment
  - Due on 11/2/2021 (Thu). In class.
- Advanced questions (5%)
  - Group assignment
  - Demonstration on your FPGA board (In class)
  - Assignment submission (Submit to eeclass)
    - ILMS submission due on 11/11/2021 (Thu). 23:59:59.
    - Source codes and testbenches
    - Lab report in PDF

Lab 4 Rules

- Please note that grading will be based on **NCVerilog**
- You can use **ANY** modeling techniques

- If not specifically mentioned, we assume the following SPEC
  - **clk** is **positive edge triggered**
  - Synchronously reset the Flip-Flops when **rst_n == 1'b0, if there exists one rst_n signal in the specification**

Lab 4 Submission Requirements

- Source codes and testbenches
  - Please follow the templates EXACTLY
  - We will test your codes by TAs' testbenches
- Lab 4 report
  - Please submit your report in a single PDF file
  - Please draw the **block diagrams** and **state transition diagrams** of your designs
  - Please explain your designs in detail
  - Please list the contributions of each team member clearly
  - Please explain how you test your design
  - What you have learned from Lab 4

Agenda

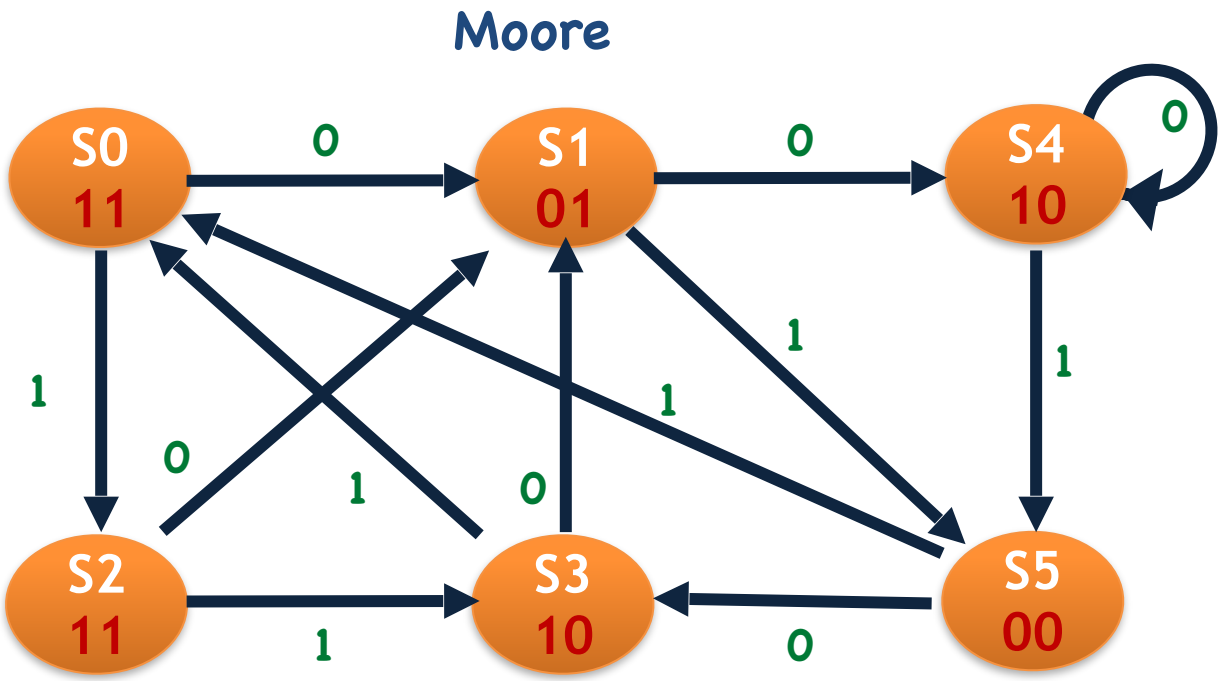
- Lab 4 Outline
- Lab 4 Basic Questions
- Lab 4 Advanced Questions

Basic Questions

- Individual assignment
- Verilog questions (due on 11/2/2021. In class.)
  - Moore machine
  - Mealy machine
  - Many-to-one linear-feedback shift register
  - One-to-many linear-feedback shift register
- Demonstrate your work by waveforms

Verilog Basic Question 1

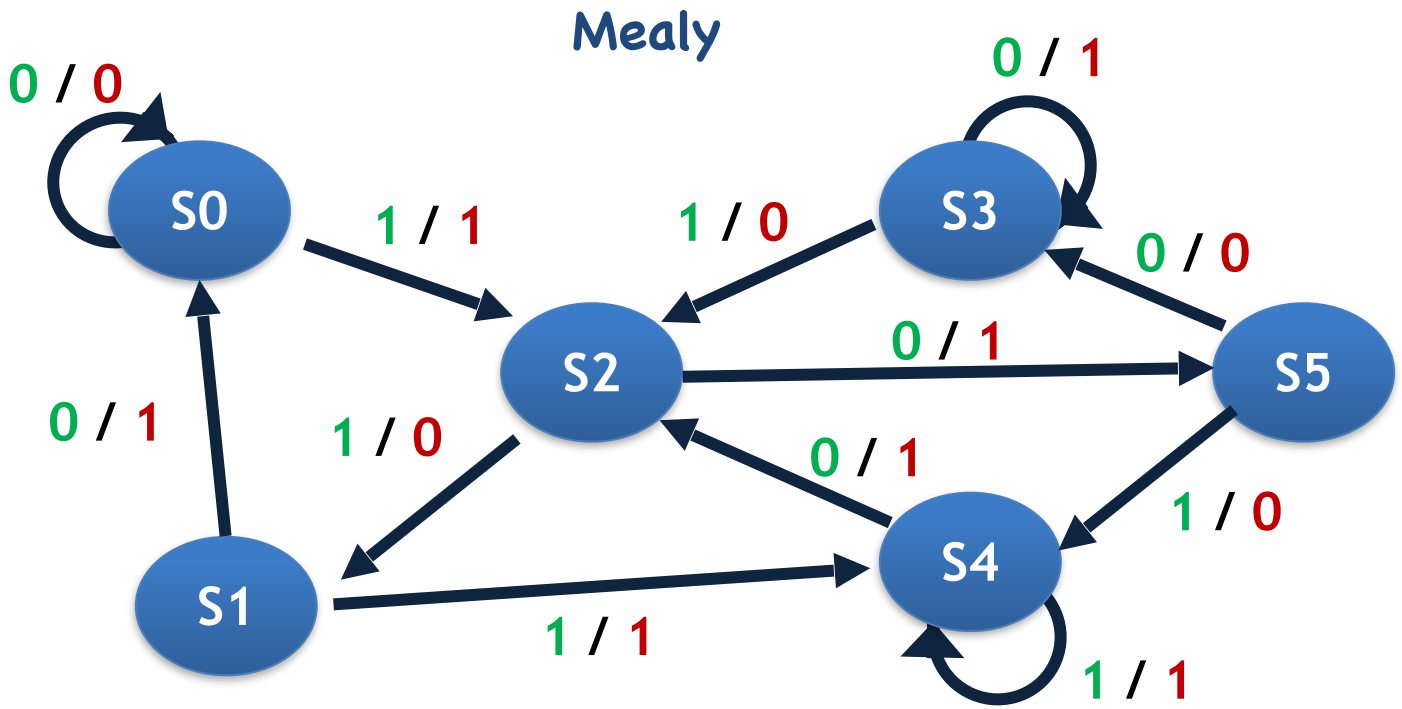
- Moore machine
  - **Green** represents input, while **red** represents output
  - Output your **current state** as well
  - When **rst_n** == 1'b0, **state** = S0



S0: 3'b000 S1: 3'b001 S2: 3'b010 S3: 3'b011 S4: 3'b100 S5: 3'b101

Verilog Basic Question 2

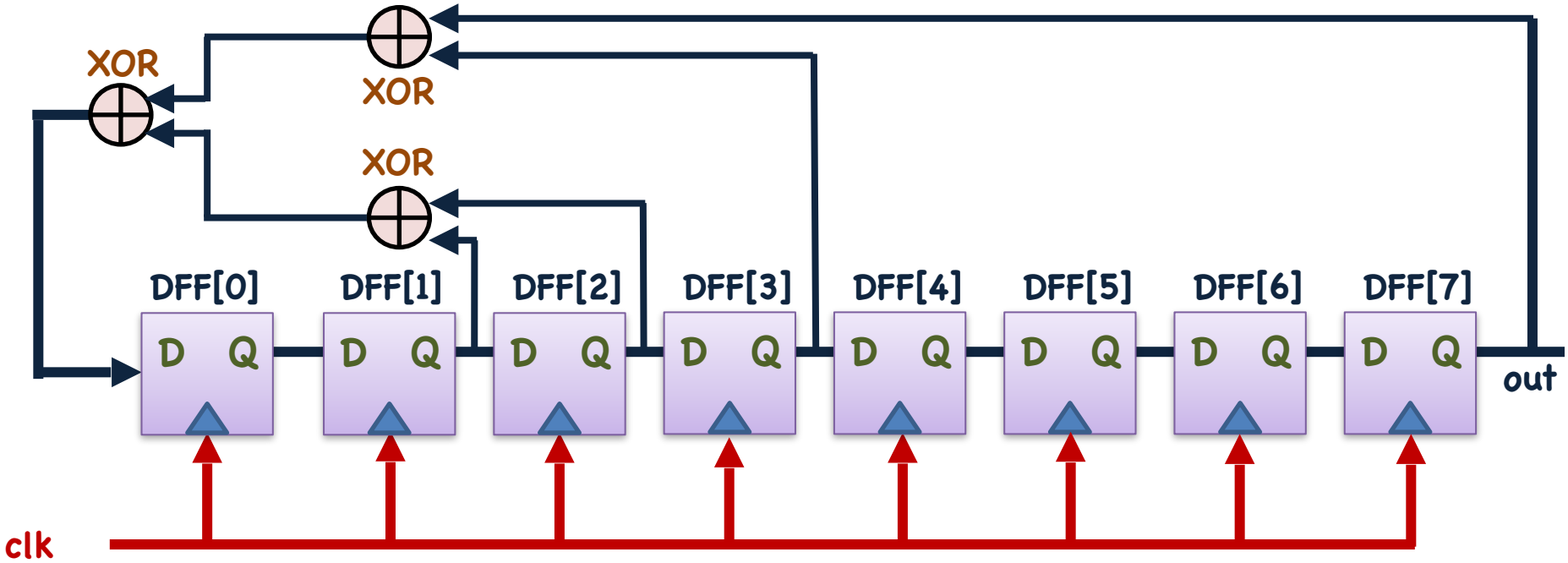
- Mealy machine
  - **Green** represents input, while **red** represents output
  - Output your **current state** as well
  - When **rst_n** == 1'b0, **state** = S0



S0: 3'b000 S1: 3'b001 S2: 3'b010 S3: 3'b011 S4: 3'b100 S5: 3'b101

Verilog Basic Question 3

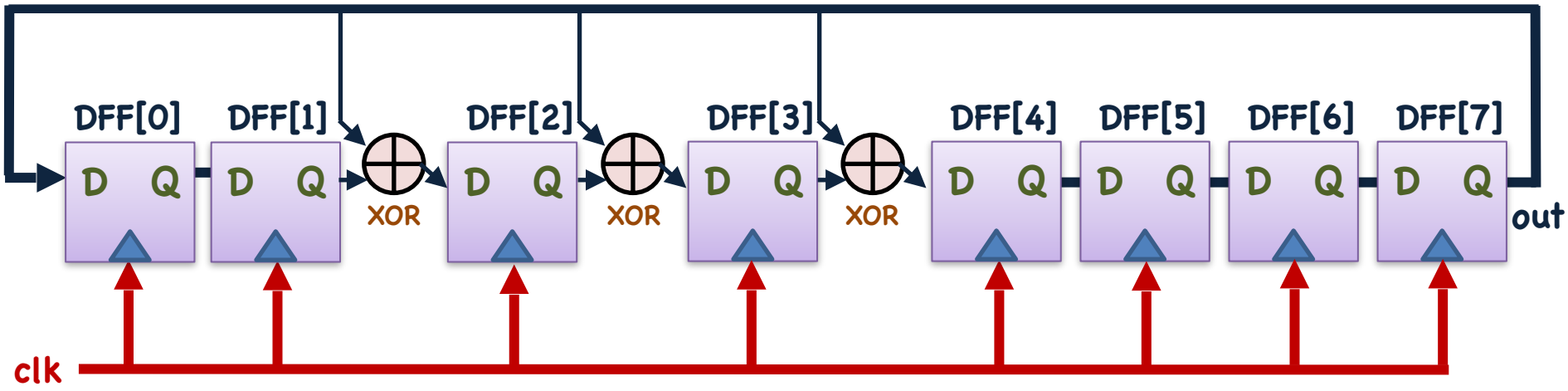
- Many-to-one linear-feedback shift register (LFSR)



- When **rst_n == 1'b0**, reset DFF[7:0] to **8'b10111101**
- Please draw the **state transition diagram** of the DFFs in LFSR for the first ten states after **rst_n** is raised to **1'b1** in your report
- Please describe what happens if we reset the DFFs to **8'd0** in your report

Verilog Basic Question 4

- One-to-many linear-feedback shift register (LFSR)



- When **RESET == 1'b0**, reset DFF[7:0] to **8'b10111101**
- Please draw the **state transition diagram** of the DFFs in LFSR for the first ten states after **rst_n** is raised to **1'b1** in your report
- Please describe what happens if we reset the DFFs to **8'd0** in your report