

Motivation

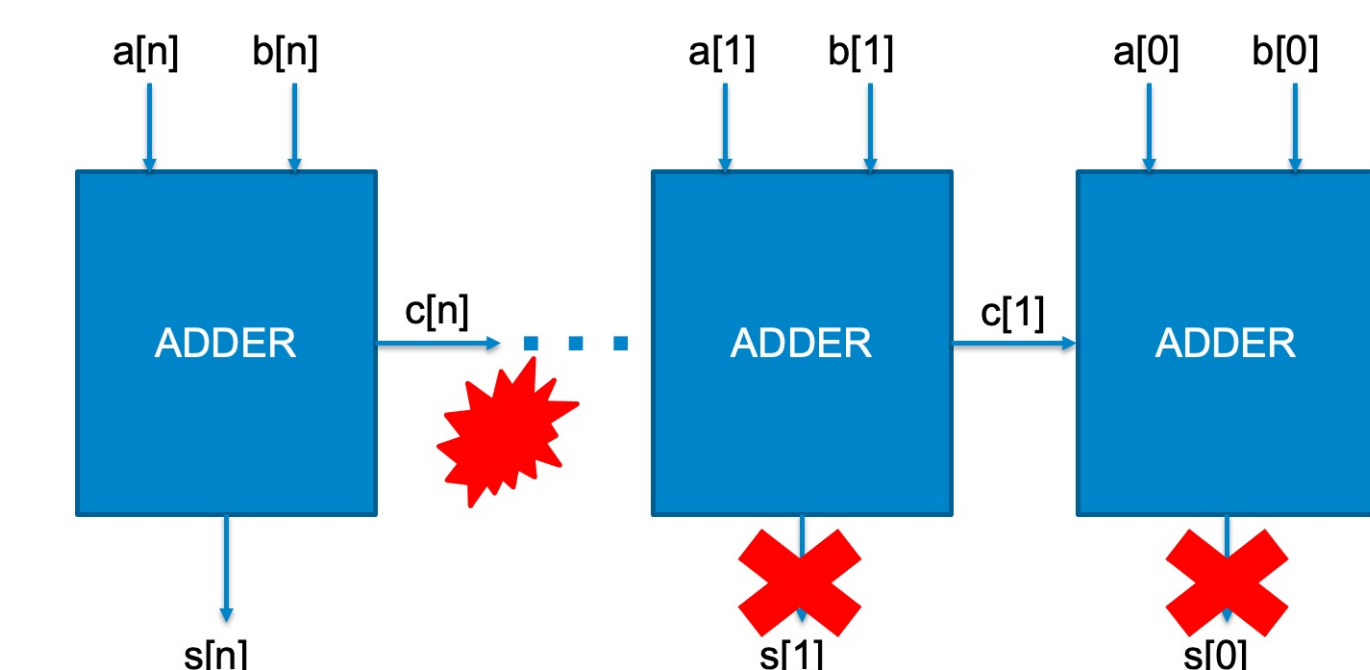
Slow, Cheap, Dynamic ← CPU GPU FPGA → Fast, Expensive, Fixed ASIC

FPGAs are configurable but have an **unchangeable microarchitecture**

Data Integrity

Speed

In some applications **accuracy is forfeited** in the pursuit of speed



Online arithmetic leads to **graceful degradation** due to MSD-first carry chains

Does high-radix online arithmetic perform better than radix-2 due to the FPGA microarchitecture?

Implementation

$$X = \sum_{i=0}^{i=N} x_i \times r^i$$

$$x_i \in \{-r + 1, \dots, -1, 0, 1, \dots, r - 1\}$$

The key to online arithmetic is **redundancy**

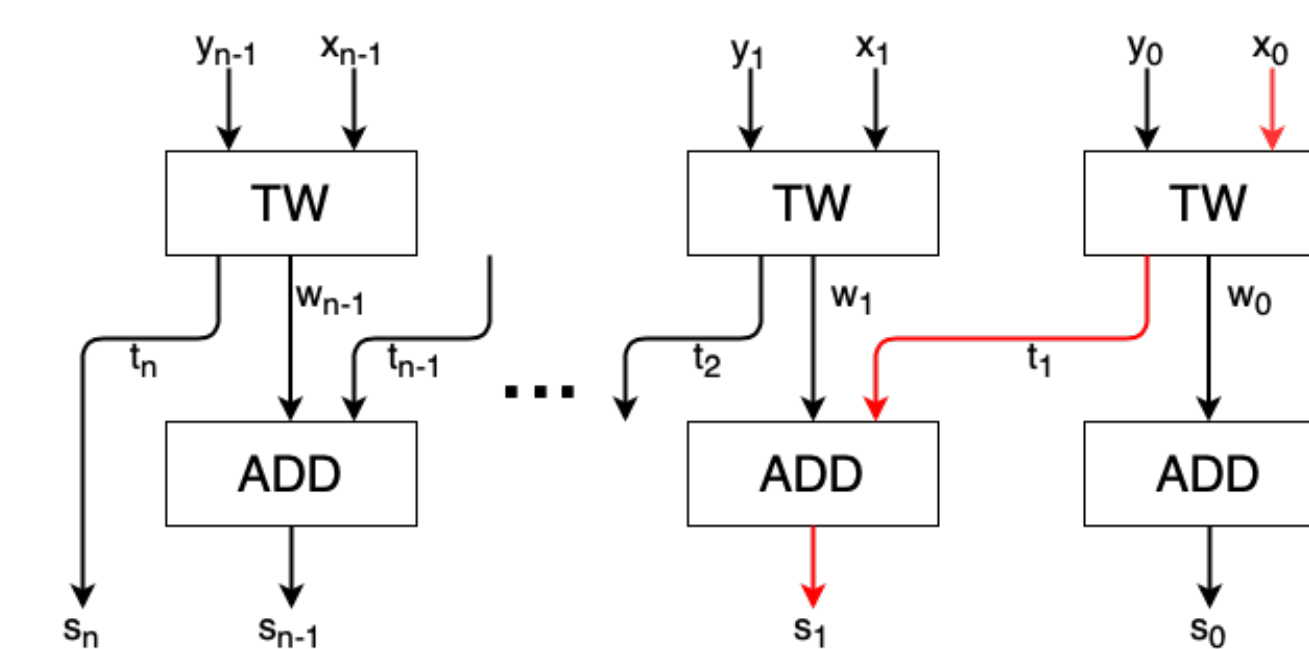


Image adapted from Digital Arithmetic textbook by Milos Ercegovac

Addition is done **fully in parallel** with a constant carry chain

Multiplication works through an **iterative residual approach**, and is pipelined

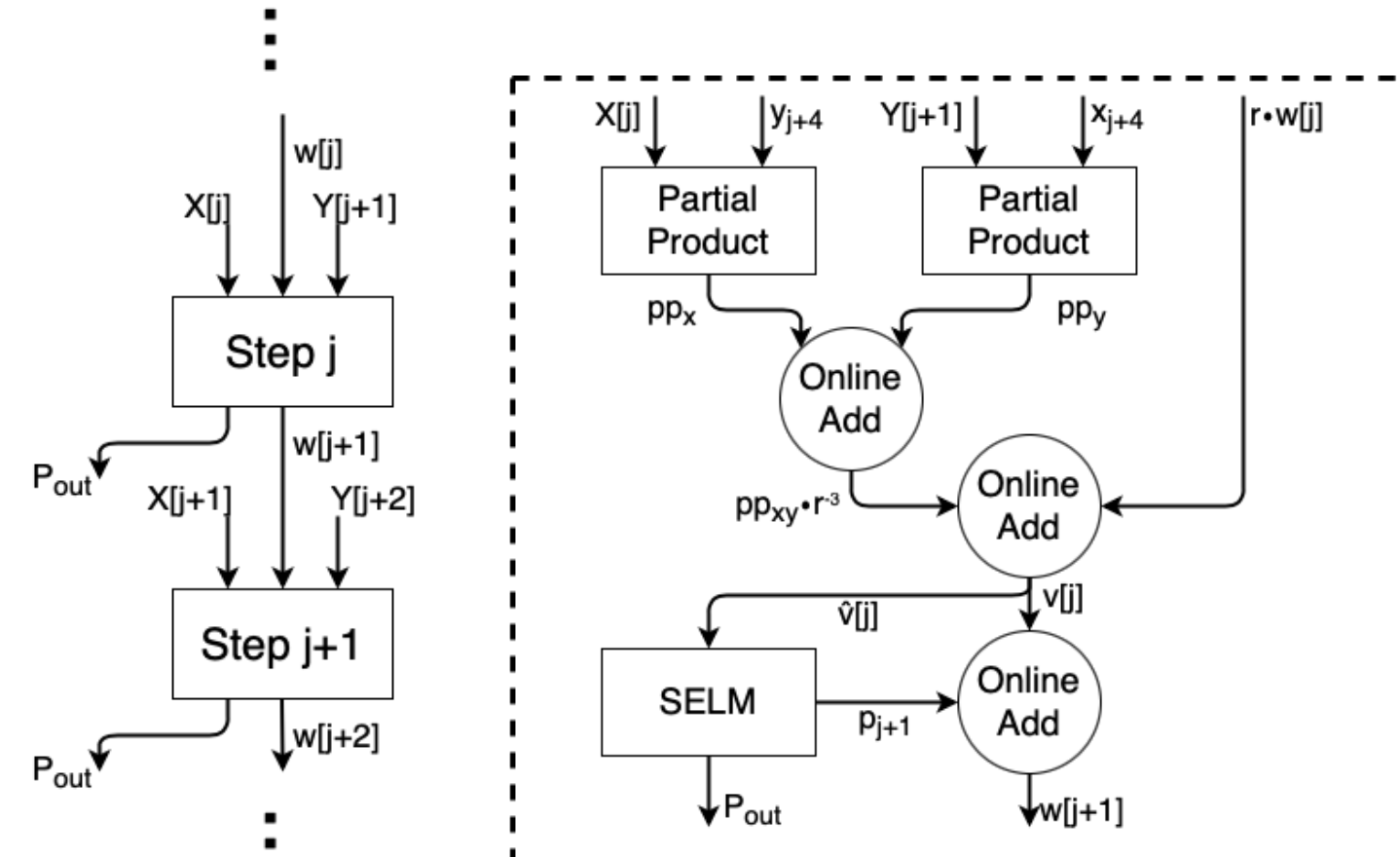
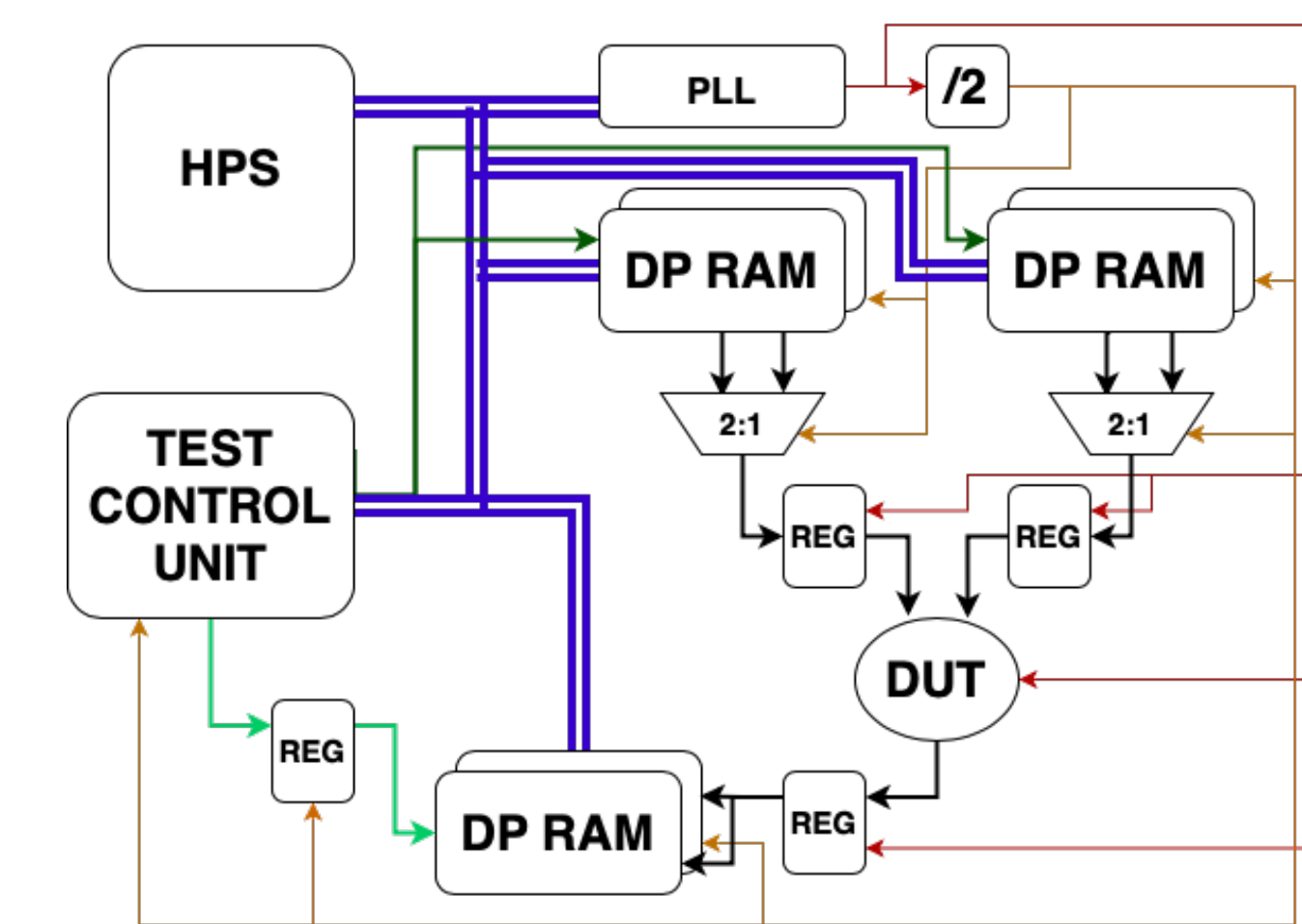


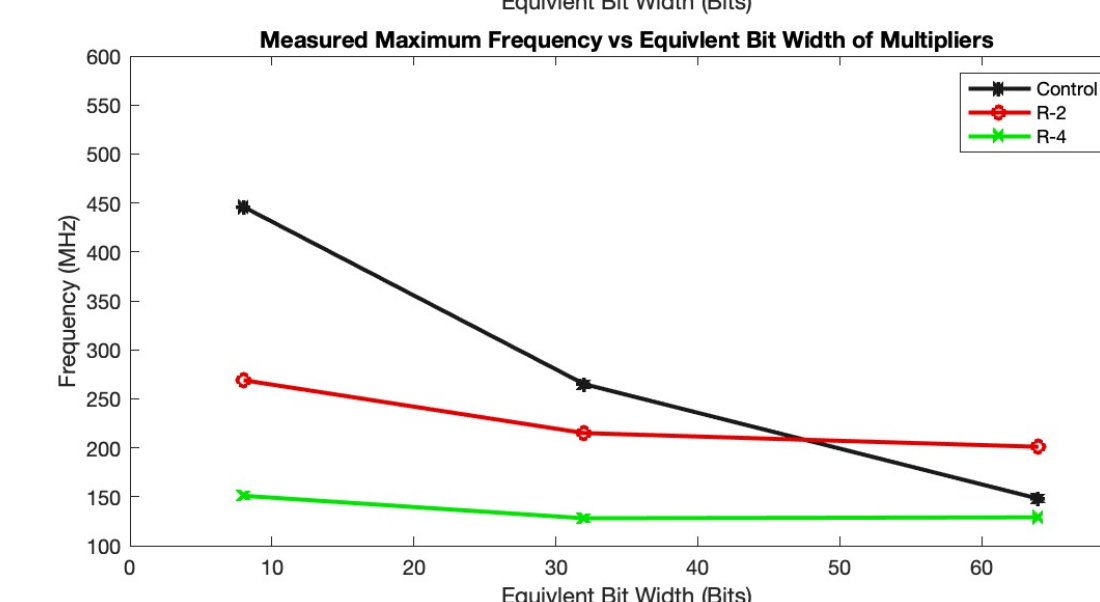
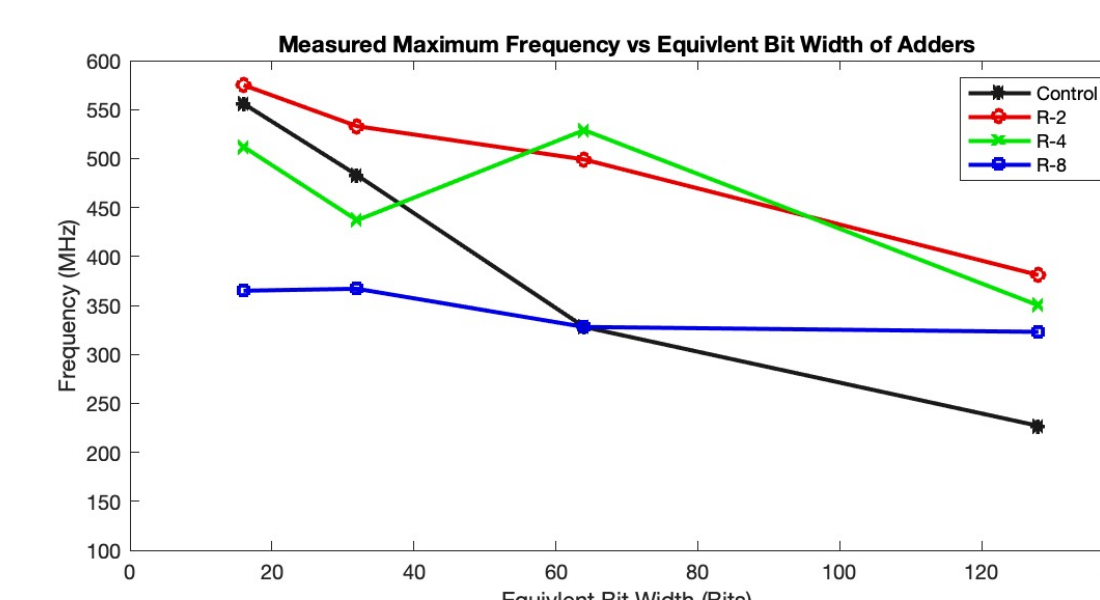
Image adapted from Kan Shi's PhD Thesis

Testing



The test bench must **withstand higher frequencies** than the DUT

Speed Data

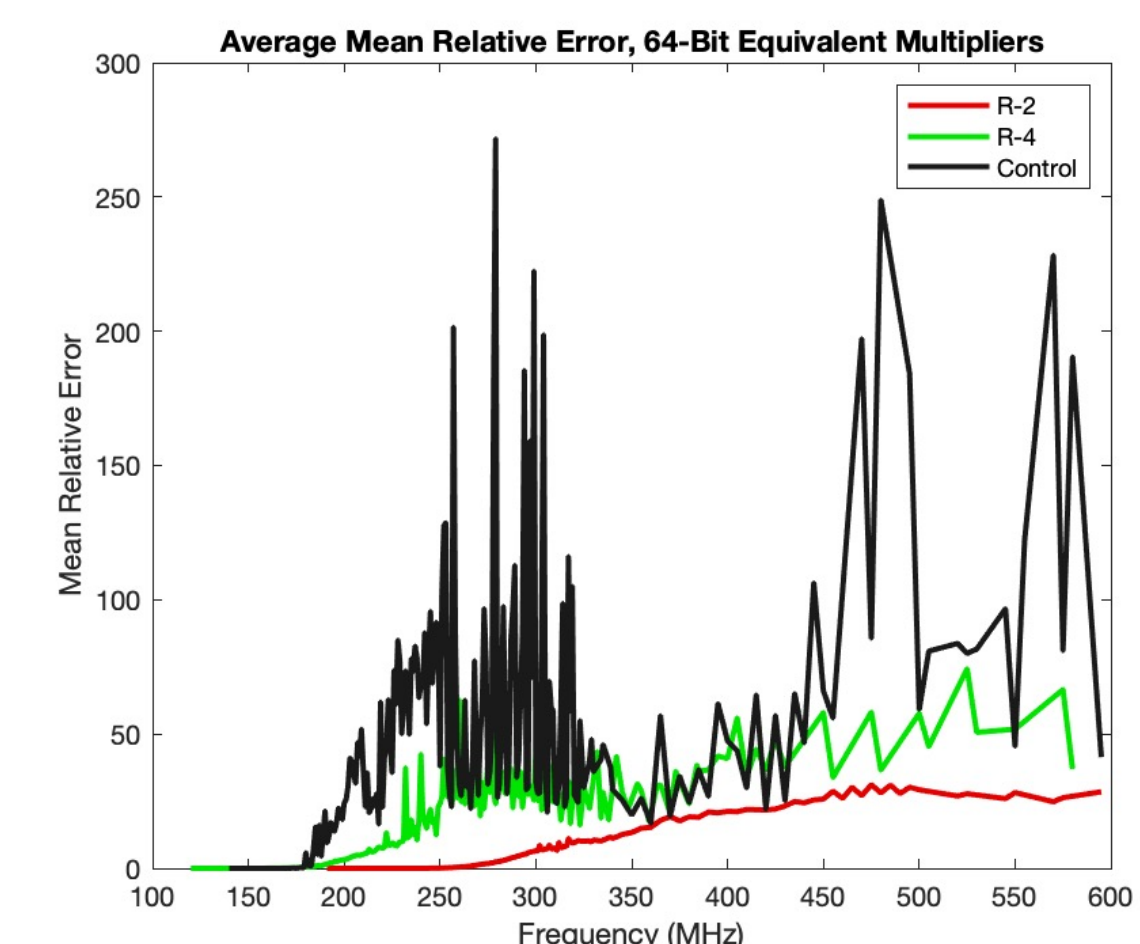
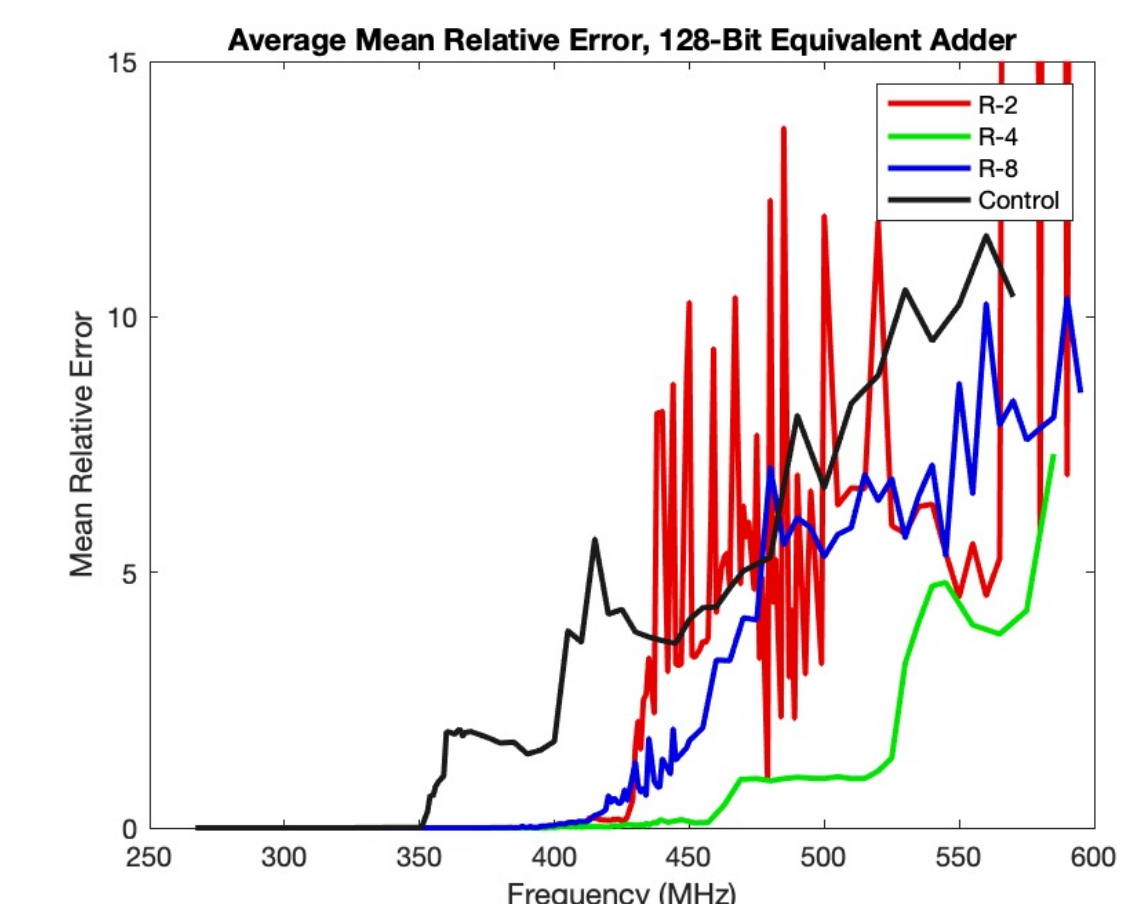


Radix-2 is **generally faster** than higher radices, especially in the multiplier

Degradation Data

Radix-4 adders degrade more advantageously than radix-2

This is not the case for **multipliers** or higher radices



Only radix-4 addition benefits from the FPGA microarchitecture over radix-2