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MSc Individual Research Project Initial Report

MSc: Analogue and Digital Integrated Circuit Design
Project Advisor: Dr. James J. Davis
Project Title: High Radix Online Arithmetic for FPGA Overclocking

Motivation and Past Work:
Field programmable gate arrays (FPGA) are a promising platform for embedded, latency-sensitive applications. In some applications however, the latency requirements become impossible to meet within the bounds of static timing analysis (STA). Dr. Kan Shi has shown that by overclocking an FPGA, reduced latency can be achieved at the cost of accuracy within the data [1]. This hit in accuracy comes as arithmetic blocks fail, causing bit errors in the results. In traditional arithmetic blocks, propagating carry signals form the critical path in the system. These carry chains cause bit errors occur to at the most significant bits (MSB) of the output, resulting in a maximal reduction in accuracy.

MSB-first, parallel online arithmetic solves this issue but reversing the order of the arithmetic operation, resulting in a graceful degradation of the output beginning in the least significant bits (LSB). Online arithmetic works on the principle of representing inputs and outputs with redundant digit sets, constraining carry propagation to a constant value independent of bit length [2]. In a later paper, Shi utilizes online arithmetic in an overclocked FPGA to reduce the error (increase the accuracy) when compared to traditional methods [3].

While in principle the use of online arithmetic provides clear performance gains, the physical design of FPGA soft logic results in inefficient implementations. These inefficiencies motivated previous attempts at tailoring online architectures to FPGA platforms, reducing resource utilization and increasing latency [4][5]. In these previous optimization attempts, the architectures operate on numbers encoding in the standard radix-2. Dr. Peter Kornerup has shown that in the case of an ASIC implementation, radix-2 encoding provides the fastest implementation [6]. However, Kornerup goes on to hypothesizes that higher radix recodings could result in performance gains in the specific case of FPGAs due to the presence of highly optimized, traditional adder architectures within the fabric.

Objectives of the project:
In this project I will implement higher-radix parallel online arithmetic operations on a Cyclone V FPGA and measure the effect of radix on degradation at overclocked frequencies. Adders, multipliers, and dividers will be tested. Traditional LSB-first operations will be used as a control. If time permits additional functions such as square root will be implemented in the online approach, and/or a common latency sensitive algorithm (such as one for computer vision) using the online blocks will be constructed and measured. Implementation on Xilinx FPGA can also be tested and compared to Intel to study the impact of the differing soft logic

architectures. The performance of the blocks will be evaluated using similar metrics as previous research and those defined in [7]. Finally, this project will also require the design and implementation of a test architecture capable of feeding and storing data at frequencies higher than the operation of the arithmetic blocks.

Progress thus far:

So far, I have developed a parallel online adder block of parametrized radix and bit length. My focus has now shifted to developing the high-speed test structure. This has involved the overhead of learning the Quartus Platform Designer workflow, and how to develop my custom IP blocks to interact with test code running on the HPS. Going forward, I will use the number of arithmetic blocks I've created and tested as a way to track my progress.

Proposed Final Report Contents Page:

1. Introduction
2. Background on Online Arithmetic
3. Explanation of Measurement Metrics
4. Experimental Setup
5. Results
6. Conclusion

References:

[1] K. Shi, D. Boland and G. A. Constantinides, "Accuracy-Performance Tradeoffs on an FPGA through Overclocking," *2013 IEEE 21st Annual International Symposium on Field-Programmable Custom Computing Machines*, Seattle, WA, USA, 2013, pp. 29-36, doi: 10.1109/FCCM.2013.10.

[2] M. D. Ercegovac and T. Lang, Digital arithmetic, Morgan Kaufmann, 2003.

[3] K. Shi, D. Boland, E. Stott, S. Bayliss and G. A. Constantinides, "Datapath synthesis for overclocking: Online arithmetic for latency-accuracy trade-offs," *2014 51st ACM/EDAC/IEEE Design Automation Conference (DAC)*, San Francisco, CA, USA, 2014, pp. 1-6, doi: 10.1145/2593069.2593118.

[4] K. Shi, D. Boland and G. A. Constantinides, "Efficient FPGA implementation of digit parallel online arithmetic operators," *2014 International Conference on Field-Programmable Technology (FPT)*, Shanghai, China, 2014, pp. 115-122, doi: 10.1109/FPT.2014.7082763.

[5] Yiren Zhao, J. Wickerson and G. A. Constantinides, "An efficient implementation of online arithmetic," *2016 International Conference on Field-Programmable Technology (FPT)*, Xi'an, 2016, pp. 69-76, doi: 10.1109/FPT.2016.7929191.

[6] P. Kornerup, "Reviewing High-Radix Signed-Digit Adders," in *IEEE Transactions on Computers*, vol. 64, no. 5, pp. 1502-1505, 1 May 2015, doi: 10.1109/TC.2014.2329678.

[7] J. Liang, J. Han and F. Lombardi, "New Metrics for the Reliability of Approximate and Probabilistic Adders," in *IEEE Transactions on Computers*, vol. 62, no. 9, pp. 1760-1771, Sept. 2013, doi: 10.1109/TC.2012.146.