Imperial College London

Graceful Degradation on FPGAs: A High-Radix Online Approach

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Motivation

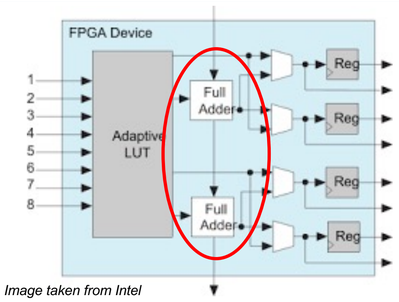
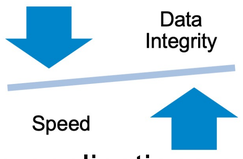
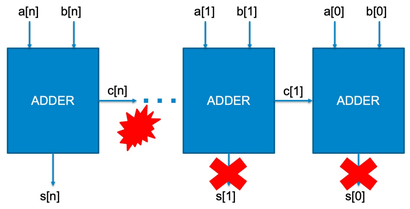


Image taken from Intel

FPGAs are configurable but have an unchangeable microarchitecture targeting LSD-first operation



In some applications accuracy is forfeited in the pursuit of speed



Online arithmetic leads to graceful degradation due to MSD-first carry chains

Does high-radix online arithmetic perform better than radix-2 on FPGAs?

Implementation

$$X = \sum_{i=0}^{i=N} x_i \times r^i$$

$$x_i \in \{-r+1, \ldots, -1, 0, 1, \ldots, r-1\}$$

The key to online arithmetic is redundancy, allowing MSDs to be guessed and LSDs to correct for error

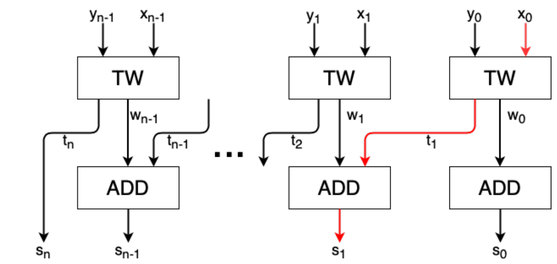


Image adapted from Digital Arithmetic textbook by Milos Ercegovac

Addition is done fully in parallel with a constant carry chain

Multiplication works through an iterative residual approach, and is pipelined

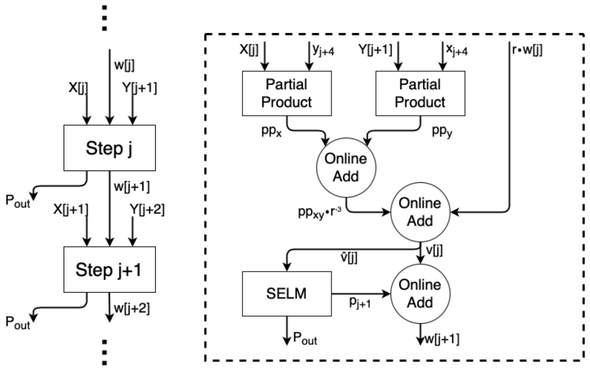
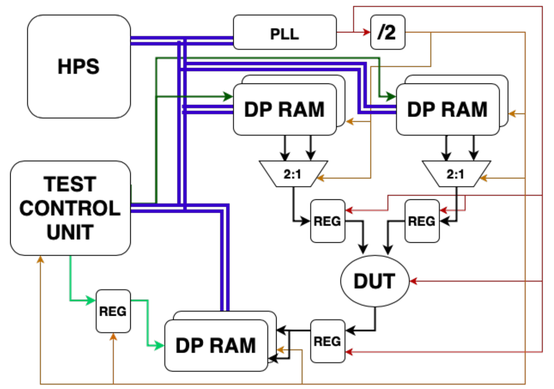


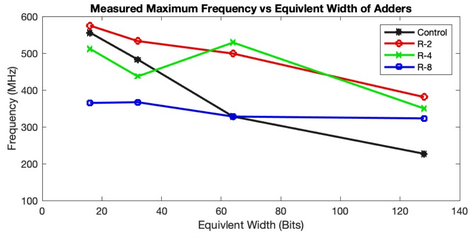
Image adapted from Kan Shi's PhD Thesis

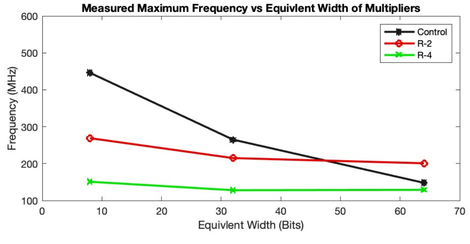
Testing



The test bench must withstand higher frequencies than the DUT

Speed Data



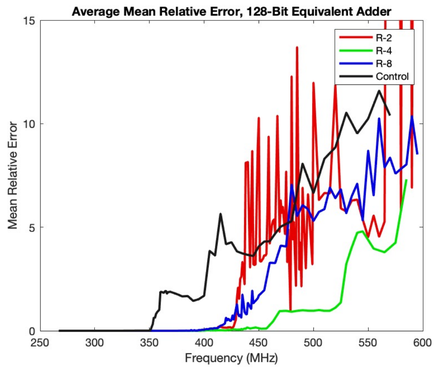


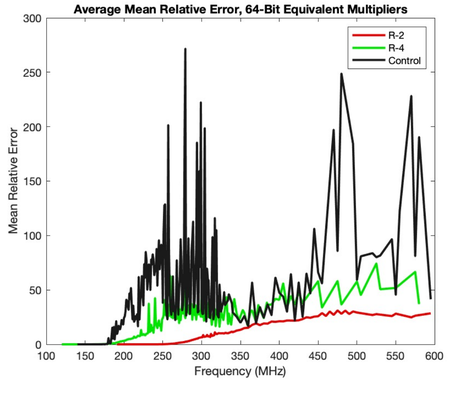
Radix-2 is generally faster than higher radices, especially in the multiplier

Degradation Data

Radix-4 adders degrade more advantageously than radix-2

This is not the case for multipliers or higher radices





Only radix-4 addition benefits from the FPGA microarchitecture over radix-2