Lab 4 COMPENG 3DQ5

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COMPENG 3DQ5

For exercise one, we implemented a design in order to overwrite the data stored in a dual access ROM. This was completed in 512 clock cycles, which is optimised to be the fastest possible way of implementing. This was done by having a read, and write clock cycle, alternating between the two methods. As seen in experiment.sv, register total for this implementation is solely restricted to the following values;

- Read_address (9)
- Read_address256 (9)
- Write_enable_a (2)
- Write_enable_b (2)
- States (4)

Figure 1 displays the critical path and timing information, this takes information from the state and writes to the ROM.

Slow 1200mV 85C Model

	Slack	From Node	To Node	Launch Clock	Latch Clock	Relationship	Clock Skew	Data Delay
1	13.601	state.S_IDLE	write_enable_b[1]	clk_50	clk_50	20.000	0.197	6.594

Figure 1

From Quartus, the amount of logic elements required for our design is 130, while this is larger than required, we designed our assigned conditions for writing to check if enable is one, which increases power efficiency as the ROM’s aren't constantly being written too.