Lab 5 COMPENG 3DQ5

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While developing the state table for this lab, an approach to minimise the amount of memory being used was taken in order to optimise the run-time complexity of the RGB VGA display. This resulted in fewer registers being used in order to store the data read from the SRAM. As shown in Appendix A, the three data registers VGA_sram_data[2:0] were untouched, and used to store the red, green and blue data bits respectively. Address registers were added in order to index the SRAM memory, and buffers were used sporadically to hold individual data bytes as required.
From the state table (Appendix B), a setup period of 8 states occurs when a new line is reached, followed by a repeating cycle of 8 states (S_9-S_16). A new line is checked for in S_13, as this allows for an offset to be detected, and skipped if a new line is required to be added. This results in a reset of the addresses by multiplying the start address by the product of the row register and a constant depending on which address is required (Figure 1).

```
red_address <= RED_START_ADDRESS + (row * 160);
green_address_e <= GREEN_EVEN_START_ADDRESS + (row * 80);
green_address_o <= GREEN_ODD_START_ADDRESS + (row * 80);
blue_address_e <= BLUE_EVEN_START_ADDRESS + (row * 80);
blue_address_o <= BLUE_ODD_START_ADDRESS + (row * 80);
```

Figure 1

The estimate of registers that were added by our group is as follows;

- Red_address (18)
- Green_address_e (18)
- Green_address_o (18)
- Blue_address_e (18)
- Blue_address_o (18)
- Row (10)
- Red_buffer (8)
- Green_buffer_e (8)
- Green_buffer_o (8)
- Blue_buffer_e (8)
- Blue_buffer_o (8)

Further states were added without changing the size of the state register (32 bits), therefore not expanding the register count. From Quartus, the estimated register count is equal to 410, 140 of those registers stem from the created registers above, and the remaining 270 are directly related to the source code provided.
The critical path is obtained from the state bit 0, to the SRAM_address[13] which has a delay of 7.373. This correlates with the expected worst case, as it originates with a memory address interfacing with the SRAM.

Appendix A

Module (instance)	Register Name	Bits	Description
Top-level experiment 1	red_address	18	Red pixel index
Top-level experiment 1	green_address_e	18	Even green pixel index
Top-level experiment 1	green_address_o	18	Odd green pixel index
Top-level experiment 1	blue_address_e	18	Even blue pixel index
Top-level experiment 1	blue_address_o	18	Odd blue pixel index
Top-level experiment 1	red_buffer	8	Buffers red value in state 10
Top-level experiment 1	green_buffer_e	8	Buffers green value in state 14
Top-level experiment 1	green_buffer_o	8	Buffers green value in state 16
Top-level experiment 1	blue_buffer_e	8	Buffers blue value in state 14
Top-level experiment 1	blue_buffer_o	8	Buffers blue value in state 16
Top-level experiment 1	row	10	Counts valid rows that are printed, used to reset addresses for indexing
Top-level experiment 1	VGA_sram_data[2]	16	Holds red data from SRAM
Top-level experiment 1	VGA_sram_data[1	16	Holds green data from SRAM
Top-level experiment 1	VGA_sram_data[0]	16	Holds blue data from SRAM

Appendix B

State Code	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
pixel_x_pos	157		158		159		160		161		162		163		164		165
SRAM_address	red_address	green_address_e	blue_address_e	green_address_o	blue_address_o		red_address		red_address	green_address_e	blue_address_e	green_address_o	blue_address_o		red_address		red_address
VGA_sram_data[2]				[R0, R1]						[R2, R3]		[R4, R5]					
VGA_sram_data[1]					[G0, G2]		[G1, G3]						[G4, G6]		[G5, G7]		
VGA_sram_data[0]						[B0, B2]		[B1, B3]						[B4, B6]		[B5, B7]	
VGA_red_buffer											R3						
VGA_green_odd_buffer									G3								G7
VGA_green_even_buffer							G2								G6		
VGA_blue_odd_buffer									B3								B7
VGA_blue_even_buffer							B2								B6		
VGA_r							R0		R1		R2		R3		R4		R5

ed																
VGA_ green							G0		G1		G2		G3		G4		G5
VGA_ blue							B0		B1		B2		B3		B4		B5