Lab 4 COMPENG 3DQ5

Joshua Umansky, George Wahba

400234265, 400371904

McMaster University

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For exercise two, the design was implemented in a finite state machine design, this design progresses through the states and increments the address according to the mode (Even or Odd) currently being tested. Delay cycles are added to counteract the delay in reading from a ROM, and allows for the read values to properly index, which is also how the expected_address was calculated. As the read_address is counting down, the expected_address follows read_address + 4 (shown in code snippet Figure 2).

```
assign BIST_expected_data[15:0] = BIST_address[15:0]+16'd4;
```

Figure 2

The starting address was manipulated to start from 0 (even) or 1 (odd) for writing functionality, depending on if even or odd was required to be implemented. For reading, the address value was set to either 3FFFE (even) or 3FFFF (odd), and then decremented through.