COMS31700: Design Verification - Calculator Design; Bug Report

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1. The port out_data2 outputs 0 for any input.
2. Port 4 does not respond to input - no output for out_resp4 or out_data4.
3. Underflow for subtraction responds with a 2 instead of 1 response code.
4. Overflow for addition responds with a 2 instead of 1 response code.
5. Invalid commands respond with response code 2 instead of 1.
6. Invalid commands respond with response code 2 instead of 1.
7. Right or left shift by 0 will output 0 as data.
8. Addition outputs 16 less if a 1 in the 5th position but not 6th.
9. Addition outputs 16 more if a 1 in the 6th position but not 5th.
10. A right shift by 1 will result in no operation.
11. Under left shift, a bit in the 5th position outputs wrong data. It will cause the output data to be more than correct answer by 2 to the power of the sum of the input data modules 32. Bits above the 5th will cause the output to be that number multiplied by 458753 more than it should.
12. Right shift on port 1 with an operator of bits below and above the 5th will only shift by the number modules 32.
13. Priority
14. Reset does not clear the output data of the ports.