Rochester Institute of Technology

EE381 — Electronics I Technical Memorandum

From: Joshua Wilkins

Partner: None

Date: Performed: 04-24-2015; Due: 05-01-2015

Subject: Laboratory #5: Two-Stage CMOS Op-Amp

Abstract

This Laboratory assignment comprised of the computational, simulational, and constructional analyses of a two stage CMOS operational amplifier. The first stage comprised of an actively loaded differential pair, the second stage comprised of an actively loaded PMOS common source amplifier. From this circuit, the general characteristics of a CMOS amplifiers was extracted and verified, including each stage gain, as well as the overall gain. The lab itself consisted of three different portions; the first tested the functionality and correctness of the op-amp, the second tested the gains at each stage, and the third tested the effect of the overall gain of the circuit. The results of this lab assignment confirm the theoretical and simulational analysis behind the experiment.

Theory

Multi-stage amplifiers can be generically implemented in a discrete amount of stages in which the gains of each stage are compounded regardless of the composition of the stage. This means that each individual stage could be either BJT-based or MOS-based and they could be single-transistor stages, such as CS or CG amplifiers, or compound-transistor stages, such as a differential or cascade amplifier. These stages can be any combination of amplifiers (generic) and the output voltage is still a combination of the gains of the individual stages irrespective of a stages composition (See Figure I below).

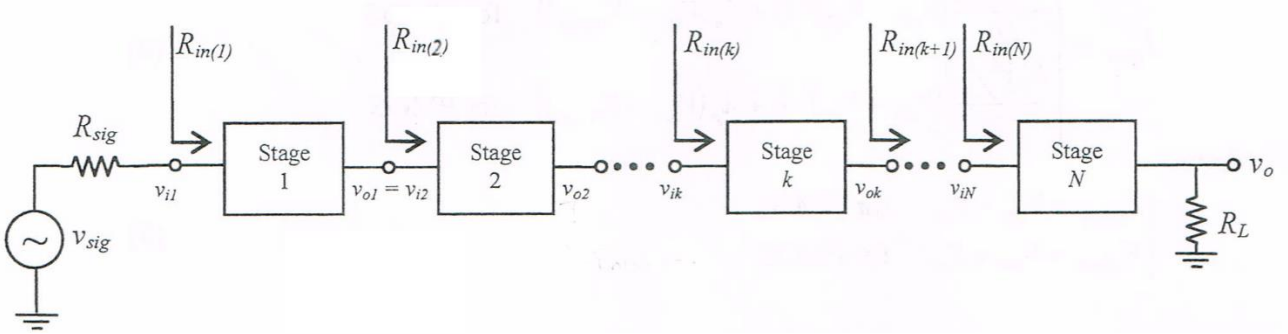

Figure I: Generic Multistage Amplifier

It should be noted that the load resistance on a particular stage is the input resistance of the next stage. In effect, the gains are dependent on the type of amplifier used in a particular stage and the input resistance of the following stage. By calculating the gain of a particular stage, denoted $A_{v(k)}$, the overall gain of the multistage op-amp is calculated as the product of each individual stages' gain:

$$A_{v(k)} \equiv \frac{V_o}{V_{i1}} = \prod_{k=1}^{N} A_{v(k)} \tag{1}$$

When the signal source itself has an associated resistance, R_{sig}, the overall gain is given by adding a factor equivalent to the voltage division that occurs between R_{sig} and $R_{in(1)}$:

$$G_v \equiv \frac{V_o}{V_{sig}} = \frac{R_{in(1)}}{R_{in(1)}+R_{sig}} \prod_{k=1}^{N} A_{v(k)}$$

The small signal output resistance for a MOSFET operating in the saturation region is given by:

$$r_0 = \frac{1}{|\lambda| I_D} \tag{2}$$

Where λ is a technology dependent parameter and can be found by measuring a the output resistance at a given bias point:

$$\lambda = \frac{g_o}{I_D} \tag{3}$$

When calculating the gain of a multistage CMOS op-amp, channel length modulation should be accounted for as the magnitude of the drain current in a MOSFET increases above its first order approximation. Thus, accounting for channel length modulation the drain current is given by:

$$i_D = \frac{1}{2} k(|V_{GS}| - |V_t|)^2 \left(1 + \lambda(|V_{DS}| - |V_{DSsat}|)\right) \tag{4}$$

Where the saturated point of V_{DS} is given by:

$$|V_{DSsat}| = |V_{GS}| - |V_t| \tag{5}$$

The analyzed circuit in this laboratory assignment, shown in Figure II below, is comprised of two stages in an op-amp. The transistors along the bottom provide the bias current for the two amplifying stages. Stage 1, given by transistors $M_1 - M_4$ form a differential amplifier while M_7 is a common source amplifier. The resistors, R_{D7} and R_{D8} can be used to center the DC output voltage to zero. The resistor, R, was calculated below to design the op-amp to have an overall small signal gain of at least 240 V/V.

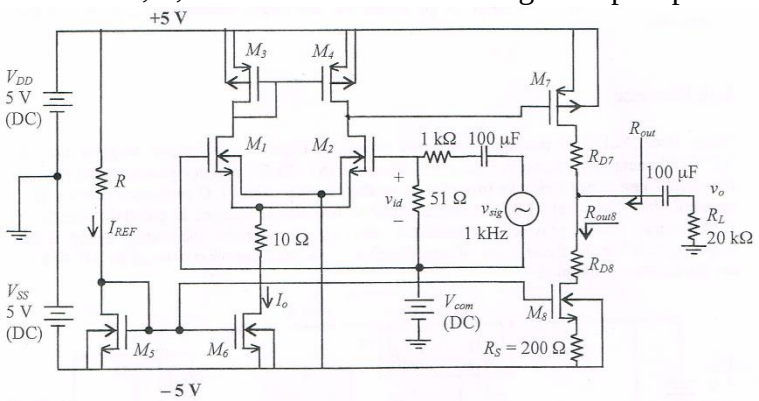

Figure II: Two Stage CMOS amplifier

Results – Theoretical

In the initial design, R_{D7} and R_{D8} were neglected in order to make the design easier. The idea was to get the overall small signal gain in terms of the reference current I_{ref}. This allows for the resistor value R to be calculated. These calculations were done by analyzing each stage of the CMOS amplifier and calculating each stages gain in terms of the reference current.

The following device parameters were given:

$|V_{to}| = .7V$, $k_n' = 25\mu A/V^2$, $k_p' = 10\mu A/V^2$, and $\frac{W}{L} = 100{:}\,1$.

An output conductance of $200\mu S$ for the NMOS devices and an output conductance of $500\mu S$ for the PMOS devices at a bias current of $I_D = 10mA$.

The channel length modulation parameters can be determined from the output conductance as seen in equation 3:

$$\lambda_n = \frac{g_o}{I_D} = \frac{200\mu S}{10\text{mA}} = .02V^{-1} \qquad \lambda_p = \frac{g_o}{I_D} = \frac{500\mu S}{10\text{mA}} = .05V^{-1}$$

Now that the channel length modulation factor has been found, the gains of the two stages can be found independently:

$$A_{v(1)} = -g_{m2}(r_{o2}||r_{o4}||R_L) \text{ where } R_L = R_{in(2)} = \infty$$

Since the first stage is a differential amplifier, the current through each of the transistors is only half of the reference current. Applying equation 2:

$$r_{02} = \frac{1}{\lambda_n {}^{I_{ref}}/_2} = \frac{2}{.02I_{ref}} = \frac{100}{I_{ref}} \qquad r_{04} = \frac{1}{\lambda_p {}^{I_{ref}}/_2} = \frac{2}{.05I_{ref}} = \frac{40}{ref}$$

The trans-conductance parameter is also related to the current through the transistor given by:

$$g_{m2} = \sqrt{2k_n' \frac{W}{L} \frac{I_{ref}}{2}} = \sqrt{25\mu A * 100 * I_{ref}} = .05\sqrt{I_{ref}}$$

It follows that the gain of stage 1 is given by:

$$A_{v(1)} = -.05\sqrt{I_{ref}} \left(\frac{100}{I_{ref}} \,||\, \frac{40}{I_{ref}} \right) = \frac{-10}{7\sqrt{I_{ref}}}$$

Since the second stage is composed of a common source amplifier, the gain of stage 2 is given by:

$$A_{v(2)} = -g_{m7}(r_{o7}||(r_{o8} + R_s)||R_L)$$

It can be assumed that $r_{o8} \gg R_s$ in this instance making the gain approximately:

$$A_{v(2)} \approx -g_{m7}(r_{o7}||r_{o8}||R_L)$$

The second stage is also related I_{ref} by a factor of ½. Thus the small signal output resistances of M_7 and M_8 are:

$$r_{08} = \frac{1}{\lambda_n {I_{ref}}/_2} = \frac{2}{.02I_{ref}} = \frac{100}{I_{ref}} \qquad r_{07} = \frac{1}{\lambda_p {I_{ref}}/_2} = \frac{2}{.05I_{ref}} = \frac{40}{I_{ref}}$$

Calculating the small signal output resistances in parallel gives:

$$r_{o7}||r_{o8} = \frac{100}{I_{ref}}||\frac{40}{I_{ref}} = \frac{200}{7I_{ref}}$$

Putting the result in parallel with the load resistance gives:

$$r_{o7}||r_{o8}||R_L = \frac{200}{7I_{ref}}||20k = \frac{20k}{700I_{ref}+1}$$

The trans-conductance parameter is once again related to the current through the transistor given by:

$$g_{m7} = \sqrt{2k_p'\frac{W}{L}\frac{I_{ref}}{2}} = \sqrt{10\mu A * 100 * I_{ref}} = \sqrt{.001I_{ref}}$$

It follows that the gain of stage 2 is given by:

$$A_{v(2)} = -\sqrt{.001I_{ref}}\left(\frac{20k}{700I_{ref}+1}\right) = \frac{-20k\sqrt{.001I_{ref}}}{700I_{ref}+1}$$

The overall small signal gain is then equal to the product of the first two gains as seen in equation 1:

$$A_v = A_{v(1)}A_{v(2)} = \frac{20k\sqrt{.001I_{ref}}}{700I_{ref}+1} * \frac{10}{7\sqrt{I_{ref}}} = \frac{200k\sqrt{.001}}{4900I_{ref}+7}$$

With the given design constraint that $A_v \geq 240V/V$, the maximum reference current I_{ref} can be found:

$$\frac{200k\sqrt{.001}}{4900I_{ref}+7} \geq 240 \rightarrow\rightarrow I_{ref} \leq 3.949mA$$

The assumption made earlier, $r_{o8} \gg R_s$, can be verified:

$$r_{o7}||(r_{o8}+R_s) = \frac{100}{I_{ref}}||\left(\frac{40}{I_{ref}}+200\right) = \frac{100}{3.95m}||\left(\frac{40}{3.95m}+200\right) = 7251.34\Omega$$

$$7251.34\Omega||20\text{k}\Omega = 5321.82\Omega$$

$$A_v = A_{v(1)}A_{v(2)} = \frac{10}{7\sqrt{I_{ref}}} * 5321.82 * \sqrt{.001I_{ref}} = 240.415V/V$$

$$100 * \frac{240.415-240}{240} = .173\%$$

Thus the assumption was valid as it only incurred .17% error.

The resistor value, R, must now be calculated to create this reference current which can be done with equation 4:

$$I_{ref} \geq \frac{1}{2} * 25\mu * 100(V_{G5} + 5 - .7)^2\big(1 + .02(.7)\big)$$

$$3.949m \geq 1.2675m(V_{G5} + 4.3)^2$$

$$-6.065V \leq V_{G5} \leq -2.5349V$$

Using Ohm's law, the value of resistor R can be calculated from the gate voltage of M_5:

$$\frac{5-(-2.5349)}{R} \leq 3.949m \;\; \rightarrow\rightarrow \;\; R \geq 1908\Omega$$

Using the closest standard 5% resistor value, $R = 2000\Omega$. Re-calculating the gain with the standard resistor value:

$$\frac{5-V_{G5}}{2000} = \frac{1}{2} * 25\mu * 100(V_{G5} + 4.3)^2\big(1 + .02(.7)\big) \;\; \rightarrow\rightarrow \;\; V_{G5} = -2.5717V$$

$$I_{ref} = \frac{5-(-2.57174)}{2000} \;\; \rightarrow\rightarrow \;\; I_{ref} = 3.786mA$$

$$A_v = \frac{200k\sqrt{.001}}{4900(3.786m)+7} \;\; \rightarrow\rightarrow \;\; A_v = \frac{247.5V}{V}$$

To find the operating range and, if needed, the addition of a supply voltage, V_{com} to bias the gates, the voltage range for each transistor should be considered:

Transistors M3 and M5 – Since the drain and gate terminals are connected, the device will always be in saturation if $V_{Ds} \geq V_{GS} - V_t \rightarrow V_{GS} \geq V_t$

Transistors M4 and M6 –These transistors have their drain terminals and gate terminals approximately equal meaning the two devices will almost always be in saturation.

Transistor M7 – Since the drain voltage, $V_{D8} \approx 0$ and the source voltage $V_{S8} = -5V$ the transistor will almost always be in saturation.

Transistor M8 –This transistor will be in saturation because $V_{D7} > V_{D9}$.

Transistors M1 and M2 are then the only two transistors that really depend on the bias voltage provided by V_{com}. With M6 on the edge of saturation, $V_{S1} = V_{S2} \approx -3.5V \;\; \rightarrow\rightarrow \;\; V_{g1} = V_{g2} = -1.25V \;\; \rightarrow\rightarrow \;\; V_{com} \geq -1.25V$.

Next the values of R_{D7} and R_{D8} were considered. Using PSPICE, a DC sweep was first made without the use of either resistor, varying the value of V_{com}, shown in Figure III below. The optimum value was seen to be $V_{com} = .2V$ although the transistors are seen to be in saturation at a value of $V_{com} \approx -1V$.

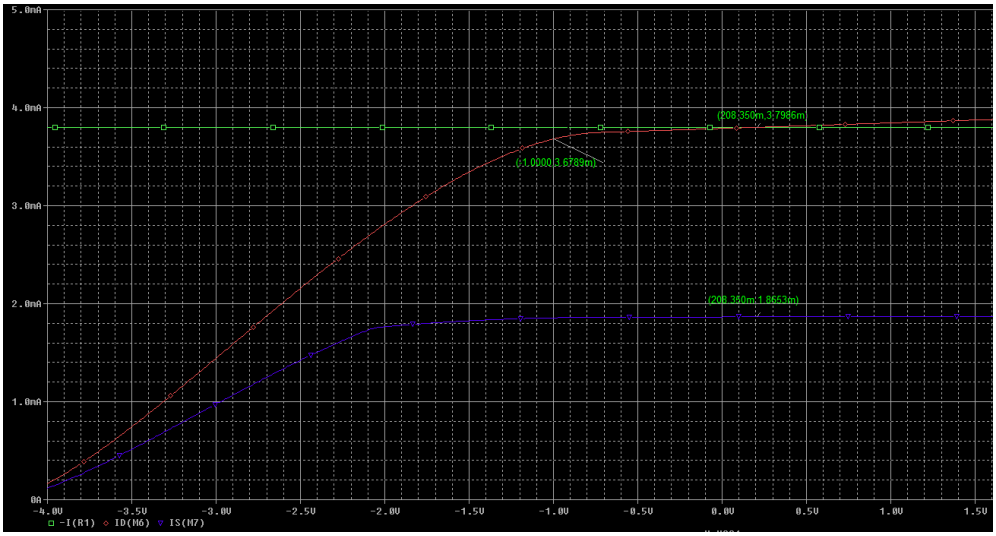

Figure III: Finding best value of V_{com} with PSPICE

Next, by parameterizing a resistor and using either of R_{D7} or R_{D8} at a time and keeping V_{com} at .2V, the best value of the two resistors was found, shown in figures IV and V below.

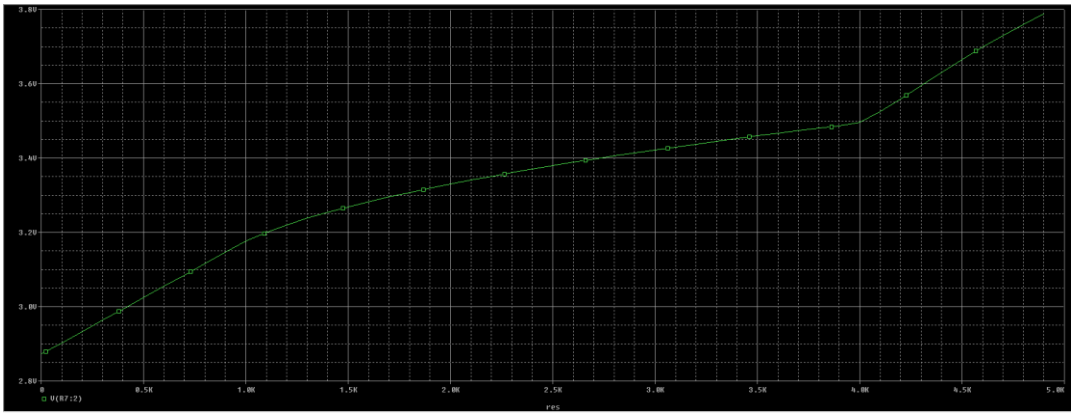

Figure IV: Finding best value of R_{D8} with PSPICE

As can be seen by the graph above (Figure IV), the best value of R_{D8} would be not to use it. This is due to the fact that as the resistance increases the value of V_o increases. Since the current value of V_o without any resistance at R_{D8}, is already positive, the R_{D8} Resistor would worsen the output DC voltage.

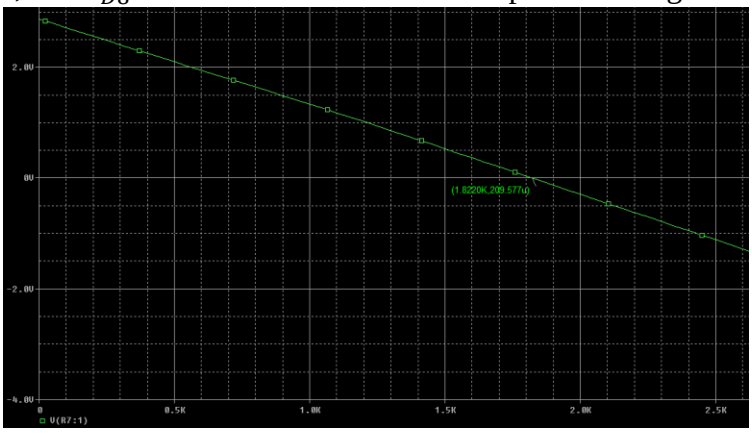

Figure V: Finding best value of R_{D7} with PSPICE

As can be seen by this graph (Figure V), the best value of R_{D7} would approximately 1822Ω. This is because at that resistance value, the DC output voltage, V_o is closest to zero. Using a standard 5% resistor value, R_{D7} should be set to 1800Ω.

Accounting for this new resistor value, the overall small signal gain increases slightly and is calculated below:

$$A_{v(1)} \text{ remains the same, } A_{v(1)} = -23.217V/V$$

$$A_{v(2)} = -g_{m7}((r_{o7} + R_{D7})||(r_{o8} + R_s)||R_L) = -11.551V/V$$

$$A_v = A_{v(1)}A_{v(2)} = 23.217 * 11.551 = 268.2V/V$$

One last thing that needs to be accounted for is the total output resistance of the op amp and the output resistance of transistor M8. These calculations are shown below:

$$R_{o8} = r_{o8} + R_{D8} + R_s = \frac{1}{\lambda_n \frac{I_{ref}}{2}} = \frac{2}{.02(3.786\text{m})} = 26413\Omega$$

$$R_{o8} = R_{o8}||(R_{D7} + r_{07}) = 8422.4\Omega$$

Results – Simulated

Following a similar approach to that shown above, Figure VI below confirms the current source design and displays the correct operating conditions of the device. From this figure, the current is shown to be approximately that of which was calculated in the theoretical analysis.

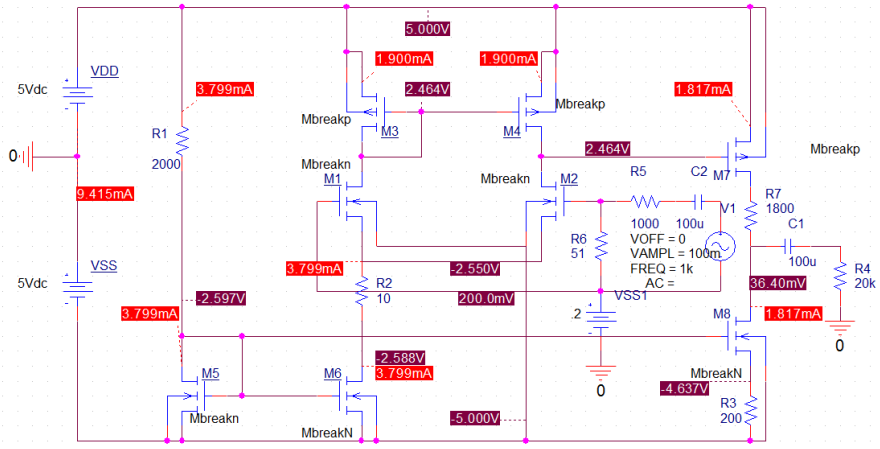

Figure VI: Standard operating Configuration Confirmation

To check the gain of the device and determine an approximate value for the best current and therefore best value of the resistor R, a simulation was run testing the gain at both stages as well as the overall gain, shown in figure VII below.

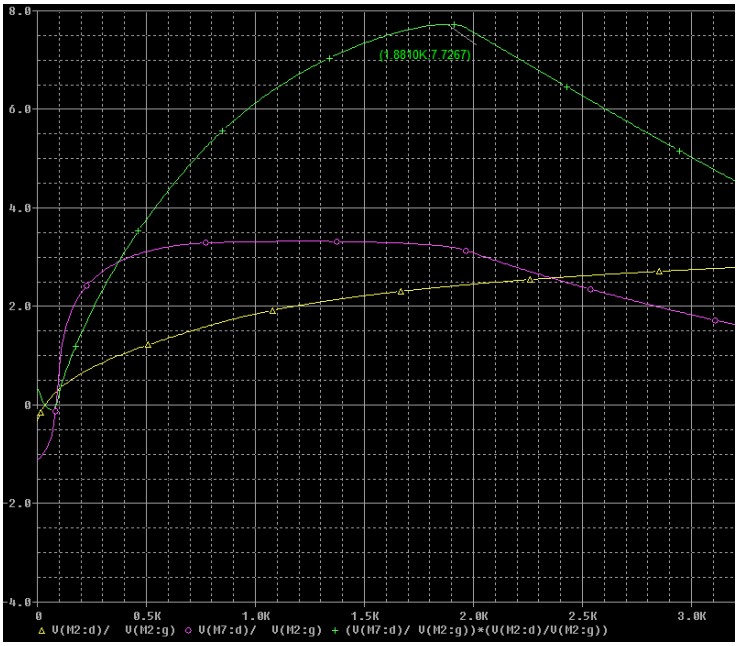

Figure VII: Confirmation of R Value by Qualitative Gain Simulation

As can be seen by the graph above, figure VII, the best value of the resistor R is approximately 1881Ω, where the green line represents the overall small signal gain and the yellow and pink lines represent the gains of the two stages.

Figures III, IV, and V above, were also a part of the simulational portion of the lab and were used to determine the best values of V_{com}, R_{D8}, and R_{D7} respectively.

The actual values of the gains were then simulated as shown below:

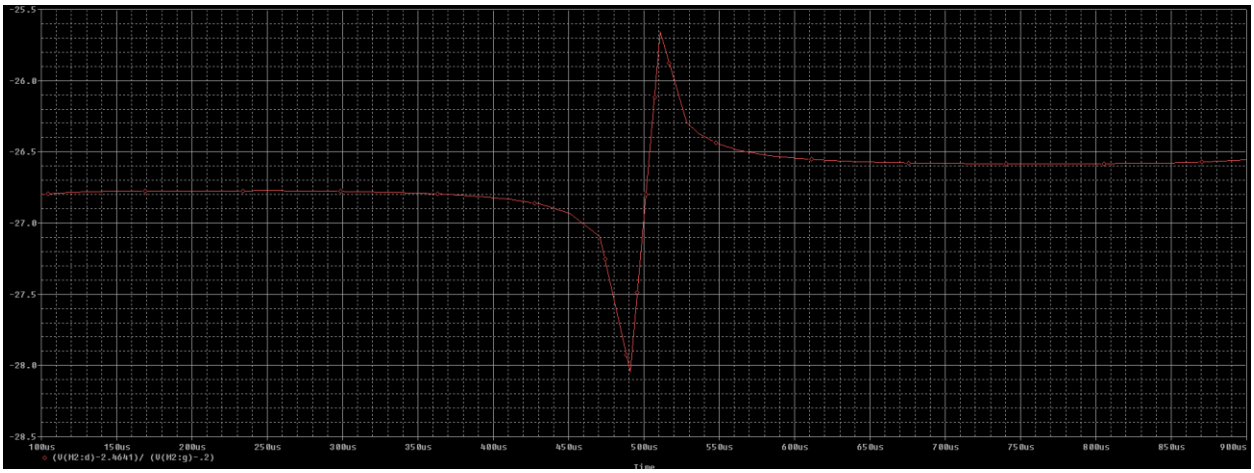

Figure VIII: $A_{v(1)}$ Quantitative Gain Simulation

From the graph above, Figure VIII, the gain of the first stage of the op-amp is seen to be approximately -26.7V/V.

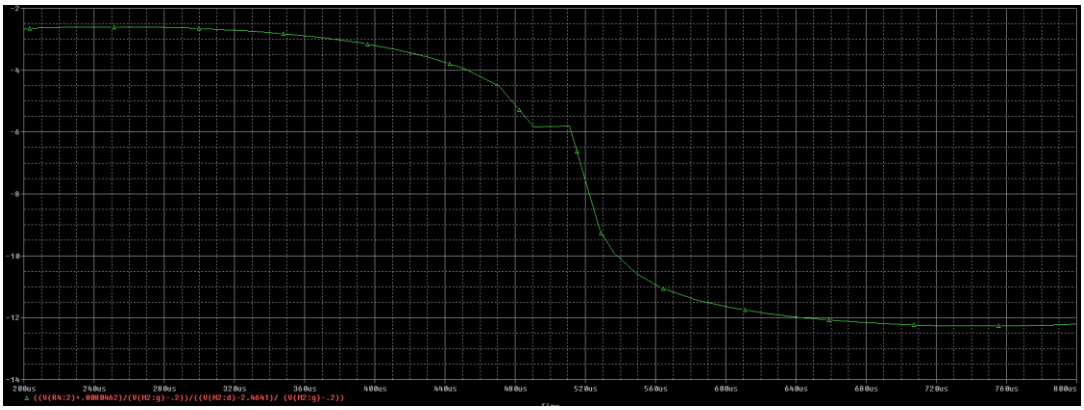

Figure IX: $A_{v(2)}$ Quantitative Gain Simulation

From the graph above, Figure IX, the gain of the second stage of the op-amp is seen to be approximately -12.2V/V. The gain of the second state saturates at a voltage of about -3V however, so the actual gain can only be considered when the input, v_{id} is negative.

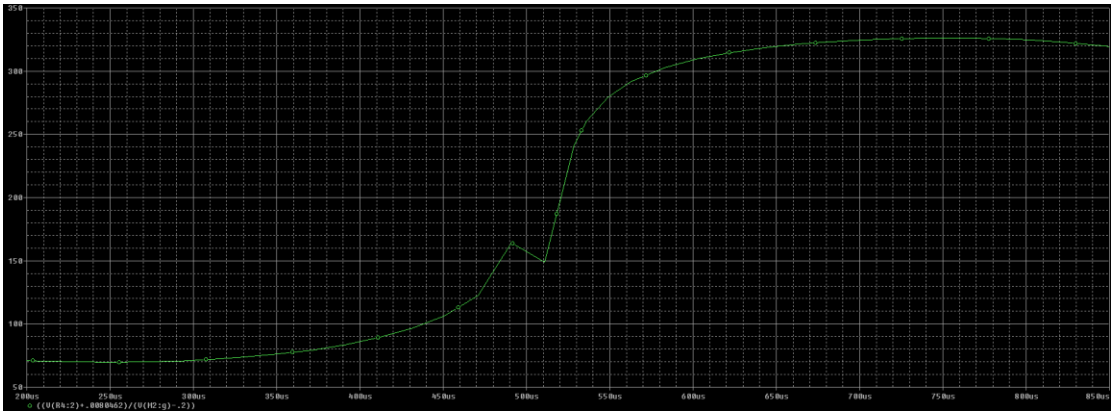

Figure X: A_v Quantitative Gain Simulation

From the graph above, Figure X, the overall small signal gain of the op-amp is seen to be approximately 330V/V. The gain of the second stage saturates at a voltage of about -3V however, so the actual gain can only be considered when the input, v_{id} is negative (the right portion of Figure X).

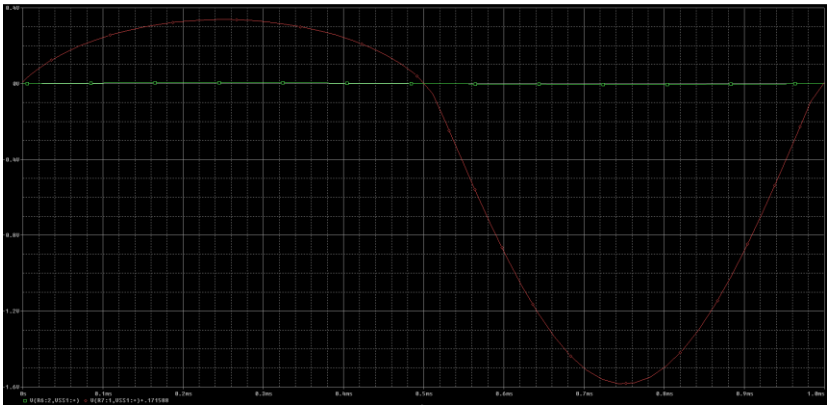

Figure XI: A_v Quantitative Gain Simulation

The output of the graph was also simulated in terms of voltage, not gain, as shown above in figure XI. From this graph, the gain can be determined by dividing the output voltage by the input voltage, v_{id}. This was calculated to be approximately 284V/V, accounting for a small offset at the output voltage.

Results – Experimental

Once again, following the same approach shown above, the circuits were constructed and the results shown below. First the design of the circuit was tested to confirm the operating conditions of the device and the reference current through the device measured to be 4.01mA. The voltage drop,v_{id}, across the 51Ω resistor was then verified to be approximately 5mV peak to peak. Then the common-mode voltage, V_{com}, was verified by increasing it until an undistorted sin wave at the output node was seen and this occurred at approximately $V_{com} = -1V$, but to keep consistent a value of .2V was used for V_{com}.

Next the DC value of the output voltage was measured and a resistor, R_{D7}, was added to bring the DC value of the output voltage down to zero. The value of R_{D7} that accomplished this was 1900Ω, and the ouput voltage at this resistance value was $V_o = .03V$. This is consistent with the simulational portion of the lab because R_{D7} was simulated to be 1800Ω.

The gains of the hardware portion are shown below:

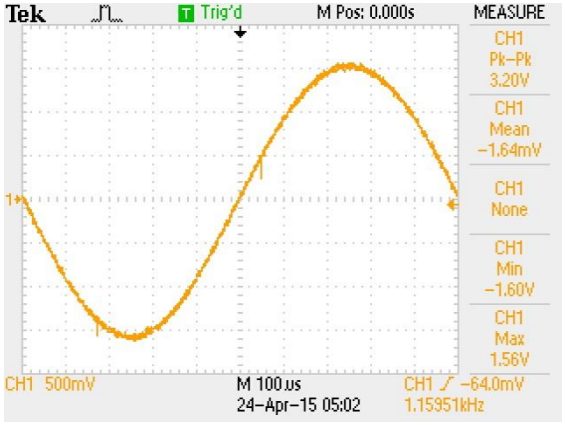

Figure XII: $A_{v(1)}$ Voltage – the Voltage seen at the drain of M2

The output of the graph is also in terms of voltage, not gain, as shown above in figure XII. From this graph, the gain can be determined by dividing the voltage by the input voltage, v_{id}. This was calculated to be approximately 16.5V/V.

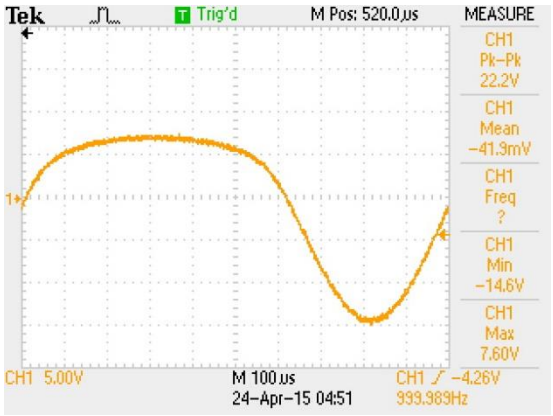

Figure XIII: A_v Voltage – the Output Voltage of the Op-Amp

The output of this graph is also in terms of voltage, not gain, as shown above in figure XIII. From this graph, the gain can be determined by dividing the voltage by the input voltage, v_{id}. This was calculated to be approximately 260V/V, accounting for a small offset at the output voltage.

The results from each portion of the lab have been tabulated in the table below:

	$A_{v(1)}$ (V/V)	$A_{v(2)}$ (V/V)	A_v (V/V)
Theoretical	-23.217	-11.551	268.2
Simulated	-26.7	-12.2	284
Experimental	-16.5	------	260

Table I: Tabulated Results of Stage and Overall small Signal Gain

Discussion

Making the logical assumption that the simulated values are the most correct due to the nature of the manufacturing process and the assumptions made in the theoretical work, it is shown that all of the results are mostly correct. The theoretical and simulated results match the closest, as expected, because these results are less prone to error. Furthermore, the experimental data should have been examined in finer detail, and not high level data. This means that in order to see the connections between the input voltage, in either the differential mode or common mode configurations, the output voltage should have had a smaller time increment. Despite this, the overall behavior of this device matches what was expected, but in a more generalized manner.

The results above were restricted to a certain input voltage range. This is because at a certain point, some or all of the transistors will go out of the saturation region, capping the output voltage. Thus if the input voltage range was too large or too small, the output would no longer be linear; it would still increase the output voltage, but exponentially decrement the amount by which the output voltage increases.

In addition, the above calculations and experimental results indicate some error in the process. Some sources of error may include old equipment, or the lack of data points in some instances. Furthermore, the lab was restricted to standardized resistor values, limiting the accurateness of the lab further. These sources of error in combination with the uniqueness of the construction of each independent transistor, resulted in some of the inconsistencies of this lab, but overall the data formed the general properties of this multistage op-amp.

Conclusion

From this lab experiment, the general properties of a multistage op-amp were extrapolated. These properties included the gains at each stage as well as the region in which the transistors remained in saturation. It was discovered that this device has a linear region of amplification between the extrema of the output voltages. From this result, it can be deduced that the input signal amplitude should be limited. The general properties of this device matched in every portion of the lab, indicating the correct setup and execution of the lab. Unfortunately the results of the experiment were not exact, but could be improved with further examination.