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Samsung SD & MicroSD Card product family

SDA 3.0 specification compliant-Up to UHS-I mode

datasheet

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1.0 PRODUCT LINE-UP

[Table 1] : PRODUCT LINE-UP

Model Number	Capacities	Remarks
MMBTR04GUDCH-xMLxx	4GB	microSD Card (x : Refer to the Ordering Information)
MMCTR08GUBCH-xMLxx	8GB	
MMCTR16GUBCJ-xMLxx	16GB	

2.0 INTRODUCTION

2.1 General Description

The microSD is a memory card that is specifically designed to meet the security, capacity, performance and enviroment requirements inherent in newly emerging audio and video consumer electronic devices. The microSD will include a copyright protection mechanism that complies with the security of the SDMI standard and will be faster and capable for higher Memory capacity. The microSD security system uses mutual authentication and a "new ciper algorithm" to protect from illegal usage of the card content. A none secured access to the user's own content is also available.
The microSD communication is based on an advanced 9 and 8-pin interface (SD:9pin, microSD:8pin)) designed to operate in at maximum operating frequency of 208MHz and 2.7V ~ 3.6V operating voltage range with 2 Type signaling(1.8V & 3.3V). More detail informations on the interface, and mechanical description is defined as a part of this specification.
UHS-I and High Speed mode Limited on this Specification.

2.2 System Features

- Compliant with SD Memory Card Specifications PHYSICAL LAYER SPECIFICATION Version 3.0
  - Based on SD Memory Card Specification 3.0 compatible Test Device.
  - Bus speed support up to SDR104(1.8V signaling, frequency up to 208MHz)
  - Bus speed support High Speed Mode for backward compatible(3.3V signaling, frequency up to 50MHz)

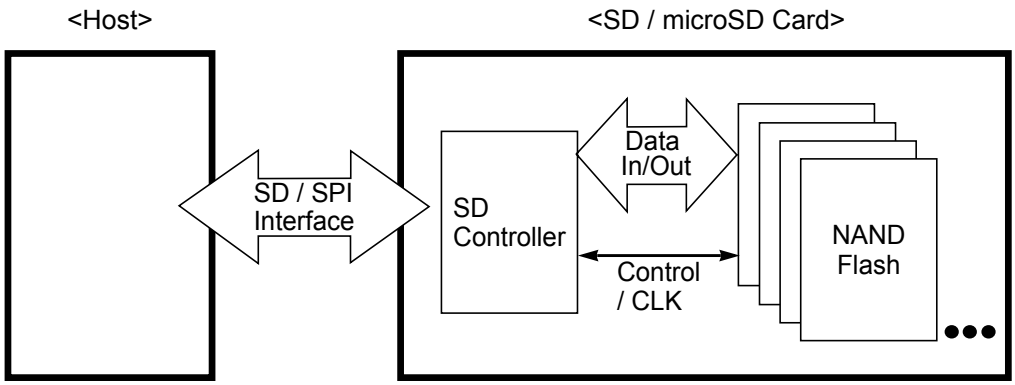
- Targeted for portable and stationary applications
- Memory capacity:
  1) Standard Capacity SD Memory Card(SDSC) : Up to and including 2 GB
  2) High Capacity SD Memory Card(SDHC) : More than 2GB and up to and including 32GB
  3) Extended Capacity SD Memory Card(SDXC) : More than 32GB and up to and including 2TB

- Voltage range:
  - High Voltage SD Memory Card – Operating voltage range: 2.7-3.6 V

- Designed for read-only and read/write cards.
- Bus Speed Mode (using 4 parallel data lines)
  1) Default mode: Variable clock rate 0 - 25 MHz, up to 12.5 MB/sec interface speed
  2) High-Speed mode: Variable clock rate 0 - 50 MHz, up to 25 MB/sec interface speed
  3) SDR12: 1.8V signaling, Frequency up to 25 MHz, up to 12.5MB/sec
  4) SDR25: 1.8V signaling, Frequency up to 50 MHz, up to 25MB/sec
  5) SDR50: 1.8V signaling, Frequency up to 100 MHz, up to 50MB/sec
  6) SDR104: 1.8V signaling, Frequency up to 208 MHz, up to 104MB/sec
  7) DDR50: 1.8V signaling, Frequency up to 50 MHz, sampled on both clock edges, up to 50MB/sec

- Switch function command supports Bus Speed Modeand future functions
- Correction of memory field errors
- Card removal during read operation will never harm the content
- Content Protection Mechanism - Complies with highest security of SDMI standard.
- Password Protection of cards (CMD42 - LOCK_UNLOCK)
- Write Protect feature using mechanical switch
- Built-in write protection features (permanent and temporary)
- Card Detection (Insertion/Removal)
- Application specific commands
- Comfortable erase mechanism
- Weight : SD Card Max. 2.5g / microSD Card Max. 1g

2.3 System Block Diagram



3.0 PRODUCT SPECIFICATION

3.1 Current Consumption

This information table below provides current consumption of Samsung microSD Card. Current consumption is measured by averaging over 1 second.
[Table 2] : Current Consumption Table

Mode	Max. Interface Frequency	Operations	Max.
Default Mode	25Mhz	Read	100mA
		Write	
High Speed Mode	50Mhz	Read	200mA
		Write	
SDR 12	25Mhz	Read	100mA
		Write	
SDR 25	50Mhz	Read	200mA
		Write	
DDR 50	50Mhz	Read	400mA
		Write	
SDR50	100Mhz	Read	400mA
		Write	
SDR 104	208Mhz	Read	400mA
		Write	

NOTE:
Current consumption on each device can be varied by NAND Flash, . of chips, test conditions and Etc. For specific information, refer to Samsung microSD Card Qualification report.

3.2 System Performance

3.2.1 Product Performance

Product Performance is based on TestMetrix compliance Tool. Note that the performance measured by TestMetrix does not represent real performance in various circumstances.

[Table 3] : Performance Information

Product Number	Write Performance (MB/s)	Read Performance (MB/s)
MMBTR04GUDCH-xMLxx	7	90
MMCTR08GUBCH-xMLxx		
MMCTR16GUBCJ-xMLxx	12	

3.2.2 Read, Write Timeout Error Conditions

SEC microSD Card shall complete the command within the time period defined as follows or give up and return and error message. If the host does not get any response with the given timeout it should assume that the card is not going to respond and try recover. For more information, refer to Section 4.6 of the SDA Physical Layer Specification, Version 3.0

[Table 4] : Timeout Error Conditions

Timing	Max. Value
Block Read Access Time	100ms
Block Write Access Time	250ms(SDSC/SDHC), 500ms(SDXC)
Initialization Time out(ACMD 41)[1]	1s

NOTE:
1) The host shall set ACMD41 timeout more than 1 second to abort repeat of issuing ACMD41 when the card does not indicate ready. The timeout count starts from the first ACMD41 which is set voltage window in the argument.

3.3 SD Mode Card Registers

•Six registers are defined within the card interface: OCR, CID, CSD, RCA, DSR and SCR. These can be accessed only by corresponding commands. The OCR, CID, CSD and SCR registers carry the card/content specific information, while the RCA and DSR registers are configuration registers storing actual configuration parameters.**OCR Register** The 32-bit operation conditions register stores the VDD voltage profile of the card. Additionally, this register includes status information bits.
See Section 5.1 of the SDA Physical Layer Specification, Version 3.00 for more information.

[Table 5] : OCR Register Definition

OCR bit	VDD Voltage Window	OCR Value
0-3	reserved	0
4	reserved	0
5	reserved	0
6	reserved	0
7	reserved for Low Voltage Range	0
8	reserved	0
9	reserved	0
10	reserved	0
11	reserved	0
12	reserved	0
13	reserved	0
14	reserved	0
15	2.7 - 2.8	1
16	2.8 - 2.9	1
17	2.9 - 3.0	1
18	3.0 - 3.1	1
19	3.1 - 3.2	1
20	3.2 - 3.3	1
21	3.3 - 3.4	1
22	3.4 - 3.5	1
23	3.5 - 3.6	1
24[3]	Switching to 1.8V Accepted (S18A)	0 or 1
24 - 29	reserved	0
30	Card Capacity Staus(CCS)[1]	-
31	Card power up status bit(busy)[2]	-

NOTE:
1) This bit is valid only when the card power up status bit is set.
2) This bit is set to LOW if the card has not finished the power up routine.
3) S18A = 0 means voltage switch is not allowed .
S18A = 1 means Votage switch is allowed and host issue CMD to invoke voltage switch sequence.

3.3.1 CID Register

The Card IDentification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual Read/Write (RW) card shall have an unique identification number. It is programmed during manufacturing and cannot be changed by card hosts. The structure of the CID register is defined in the following paragraphs:

[Table 6] : CID Register Fields

Name	Field	Type	Width	CID Value		
				4GB	8GB	16GB
Manufacturer ID	MID	Binary	8	CID Register Value can be provided by Customer Request		
OEM/Application ID	OID	ASCII	16			
Product name	PNM	ASCII	40			
Product revision	PRV	BCD	8			
Product serial number	PSN	Binary	32			
Reserved	-	-	4			
Manufacturing date	MDT	BCD	12			
CRC7 checksum	CRC	Binary	7			
not used, always '1'	-	-	1			

3.3.2 CSD Register (CSD Version 1.0)

The Card-Specific Data register provides information on how to access the card contents. The CSD defines the data format, error correction type, maximum data access time, data transfer speed, whether the DSR register can be used etc. The programmable part of the register (entries marked by W or E, see below) can be changed by CMD27. The type of the entries in the table below is coded as follows: R = readable, W(1) = writable once, W=multiple writable.

[Table 7] : The CSD Register Fields (CSD Version 1.0)

Name	Field	Width	Cell Type	CSD-slice	CSD Value		
					4GB	8GB	16GB
CSD structure	CSD_STRUCTURE	2	R	[127:126]	Version 1.0		
Reserved	-	6	R	[125:120]	-		
Data read access-time 1	TAAC	8	R	[119:112]	N/A		
Data read access-time 2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]	N/A		
Max. Data transfer rate	TRAN_SPEED	8	R	[103:96]	N/A		
Card command classes	CCC	12	R	[95:84]	N/A		
Max. read data block length	READ_BL_LEN	4	R	[83:80]	N/A		
Partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]	N/A		
Write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]	N/A		
Read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]	N/A		
DSR implemented	DSR_IMP	1	R	[76:76]	N/A		
Reserved	-	2	R	[75:74]	-		
Device size	C_SIZE	12	R	[73:62]	N/A		
Max. read current @ V_{DD} min	VDD_R_CURR_MIN	3	R	[61:59]	N/A		
Max. read current @ V_{DD} max	VDD_R_CURR_MAX	3	R	[58:56]	N/A		
Max. write current @ V_{DD} min	VDD_W_CURR_MIN	3	R	[55:53]	N/A		
Max. write current @ V_{DD} max	VDD_W_CURR_MAX	3	R	[52:50]	N/A		
Device size multiplier	C_SIZE_MULT	3	R	[49:47]	N/A		
Erase single block enable	ERASE_BLK_EN	1	R	[46:46]	N/A		
Erase sector size	SECTOR_SIZE	7	R	[45:39]	N/A		
Write protect group size	WP_GRP_SIZE	7	R	[38:32]	N/A		
Write protect group enable	WP_GRP_ENABLE	1	R	[31:31]	N/A		
Reserved (Do Not Use)		2	R	[30:29]	-		
Write speed factor	R2W_FACTOR	3	R	[28:26]	N/A		
Max. write data block length	WRITE_BL_LEN	4	R	[25:22]	N/A		
Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	[21:21]	N/A		
Reserved	-	5	R	[20:16]	-		
File format group	FILE_FORMAT_GRP	1	R/W(1)	[15:15]	N/A		
Copy flag (OTP)	COPY	1	R/W(1)	[14:14]	N/A		
Permanent write protection	PERM_WRITE_PROTECT	1	R/W(1)	[13:13]	N/A		
Temporary write protection	TMP_WRITE_PROTECT	1	R/W	[12:12]	N/A		
File format	FILE_FORMAT	2	R/W(1)	[11:10]	N/A		
Reserved		2	R/W	[9:8]	-		
CRC	CRC	7	R/W	[7:1]	N/A		
Not used, always '1'	-	1	-	[0:0]	-		

3.3.3 CSD Register (CSD Version 2.0)

The following Table shows Definition of the CSD Version 2.0 for the High Capacity SD Memory Card and Extended Capacity SD Memory Card. The following sections describe the CSD fields and the relevant data types for the High Capacity SD Memory Card.

CSD Version 2.0 is applied to only the High Capacity SD Memory Card. The field name in parenthesis is set to fixed value and indicates that the host is not necessary to refer these fields. The fixed values enables host, which refers to these fields, to keep compatibility to CSD Version 1.0. The Cell Type field is coded as follows: R = readable, W(1) = writable once, W = multiple writable.

[Table 8] : The CSD Register Fields (CSD Version 2.0)

Name	Field	Width	Cell Type	CSD-slice	CSD Value		
					4GB	8GB	16GB
CSD structure	CSD_STRUCTURE	2	R	[127:126]	CSD Version 2.0		
Reserved	-	6	R	[125:120]	-		
Data read access-time	(TAAC)	8	R	[119:112]	1000.00 us		
Data read access-time in CLK cycles (NSAC*100)	(NSAC)	8	R	[111:104]	0 cycles		
Max. Data transfer rate	(TRAN_SPEED)	8	R	[103:96]	25 Mbit/s or 50 Mbit/s		
Card command classes	CCC	12	R	[95:84]	class 0 2 4 5 7 8 10		
Max. read data block length	(READ_BL_LEN)	4	R	[83:80]	512 bytes		
Partial blocks for read allowed	(READ_BL_PARTIAL)	1	R	[79:79]	0		
Write block misalignment	(WRITE_BLK_MISALIGN)	1	R	[78:78]	0		
Read block misalignment	(READ_BLK_MISALIGN)	1	R	[77:77]	0		
DSR implemented	DSR_IMP	1	R	[76:76]	0		
Reserved	-	6	R	[75:70]	-		
Device size	C_SIZE	22	R	[69:48]	7525	15053	30173
Reserved	-	1	R	[47:47]	-		
Erase single block enable	(ERASE_BLK_EN)	1	R	[46:46]	1		
Erase sector size	(SECTOR_SIZE)	7	R	[45:39]	128 blocks		
Write protect group size	(WP_GRP_SIZE)	7	R	[38:32]	1 sectors		
Write protect group enable	(WP_GRP_ENABLE)	1	R	[31:31]	0		
Reserved	-	2	R	[30:29]	-		
Write speed factor	(R2W_FACTOR)	3	R	[28:26]	4		
Max. write data block length	(WRITE_BL_LEN)	4	R	[25:22]	512 bytes		
Partial blocks for write allowed	(WRITE_BL_PARTIAL)	1	R	[21:21]	0		
Reserved	-	5	R	[20:16]	-		
File format group	(FILE_FORMAT_GRP)	1	R	[15:15]	0		
Copy flag (OTP)	COPY	1	R/W(1)	[14:14]	0		
Permanent write protection	PERM_WRITE_PROTECT	1	R/W(1)	[13:13]	0		
Temporary write protection	TMP_WRITE_PROTECT	1	R/W	[12:12]	0		
File format	(FILE_FORMAT)	2	R	[11:10]	0		
Reserved		2	R	[9:8]	-		
CRC	CRC	7	R/W	[7:1]	-		
Not used, always '1'	-	1	-	[0:0]	-		

3.3.4 RCA Register

The writable 16-bit relative card address register carries the card address that is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA register is 0x0000. The value 0x0000 is reserved to set all cards into the Stand-by State with CMD7.

3.3.5 SCR Register

In addition to the CSD register, there is another configuration register named SD CARD Configuration Register (SCR). SCR provides information on the SD Card's special features that were configured into the given card. The size of SCR register is 64bits. The register shall be set in the factory by the SD Card manufacturer. The following table describes the SCR register content.

[Table 9] : The SCR Fields

Name	Field	Width	Cell Type	SCR-slice	SCR Value		
					4GB	8GB	16GB
SCR structure	SCR_STRUCTURE	4	R	[63:60]	SCR Version 1.0		
SD Memory Card - Spec. Version	SD_SPEC	4	R	[59:56]	Version 2.00 or Version 3.0x		
data_status_after erases	DATA_STAT_AFTER_ERASE	1	R	[55:55]	0		
SD Security Support	SD_SECURITY	3	R	[54:52]	SDHC Card (Security Version 2.00)		
DAT Bus widths supported	SD_BUS_WIDTHS	4	R	[51:48]	1 bit(DAT0) + 4 bit(DAT0-3)		
Spec. Version 3.00 or Higher	SD_SPEC3	1	R	[47]	Version 3.0X or later		
Reserved		13	R	[46:34]	-		
Command Support bits	CMD_SUPPORT	14	R	[33:32]	Speed Class Control (CMD20) & Set Block Count (CMD23)		
Reserved for manufacturer usage-		32	R	[31:0]	-		

3.3.6 SD Status Register

The SD Status contains status bits that are related to the SD Memory Card proprietary features and may be used for future application specific usage. The size of the SD Status is one data block of 512bit. The content of this register is transmitted to the Host over the DAT bus along with 16bit CRC. The SD Status is sent to the host over the DAT bus if ACMD13 is sent (CMD55 followed with CMD13). ACMD13 can be sent to a card only in 'tran_state' (card is selected). SD Status structure is described in below. Unused reserved bits shall be set to 0.

[Table 10] : SD Status Register

Bits	Field	Cell Type	Data			Value		
			4GB	8GB	16GB	4GB	8GB	16GB
511:510	DATA_BUS_WIDTH	S R	0x00			1bit width or 4bit width		
509	SECURED_MODE	S R	0x00			-		
508:502	Reserved for Security Functions (Refer to Part 3 Security Specification)							
501:496	Reserved							
495:480	SD_CARD_TYPE	S R	0x0000			Regular SD RD/WR Card		
479:448	SIZE_OF_PROTECTED_AREA	S R	0x2000000	0x3000000	0x4000000	-		
447:440	SPEED_CLASS	S R	0x3		0x4	Class 6		Class 10
439:432	PERFORMANCE_MOVE	S R	0x3		0x0	3 [MB/sec]		Sequential Write (SPEC 3.0)
431:428	AU_SIZE	S R	0x9			4MB		
427:424	Reserved							
423:408	ERASE_SIZE	S R	0x8			8 AU		
407:402	ERASE_TIMEOUT	S R	0x4			4 sec		
401:400	ERASE_OFFSET	S R	0x1			1 sec		
399:396	UHS_SPEED_GRADE	S R	0x0		0x1	Less than 10MB/sec		10MB/sec and above
395 :392	UHS_AU_SIZE	S R	0x9			4 MB		
391 : 312	Reserved							
311:0	Reserved for Manufacturer							

NOTE:
- Speed Class that supports Class 10 shall not use the Pm value stored in the SD Status to calculate performance in any fragmented AU. Class 10 Performance is defined only for entirely free AUs
- In contrast with speed Class , Pm is not supported in UHS-1 card. which means Pm shall be set to '0' in SD statns of UHS-1 card.

3.4 SPI Mode Card Registers

Unlike the SD Memory card protocol (where the register contents is sent as command response),reading the contents of the CSD and CID registers in SPI mode is a simple read-block transaction. The card will respond with a standard response token followed by data block of 16 bytes suffixed with a 16-bit CRC.
The data timeout for the CSD command cannot be set to the cards TAAC since this value is stored in the card's CSD. Therefore, the standard response timeout value(N_{CR}) is used for read latency of the CSD register.

3.5 User Capacity

This information table below provides user capacity of Samsung microSD Card.
Product user density is based on SD Formatter 3.1 tool with FAT File system.
SD Formatter 3.1 software formats all SD Cards and SDHC Cards using a formatting program that complies with official SD memory card requirements.

[Table 11] : User Capacity

Product Number	File System	Tot. Sector No.	User Capacity[Byte]
MMBTR04GUDCH-xMLxx	FAT 32	7,690,240	3,937,402,880
MMCTR08GUBCH-xMLxx		15,398,912	7,884,242,944
MMCTR16GUBCJ-xMLxx		30,881,792	15,811,477,504

NOTE :
SD or SDHC Card file systems form attached with generic operating system formatting software do not comply with official SD memory card requirement and optimum performance may not be experienced

4.0 INTERFACE DESCRIPTION

4.1 microSD SD mode Bus Topology / microSD SPI Bus Topology

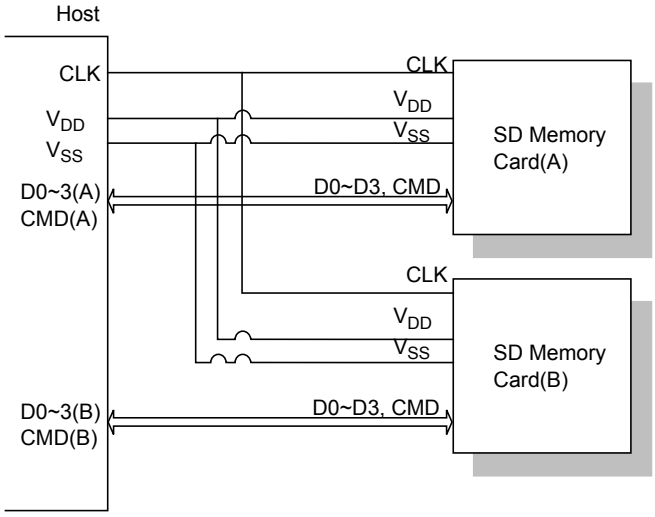


Figure 1. SD Memory Card System Bus Topology

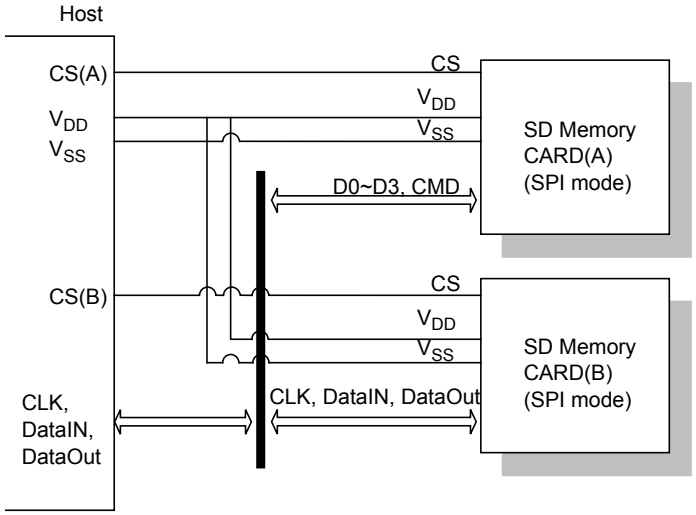


Figure 2. SD Memory Card system (SPI mode) Bus Topology

The microSD Memory Card system defines two alternative communication protocols: SD and SPI. The host system can choose either one of modes. The card detects which mode is requested by the host when the reset command is received and expects all further communication to be in the same communication mode. Common bus signals for multiple card slots are not recommended. A single SD bus should connect a single SD card. Where the host system supports a high-speed mode, a single SD bus shall be connected to a single SD card.

The microSD bus includes the following signals:

- CMD : Bidirectional Command/Response signal
- DAT0 - DAT3 : 4 Bidirectional data signals
- CLK : Host to card clock signal
- V_{DD}, V_{SS1}, V_{SS2}: Power and ground signals

The microSD Card bus has a single master (application), multiple slaves (cards), synchronous start topology (refer to Figure 1,Figure 2). Clock, power and ground signals are common to all cards. Command (CMD) and data (DAT0-DAT3) signals are dedicated to each card providing continues point to point connection to all the cards.

During initialization process, commands are sent to each card individualy, allowing the application to detect the cards and assign logical addresses to the physical slots. Data is always sent (received) to (from) each card individually. However, in order to simplify the handling of the card stack, after initialization process, all commands may be sent concurrently to all cards. Addressing information is provided in the command packet.

SD Bus allows dynamic configuration of the number of data lines. After power-up, be defalut, the microSD Card will use only DAT0 for data transfer. After initialization, the host can change the bus width(number of active data lines). This feature allows and easy trade off between hardware cost and system performance. Note that while DAT1-DAT3 are not in use, the related Host's DAT lines should be in tri-state (input mode). For SDIO cards DAT1 and DAT2 are used for signaling.

The SPI compatible communication mode of the microSD Memory Card is designed to communicate with a SPI channel, commonly found in various microcontrollers in the market. The interface is selected during the first reset command after power up and cannot be changed as long as the part is powered on.
The SPI standard defines the physical link only, and not complete data transfer protocol. The microSD Card SPI implementation uses the same command set of the SD mode. From the application point of view, the advantage of the SPI mode is the capability of using an off-the-shelf host, hence reducing the design-in effort to minimum. The disadvantage is the loss of performance, relatively to the SD mode which enables the wide bus option.

The microSD Card SPI interface is compatible with SPI hosts available on the market. As any other SPI device the microSD Card SPI channel consists the following four signals:

- CS : Host to card Chip Select signal
- CLK : Host to card clock signal
- DataIN : Host to card data signal
- DataOut: Card to host data signal

Another SPI common characteristic is byte transfers, which is implemented in the card as well. All data tokens are multiples of bytes (8 bit) and always byte aligned to the CS signal.

The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal .

The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.

4.2 Bus Protocol

4.2.1 SD Bus

For more details, refer to Section 3.6.1 of the SDA Physical Layer Specification, Version 3.0

4.2.2 SPI Bus

For more details, refer to Chapter 7 of the SDA Physical Layer Specificaation, Version 3.0

4.3 microSD Card Pin Assignment

4.3.1 SD Card Pin Assignment

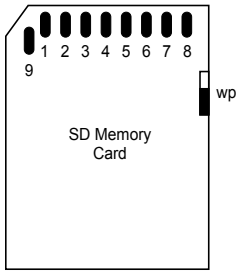


Figure 3. SD Memory Card shape and interface (top view)

The SD Memory Card has the form factor 24 mm x 32 mm x 2.1 mm or 24 mm x 32 mm x 1.4 mm.
Figure 3 shows the general shape of the shape and interface contacts of the SD Memory Card. The detailed physical dimensions and mechanical description are given in section 5.4.

The following Table defines the card contacts:

[Table 12] : SD Memory Card Pad Assignment

Pin #	Name	Type[1]	Description	Name	Type	Description
SD Mode				SPI Mode		
1	CD/DAT3[2]	I/O/PP[3]	Card Detect / Data Line [Bit 3]	CS	I[3]	Chip Select (neg true)
2	CMD	I/O/PP	Command/Response	DI	I	Data In
3	VSS1	S	Supply voltage ground	VSS	S	Supply voltage ground
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS2	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]	DO	O/PP	Data Out
8	DAT1[4]	I/O/PP	Data Line [Bit 1]	RSV		
9	DAT2[5]	I/O/PP	Data Line [Bit 2]	RSV		

NOTE:
1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers;
2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command
4) DAT1 line may be used as Interrupt Output (from the Card) in SDIO mode during all the times that it is not in use for data transfer operations (refer to "SDIO Card Specification" for further details).
5) DAT2 line may be used as Read Wait signal in SDIO mode (refer to "SDIO Card Specification" for further details).

4.3.2 microSD Card Assignment

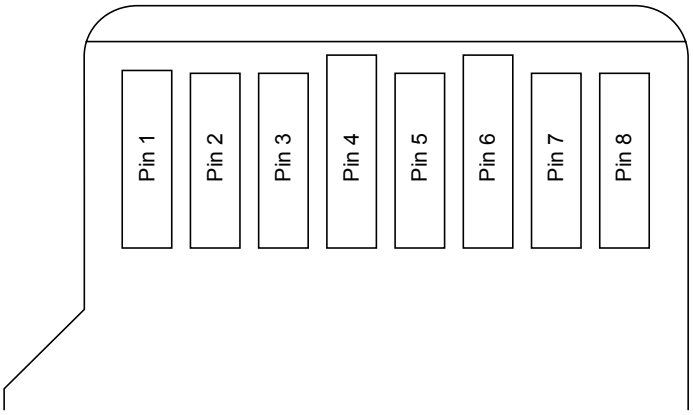


Figure 4. Contact Area

[Table 13] : microSD Contact Pad Assignment

Pin #	SD Mode			SPI Mode		
	Name	Type[1]	Description	Name	Type[1]	Description
1	DAT2[2.5]	I/O/PP	Data Line [Bit 2]	RSV		Reserved
2	CD/DAT3[2]	I/O/PP[3]	Card Detect / Data Line [Bit 3]	CS	I[3]	Chip Select (neg true)
3	CMD	PP	Command/Response	DI	I	Data In
4	VDD	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	I	Clock
6	VSS	S	Supply voltage ground	VSS	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]	DO	O/PP	Data Out
8	DAT1[2.4]	I/O/PP	Data Line [Bit 1]	RSV[4]		

NOTE:
1) S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers ;
2) The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
3) At power up this line has a 50KOhm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42)
4) DAT1 line may be used as Interrupt Output (from the Card) in SDIO mode during all the times that it is not in use for data transfer operations (refer to "SDIO Card Specification" for further details).
5) DAT2 line may be used as Read Wait signal in SDIO mode (refer to "SDIO Card Specification" for further details).

4.4 Mechanical Specification

This section describes the mechanical and electrical features, as well as SEC microSD Card environmental reliability and durability specifications. For more details you can refer to SDA Physical Layer Specification Version 2.00, Section 8.1. For more details and Section 3.0 Mechanical Specification for microSD Memory Card.

4.4.1 Mechanical Form Factor of microSD

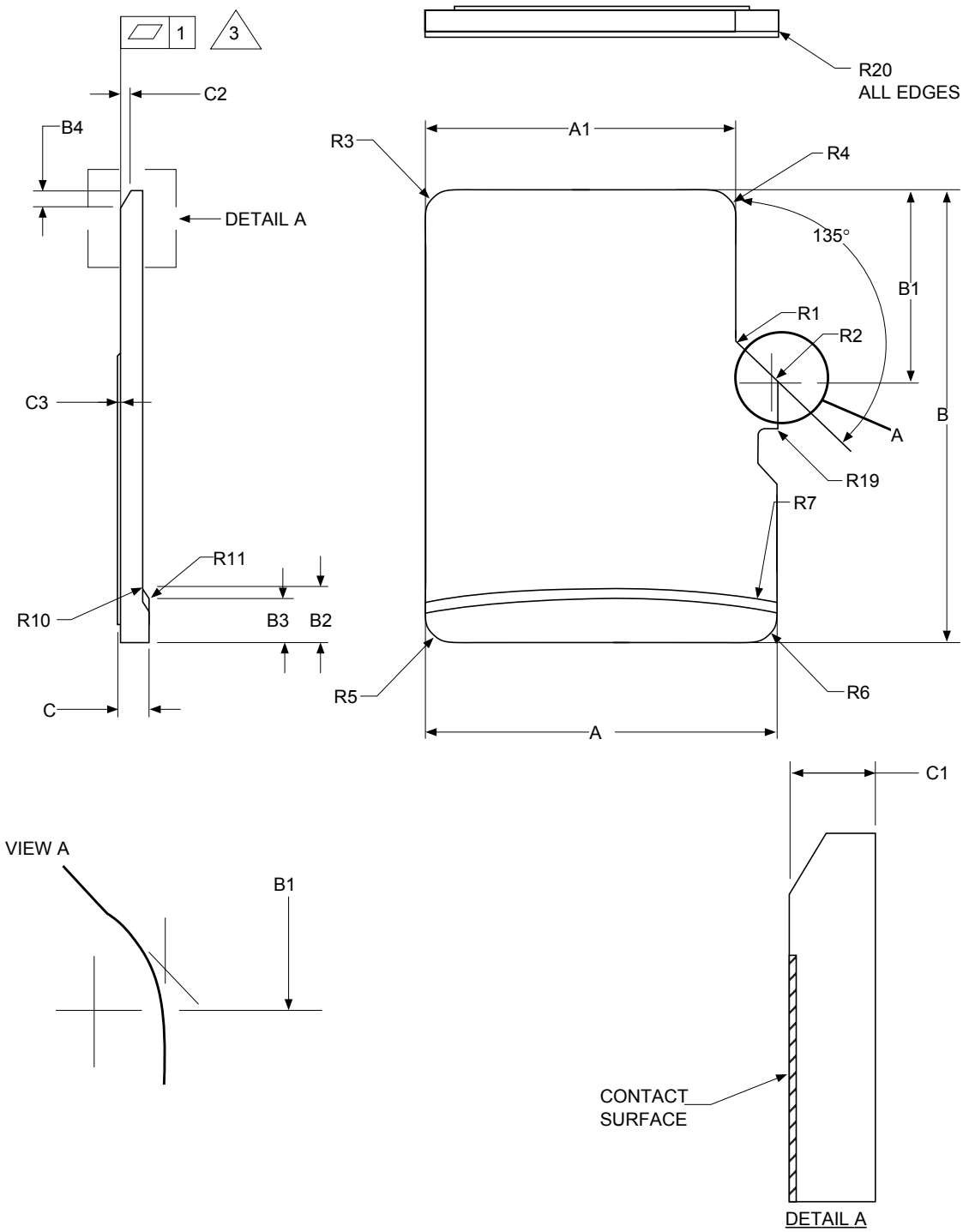


Figure 5. Mechanical Description: Top View

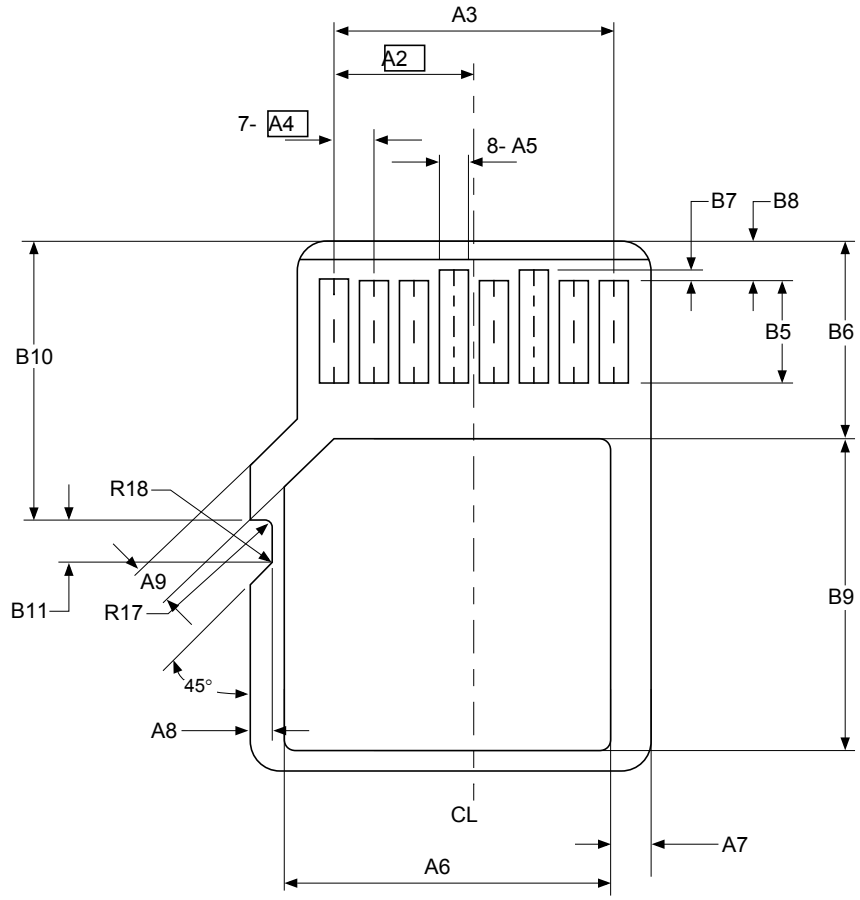


Figure 6. : Mechanical Description: Bottom View

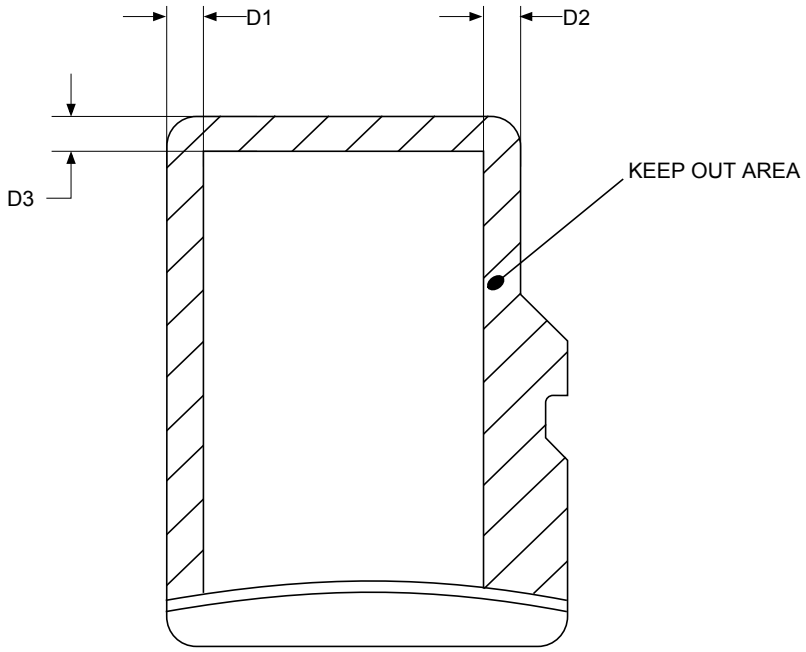


Figure 7. Mechanical Description: Keep Out Area

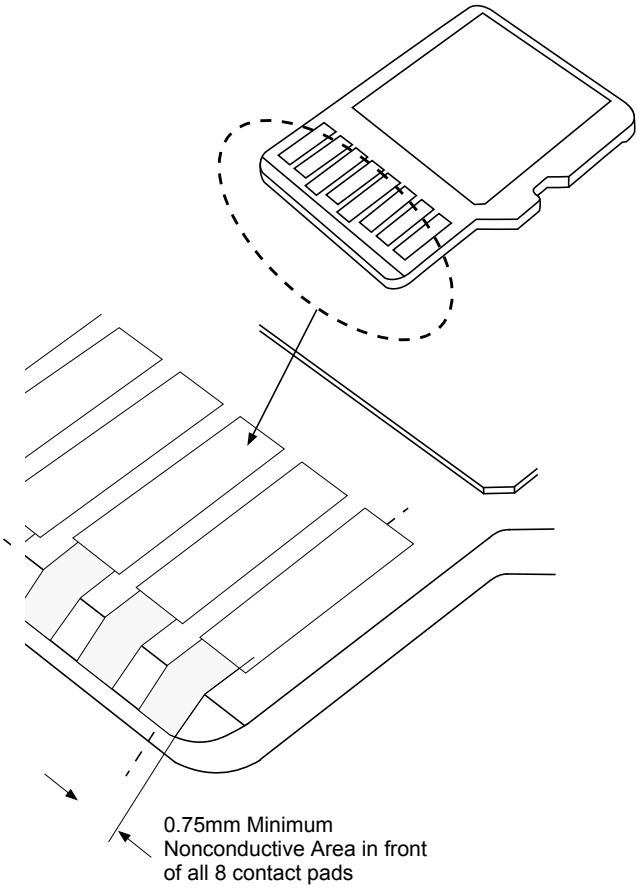


Figure 8. Nonconductive Area in Front of Contact Pad

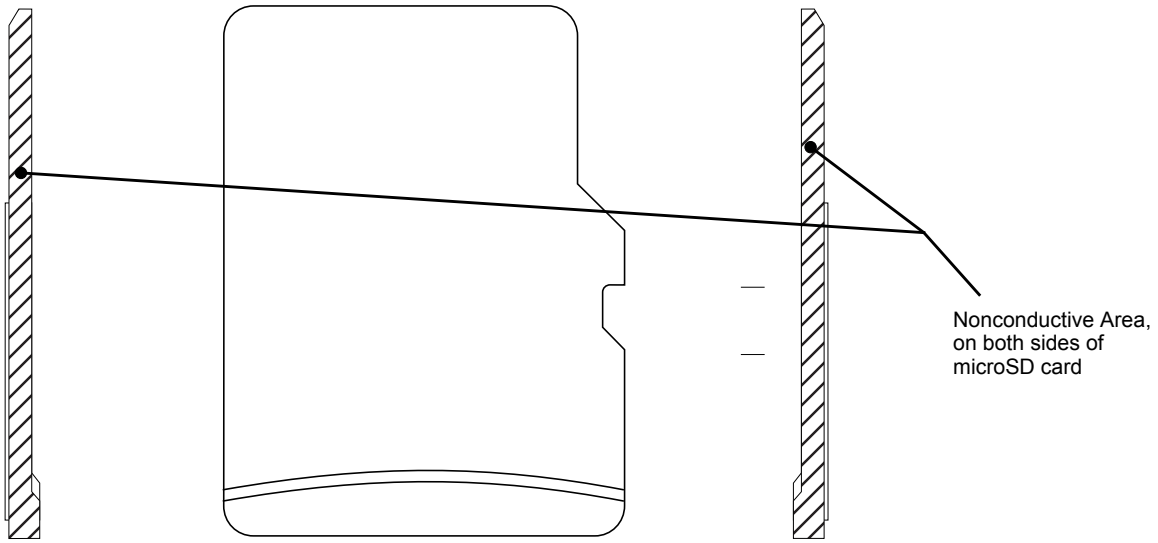


Figure 9. Nonconductive Area on Sides of Card

[Table 14] : microSD Package: Dimensions

	COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX	NOTE
A	10.90	11.00	11.10	
A1	9.60	9.70	9.80	
A2	-	3.85	-	BASIC
A3	7.60	7.70	7.80	
A4	-	1.10	-	BASIC
A5	0.75	0.80	0.85	
A6	-	-	8.50	
A7	0.90	-	-	
A8	0.60	0.70	0.80	
A9	0.80	-	-	
B	14.90	15.00	15.10	
B1	6.30	6.40	6.50	
B2	1.64	1.84	2.04	
B3	1.30	1.50	1.70	
B4	0.42	0.52	0.62	
B5	2.80	2.90	3.00	
B6	5.50	-	-	
B7	0.20	0.30	0.40	
B8	1.00	1.10	1.20	
B9	-	-	9.00	
B10	7.80	7.90	8.00	
B11	1.10	1.20	1.30	
C	0.90	1.00	1.10	
C1	0.60	0.70	0.80	
C2	0.20	0.30	0.40	
C3	0.00	-	0.15	
D1	1.00	-	-	
D2	1.00	-	-	
D3	1.00	-	-	
R1	0.20	0.40	0.60	
R2	0.20	0.40	0.60	
R3	0.70	0.80	0.90	
R4	0.70	0.80	0.90	
R5	0.70	0.80	0.90	
R6	0.70	0.80	0.90	
R7	29.50	30.00	30.50	
R10	-	0.20	-	
R11	-	0.20	-	
R17	0.10	0.20	0.30	
R18	0.20	0.40	0.60	
R19	0.05	-	0.20	
R20	0.02	-	0.15	

NOTE:
1) DIMENSIONING AND TOLERTANCING PER ASME Y14.5M-1994.
2) DIMENSIONS ARE IN MILLIMETERS.
3) COPLANARITY IS ADDITIVE TO C1 MAX THICKNESS.

4.4.2 Electrical features, Environmental Reliability and Durability

SEC microSD Card Electrical features, Environmental Reliabilities and Durabilities conform to SDA Physical Layer Specification Version 2.00, Section 8.1. For more details and informations of SEC microSD Card Data, refer to Product Qualification Report.

4.5 Electrical Interface

The following sections provide valuable information about the electrical interface. See Chapter 6 of the SDA Physical Layer Specification, Version 3.00 for more detail information.

4.5.1 Power Up

The power-up of the microSD Card bus is handled locally in each SD Card and in the host

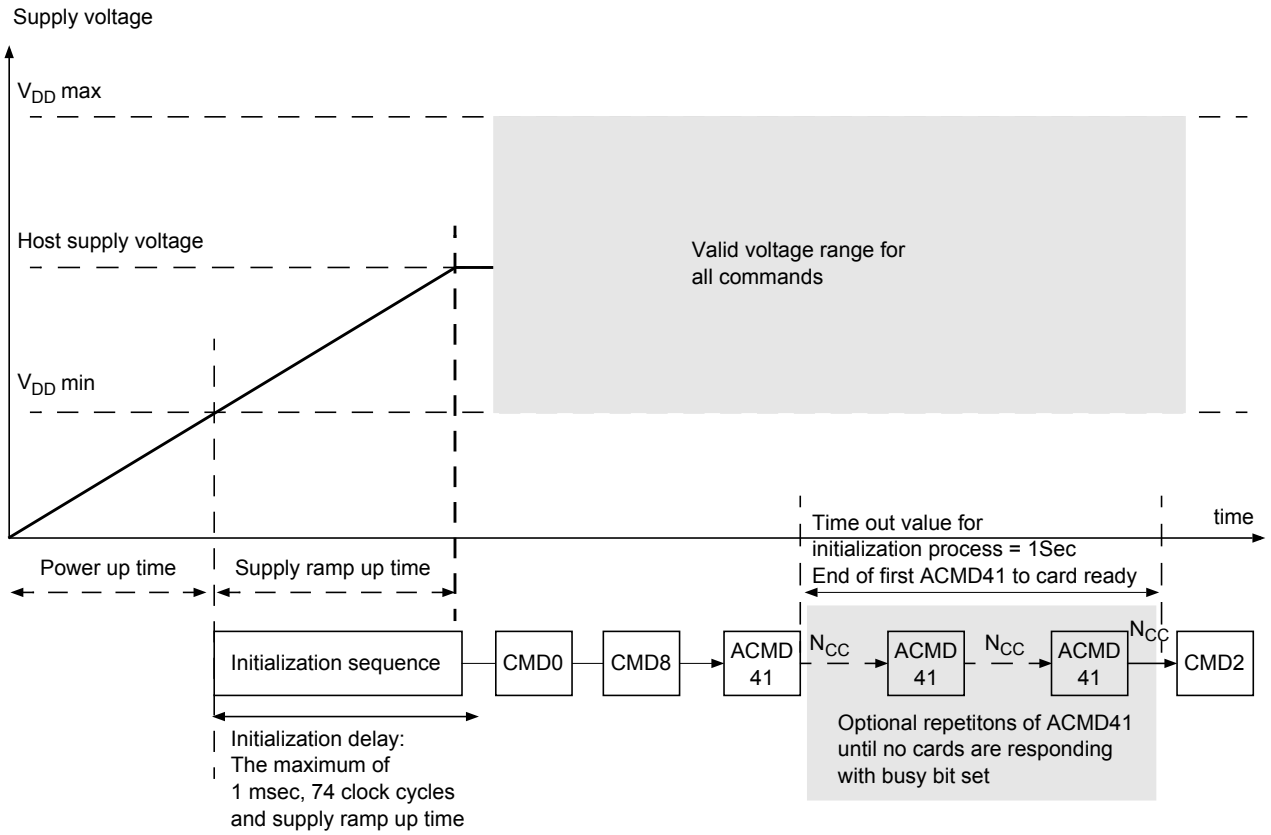


Figure 10. Power-up Diagram

.• Power up time is defined as voltage rising time from 0 volt to VDD(min.) and depends on application parameters such as the maximum number of SD Cards, the bus length and the characteristic of the power supply unit.

• Supply ramp up time provides the time that the power is built up to the operating level (the host supply voltage) and the time to wait until the SD card can accept the first command,

• The host shall supply power to the card so that the voltage is reached to VDD(min.) within 250ms and start to supply at least 74 SD clocks to the SD card with keeping CMD line to high. In case of SPI mode, CS shall be held to high during 74 clock cycles.

• After power up (including hot insertion, i.e. inserting a card when the bus is operating) the SD Card enters the *idle state*. In case of SD host, CMD0 is not necessary. In case of SPI host, CMD0 shall be the first command to send the card to SPI mode.

• CMD8 is added in the Physical Layer Specification Version 2.00 to support multiple voltage ranges and used to check whether the card supports supplied voltage. The version 2.00 host shall issue CMD8 and verify voltage before card initialization. The host that does not support CMD8 shall supply high voltage range.

• ACMD41 is a synchronization command used to negotiate the operation voltage range and to poll the cards until they are out of their power-up sequence. In case the host system connects multiple cards, the host shall check that all cards satisfy the supplied voltage. Otherwise, the host should select one of the cards and initialize.

4.5.2 Reset Level Power Up

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.

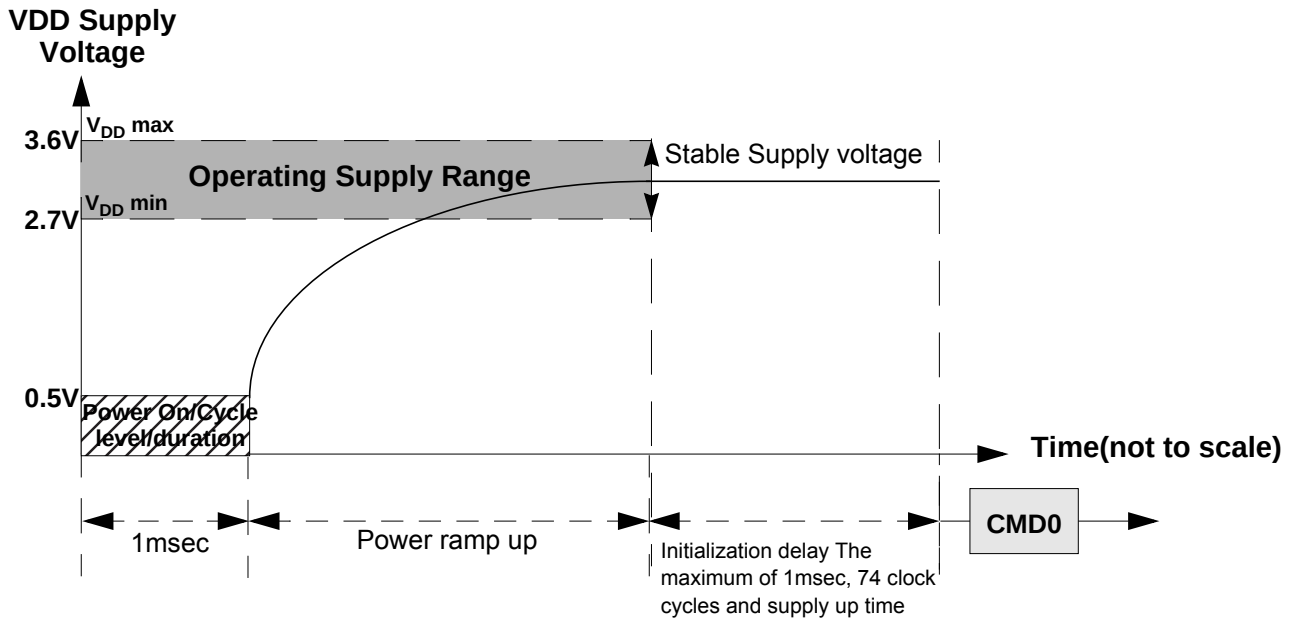


Figure 11. change of Figure for power up

- To assure a reliable SD Card hard reset of Power On and Power Cycle, Voltage level shall be below 0.5V and Time duration shall be at least 1ms.

- The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD(min.) and VDD(max.) and host can supply SDCLK.

Followings are recommendation of Power ramp up:
(1) Voltage of power ramp up should be monotonic as much as possible.
(2) The minimum ramp up time should be 0.1ms.
(3) The maximum ramp up time should be 35ms for 2.7~3.6V power supply.

4.5.3 Power Down and Power Cycle

- When the host shuts down the power, the card VDD shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.

- If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in *Inactive State.* To create a power cycle the host shall follow the power down description before power up the card (i.e. the card VDD shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

4.5.4 Bus Operating Conditions for 3.3V Signaling

SPI Mode bus operating conditions are identical to SD Card mode bus operating conditions.

4.5.4.1 Threshold Level for High Voltage Range

[Table 15] : Threshold Level for High Voltage

Parameter	Symbol	Min	Max.	Unit	Remark
Supply Voltage	V_{DD}	2.7	3.6	V	
Output High Voltage	V_{OH}	0.75*V_{DD}		V	I_{OH} = -2mA V_{DD} min
Output Low Voltage	V_{OL}		0.125*V_{DD}	V	I_{OL} = 2mA V_{DD} min
Input High Voltage	V_{IH}	0.625*V_{DD}	V_{DD}+0.3	V	
Input Low Voltage	V_{IL}	Vss-0.3	0.25 *V_{DD}	V	
Power Up Time	=		250	ms	From 0V to V_{DD} min

4.5.4.2 Bus Signal Line Load

The total capacitance of the SD Memory Card bus is the sum of the bus host capacitance CHOST, the bus capacitance CBUS itself and the capacitance CCARD of each card connected to this line:

Total bus capacitance = CHOST + CBUS + N * CCARD

Where N is the number of connected cards.

[Table 16] : Bus Operating Conditions - Signal Line's Load

Parameter	Symbol	Min	Max.	Unit	Remark
Pull-up resistance	R_{CMD} R_{DAT}	10	100	KOhm	to prevent bus floating
Total bus capacitance for each signal line	C_L		40	pF	1 card CHOST+CBUS shall not exceed 30 pF
Capacitance of the card for each siginal pin	C_{CARD}		10	pF	
Maximum signal line inductance			16	nH	f_{PP} <= 20 MHz
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	KOhm	May be used for card detection
Capacity Connected to Power Line	CC		5	uF	To Prevent inrush current

Note that the total capacitance of CMD and DAT lines will be consist of CHOST, CBUS and one CCARD only because they are connected separately to the SD Memory Card host.

Host should consider total bus capacitance for each signal as the sum of CHOST, CBUS, and CCARD, these parameters are defined by per signal. The host can determine CHOST and CBUS so that total bus capacitance is less than the card estimated capacitance load (CL=40 pF). The SD Memory Card guarantees its bus timing when total bus capacitance is less than maximum value of CL (40 pF). To limit inrush current caused by host insertion, card maximum capacitance between VDD - VSS is defined as 5uF. To support host hot insertion, the host should consider decoupling capacitor connected to power line. As microSD card Cc is 5uF(Max.), 45uF(min.) is recommended for Decoupling capacitor. For more details, please refer to Appendix E of the SDA Physical Layer Specification 3.00.

4.5.5 Driver Strength for 1.8V Signaling

4.5.5.1 I/O Drive Strength Types

[Table 17] : I/O Driver Strength Types

Driver Type	Nominal Impedance	Driving capability	UHS50 Card	UHS104 Card
A	33Ω	x1.5	Optional	Mandatory
B	50Ω	x1	Mandatory	Mandatory
C	66Ω	x0.75	Optional	Mandatory
D	100Ω	x0.5	Optional	Mandatory

NOTE :
Nominal impedance is defined by I-V characteristics of output driver at 0.9V.

(1) Driver Type A
Type A driver is the x15 driver, defined as 33 ohm nominal driver, and supporting up to 208MHz operation.
(2) Driver Type B
Type B driver is the default driver strength, targeted for a fixed impedance distributed system with 50 ohm transmission line, at all available frequencies. Therefore, it is defined as 50 ohm nominal driver. This driver can support total C_L of about 15pF for UHS104 card and about 30pF for UHS50 card. Driver strength B is the reference driver for definitions of all the rest of the driver strengths.
(3) Driver Type C
Type C driver is the x0.75 driver, it is the weakest driver that supports 208MHz operation, and is defined as 66 ohm nominal driver
(4) Driver Type D
Type D driver is a x0.5 driver, it is best for a system which the speed is not critical, but the more important is low noise / low EMI.
Type D generates the slowest rise / fall time. Using a very slow rise time, the system usually will be considered as a lumped load system.
Type D is defined as 100 ohm nominal driver, and the maximum operating frequency is depends on th host design.

4.5.5.2 I/O Driver Target AC Characteristics

The characteristics of output driver are measured by under all maximum to minimum delay conditions.

4.5.5.3 Requirement for Rise/Fall Time

[Table 18] : I/O Driver Design Target

Driver Type	Symbol	Driver Rise / Fall Time Requirenments				Condition
		Min.	Typ.	Max.	Units	C_L
Type B for UHS104	T_RB, T_FB	0.40	0.88	1.32	ns	15pF
Type B for UHS50	T_RB, T_FB	0.70	1.83	2.75	ns	30pF

NOTE:
1. Typical rise / fall time values are a design target. Any actual rise / fall time that is between the minimum and the maximum is conforming to this specification.
2. Output rise time is measured between V_{OL} (0.45V) to V_{OH}(1.4V),output fall time is measured between V_{OH}(1.4V) to V_{OL}(0.45V).
3. The I-V curve(current-voltage characteristics) of drivers types A,C and D are approximately x1.5,x0.75 and x0.5 from the default driver type B

4.5.5.4 Requirement for Rise/Fall Time

[Table 19] : Design Target for Ratio of Rise / Fall Time

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
The Ratio of Rise / Fall Time	R_{RF}	0.7	1.0	1.4	-	$R_{RF}=T_R/T_F$

4.5.5.5 Output Driver Test Circuit

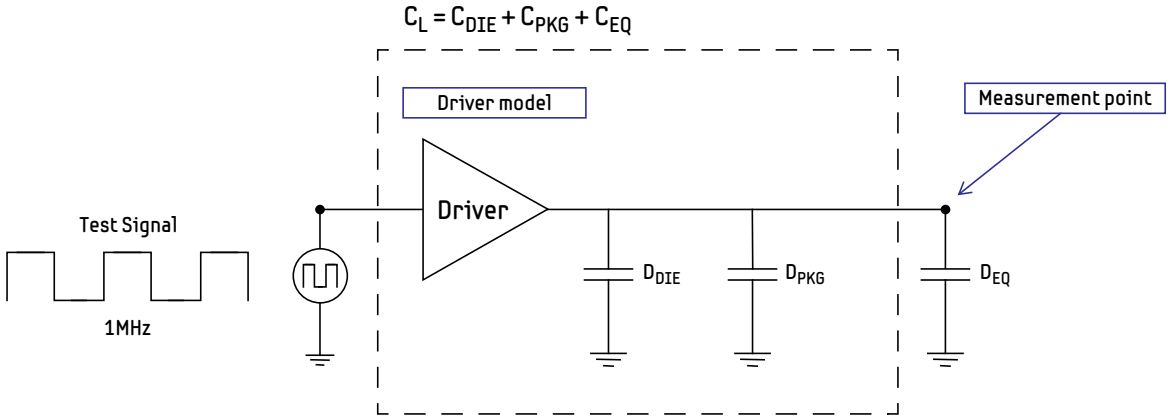


Figure 12. Outputs Test Circuit for Rise/Fall Time Measurement

NOTE :
1) The ratio of rise time to fall time is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given temperature and voltage combination, it represents the maximum difference between rise and fall time due to process variation.
2) Terminology is defined as follows:

[Table 20] : Card Capacitance Range

Capacitance	Min	Max	Units	Notes
C_{CARD} (C_{DIE} + C_{PKG})	5	10	pF	---

4.5.5.6 Driver Strength Selection

[Table 21] : Output Driver Type Support Bits

CMD6 Status Bit	Meaning
432	Support bit of Type B Driver (Always 1 as default)
433	Support bit of Type A Driver
434	Support bit of Type C Driver
435	Support bit of Type D Driver

[Table 22] : Approximation of Total Capacitance for Each of Drive Strength

Driver Type	Type A	Type B	Type C	Type D
C_L at 208MHz	21pF	15pF	11pF	Note1
C_L at 100MHz SDR C_L at 50 MHz DDR	43pF	30pF	23pF	Note1

NOTE :
1) Type D support total CL of about 22pF or more, for slower rise / fall time than at 100MHz SDR operation. When selecting type D driver, the maximum frequency is determined by the host system.

4.5.6 Bus Operating Condition for 1.8V Signaling

4.5.6.1 Threshold Level for 1.8V Singnaling

[Table 23] : Threshold Level for 1.8V Signaling

Patameter	Symbol	Min.	Max.	Unit	Remark
Supply Voltage	V_{DD}	2.70	3.60	V	
Regulator Voltage	V_{DDIO}	1.70	1.95	V	Generated by V_{DD}
Output High Voltage	V_{OH}	1.40	-	V	I_{OH}= -2mA
Output Low Voltage	V_{OL}	-	0.45	V	I_{OL} = 2mA
Input High Voltage	V_{IH}	1.27	2.00	V	
Input Low Voltage	V_{IL}	V_{SS}-0.30	0.58V	V	

4.5.6.2 Leakage Current

[Table 24] : Input Leakage Current

Patameter	Symbol	Min.	Max.	Unit	Remark
Input Leakage Current		-2	2	μA	DAT3 pull-up is disconnected.

4.6 Bus Signal Levels

As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.

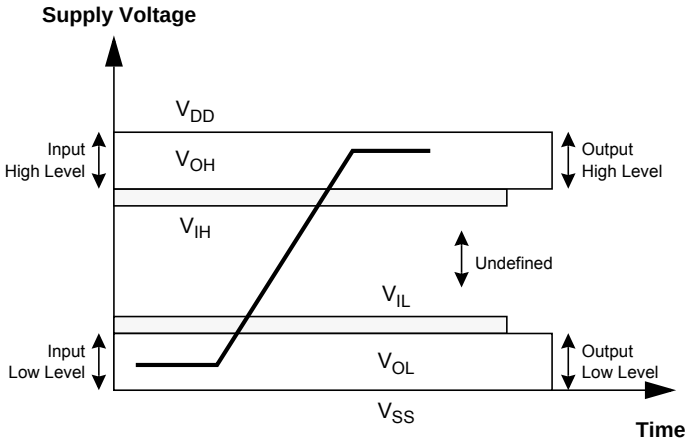


Figure 13. Bus Signal Levels

To meet the requirements of the JEDEC specification JESD8-1A and JESD8-7, the card input and output voltages shall be within the specified ranges shown in Table 5-2 for any VDD of the allowed voltage range.

4.6.1 Bus Timing (Default Mode)

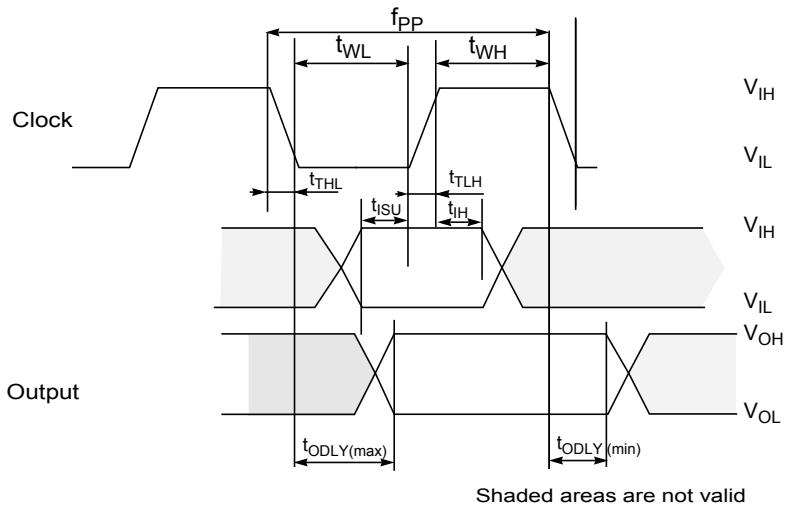


Figure 14. Timing diagram data input/output referenced to clock (Default)

[Table 25] : Bus Timing - Parameter Values (Default)

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK (All values are referred to min. (V_{IH}) and max. (V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	C_{CARD} <= 10 pF (1 card)
Clock frequency Identification Mode	f_{OD}	0[1] / 100	400	kHz	C_{CARD} <= 10 pF (1 card)
Clock low time	t_{WL}	10		ns	C_{CARD} <= 10 pF (1 card's)
Clock high time	t_{WH}	10		ns	C_{CARD} <= 10 pF (1 card)
Clock rise time	t_{TLH}		10	ns	C_{CARD} <= 10 pF (1 card)
Clock fall time	t_{THL}		10	ns	C_{CARD} <= 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{CARD} <= 10 pF (1 card)
Input hold time	t_{IH}	5		ns	C_{CARD} <= 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	C_L <= 40 pF (1 card)
Output delay time during Identification Mode	t_{ODLY}	0	50	ns	C_L<= 40 pF (1 card)

NOTE:
1) OHz means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required

4.6.2 Bus Timing (High-speed Mode)

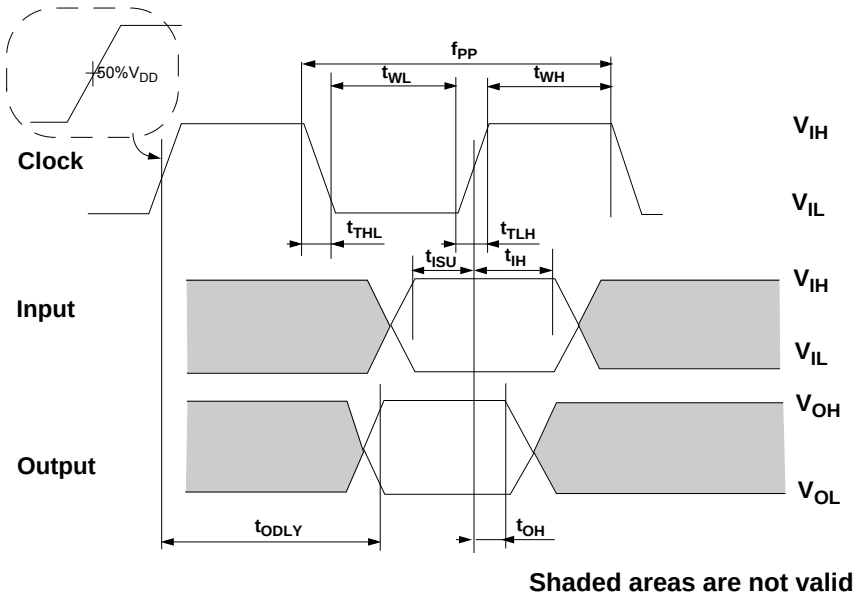


Figure 15. Timing Diagram data Input/Output Refrenced to Clock (High-Speed)

[Table 26] : Bus Timing - Parameter Values (High-Speed)

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK (All values are referred to min. (V_{IH}) and max. (V_{IL})					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	C_{CARD} <= 10 pF (1 card)
Clock low time	t_{WL}	7		ns	C_{CARD} <= 10 pF (1 card)
Clock high time	t_{WH}	7		ns	C_{CARD} <= 10 pF (1 card)
Clock rise time	t_{TLH}		3	ns	C_{CARD} <= 10 pF (1 card)
Clock fall time	t_{THL}		3	ns	C_{CARD} <= 10 pF (1 card)
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{CARD} <= 10 pF (1 card)
Input hold time	t_{IH}	2		ns	C_{CARD} <= 10 pF (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output delay time during Data Transfer Mode	t_{ODLY}		14	ns	C_L<= 40 pF (1 card)
Output Hold time	t_{OH}	2.5		ns	C_L <= 15 pF (1 card)
Total Systme capacitance for each line[1)]	C_L		40	pF	1 card

NOTE:
1) In order to satisfy severe timing, host shall drive only one card.

4.6.3 Bus Timing Specification in SDR12, SDR25, SDR50 and SDR104 Modes

4.6.3.1 Clock Timing

SDCLK input shall satisfy the clock timing over all variable conditions, and is measured as close as possible to SD socket pins to the card while CMD and DAT[3:0] are in quiet state(not toggling).VIH denotes V_{IH} (min.) and VIL denotes VIL(max.) in Figure 19.

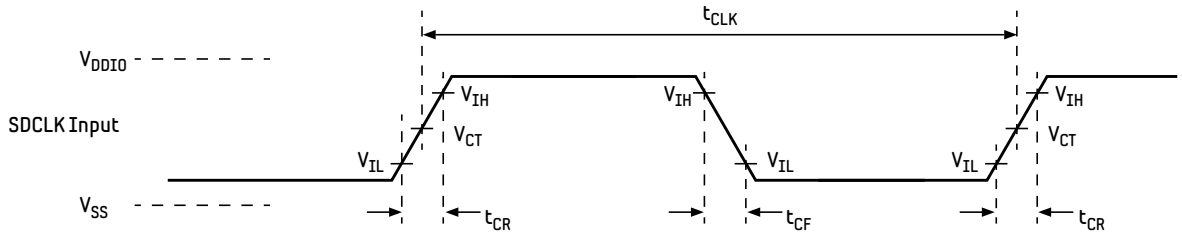


Figure 16. Clock Signal Timing

[Table 27] : Clock Signal Timing

Symbol	Min.	Max.	Unit	Remark
t_{CLK}	4.80	-	ns	208MHz (Max.), Between rising edge, V_{CT}= 0.975V
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} < 0.96ns (max.) at 208MHz, C_{CARD}=10pF t_{CR}, t_{CF} < 2.00ns (max.) at 100MHz, C_{CARD}=10pF The absolute maximum value of t_{CR}, t_{CF} is 10ns regardless of clock frequency.
Clock Duty	30	70	%	

4.6.3.2 Card Input Timing

The new parameter Clock Threshold(VCT) is introduced to indicate clock reference point and is defined as 0.975V. Data setup time and hold time are measure at Data Threshold(VIH(min.) and VIL(max.)). VIH denotes V_{IH} (min.) and VIL denotes VIL(max.) in Figure 20

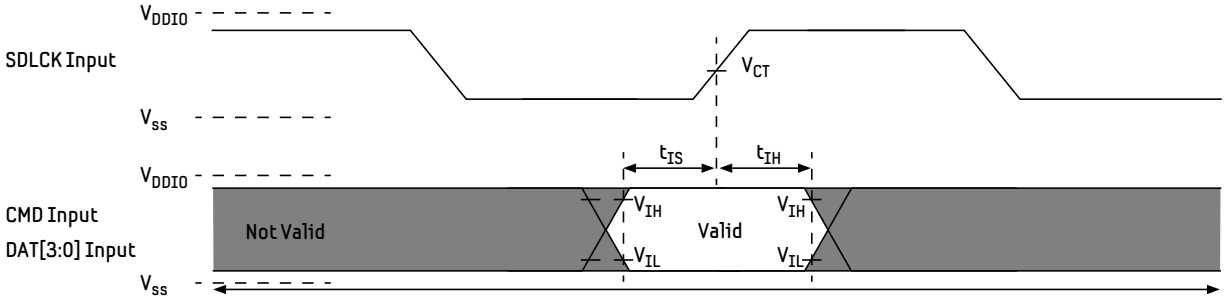


Figure 17. Card Input Timing

[Table 28] : SDR50 and SDR104 Input Timing

Symbol	Min.	Max.	Unit	SDR104 mode
t_{IS}	1.40	-	ns	C_{CARD}=10pF, V_{CT}= 0.975V
t_{IH}	0.80		ns	C_{CARD}=5pF, V_{CT}= 0.975V
Symbol	**Min.**	**Max.**	**Unit**	**SDR50 mode**
t_{IS}	3.00	-	ns	C_{CARD}=10pF, V_{CT}= 0.975V
t_{IH}	0.80	-	ns	C_{CARD}=5pF, V_{CT}= 0.975V

4.6.4 Card Output Timing

4.6.4.1 Frequency Range Consideration

The maximum frequency of UHS-I is 208MHz. Hosts can use any frequency less than the UHS-I card supported. Considering the relation between clock period and output delay time, there is a border frequency around 100MHz. Therefore, two output timing diagrams are defined in this document.

(1) Fixed Output Data Window Case (SDR12, SDR25, SDR50 and DDR50)
If output delay is less than clock period (t_{ODLY}(max.) < t_{CLK}), DAT[3:0] can be sampled by SDCLK because fixed data window synchronized to SDCLK is always available. Considering t_{ODLY} (delay from SDCLK input to CMD and DAT[3:0] output), overlapped area of valid window is available under all maximum and minmum delay conditions (Variation of Temperature and voltage). Refer to Figure 21. Fixed Output Data Window Timing (Figure 22) defines overlapped area of valid data window.
Host can create sampling clock by loopback SDCLK method (refer to Appendix C.1). This timing mode enables the host to configure a simple data receiver circuit. The Fixed Output Data window case is supported in SDR12, SDR25, SDR50 and DDR50. The frequency range is up to 100MHz.

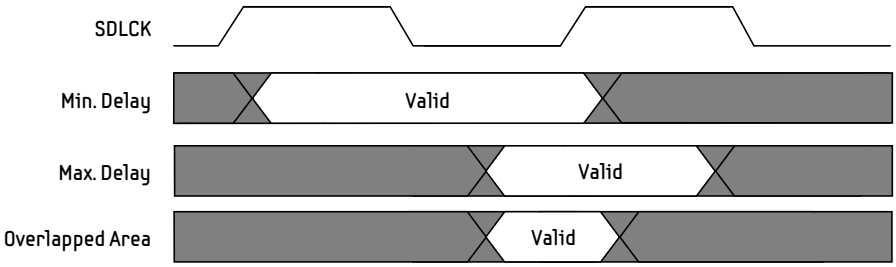


Figure 18. Fixed Output Data Window

(2) Variable Output Data Window Case(SDR104)
Output delay may be bigger than one clock period. In this case, another timing parameter t_{OP} is adopted. t_{OP} is the momentary output phase from SDCLK input to CMD and DAT[3:0] output. After initialization, the t_{OP} can start at any phase in relation to the clock. At the initialization step the host should take care to find the optimal sampling point for the card outputs. The Variable Output Data Window is supported in SDR104. The frequency range is up to 208MHz.

Application Notes:
The fixed timing supported host can use SDR12, SDR25 and SDR50 modes and cannot use SDR104 mode.

4.6.4.2 Output Timing of Fixed Data Window (SDR12, SDR25 and SDR50)

Figure 22 shows card output timing of fixed data window and Table 29 shows required values of this timing for SDR12, SDR25 and SDR50. A valid window is specified by the minmum and maximum of output delay (t_{ODLY}). The valid data window synchronized to SDCLK is available regardless of all temperature and voltage variation. Output valid window is calculated by t_{CLK} - t_{ODLY} + t_{OH}. Host can create sampling clock by delayed SDCLK. V_{OH} denote V_{OH}(min.) and V_{OL} denotes V_{OL}(max.) in Figure 22

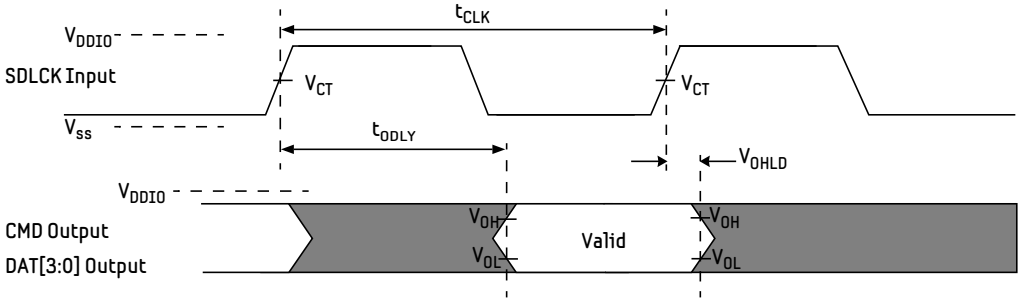


Figure 19. Output Timing of Fixed Data Window

[Table 29] : Output Timing of Fixed Data Window

Symbol	Min.	Max.	Unit	Remark
t_{ODLY}	-	7.5	ns	t_{CLK} >= 10.0ns, C_L = 30pF, using driver Type B. for SDR50,
t_{ODLY}	-	14	ns	t_{CLK} >= 20.0ns, C_L = 40pF, using driver Type B. for SDR25 and SDR12,
t_{OH}	1.5	-	ns	Hold time at the t_{ODLY} (min.), C_L = 15pF

4.6.4.3 Output Timing of Variable Window (SDR104)

Figure 23 shows card output timing of variable data window and Table 30 shows required values of this timing. t_{OP} is introduced to express output delay. t_{OP} does not include a long term temperature drift in contrast t_{ODLY} which includes all delay variation. The temperature drift is expressed by ΔT_{OP}. t_{OP} after initialization, can be in range from 0 to 2UI. On determining sampling point of data, a long term drift, which is mainly depends on temperature drift, should be considered. Output valid data window(t_{ODW}) is available regardless of the drift (ΔT_{OP}) but position of data window varies by the drift. V_{OH} denotes V_{OH}(min.) and V_{OL} denotes V_{OL}(max.) in Figure 23

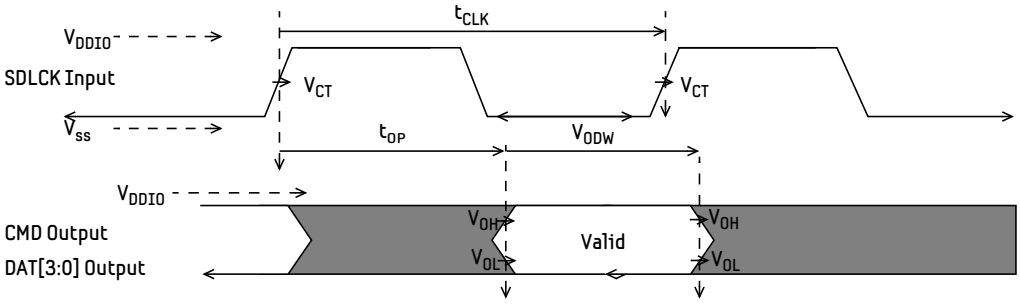


Figure 20. Output Timing of Variable Data Window

[Table 30] : Output Timing of Variable Data Window

Symbol	Min.	Max.	Unit	Remark
t_{OP}	0	2	UI	Card Output Phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temperature change after tuning
t_{ODW}	0.60	-	UI	t_{ODW} = 2.88ns at 208MHz

Card ΔT_{OP} is the total allowable shift of output valid window (T_{ODW}) from last system Tuning procedure.

Card ΔT_{OP} = 1550pS for junction temperature of ΔT= 90 deg.C during operation.
Card ΔT_{OP} = -350pS for junction temperature of ΔT= -20 deg.C during operation.

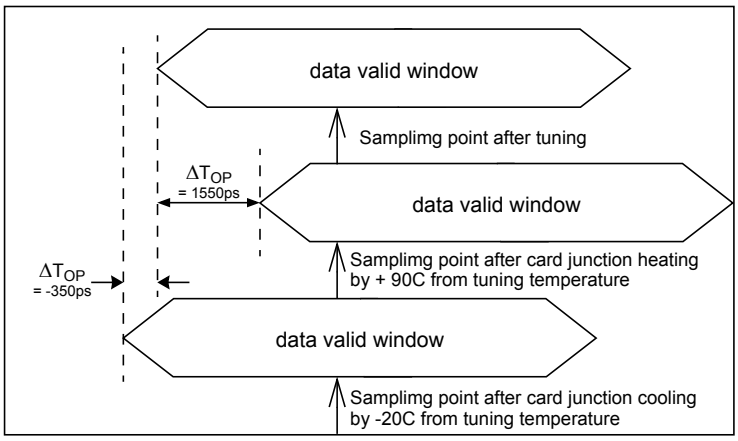


Figure 21. ΔtOP Consideration for Variable Data Window Mode

The range of ΔT_{OP} is 2600ps when card junction temperature changes from -25 deg. C to 125 deg. C during operation.

It is important note that Figure 22 and Figure 23 are output timings of the same output circuit expressed under different conditions. Two output timing figures are required because two types of read data sampling methods are presumed depends on host implementation. These output timings are defined at the test circuit measurement point.T_{ODW} for card is defined in this table, using an external noise free test circuit. The valid window defined by output timings include skew among CMD and DAT[3:0] created by the card.
The host designer should consider the host transmission path which will add some Signal Integrity induced noise, skew between bus members, and timing errors. Expected T_{ODW} at host input is lager than 0.50UI.

Application Notes:
The host needs to consider drift of data window. A temperature drift after tuning procedure completes translates into a limited output valid window drift (ΔT_{OP}). The Host designer should take into consideration this drift, and design correctly to avoid being affected by this drift.
It is good practice to activate tuning procedure after sleep.
Host can use different techniques to overcome temperature effect (include reducing operating frequency).

4.6.5 Bus Timing specification in DDR50 Mode

4.6.5.1 Clock Timing

Figure 25 shows clock signal timing and Table 31 shows required values of this timing. Clock timing is requirement for the host. t_{CLK} is used to define rise / fall timing. Rise and fall time shall be less than 0.2* t_{CLK}. SDCLK input shall satisfy the clock timing over all variable Conditions, and is measured as close as possible to SD socket pins to the card while CMD and DAT[3:0] are in quiet state (not toggling). V_{IH} denote V_{IH}(min.) and V_{IL} denotes V_{IL}(max.) in Figure 25

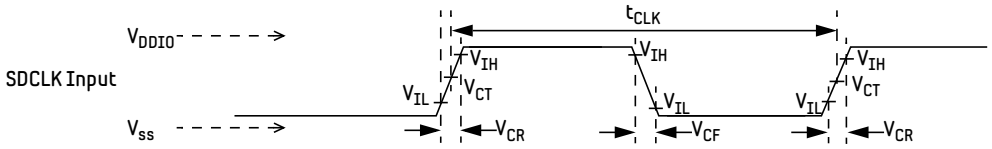


Figure 22. Clock Signal Timing

[Table 31] : Clock Signal Timing

Symbol	Min.	Max.	Unit	Remark
t_{CLK}	20	-	ns	50MHz (Max.), Between rising edge
t_{CR}, t_{CF}	-	0.2* t_{CLK}	ns	t_{CR}, t_{CF} <4.00ns (max.) at 50MHz, C_{CARD}=10pF
Clock Duty	45	55	%	

CMD signal timings are not shown in Figure 26. For CMD Signal timing refers to Figure 20 and Figure 22 (Timing Diagram of SDR mode).

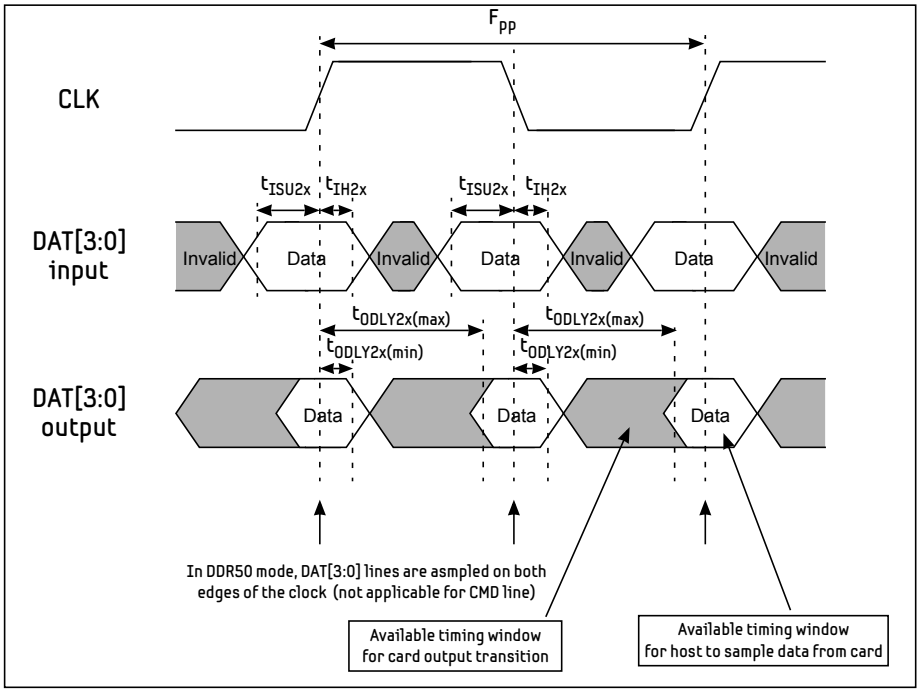


Figure 23. Timing Diagram DAT Inputs/Outputs Referenced to CLK in DDR50 Mode

[Table 32] : Bus Timings - Parameters Values (DDR50 mode)

Parameter	Symbol	Min	Max	Unit	Remark
Inpuy CMD (referenced to CLK rising edge)					
Input set-up time	t_{ISU}	6	-	ns	C_{CARD} ≤10pF (1 card)
Input hold time	t_{IH}	0.8	-	ns	C_{CARD} ≤10pF (1 card)
Output CMD (referenced to CLK rising edge)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	13.7	ns	C_L≤30pF(1 card)
Output hold time	t_{OH}	1.5	-	ns	C_L≥15pF(1 card)
Inputs DAT (referenced to CLK rising and falling edges)					
Input set-up time	t_{ISU2x}	3	-	ns	C_{CARD}≤10pF (1 card)
Input hold time	t_{IH2x}	0.8	-	ns	C_{CARD} ≤10pF (1 card)
Outputs DAT (referenced to CLK rising and falling edges)					
Output Delay time during Data Transfer Mode	t_{ODLY2x}	-	7.0	ns	C_L≤25pF(1 card)
Output hold time	t_{ODLY2x}	1.5	-	ns	C_L≥15pF(1 card)

5.0 MICROSD CARD FUNCTIONAL DESCRIPTION

5.1 General

SEC microSD Card Functional Description contained in this chapter; Section 6.2~6.14; basically, comfort to SDA Physical Layer Specification, Version 3.00. See Chapter 4 of the SDA Physical Layer Specification, Version 3.00 for detail information and guide.

5.2 Card Identification Mode

While in Card Identification mode the host resets all the cards that are in card identification mode, validates operation voltge range, identifies cards and asks them to publish Relative Card Address(RCA). This operation is done to each card separately on its own CMD line. Refer to Section 4.2 of the SDA Physical Layer Specification, Version 3.00 for detail information and guide[1)]

NOTE :
The products on this specification support UHS-1 mode. For correct identification flow, please refer to Section 4.2 of the SDA Physical Layer Specification, Version 2.00.

5.3 Clock Control

The microSD Memory Card bus clock signal can be used by the host to change the cards to energy saving mode or to control the data flow(to avoid under-run or over-run conditions) on the bus. Refer to Section 4.4 of the SDA Physical Layer Specification, Version 3.00 for detail information and guide

5.4 Cyclic Redundancy Code

The CRC is intended for protecting SD Card commands, responses and data transfer against transmission errors on the SD Card bus. One CRC is generated for every command and checked for every response on the CMD line. For data blocks one CRC per transferred block, per data line, is generated. The CRC is generated and checked as described in the Section 4.5 of the SDA Physical Layer Specification, Version 3.0

5.5 Command

There are four kinds of commands defined to control the SD Card:

* Broadcast commands (bc), no response - The broadcast feature is only if all the CMD lines are connected together in the host. If they are separated then each card will accept it separately on his turn.
* Broadcast commands with response (bcr) - response from all cards simultaneously. Since there is no Open Drain mode in SD Card, this type of command is used only if all the CMD lines are separated. The command will be accepted and responded to by every card seperately.
* Addressed (point-to-point) commands (ac) - no data transfer on DAT lines
* Addressed (point-to-point) data transfer commands (adtc), data transfer on DAT lines

All commands and responses are sent over the CMD line of the SD Card bus. The command transmission always starts with the left bit of the bitstring corresponding to the command code word. For more details, refer to the Section 4.7 of the SDA Physical Layer Specification, Version 3.0.

NOTE:
Limited Vendor CMD information, only for certain customer and application, can be provided under appropriate purpose of usage.

5.6 Memory Array Partitioning

The basic unit of data transfer to/from the SD Card is one byte. All data transfer operations which require a block size always define block lengths as integer multiples of bytes. Some special functions need other partition granularity.

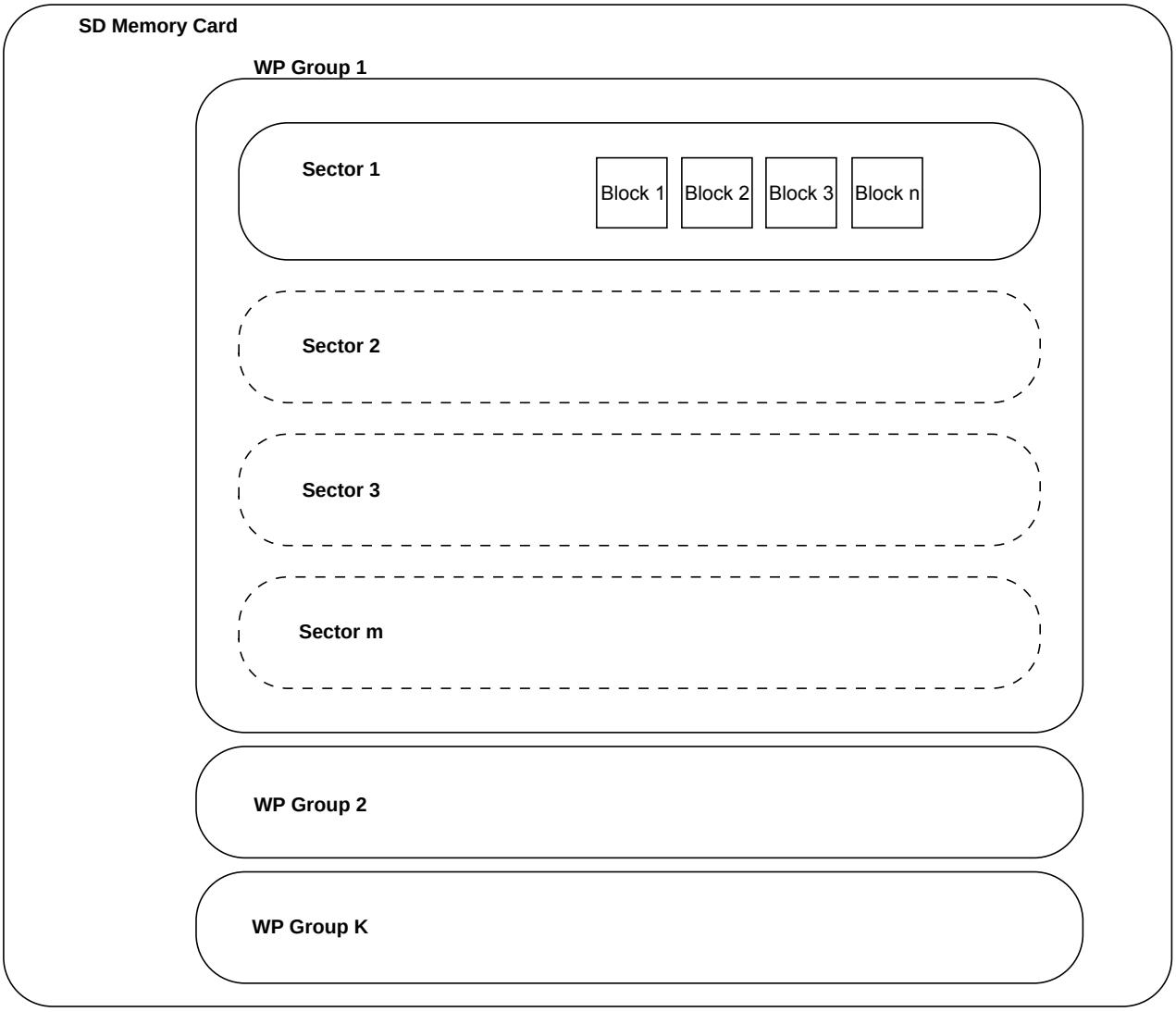


Figure 24. Write Protection Hierarchy

For block oriented commands, the following definition is used:

- Block: is the unit that is related to the block oriented read and write commands. Its size is the number of bytes that will be transferred when one block command is sent by the host. The size of a block is either programmable or fixed. The information about allowed block sizes and the programmability is stored in the CSD.
- For devices that have erasable memory cells, special erase commands are defined. The granularity of the erasable units is in general not the same as for the block oriented commands:
- Sector: is the unit that is related to the erase commands. Its size is the number of blocks that will be erased in one portion. The size of a sector is fixed for each device. The information about the sector size (in blocks) is stored in the CSD. Note that if the card specifies AU size, sector size should be ignored.
- AU (Allocation Unit): is a physical boundary of the card and consists of one or more blocks and its size depends on each card. The maximum AU size is defined for memory capacity. Furthermore AU is the minimal unit in which the card guarantees its performance for devices which complies with Speed Class Specification. The information about the size and the Speed Class are stored in the SD Status. AU is also used to calculate the erase timeout and UHS speed Grade
- WP-Group: is the minimal unit that may have individual write protection for devices which support write-protected group. Its size is the number of groups that will be write-protected by one bit. The size of a WP-group is fixed for each device. The information about the size is stored in the CSD. The High Capacity SD Memory Card does not support the write protect group command.

5.7 Timings

Refer to Section 4.12 of the SDA Physical Layer Specification, Version 3.0 for detail information and guide[1)]

NOTE :
1) The product on this specification supports UHS-1 mode.

5.8 Speed Class Specification

Refer to Section 4.13 of the SDA Physical Layer Specification, Version 3.0 for detail information and guide[1)]

NOTE :
1)The product on this specification supports UHS-1 mode.

5.9 Erase Timeout Calculation

Refer to Section 4.14 of the SDA Physical Layer Specification, Version 3.0 for detail information and guide[1)]

NOTE :
1) The product on this specification supports UHS-1 mode.

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