ECEA 302 Assignment 3 Joshua Bentell

1) Concurrent operation allowing processing of multiple instructions at same time and unrolling of the loop so that it runs in less clock cycles

Reconfigurable - Easy to remotely update, versatile in application

high speed I/O - allows fast data collection and output especially RF signals

2 FPGA is reconfigurable and has a fast development time revision
it is also cheaper to prototype get and FPGA
ASICs are special purpose and can take many months to develop. These are also very costly in low volume.
You can also change internals on the fly of FPGAs
ASICs tend to be faster and power efficient due to lower overhead.

3 key advantage is development speed, much faster to do RTL and RTL sims take much longer to develop and run than a language like C and HLS gives you the flexibility to quickly iterate and to prove functionality and then optimize later

4 Test bench is made by calling the function, providing test data and comparing to the expected output.
↳ this can then be used as an RTL test.
↳ Misses out on the timing in the RTL test code.

5 Anything that involves a loop such as convolution filters can be optimized by unrolling the loop

6 To convert C code to RTL you first extract the control state parts such as functions and loops and ~~control~~ segments in functions

represent it as a state machine.

The data path is then extracted which contains all the read, write and operations that will be performed on variables.

This is then scheduled with the system clock to determine when the operations should occur and how many per clock cycle. This is done making use of the extracted control flow and data path.

Finally, depending on how it was scheduled the binding process will decide whether to use separate components to perform the required operations. These decisions are made by the dependencies of operations and whether those same operations are required at the ~~same~~ same time