1) **List three advantages of scaling down the feature sizes of silicon devices**

    a) More compact chips, more per unit area
    b) Lower capacitance
    c) Higher Speed -> More performance

2) **List two consequences of scaling down the feature sizes of silicon devices.**

    a) Higher complexity
    b) Higher Temperature

3) **Briefly discuss and compare the performance and typical uses of microprocessors and FPGAs.**

Microprocessors are typically used as the main brains of systems where the sensing and number crunching is primarily done, as well as the outputs. FPGAs are typically used in conjunction with microcontrollers as a form of hardware acceleration.

Microprocessors are typically used in this role as they are cheaper and provide a much faster development time over FPGAs, and as a result of their operation, consume less power. FPGAs are used for hardware acceleration as they are able to process multiple instructions at once and are more expensive.

Because FPGAs can perform multiple operations at once, they are able to run at a lower clock speed for the same performance as a microcontroller. FPGAs offer the ability to unwrap sequential code and drastically reduce the time it takes to complete things like loops. So FPGAs tend to have higher performance over microcontrollers.

FPGAs can be configured to have a microprocessor on them which allows a designer to reduce the overall cost of the system if there was intention for a microprocessor and FPGA in it. This allows them to contain both applications on one chip. In addition to this the hardware acceleration the FPGA component would provide is easy to reconfigure on the fly.

4) **List four advantages of integrating a microprocessor and an FPGA onto a single chip.**

    a) Higher Speed
    b) Smaller Size
    c) Lower PCB Complexity
    d) Overall Power Reduction

5) **Provide one application or product example that benefits from having both a microprocessor and a FPGA.**

One application example that benefits from having a microprocessor and a FPGA is image processing. This can be both as an input or output, but because the image can be represented as a matrix, you are able to perform an entire operation on it in one clock cycle. So you are able to filter an image from a sensor and then evaluate it with a microprocessor,

or manipulate one that you are outputting to a TV very fast after figuring out what you are going to display with a microprocessor.

6) **In a RF receiver signal chain, why is it advantageous to have the ADC as close as possible to the Antenna**

It is advantageous to do so as this reduces the noise that the analog system will introduce and also reduce the number of harmonics generated in the process. This is because the analog amplification and filtering is a noisy process.

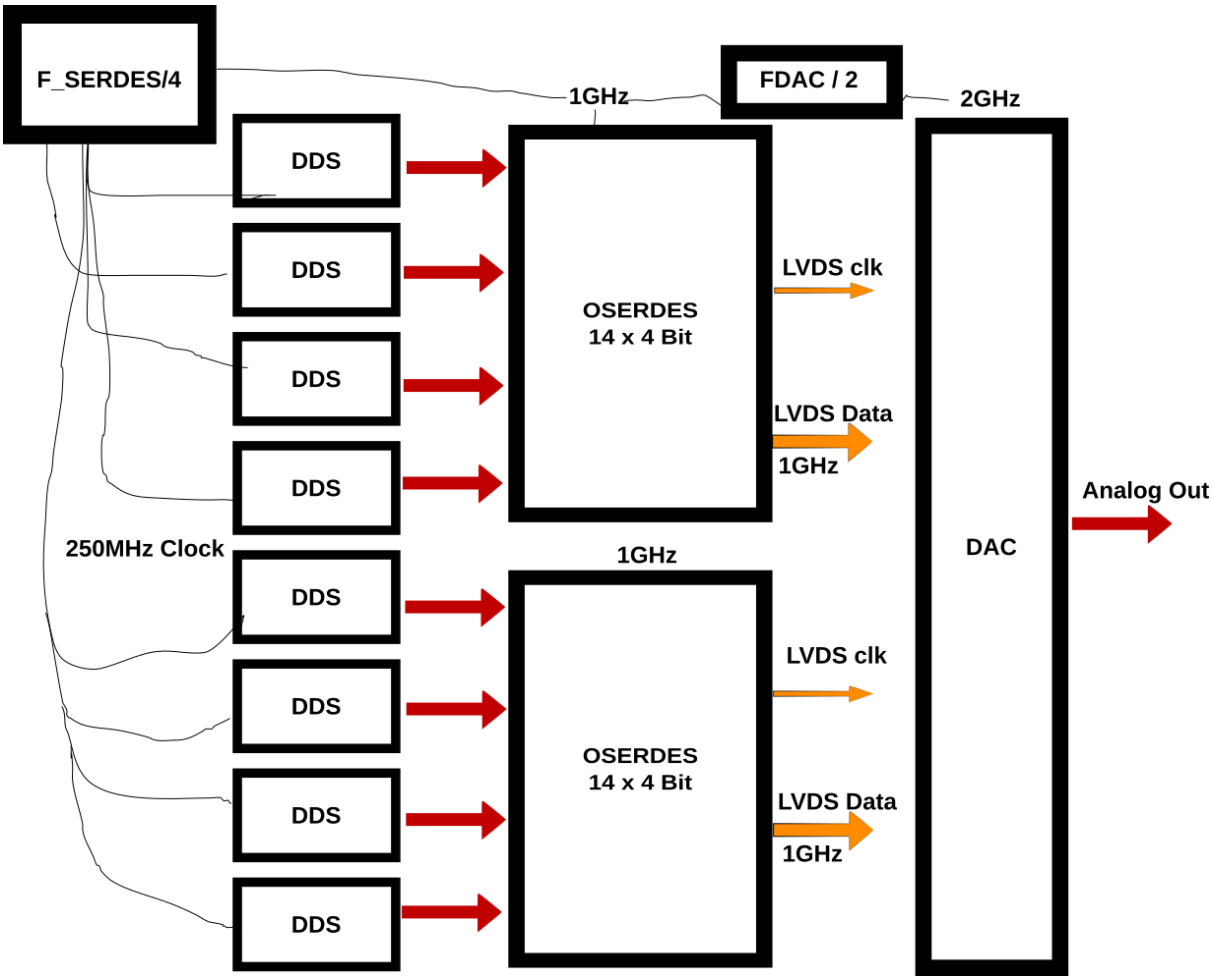
7) **Describe the operation of the OSERDES and ISERDES FPGA I/O blocks**

The SERDES blocks are Serial and parallel converters. The OSERDES block converts parallel to serial by reading all the parallel bits into a shift register at once and then using a bit to tell it to shift the data out onto a serial bus. The ISERDES block converts Serial to parallel by shifting in data on a clock that it has to figure out (due to it being far away, can also use the same clock) and then taking the output of each bit in the shift register resulting in parallelised data.

This allows us to generate a high speed serial waveform by generating a slower parallel set of data.

8) **) Describe, with the aid of diagrams, how you would connect the AD9739 DAC to a Xilinx 7 series device and run the DAC at 2GSPS (note: you do not need to create a detailed schematic diagram)**

To connect the output of a FPGA to a 2 GSPS dac you would first use 4 Direct digital synthesisers at a quarter of the frequency and then output the 14 Bit words from these into an OSERDES device such that the output of the FPGA was 14 4 bit wide words. This comes out at 1 GHz which is then put into the DAC powered off of a 2 GHz Clock. The section before the dac is done twice to generate a string of odd and even bits which the DAC is then able to reassemble.


F_SERDES/4
1GHz
FDAC / 2
2GHz
DDS
DDS
DDS
DDS
OSERDES
14 x 4 Bit
LVDS clk
LVDS Data
1GHz
250MHz Clock
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LVDS Data
1GHz
DAC
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