ECEN302 Lab 7 - TCL scripts and Packaging IP

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1 Introduction

The primary objective of this lab was to wrap up a module as an IP Block. This was done so that an understanding was gained of how to compartmentalise and modularise the program written for an FPGA was acquired for the purpose of speeding up development time in future endeavors.

2 Methodology

The module being packed up in this lab is a PWM sine wave generator. This module takes the first nine switches as inputs to provide a binary weighting to a unity sine wave. Flicking the switches on would increase the time it takes for a point on the output sine wave to be generated; this in turn lowers the frequency of the output sine wave. The AUD_SD port of the module was used to turn off the low pass filter which stops the audio signal from outputting. The AUD_PWM is the output port for the generated tone.