ECEN454 Ref Sheet © Josh Wright February 1, 2017

Metric Prefixes

peta	P	10^{15}	1 000 000 000 000 000
tera	T	10^{12}	1 000 000 000 000
giga	G	10^{9}	1 000 000 000
mega	M	10^{6}	1 000 000
kilo	k	10^{3}	1 000
hecto	h	10^{2}	100
deca	da	10^{1}	10
one		10^{0}	1
deci	d	10^{-1}	0.1
centi	c	10^{-2}	0.01
milli	m	10^{-3}	0.001
micro	μ	10^{-6}	0.000 001
nano	n	10^{-9}	0.000 000 001
pico	p	10^{-12}	0.000 000 000 001
femto	f	10^{-15}	0.000 000 000 000 001

De Morgan's Laws

- $\overline{AB} = \overline{A} + \overline{B}$
- $\overline{A + B} = (\overline{A})(\overline{B})$

Silicon

- Si
- P-type:
  - doped with material to remove electrons (add electron holes), usually Boron (B), Aluminum (Al), or Gallium (Ga)
- N-type:
  - doped with material to add electrons, usually Antimony (Sb), Arsenic (As), or Phosphorous (P)
- Silicon dioxide: SiO_2

Transistors

- pMOS:
  - has the bubble
  - on when input is 0, off when input is 1
- nMOS
  - no bubble
  - on when input is on, off when input is off

D Flip Flop vs Latch

- latch is level triggered
- flip flop is edge triggered

Fabrication

- n-well: use diffusion or ion implantation
- positive lithography: expose to UV where you want to remove material
- negative lithography: expose to UV where you want to keep material

Stick Diagram vs Boolean Function

- TODO
- there is more than one way of making a stick diagram for an expression
  - stuff in series could be in different order, for instance
- if you do it manually, you need to check it with tools:
  - LVS: Layout Vs Schematic
  - DRC: Design Re-Check
  - These aren't really needed for designs automatically generated from verilog code, because of course that's correct

Lithography

- the process of printing onto a chip at nanometer scale
- generally uses UV light, wavelength around 150nm
  - must use fancy tricks to make 10nm features with 150nm light
  - would be nice to use even lower wavelength X-rays, but those are hard to focus
- negative lithography: use the lithography mask to cover what you want to keep.
- positive lithography: mask what you want to remove
- a lens is used to focus the light
  - ideally, want a point source for the light, but that is not practical
  - Optical Proximity Effect: what happens when your focus from the lens is not just right
  - results in rounded corners, inaccurate critical dimensions, and shorter wire ends
  - can use Optical Proximity Correction to fix: basically over-emphasize all the features, and/or add extra lines at outset

MOS transitive I-V Characteristics and Parasitics

- Transistors are not really ideal switches, they have 3 zones of operation: cutoff, linear, saturation
- definitions:
  V_{gs}: voltage gate to source
  V_{gd}: voltage gate to drain
  V_{ds}: voltage source to drain (across the channel)
  V_t: critical voltage at which transistor is saturated
  channel: space between the source and drain, where the electrons flow
- remember that the gate is insulated from the area under it by a thin layer of Silicon Dioxide (SiO_2)
- by convention, the source is the terminal at lower voltage
- **cutoff**:
  - when $V_{gs} < 0$
  - electrons on the gate attract positive voids in the silicon below, and inhibit current flow. Therefore, the transistor is closed.
  - $I_{ds} = 0$
- **linear**:
  - $V_{gs} > V_t, V_{gd} = V_{gs}, V_{ds} = 0$ or $V_{gs} > V_t, V_{gs} > V_{gd} > V_t, 0 < V_{ds} < V_{gs} - V_t$
  - I_{ds} linearly proportional to V_{ds}
  - channel of electrons forms, allowing current to flow
- **saturated:**
  - $V_{gs} > V_t, V_{gd} < V_t, V_{ds} > V_{gs} - V_t$
  - channel pinches off due to electrons attracting to source
  - I_{ds} is independent of V_{ds}
- capacitor effect:
  - gate and channel can have a parallel plate capacitor effect, with the thin layer of SiO_2 acting as the insulator
  - $C = \frac{Q}{V} = \eta_{SiO_2} wl/t_{SiO_2}, V = V + gc - V_t = (v_{gs} - Vds/2) - V_t$
    l, w: length, width of section of gate above channel
- carrier velocity: velocity of the electrons?
  - proportional to the electric field running horizontally between source and drain
  - $v = \mu E, E = V_{ds}/L, t = L/v = L/(\mu E) = L/(\mu \frac{V_{ds}}{L})$
    μ: mobility. electrons move about twice as fast as positive voids
    L: length of channel
- Shockley model of transistor: TODO
  - 1st order model: $\beta = \mu C_{SiO_2} \frac{w}{l}$
    $I_{ds} | V_{gs} < V_t = 0$: cutoff
    $I_{ds} | V_{ds} < V_{dstat} = \beta(V_{gs} - V_t - V_{ds}/2)V_{ds}$: linear
    $I_{ds} | V_{ds} < V_{dstat} = \frac{\beta}{2}(V_{gs} - V_t)^2$: saturation
  - Must be able to derive this model on exam!