CprE 381, Computer Organization and Assembly Level Programming

Team Contract – Project Part 1

Project Teams Group: Sec C 03

Team Members: Joseph Barnes III

Josh Arceo

Quincy Wiseman

Discuss the following aspects of teamwork with your team – make sure to get input from each member. Write down your team's consensus for each of the bolded headings. Italicized text contains instructions and examples and should be deleted once you've read it. Please see the example contract for rough length expectations.

Course Goals: *List and acknowledge the goals of your individual team members.*
Joseph – Get an A/B/C in the course, prepare myself for each exam, make sure I finish my part for the project.
Quincy- minimize the number of lost points, get an A/B/C Pass in the course
Examples may include:

- *learn everything about computer architecture*
- *know enough to understand security risks posed by hardware primitives*
- *get an A/B/C/Pass in the course*
- *minimize the number of lost points*
- *prepare myself for a career in hardware design*
- *prepare myself to be able to do research involving FPGAs*
- *be able to explain the workings of a stored-program computer from gates to C*

Team Expectations:

- **Conduct:** *What are the expectations for personal conduct of group members?*
  - Give feedback to each other
  - Be respectful
  - Ask questions
- **Communication:** *What is the best mode of communication for the group? How often should communication occur? How fast should a response be expected?*
  - Communication through a groupchat (IMessage, Snapchat, or Discord).
  - Communicate as much as needed as we progress through the labs.
- **Group conventions:** *Naming conventions? Compilation and simulation methodology? Testbench strategies? Do file usage? Version control strategies? Commenting standards?*

    - Underscores > CamelCase
    - Use do files to consistently load memory for each simulation run
    - Ece GitLab
- **Meetings:** *Given the significant portion of the course that the lab covers, it is expected that your team will spend more time working on the labs than in your scheduled lab sections. How will your group expect to handle this? Please include at least two additional times outside of lab that your team can meet (preferably in-person).*
    - Work together in-person outside of lab on Tuesdays at 4pm.
    - Work separately on responsibilities outside of lab sections.
- **Peer Evaluation Criteria:** *Please create a brief criteria for how effort and contribution are defined. Note that teams with **vastly** divergent scores may require a meeting with course instructor and result in different grades for different group members. Teams with reasonably equitable scores will receive the same grade*
    - *Contribution will be defined by effort and objective results, if someone is falling behind on their work and not keeping up with the timeline, they will receieve a lower score*
    - *Members should communicate if they have issues keeping up so we can help each other out, and be more understanding when scoring each other*

Role Responsibilities: *Complete the following planning table. Each lab part should be the responsibility of one team member. Also make sure that no one team member is the lead on both the design and test aspects of a single lab part. These guidelines aid in all students having a complete view of the lab. Note that the non-lead is encouraged to participate and support the lead wherever possible, increasing both the quality of the lab part and each team member's knowledge.*

Lab Part	Estimated Time	Design		Test	
		Lead	Timeline	Lead	Timeline
High-level design	1 hr	Joseph	Oct.9	Quincy	Oct.9
Test programs	4 hr	Whole Group	Oct 21	Whole Group	Oct 23
Control logic	2 hr	Quincy	Oct.9	Joseph	Oct.9
Fetch logic	3 hr	Joseph	Oct 16	Josh	Oct 16
Barrel shifter	2 hr	Josh	Oct.9	Quincy	Oct 9
ALU integration + Misc updates	2 hr	Josh	Oct 19	Quincy	Oct 19
High-level integration	4 hr	Josh	Oct.21	Joseph	Oct.22
Synthesis (human effort)	1.5 hr	Quincy	Oct 23	Josh	Oct 24

*Estimated Time is given as a **very rough** guide for even distribution of tasks assuming you've already read through the lab document and have the prerequisite knowledge. Depending on your group's skill and prerequisite knowledge, some tasks may take disproportionately long or short. For your future planning, track this – for future prelabs*

you will be asked to note why past tasks took longer than expected and how you might avoid such issues in the future.

Integrity of Work: *Do not delete the following.* We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

Student Signature Joseph Barnes III **Date** 10/02/2024

Student Signature Joshua Arceo **Date** 10/02/2024

Student Signature Quincy Wiseman **Date** : 10/02/2024