

CprE 381, Computer Organization and Assembly Level Programming

Team Contract – Project Part 2

Project Teams Group #: Sec C 03

Team Members: Evan Shiber

Josh Arceo

Joseph Barnes III

Discuss the following aspects of teamwork with your team – make sure to get input from each member. Write down your team's consensus for each of the bolded headings. Italicized text contains instructions and examples and should be deleted once you've read it. Please see the example contract for rough length expectations.

Course Goals: *List and acknowledge the goals of your individual team members.*

Examples may include:

- *learn everything about computer architecture*
- *know enough to understand security risks posed by hardware primitives*
- *get an A/B/C/Pass in the course*
- *minimize the number of lost points*
- *prepare myself for a career in hardware design*
- *prepare myself to be able to do research involving FPGAs*
- *be able to explain the workings of a stored-program computer from gates to C*

Joseph

- *Get an A/B/C in the course*
- *Prepare myself for each exam*
- *Make sure I finish my part for the project*

Evan

- *Get \geq B in the course*
- *Maximize points through detailed view of rubric and requirements*
- *Ensure proper project contributions*

Josh

- *Get an A or high B*
- *Understand concepts of computer design and architecture*
- *Understand how I can apply these concepts to future courses*

Team Expectations:

- **Conduct:** *What are the expectations for personal conduct of group members?*
 - *Be respectful*
 - *Give each other feedback*
 - *Ask questions*
- **Communication:** *What is the best mode of communication for the group? How often should communication occur? How fast should a response be expected?*
 - *Communicate through a groupchat*
 - *(IMessage, Snapchat, or Discord)*
 - *Communicate as much as needed as we progress through the labs*
- **Group conventions:** *Naming conventions? Compilation and simulation methodology? Testbench strategies? Do file usage? Version control strategies? Commenting standards?*
 - *GitLab*
 - *Ensure test benches cover ALL edge cases*
 - *We had this issue in part 1, where the test bench seemed to work but not all edge cases were covered and issues were discovered VERY late into development.*
 - *Comments should be added for each instruction defining it's ALUOP, its opcode and function code.*
- **Meetings:** *Given the significant portion of the course that the lab covers, it is expected that your team will spend more time working on the labs than in your scheduled lab sections. How will your group expect to handle this? Please include at least two additional times outside of lab that your team can meet (preferably in-person).* *Examples of other issues to consider include:*
 - *Work together in-person outside of lab on Tuesday at 4pm*
 - *Work separately on responsibilities outside of lab sections*
- **Peer Evaluation Criteria:** *Now that you have experience working on a 381 lab with a team, please create a brief criteria for how effort and contribution are defined. Note that teams with **vastly** divergent scores may require a meeting with course instructor and result in different grades for different group members. Teams with reasonably equitable scores will receive the same grade.*
 - *Completing components on time will be a key criteria in effort and contribution.*
 - *If there are any reasons/issues for a member not being able to complete one of their components/tasks on time they must notify the other members as quickly as possible, and potentially ask for someone to cover the remaining work for that component.*

Role Responsibilities: Complete the following planning table. Each lab part should be the responsibility of one team member. Also make sure that no one team member is the lead on both the design and test aspects of a single lab part. These guidelines aid in all students having a complete view of the lab. Note that the non-lead is encouraged to participate and support the lead wherever possible, increasing both the quality of the lab part and each team member's knowledge.

Lab Part		Estimated Time	Design		Test	
			Lead	Deadline	Lead	Deadline
Software-Scheduled Pipeline	Control Signals	0.5 hr	Josh	11/4	Joseph	11/5
	Datapath	3 hr	Josh	11/8	Joseph	11/9
	Testing	3 hr	ALL	11/10	ALL	11/11
	Synthesis (human effort)	0.5 hr	ALL	11/12	ALL	11/13
Hardware-Scheduled Pipeline	Pipeline Register Update	1 hr	Joseph	11/10	Evan	11/11
	Data Hazard Avoidance	4 hr	Evan	11/12	Josh	11/13
	Control Hazard Avoidance	2-6 hr based on group size	ALL	11/14	Josh	11/15
	Integration (Hardware-Schedule Pipeline)	3 hr	Joseph	11/18	Evan	11/19
	Testing	3 hr	ALL	11/20	ALL	11/21
	Synthesis	0.5 hr	ALL	11/20	ALL	11/21

*Estimated Time is given as a **very rough** guide for even distribution of tasks assuming you've already read through the lab document and have the prerequisite knowledge. Please note that to be done properly, the test programs will require significant time investment, but will result in a much stronger final design.*

Integrity of Work: Do not delete the following. We agree that the work we provide to other team members and ultimately submit for a grade is a direct result of our own work as described in the course syllabus. Specifically, we will generate all VHDL code ourselves and not copy VHDL code from online sources, other groups, book companion material, or past student projects to which anyone outside of my team has contributed.

Student Signature Joshua Arceo

Date 10/30/24

Student Signature Joseph Barnes III

Date 10/30/24

Student Signature Evan Shiber

Date 10/30/24