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January 29, 2019

PROJECT 7

Due: March 23, 2017

Integrated 16-bit architecture with a custom 3-stage pipeline module

OBJECTIVES:

1. Design, simulate and implement a 3-state pipeline system in VHDL using Intel Quartus Prime and compare it to a reference system without pipeline to verify the performance enhancement. Your system should have the following features:

   Reference system:

   a. Modify the simple CPU example given in class to include a memory module that has 4kbytes of 16 bits words (address width of 12 bits). See appendix for a suggested approach. System modification requires changing the microprocessor module (change address width) and the controller module (to deal with the new memory timing) in addition to the memory module.
   b. Write a benchmark program for matrix addition that can run in the reference architecture. Matrix size should be at least 15x15.

   Enhanced system:

   i. Modify the CPU example given to upgrade the system with a pipeline order 3. (SimpleCompArch2019_InstCycleOptimized4Pipelining). You should follow the next steps:
      1. Analyze all the supported micro-instructions and determine: number of cycles needed to execute, resources required in each cycle and resource conflict that exist between each one of the micro-instructions if they were executing concurrently.
      2. Analyze what are the modifications required to resolve the resource conflicts with minimum changes to the architecture. Some of the changes could be, if needed:
         a. Modifying the controller module to allow 3 instructions be fetch, decoded and executed concurrently.
         b. Add another port to the memory for reading data and instruction concurrently, add more ports to the register file, etc.
      3. Run the benchmark program wrote above in the new architecture to evaluate performance enhancement.

   c. Design an interface that enables you to run your benchmark program in the DE2-115 boards used in the lab and debug the results.

   Hint. You can display the results using the seven-segment, LCD or VGA displays. Halt the processor when the output values are available and use one of the push button to resume displaying the results. A de-bouncing mechanism must be used with the push button to avoid recurrent program without displaying the results.

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Deliverables:
A project report will be submitted digitally (through D2L dropbox) with the following information:

i. Introduction
ii. Design
- Should contain information about the HW and SW modifications introduced.
- Should contain the analysis made to the instruction set in order to introduce the pipeline.
- Should explain any HW changed introduced to support the pipeline.

iii. Results
- Should contain results of the simulation of the systems with and without the pipeline implementation when executing the requested matrix multiplication code.
- Results of your performance evaluation on the architectures.

iv. Conclusion: conclusions about the implementation of the modifications to the system highlighting strength and weaknesses.

Report (20%):
The report should not exceed 10 single spaced pages written with "Times New Roman" font size 10. You can attach additional pages as appendix.

Demonstration (60%):
Students will demonstrate the developed architecture in the lab for all other teams in the course.
Marking scheme:
- Reference System – 15%
- Enhanced system – 25%
- SW completion – 5%
- Board implementation and visualization of results – 15%

Presentation (20%):
All team will have 15 minutes presentation followed by 10 minutes questions. Each team member must present a part of the research and will be evaluated based upon his/her performance presenting the project and answering the questions.

All the dates for all the activities are displayed in the course schedule.

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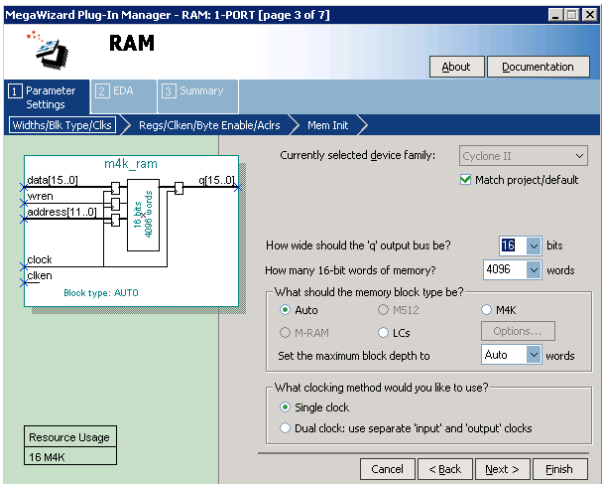
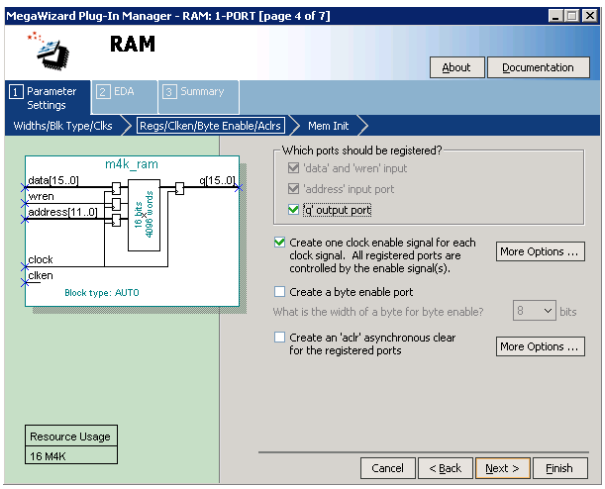
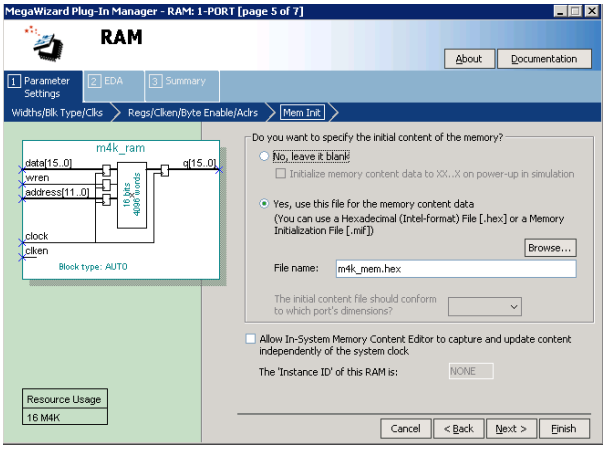
Appendix







*Figures show the memory module M4K but the FPGA in the DE2Board has M9K modules. The design procedure, however, is the same.