NOTE: Use of internet is permitted **only** to access software website, calculators are permitted and your answers must include worked solutions. If you require extra sheet(s) please write your name and student number at the top of each additional sheet. <https://logic.ly/>

# Part A

## Objective

Understand various logic gates

|  |
| --- |
| 1. Draw a labelled Gate Symbol, Functional Notation and truth table for the gates listed in the table below: |
| |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | **Inputs** | |  | **Output(s) Truth Table** | | |  | | **A** | **B** | **AND** | **OR** | **XOR** | **NAND** | **NOR** | | **0** | **0** | 0 | 0 | 0 | 1 | 1 | | **0** | **1** | 0 | 1 | 1 | 1 | 0 | | **1** | **0** | 0 | 1 | 1 | 1 | 0 | | **1** | **1** | 1 | 1 | 1 | 0 | 0 | | **Gate Symbol** | |  |  |  |  |  | | **Functional**  **Notation** | | A^B | AvB | ¬(A==B) | ¬(A&&B) | ¬(A||B) | |

|  |
| --- |
| 2. Construct the logic circuit below using Lab Logic and detail the functional notation and truth table for a two input **AND** gate.    Switches AND Gate LED Output |
| |  |  |  | | --- | --- | --- | | A | B | AND | | 0 | 0 | 0 | | 0 | 1 | 0 | | 1 | 0 | 0 | | 1 | 1 | 1 | |

# Part B

## Objective

Understand the construction of Logic Gates from various combinations of logic gates

|  |
| --- |
| 1. Using Lab Software prove that combining and **AND** and a **NOT** constructs a **NAND** Gate      **NOTE:** solution must be demonstrated to Lecturer prior to leaving laboratory |
| |  |  |  |  | | --- | --- | --- | --- | | Demonstrated to lecturer | Yes |  | No | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 2. Prove using Lab Software and a truth table that the circuit below is a XOR Gate. Place an LED on the output of the constructed circuit.        **NOTE:** solution must be demonstrated to Lecturer prior to leaving laboratory     |  |  |  | | --- | --- | --- | | **Inputs** | |  | | **A** | **B** | **XOR** | | **0** | **0** | 0 | | **0** | **1** | 1 | | **1** | **0** | 1 | | **1** | **1** | 0 |       A{0} B{0} XOR{0}  Diagram  Description automatically generated with medium confidence  A{0} B{1} XOR{1}  Diagram  Description automatically generated with medium confidence  A{1} B{0} XOR{1}  A picture containing diagram  Description automatically generated  A{1} B{1} XOR{0}  Diagram  Description automatically generated   |  |  |  |  | | --- | --- | --- | --- | | Demonstrated to lecturer | Yes |  | No | |
| 3. Prove DeMorgan’s Law ¬(A  B) = ¬A  ¬B using Lab Software |
| |  |  |  |  | | --- | --- | --- | --- | | Demonstrated to lecturer | Yes |  | No | |

# Part C

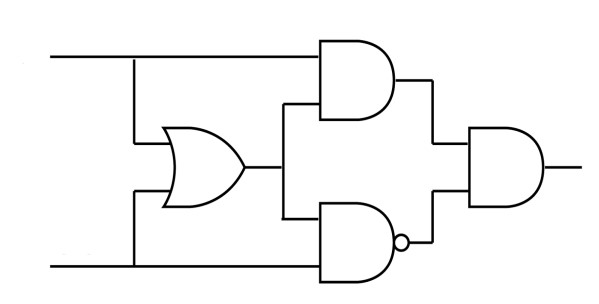
## Objective

1. Understand the construction of Logic Circuits from various combinations of Logic Gates.

1. Record the truth tables for the circuits below

1. Suggest what these circuits could be used for

1

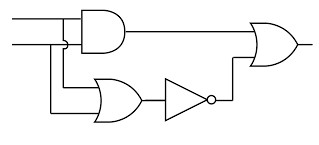


|  |  |  |
| --- | --- | --- |
| A | B | Output |
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |

Use: Light

Switch

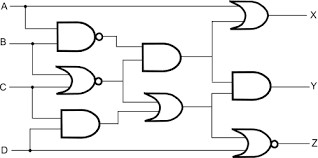
2



|  |  |  |
| --- | --- | --- |
| A | B | Output |
| 0 | 0 | 1 |
| 1 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 1 | 1 |

Use

3



|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| A | B | C | D | X | Y | Z |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 1 | 0 | 1 |

## Hand up this practical report at the end of session and ensure it has been checked

|  |  |  |  |
| --- | --- | --- | --- |
| **Student Name** |  | **Student Number** |  |
| **Date** |  | **Checked** |  |
| **Group** | **A / B** |  |  |