Stephen Lasko
Joshua Dinerman

Lab 1 Report

Design Block 1:

Design block 1 has 2 primary functions. The first is to take the inputs of board-mounted switches and use them to control the corresponding LEDs. When flipped down, each corresponding LED will be off, while flipping the switches up will cause the corresponding LED to turn on. By holding down an onboard button, these operations become inverted, a switch flipped down turning the LEDs on, and a switch flipped up turning them off. This button only inverts the effect while pushed down, and the original settings are restored when released. This is accomplished by simply taking the switch input and inverting it (as a switch flipped down is interpreted as a logic high) before assigning it to the corresponding LEDs, and if the button is pressed, assigning the LEDs to the raw switch input. The second primary function of the design block is to display a birthday on the 7 segment display and switch to another birthday when a second onboard button is pressed. Similar to the other function, the button is only effective when pressed down, and restores the original settings when released. This is accomplished with 2 separate modules. The lowest level module takes in a 32-bit integer outputs an 8-bit display driver, which controls a singular 7 segment display. This is a simple multiplexor, assigning the input integer to its corresponding display configuration. The next module up calls this module for each display. This module has preset integer variables storing each individual integer in the birthdays. It assigns a wire connected to the input of each 7 segment display to the correct value depending on whether the onboard button is being pressed, just like the other function.

The hierarchy is as follows:

- Design1_top.v
    - led_switch.v
    - sevensegcall.v
        - sevenseg.v

Design1_top calls led_switch and sevensegcall, and sevensegcall calls sevenseg.

The testbench starts by assigning all switches to logic low and printing the output of the LEDs, which is logic high. It then simulates holding down the button and showing all LEDs invert. Then, it simulates an input and shows the LEDs reflect that input. Then, it

tests the 7 segment code. It sets the button to unpressed and displays the binary driving each display. It then simulates the button being held down and shows the binary for each display again, now changed to the new date.

We had an issue with the text file, for some reason the text file is blank when vvp is run.

This module works exactly as specified when compiled and uploaded to the DE-10 Lite board.

Design Block 2:

Design block 2 takes the inputs of the switches on the board, and interprets them as 2 4 bit 2s complement numbers. The program calculates the sign and magnitude of the numbers and displays them on the 7 segment displays. It also calculates the sum of the two numbers, and displays OF if an overflow is detected. If one of the onboard buttons is pressed, it subtracts the inputs instead of dividing them. The program uses a value and state table, which determines if the input value is a state or a value, and compares the two inputs to display the correct result.

The hierarchy is as follows:

- Design2_top.v
    - fullAdder.v
    - sevensegcall2.v
        - sevenseg2.v

Design2_top calls fullAdder and sevensegcall2, and sevensegcall2 calls sevenseg2.

The test bench tests positive and negative inputs through both the sum and subtraction modes. It also tests for an overflow. It outputs the results of the 7 segment displays in binary.

The test bench compiles, but there is an issue with inputting the switches and/or outputting LED and 7 segment display status.

This module works exactly as specified when compiled and uploaded to the DE-10 Lite board.

Design Block 3:

The main function of design block 3 is to take in 2 inputs, provided as 2 4 bit binary numbers through the use of the onboard switches. It takes these inputs, and determines if they are equal, or if one is larger. Then, it displays this with the 3 rightmost LEDs on the board. There are also two switches on the left, which when both moved up, interpret the inputs as signed 2s complement numbers, and calculate accordingly. The program also displays these numbers to the onboard 7 segment displays.

The hierarchy is as follows:

- Design3_top.v
    - sevensegcall3.v
        - sevenseg3.v

Design3_top calls sevensegcall3, and sevensegcall3 calls sevenseg3.

Test bench calls numbers greater, less, and equal in unsigned binary and in two's complement. Displays binary representation of seven-segment displays and relevant LEDs.

The test bench compiles, but there is an issue with inputting the switches and/or outputting LED and 7 segment display status.

This module works exactly as specified when compiled and uploaded to the DE-10 Lite board.

Integrated Block:

The design block for integrating all other blocks, named Lab1_top, is a fairly basic program. When the left 2 switches are switched down, it operates design block 1. When the leftmost switch is down, and the second from the left is up, it operates design block 2. When the leftmost switch is up, it operates design block 3, which uses the switch second from the left in its operation. The corresponding LEDs also light up by simply inverting the input from the switches (as they are logic high inputs) and pushing that to the corresponding LEDs. The program works by taking all input from the board and running it through each design block. The block, however, does not directly output their results to the board. Instead, the board outputs are assigned within if statements to whichever design block outputs are desires. The if statements determine which module is selected through the 2 leftmost switches. It then assigns the board outputs to the corresponding outputs of the correct design block.

The hierarchy is as follows:

- Lab1_top.v
    - Design1_top.v
        - led_switch.v
        - sevensegcall.v
            - sevenseg.v
    - Design2_top.v
        - fullAdder.v
        - sevensegcall2.v
            - sevenseg2.v
    - Design3_top.v
        - sevensegcall3.v
            - sevenseg3.v

Lab1 calls each design block. The Design blocks have the same hierarchy as before.

This program requires no test bench, as stated in the project specifications.

This module works exactly as specified when compiled and uploaded to the DE-10 Lite board.