

CPEN 311: Lab 5

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Directory Path of SOF File

The SOF file for this lab is located in the rtl folder of the submission. It is called "dds_and_nios_lab_time_limited.sof".

Status of the Lab

This lab is fully functional. It does everything that the lab handout says, and is identical to the given solution. The bonus was not implemented

How to Run the Simulations

To run the simulations, follow the instructions below:

1. Go to the sim directory, and open "Lab_5.mpf" with ModelSim.
2. To run a simulation, click on "Start Simulation", which is located under "Simulate", in the top toolbar. This will open a "Start Simulation" window.
3. In the "Start Simulation" window, expand the "work" directory, choose the desired testbench "_tb" file, and click "OK".
4. Choose the desired signals to show on the wave form, and then run the simulation. To run the simulation, go to "Simulate", and then, under "Run", click on "Run -All". This will update the waveform window to show the results of the simulation.

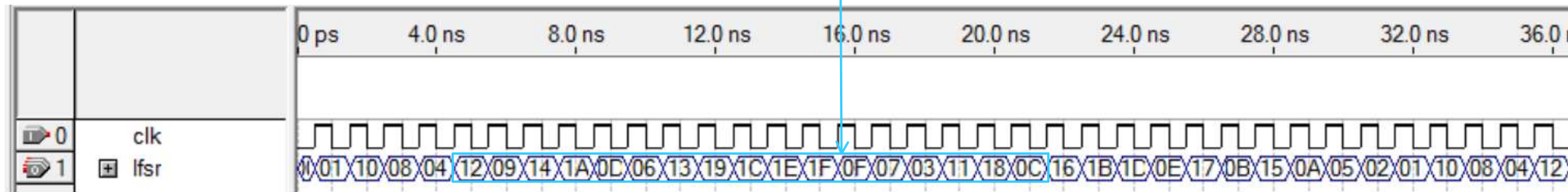
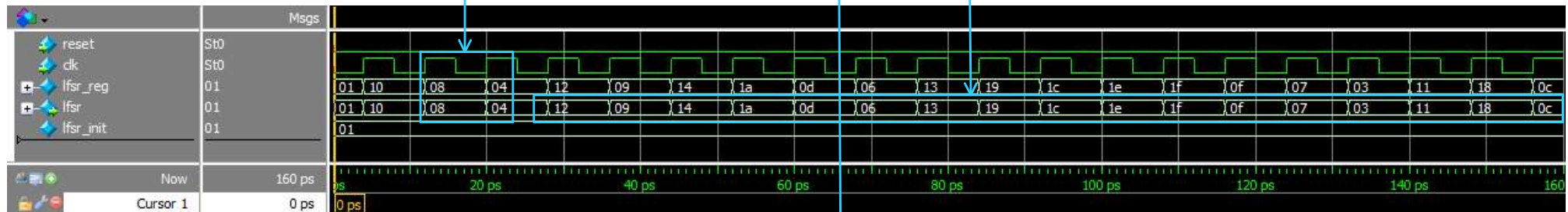
Additional Information

If something appears to be missing, or if a file is corrupt or not working, please email us at ardavanpourkeramati@gmail.com or joshua.wu2009@gmail.com.

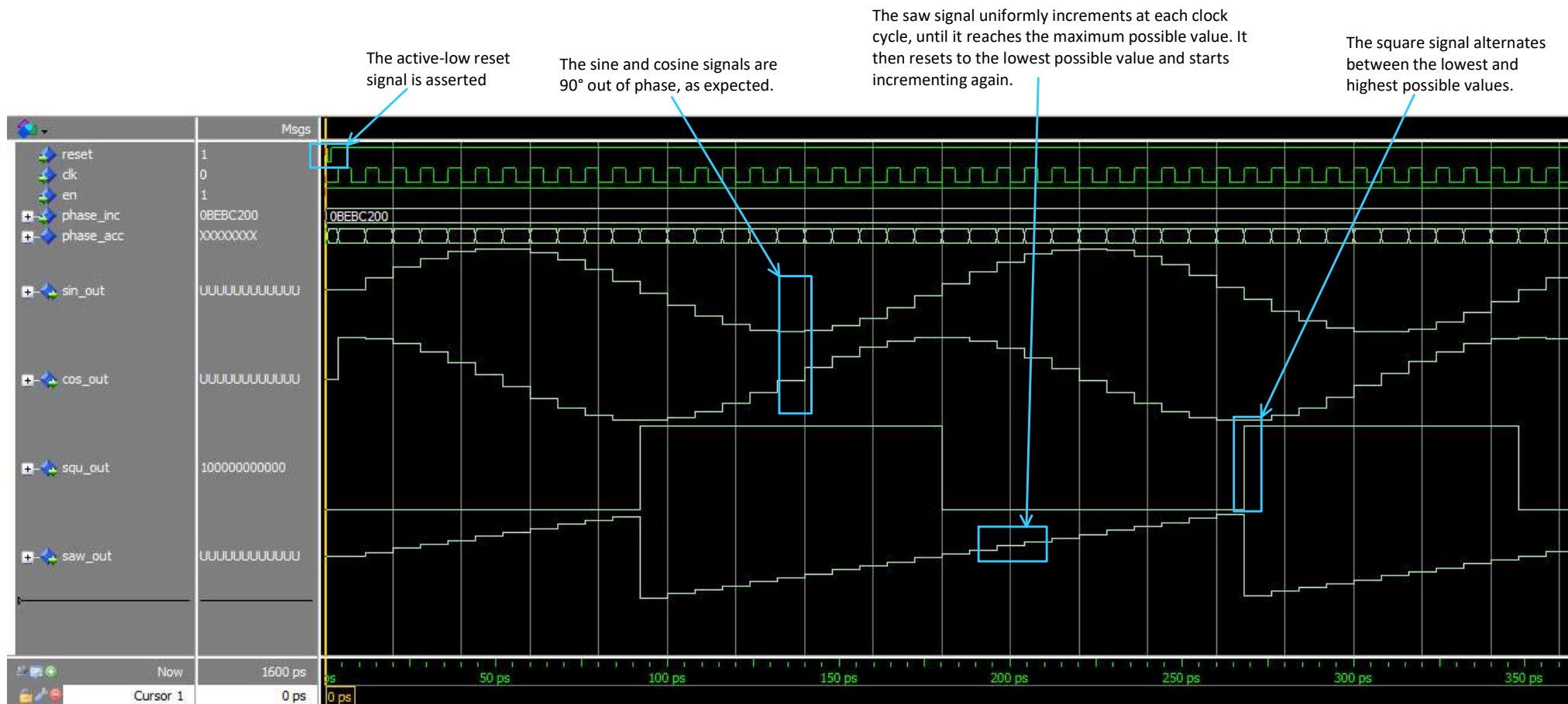
Annotated Simulation of LFSR

At the rising edge of each clock, the lfsr output is updated to the next pseudo-random value.

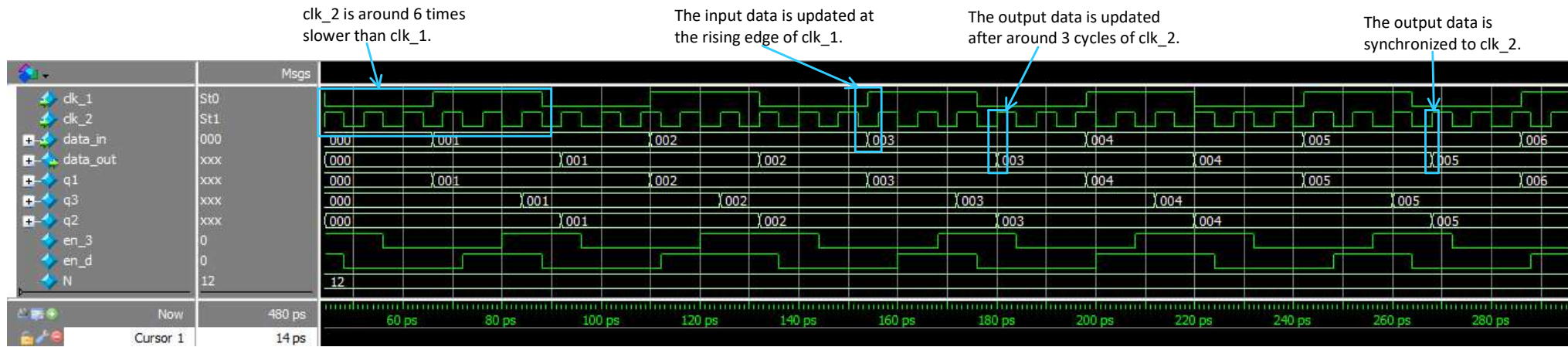
The lfsr values are identical to the values in the Lab 5 instruction manual.



Annotated Simulation of DDS



Annotated Simulation of Slow to Fast Synchronizer

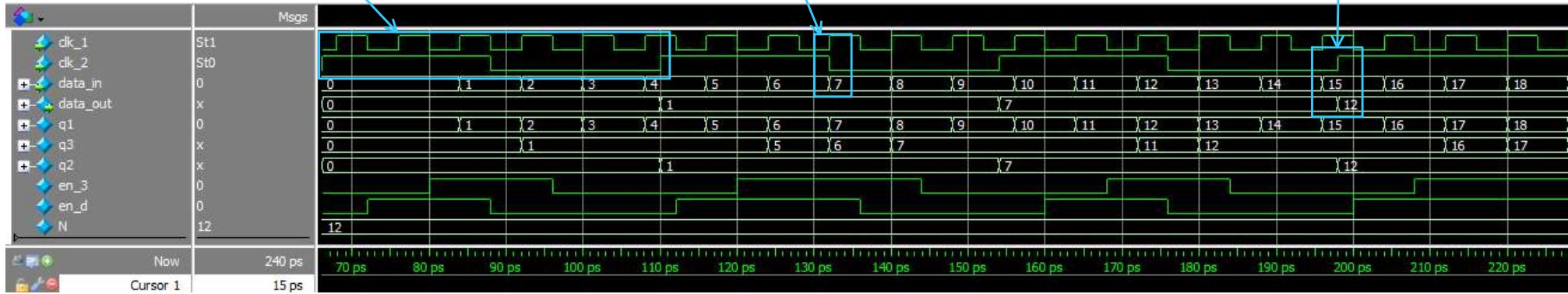


Annotated Simulation of Fast to Slow Synchronizer

clk_1 is around 6 times faster than clk_2.

The input data is updated on each rising edge of clk_1.

On each rising edge of clk_2, the output data is updated with the input data from around 2-3 clk_1 cycles ago. This is due to how the input data is captured and stored for synchronization purposes.



SignalTap Annotation of LFSR Instantiation

SignalTap II Logic Analyzer - C:/Users/joshu/Documents/CPEN311/lab5_submission/rtl/Lab5_template_de1soc/dds_and_nios_lab - dds_and_nios_lab - [SignalTap_Final.stp]

File Edit View Project Processing Tools Window Help

Instance Manager: Ready to acquire

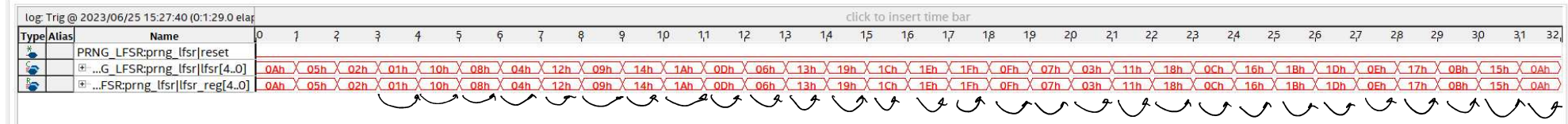
Instance	Status	Enabled	LEs: 2477	Memory: 217	Small: 0/0	Medium: 5/3!	Large: 0/0
inst_lfsr	Not running	<input checked="" type="checkbox"/>	602 cells	5632 bits	0 blocks	1 blocks	0 blocks
inst_dds	Not running	<input checked="" type="checkbox"/>	1875 cells	16128 bits	0 blocks	4 blocks	0 blocks

JTAG Chain Configuration: JTAG ready

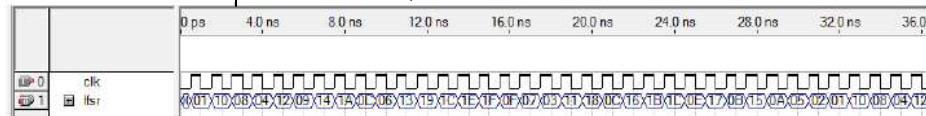
Hardware: DE-SoC [USB-1] Setup...

Device: @2: 5CSE(BA5)MA5 Scan Chain

>> SOF Manager: ne_limited.sof ...

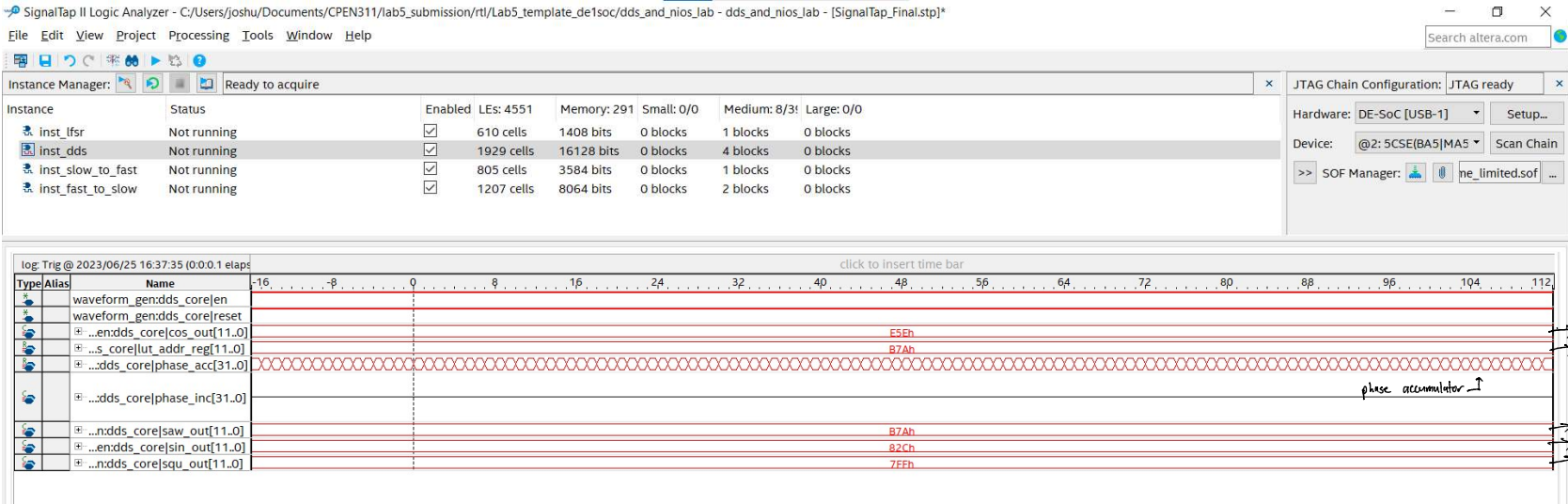
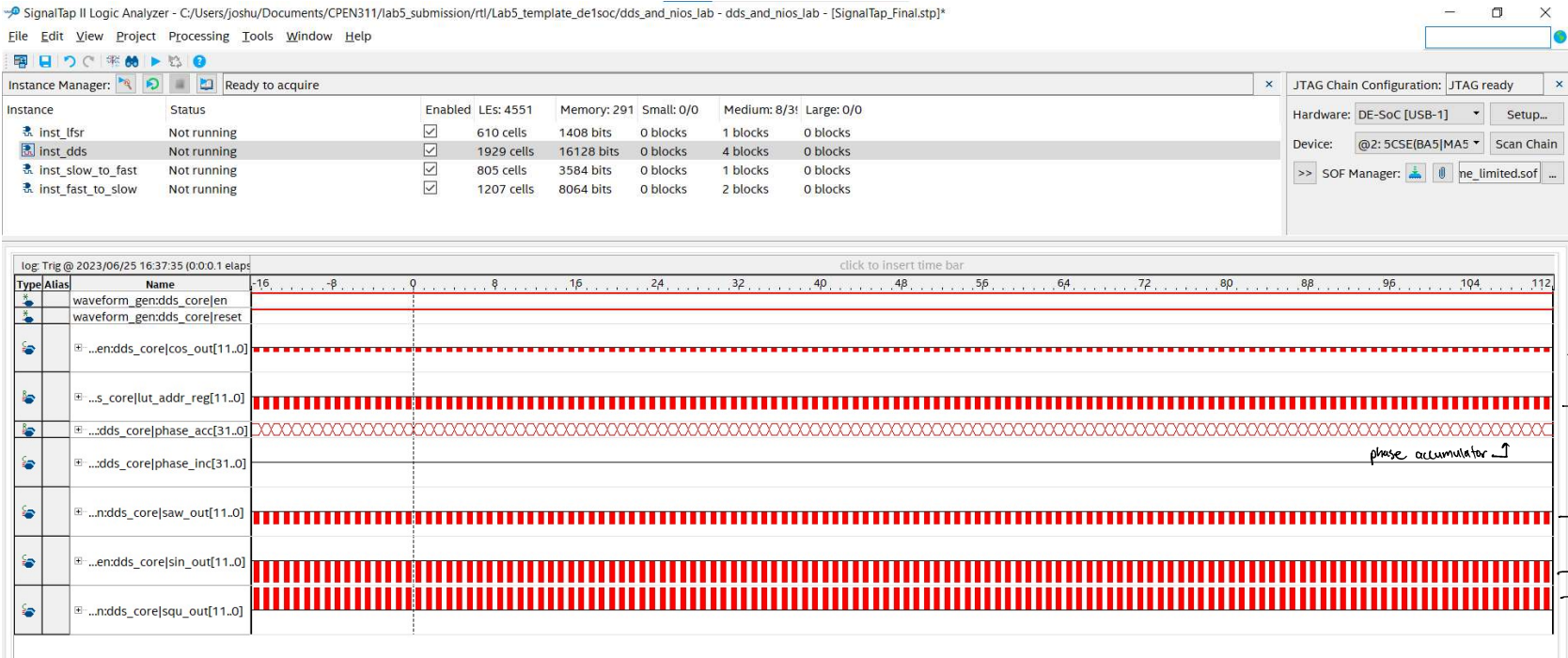


Matches with LFSR sequence in lab manual

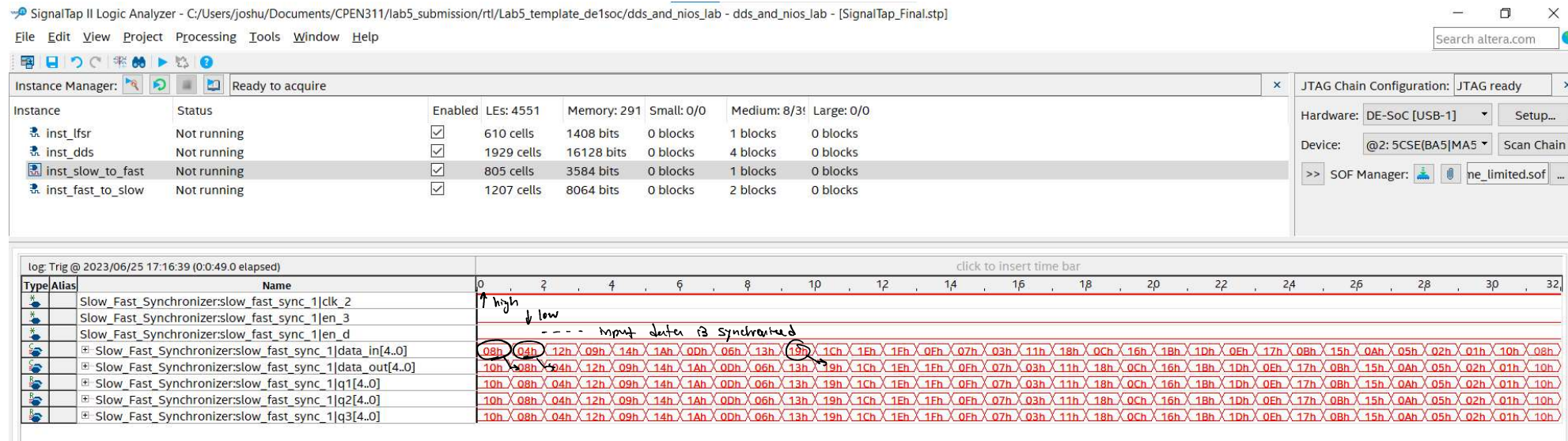


Matches pseudorandom bit sequence

SignalTap Annotation of DDS Instantiation



SignalTap Annotation of Slow to Fast Instantiation



SignalTap Annotation of Fast to Slow Instantiation

SignalTap II Logic Analyzer - C:/Users/joshu/Documents/CPEN311/lab5_submission/rtl/Lab5_template_de1soc/dds_and_nios_lab - dds_and_nios_lab - [SignalTap_Final.stp]

File Edit View Project Processing Tools Window Help

Instance Manager: Ready to acquire

Instance	Status	Enabled	LEs: 4551	Memory: 291	Small: 0/0	Medium: 8/3!	Large: 0/0
inst_lfsr	Not running	<input checked="" type="checkbox"/>	610 cells	1408 bits	0 blocks	1 blocks	0 blocks
inst_dds	Not running	<input checked="" type="checkbox"/>	1929 cells	16128 bits	0 blocks	4 blocks	0 blocks
inst_slow_to_fast	Not running	<input checked="" type="checkbox"/>	805 cells	3584 bits	0 blocks	1 blocks	0 blocks
inst_fast_to_slow	Not running	<input checked="" type="checkbox"/>	1207 cells	8064 bits	0 blocks	2 blocks	0 blocks

JTAG Chain Configuration: JTAG ready

Hardware: DE-SoC [USB-1] Setup...

Device: @2: 5CSE(BA5)MA5 Scan Chain

>> SOF Manager: ne_limited.sof ...

log: Trig @ 2023/06/25 17:18:08 (0:0:0.2 elapsed)

click to insert time bar

Type	Alias	Name	Value
*		Fast_Slow_Synchronizer:fast_slow_sync_1 clk_2	
*		Fast_Slow_Synchronizer:fast_slow_sync_1 en_3	
*		Fast_Slow_Synchronizer:fast_slow_sync_1 en_d	
*		Fast_Slow_Synchronizer:fast_slow_sync_1 data_in[11.0]	667h
*		Fast_Slow_Synchronizer:fast_slow_sync_1 data_out[11.0]	715h
*		Fast_Slow_Synchronizer:fast_slow_sync_1 q1[11.0]	667h
*		Fast_Slow_Synchronizer:fast_slow_sync_1 q2[11.0]	715h
*		Fast_Slow_Synchronizer:fast_slow_sync_1 q3[11.0]	6A6h

667h 715h 6A6h

same as R2