Path Summary

	Property	Value
1	From Node	RAMTest:inst1|altsyncram:altsyncram_component|altsyncram_3vj1:auto_generated|ram_block1a12~porta_re_reg
2	To Node	RAM:data|altsyncram:altsyncram_component|altsyncram_82j1:auto_generated|ram_block1a0~porta_address_reg0
3	Launch Clock	CLK
4	Latch Clock	CLK
5	Data Arrival Time	17.025
6	Data Required Time	12.370
7	Slack	-4.655 (VIOLATED)

Statistics

	Property	Value	Count	Total Delay	% of Total	Min	Max
1	Setup Relationship	10.000					
2	Clock Skew	-0.039					
3	Data Delay	14.664					
4	Number of Logic Levels		13				
5	Physical Delays						
1	Arrival Path						
1	Clock						
1	IC		3	0.930	39	0.000	0.750
2	Cell		3	1.431	61	0.000	0.835
2	Data						
1	IC		18	7.789	53	0.000	1.173
2	Cell		19	6.649	45	0.058	2.444
3	uTco		1	0.226	2	0.226	0.226
2	Required Path						
1	Clock						
1	IC		3	0.916	40	0.000	0.743
2	Cell		3	1.394	60	0.000	0.798

Data Path

Data Arrival

	Total	Incr	RF	Type	Fanout	Location	Element
1	0.000	0.000					launch edge time
2	2.361	2.361					clock path
1	0.000	0.000					source latency
2	0.000	0.000			1	PIN_23	CLK
3	0.000	0.000	RR	IC	1	IOIBUF_X0_Y11_N8	CLK~input|i

	Total	Incr	RF	Type	Fanout	Location	Element
4	0.596	0.596	RR	CELL	1	IOIBUF_X0_Y11_N8	CLK~input|o
5	0.776	0.180	RR	IC	1	CLKCTRL_G2	CLK~inputclkctrl|inclk[0]
6	0.776	0.000	RR	CELL	1255	CLKCTRL_G2	CLK~inputclkctrl|outclk
7	1.526	0.750	RR	IC	3	M9K_X27_Y17_N0	inst1|altsyncram_component|auto_generated| ram_block1a12|clk0
8	2.361	0.835	RR	CELL	4	M9K_X27_Y17_N0	RAMTest:inst1|altsyncram:altsyncram_component| altsyncram_3vj1:auto_generated| ram_block1a12~porta_re_reg
3	17.025	14.664					data path
1	2.587	0.226		uTco	4	M9K_X27_Y17_N0	RAMTest:inst1|altsyncram:altsyncram_component| altsyncram_3vj1:auto_generated| ram_block1a12~porta_re_reg
2	5.031	2.444	FR	CELL	32	M9K_X27_Y17_N0	inst1|altsyncram_component|auto_generated| ram_block1a12|portadataout[2]
3	5.718	0.687	RR	IC	1	LCCOMB_X28_Y17_N20	inst8|inst10|sti~0|datac
4	5.959	0.241	RR	CELL	17	LCCOMB_X28_Y17_N20	inst8|inst10|sti~0|combout
5	6.195	0.236	RR	IC	1	LCCOMB_X28_Y17_N6	inst8|inst10|RnSelect~11|datad
6	6.315	0.120	RF	CELL	29	LCCOMB_X28_Y17_N6	inst8|inst10|RnSelect~11|combout
7	6.744	0.429	FF	IC	1	LCCOMB_X29_Y17_N8	inst8|inst10|RxSelect[1]~0|datac
8	6.986	0.242	FF	CELL	22	LCCOMB_X29_Y17_N8	inst8|inst10|RxSelect[1]~0|combout
9	7.695	0.709	FF	IC	1	LCCOMB_X29_Y20_N10	inst8|inst2|LPM_MUX_component|auto_generated| result_node[3]~0|datac
10	7.937	0.242	FF	CELL	1	LCCOMB_X29_Y20_N10	inst8|inst2|LPM_MUX_component|auto_generated| result_node[3]~0|combout
11	8.137	0.200	FF	IC	1	LCCOMB_X29_Y20_N30	inst8|inst2|LPM_MUX_component|auto_generated| result_node[3]~1|datad
12	8.266	0.129	FR	CELL	8	LCCOMB_X29_Y20_N30	inst8|inst2|LPM_MUX_component|auto_generated| result_node[3]~1|combout
13	9.084	0.818	RR	IC	1	LCCOMB_X25_Y19_N10	inst8|inst16|inst5|LPM_MUX_component| auto_generated|result_node[11]~6|datac
14	9.312	0.228	RF	CELL	8	LCCOMB_X25_Y19_N10	inst8|inst16|inst5|LPM_MUX_component| auto_generated|result_node[11]~6|combout
15	10.269	0.957	FF	IC	1	LCCOMB_X29_Y21_N28	inst8|inst16|inst5|LPM_MUX_component| auto_generated|result_node[0]~136|datab
16	10.611	0.342	FF	CELL	1	LCCOMB_X29_Y21_N28	inst8|inst16|inst5|LPM_MUX_component| auto_generated|result_node[0]~136|combout
17	10.811	0.200	FF	IC	1	LCCOMB_X29_Y21_N6	inst8|inst16|inst5|LPM_MUX_component| auto_generated|result_node[0]~137|datad
18	10.921	0.110	FF	CELL	18	LCCOMB_X29_Y21_N6	inst8|inst16|inst5|LPM_MUX_component| auto_generated|result_node[0]~137|combout
19	11.842	0.921	FF	IC	1	LCCOMB_X24_Y19_N4	inst8|inst6|LPM_ADD_SUB_component|

	Total	Incr	RF	Type	Fanout	Location	Element
							auto_generated|_~16|datad
20	11.952	0.110	FF	CELL	1	LCCOMB_X24_Y19_N4	inst8|inst6|LPM_ADD_SUB_component| auto_generated|_~16|combout
21	12.188	0.236	FF	IC	2	LCCOMB_X24_Y19_N16	inst8|inst6|LPM_ADD_SUB_component| auto_generated|result_int[1]~2|datab
22	12.634	0.446	FR	CELL	1	LCCOMB_X24_Y19_N16	inst8|inst6|LPM_ADD_SUB_component| auto_generated|result_int[1]~2|cout
23	12.634	0.000	RR	IC	2	LCCOMB_X24_Y19_N18	inst8|inst6|LPM_ADD_SUB_component| auto_generated|result_int[2]~4|cin
24	13.071	0.437	RF	CELL	3	LCCOMB_X24_Y19_N18	inst8|inst6|LPM_ADD_SUB_component| auto_generated|result_int[2]~4|combout
25	13.498	0.427	FF	IC	2	LCCOMB_X23_Y19_N18	inst8|inst3|LPM_ADD_SUB_component| auto_generated|result_int[1]~2|datab
26	13.944	0.446	FR	CELL	1	LCCOMB_X23_Y19_N18	inst8|inst3|LPM_ADD_SUB_component| auto_generated|result_int[1]~2|cout
27	13.944	0.000	RR	IC	2	LCCOMB_X23_Y19_N20	inst8|inst3|LPM_ADD_SUB_component| auto_generated|result_int[2]~4|cin
28	14.002	0.058	RF	CELL	1	LCCOMB_X23_Y19_N20	inst8|inst3|LPM_ADD_SUB_component| auto_generated|result_int[2]~4|cout
29	14.002	0.000	FF	IC	2	LCCOMB_X23_Y19_N22	inst8|inst3|LPM_ADD_SUB_component| auto_generated|result_int[3]~6|cin
30	14.060	0.058	FR	CELL	1	LCCOMB_X23_Y19_N22	inst8|inst3|LPM_ADD_SUB_component| auto_generated|result_int[3]~6|cout
31	14.060	0.000	RR	IC	2	LCCOMB_X23_Y19_N24	inst8|inst3|LPM_ADD_SUB_component| auto_generated|result_int[4]~8|cin
32	14.497	0.437	RF	CELL	2	LCCOMB_X23_Y19_N24	inst8|inst3|LPM_ADD_SUB_component| auto_generated|result_int[4]~8|combout
33	15.067	0.570	FF	IC	1	LCCOMB_X23_Y19_N4	inst8|inst4|LPM_MUX_component|auto_generated| result_node[4]~11|datac
34	15.309	0.242	FF	CELL	5	LCCOMB_X23_Y19_N4	inst8|inst4|LPM_MUX_component|auto_generated| result_node[4]~11|combout
35	15.535	0.226	FF	IC	1	LCCOMB_X23_Y19_N10	mux2|$00000|auto_generated|result_node[4]~4|datac
36	15.776	0.241	FF	CELL	4	LCCOMB_X23_Y19_N10	mux2|$00000|auto_generated|result_node[4]~4| combout
37	16.949	1.173	FF	IC	1	M9K_X27_Y18_N0	data|altsyncram_component|auto_generated| ram_block1a0|portaaddr[4]
38	17.025	0.076	FF	CELL	0	M9K_X27_Y18_N0	RAM:data|altsyncram:altsyncram_component| altsyncram_82j1:auto_generated| ram_block1a0~porta_address_reg0

Data Required

	Total	Incr	RF	Type	Fanout	Location	Element
1	10.000	10.000					latch edge time
2	12.322	2.322					clock path
1	10.000	0.000					source latency
2	10.000	0.000			1	PIN_23	CLK
3	10.000	0.000	RR	IC	1	IOIBUF_X0_Y11_N8	CLK~input|i
4	10.596	0.596	RR	CELL	1	IOIBUF_X0_Y11_N8	CLK~input|o
5	10.769	0.173	RR	IC	1	CLKCTRL_G2	CLK~inputclkctrl|inclk[0]
6	10.769	0.000	RR	CELL	1255	CLKCTRL_G2	CLK~inputclkctrl|outclk
7	11.512	0.743	RR	IC	3	M9K_X27_Y18_N0	data|altsyncram_component|auto_generated|ram_block1a0|clk0
8	12.310	0.798	RR	CELL	0	M9K_X27_Y18_N0	RAM:data|altsyncram:altsyncram_component|altsyncram_82j1:auto_generated|ram_block1a0~porta_address_reg0
9	12.322	0.012					clock pessimism removed
3	12.370	0.048		uTsu	0	M9K_X27_Y18_N0	RAM:data|altsyncram:altsyncram_component|altsyncram_82j1:auto_generated|ram_block1a0~porta_address_reg0