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Título: GPIOs, Timers y FSM

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1. Resumen

2. Nota teórica

En esta sección se muestran las descripciones generales de todos los componentes usados para construir el circuito solicitado.

Microcontrolador ATTiny4313

El ATtiny2313A/4313 es un microcontrolador CMOS de 8 bits de bajo consumo basado en el AVR mejorado. Arquitectura RISC. Al ejecutar poderosas instrucciones en un solo ciclo de reloj, el ATtiny2313A/4313 logra rendimientos cercanos a 1 MIPS por MHz, lo que permite al sistema diseñador para optimizar el consumo de energía frente a la velocidad de procesamiento [1]. Por lo que se requiere estudiar el diagrama de pines mostrado en la figura 1

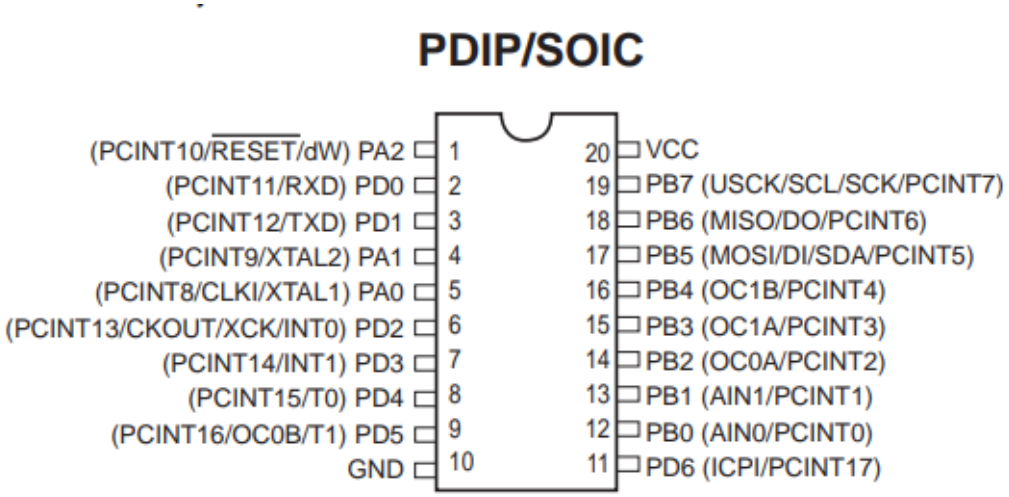


Figura 1: Pines del ATtiny4313. Tomado de [1].

Características generales

A continuación, se describen las características de cada pin para tener un mejor entendimiento de lo que se puede hacer con cada uno de ellos [1].

1. PA2-RESET/dW/PCINT10: RESET: entrada activa en bajo y activada por un 1 el `RSTDISBL` fuse. El pullup se activa y el controlador de salida y la entrada digital se desactivan cuando se usa el pin de RESET. `dW`: Cuando el fusible debugWIRE Enable (DWEN) está programado y los bits de bloqueo están sin programar, se activa el sistema debugWIRE dentro del dispositivo de destino. El pin RESET del puerto está configurado como un pin de I/O bidireccional de cable Y (drenaje abierto) con pull-up habilitado y se convierte en la puerta de enlace de comunicación entre el objetivo y el emulador. Sirve como I/O y tiene la opción de RESET. Solo que debe ponersele un 0 para que funcione como I/O. Tiene una resistencia interna de pull up. `PCINT10`: Fuente de interrupción de cambio de pin. El pin PA2 sirve como una fuente de interrupción externa.

2. PD0-RXD/PCINT11. `RXD`: UART receptor de datos. `PCINT11`: El pin PD0 sirve como fuente de interrupción externa.

3. PD1-TXD/PCINT12. `TXD`: UART transmisor de datos. `PCINT12`: El pin PD0 sirve como fuente de interrupción externa.

4. PA1-XTAL2/PCINT9. `XTAL2`: chip de reloj oscilador. Se utiliza como pin de reloj para todas las fuentes de reloj de chip excepto oscilador RC interno calibrable y reloj externo. Cuando se utiliza como pin de reloj, el pin no se puede utilizar como pin de I/O. Cuando se utiliza un oscilador RC interno calibrable o un reloj externo como en las fuentes de reloj del chip, PA1 sirve como un pin de I/O normal. Este pin sirve como fuente de interrupción externa.

5. PA0-`XTAL1/CLKI/PCINT8`. `XTAL1`: oscilador de reloj de chip. Se utiliza para todas las fuentes de reloj de chip excepto oscilador RC interno calibrable. Cuando se usa como pin de reloj, el pin no se puede usar como pin de I/O. Cuando se utiliza un oscilador RC interno calibrable como fuente de reloj de chip, PA0 sirve como pin de I/O. Este pin sirve como fuente de interrupción externa.

6. PD2-INT0/XCK/CKOUT/PCINT13. `INTO`: este pin sirve como fuente de interrupción externa para el MCU. `XCK`: USART Reloj de transferencia utilizado sólo en el modo de transferencia síncrona.`CKOUT`: reloj sistema de salida.

7. PD3-INT1/PCINT14. Ambas descripciones representan la misma equivalencia, ya que su objetivo final es que el pin PD3 sirve como fuente de interrupción externa.

8. PD4-TO/PCINT15. `TO`: timer/counter0 la entrada del reloj contador externo se habilita configurando (uno) los bits CS02 y CS01 en el registro de control del timer/counter0 (TCCR0).`PCINT15`: este pin sirve como fuente de interrupción externa.

9. PD5-OC0B/T1/PCINT16.`OC0B`: Output Compare Match B. `T1`: La entrada del contador externo se habilita configurando (uno) los bits CS02 y CS01 en el registro de control del timer1/counter1 (TCCR1) `PCINT16`: este pin sirve como fuente de interrupción externa.

10. GND: nodo de tierra.

11. PD6-ICPI/PCINT17.`ICPI`: entrada de captura. Este pin puede actuar como un pin de captura de entrada para el timer/counter1. `PCINT17`: este pin sirve como fuente de interrupción externa.

12. PB0-AIN0/PCINT0. `AIN0`: es un comparador análogo de entrada positiva. Configure el pin del puerto como entrada con el pull-up interno apagado para evitar que la función del puerto digital interfiera con la función del comparador analógico `PCINT0`: este pin sirve como fuente de interrupción externa.

13. PB1-AIN1/PCINT1. `AIN1`: es un comparador análogo de entrada negativa. `PCINT1`: este pin sirve como fuente de interrupción externa.

14. PB2-OC0A/PCINT2.Output Compare Match A output. `OC0A`: el pin PB2 puede servir como salida externa para comparación de salida de timer/counter0 A. El pin debe configurarse como salida (configurando DDB2 igual 1) y cumplir esta función. `PCINT2`: este pin sirve como fuente de interrupción externa.

15. PB3-OC1A/PCINT3. `OC1A`:Output Compare Match A output. El pin PB3 puede servir como salida externa para comparación de salida de timer/counter1 A. El pin debe configurarse como salida (configurando DDB3 igual 1) y cumplir esta función. `PCINT3`: este pin sirve como fuente de interrupción externa.

16. PB4-OC1B/PCINT4. `OC1B`: Output Compare Match B output. Se puede configurar DDB4 igual a 1 para activar esta función. `PCINT4`: este pin sirve como fuente de interrupción externa.

17. PB5-DI/SDA/PCINT5.`DI`: Entrada de datos de interfaz serie universal en modo de tres cables. El modo de tres cables no anula las funciones normales del puerto, por lo que el pin debe configurarse como entrada.`SDA`: modo serial interfaz de datos de dos cables.`PCINT5`: este pin sirve como fuente de interrupción externa.

18. PB6-DO/PCINT6. `DO`: Salida de datos de interfaz serie universal en modo de tres cables. Modo de tres cables de salida de datos anula el valor de PORTB6 y se dirige al puerto cuando el bit de dirección de datos DDB6 es uno. Sin embargo, el bit PORTB6 aún controla el pull-up, lo que permite el pull-up si se ingresa la dirección y PORTB6 en 1. `PCINT6`: este pin sirve como fuente de interrupción externa.

19. PB7-USCK/SCL/PCINT7. `USCK`: interfaz serial de reloj modo de 3 cables. `SCL`: reloj serial para USI modo de dos cables. `PCINT7`: este pin sirve como fuente de interrupción externa.

20. VCC: fuente de alimentación.

En la figura 2 se muestra el diagrama de bloques de este microcontrolador.

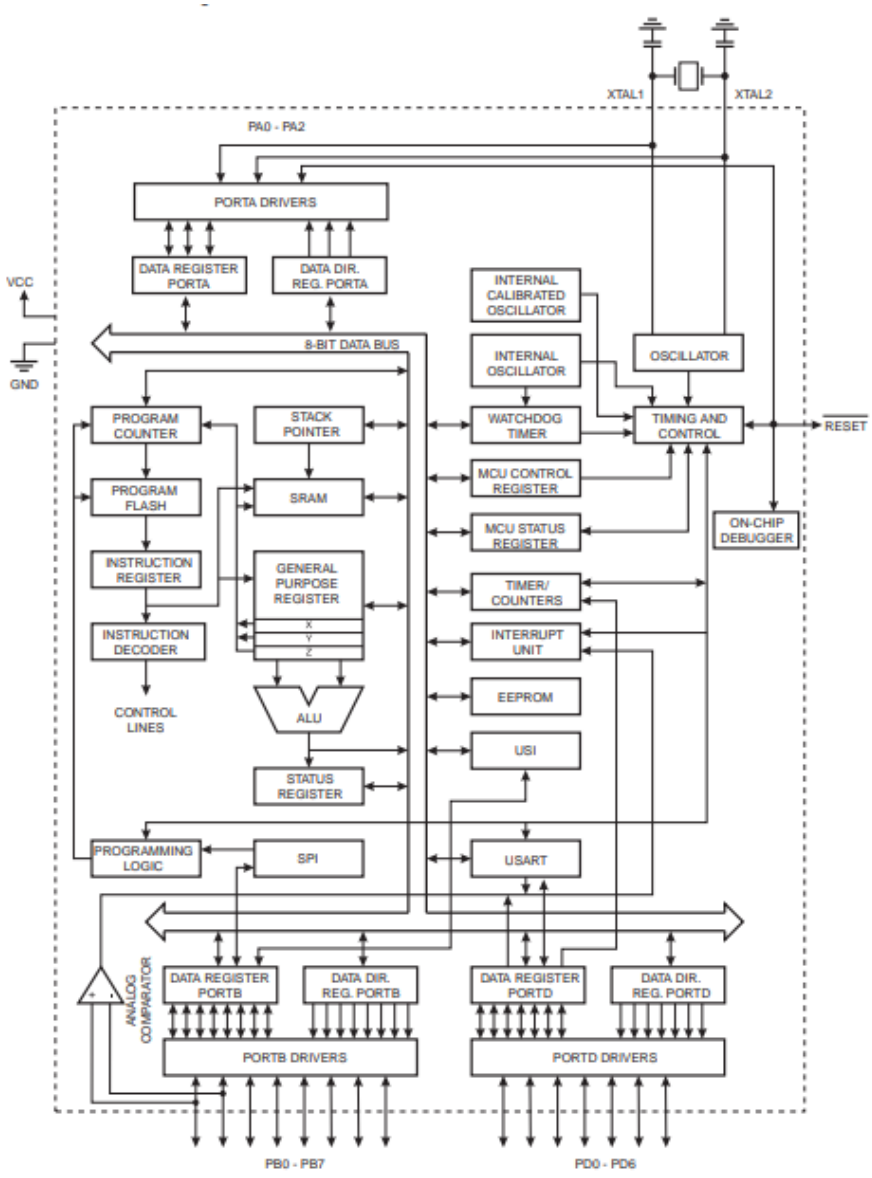
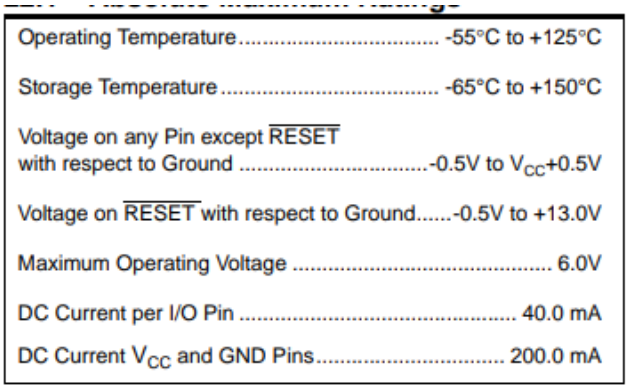


Figura 2: Diagrama de bloques del ATtiny4313. Tomado de [1].

Otro detalle importante es considerar los valores máximos con los que se puede trabajar el ATtiny4313.



Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin except $\overline{\text{RESET}}$ with respect to Ground	-0.5V to V_{CC}+0.5V
Voltage on $\overline{\text{RESET}}$ with respect to Ground	-0.5V to +13.0V
Maximum Operating Voltage	6.0V
DC Current per I/O Pin	40.0 mA
DC Current V_{CC} and GND Pins	200.0 mA

Figura 3: Diagrama de bloques del ATtiny4313. Tomado de [1].

Lista de componentes

Tabla 1: Lista de equipos

Componente	Cantidad	Precio
-	-	-
-	-	-
Total		

Diseño del circuito

3. Desarrollo/Análisis

4. Conclusiones y recomendaciones

Referencias

[1] Atmel. Features attiny2313a/attiny4313. Atmel, https://ww1.microchip.com/downloads/en/DeviceDoc/doc8246.pdf, Agosto 2017. Accedido en enero de 2024.

5. Anexos

Aquí van las hojas del fabricante de los componentes usados para este laboratorio.

Features

- High Performance, Low Power AVR® 8-Bit Microcontroller
- Advanced RISC Architecture
  - 120 Powerful Instructions – Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 20 MIPS Throughput at 20 MHz
- Data and Non-volatile Program and Data Memories
  - 2/4K Bytes of In-System Self Programmable Flash
    - Endurance 10,000 Write/Erase Cycles
  - 128/256 Bytes In-System Programmable EEPROM
    - Endurance: 100,000 Write/Erase Cycles
  - 128/256 Bytes Internal SRAM
  - Programming Lock for Flash Program and EEPROM Data Security
- Peripheral Features
  - One 8-bit Timer/Counter with Separate Prescaler and Compare Mode
  - One 16-bit Timer/Counter with Separate Prescaler, Compare and Capture Modes
  - Four PWM Channels
  - On-chip Analog Comparator
  - Programmable Watchdog Timer with On-chip Oscillator
  - USI – Universal Serial Interface
  - Full Duplex USART
- Special Microcontroller Features
  - debugWIRE On-chip Debugging
  - In-System Programmable via SPI Port
  - External and Internal Interrupt Sources
  - Low-power Idle, Power-down, and Standby Modes
  - Enhanced Power-on Reset Circuit
  - Programmable Brown-out Detection Circuit
  - Internal Calibrated Oscillator
- I/O and Packages
  - 18 Programmable I/O Lines
  - 20-pin PDIP, 20-pin SOIC, 20-pad MLF/VQFN
- Operating Voltage
  - 1.8 – 5.5V
- Speed Grades
  - 0 – 4 MHz @ 1.8 – 5.5V
  - 0 – 10 MHz @ 2.7 – 5.5V
  - 0 – 20 MHz @ 4.5 – 5.5V
- Industrial Temperature Range: -40°C to +85°C
- Low Power Consumption
  - Active Mode
    - 190 µA at 1.8V and 1MHz
  - Idle Mode
    - 24 µA at 1.8V and 1MHz
  - Power-down Mode
    - 0.1 µA at 1.8V and +25°C

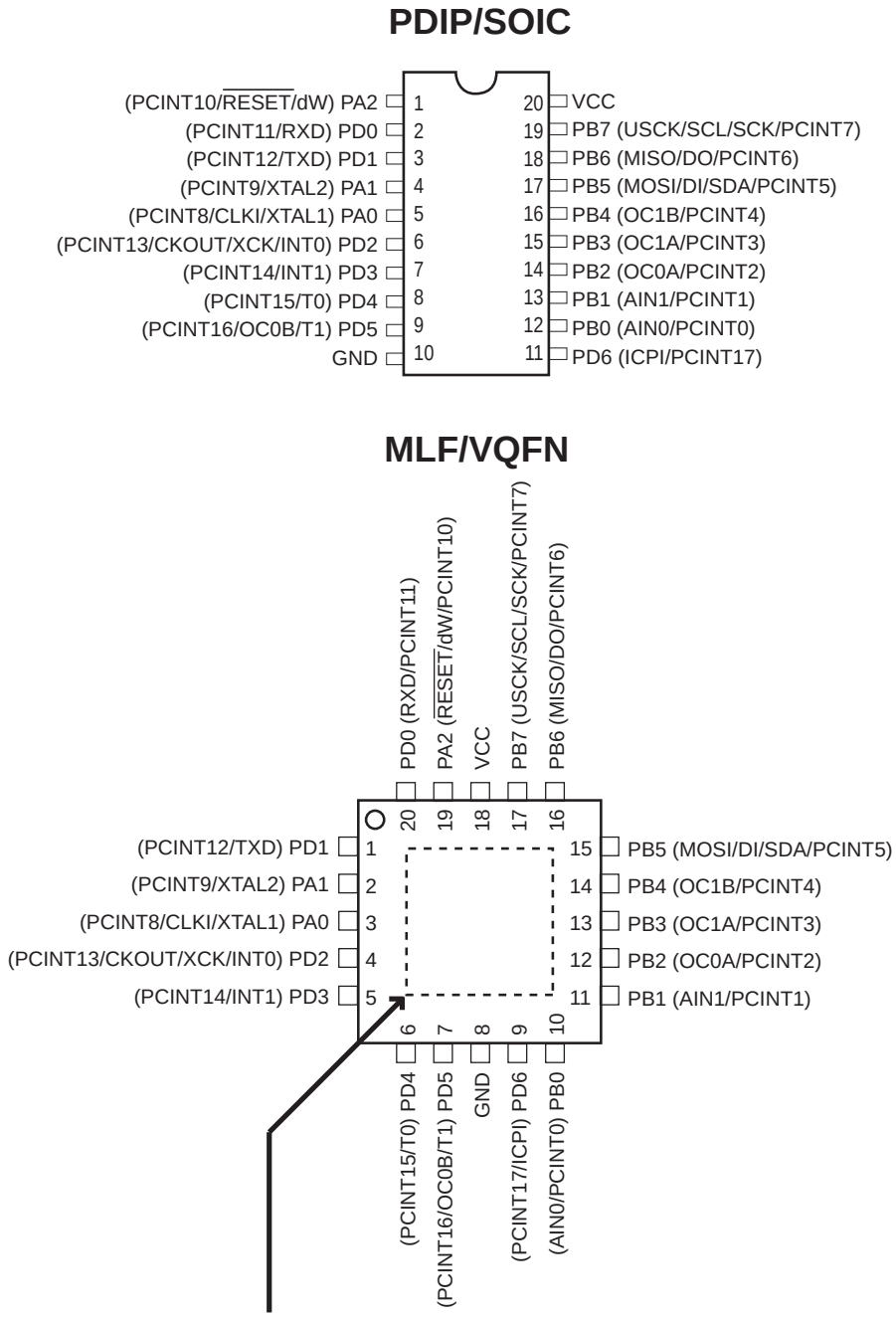
8-bit AVR® Microcontroller with 2/4K Bytes In-System Programmable Flash

ATtiny2313A
ATtiny4313

Rev. 8246B–AVR–09/11

1. Pin Configurations

Figure 1-1. Pinout ATtiny2313A/4313



NOTE: Bottom pad should be soldered to ground.

1.1 Pin Descriptions

1.1.1 VCC

Digital supply voltage.

1.1.2 GND

Ground.

1.1.3 Port A (PA2..PA0)

Port A is a 3-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability, except PA2 which has the $\overline{\text{RESET}}$ capability. To use pin PA2 as I/O pin, instead of RESET pin, program (“0”) RSTDISBL fuse. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the ATtiny2313A/4313 as listed on page 62.

1.1.4 Port B (PB7..PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATtiny2313A/4313 as listed on page 63.

1.1.5 Port D (PD6..PD0)

Port D is a 7-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATtiny2313A/4313 as listed on page 67.

1.1.6 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running and provided that the reset pin has not been disabled. The minimum pulse length is given in Table 22-3 on page 201. Shorter pulses are not guaranteed to generate a reset. The Reset Input is an alternate function for PA2 and dW.

The reset pin can also be used as a (weak) I/O pin.

1.1.7 XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit. XTAL1 is an alternate function for PA0.

1.1.8 XTAL2

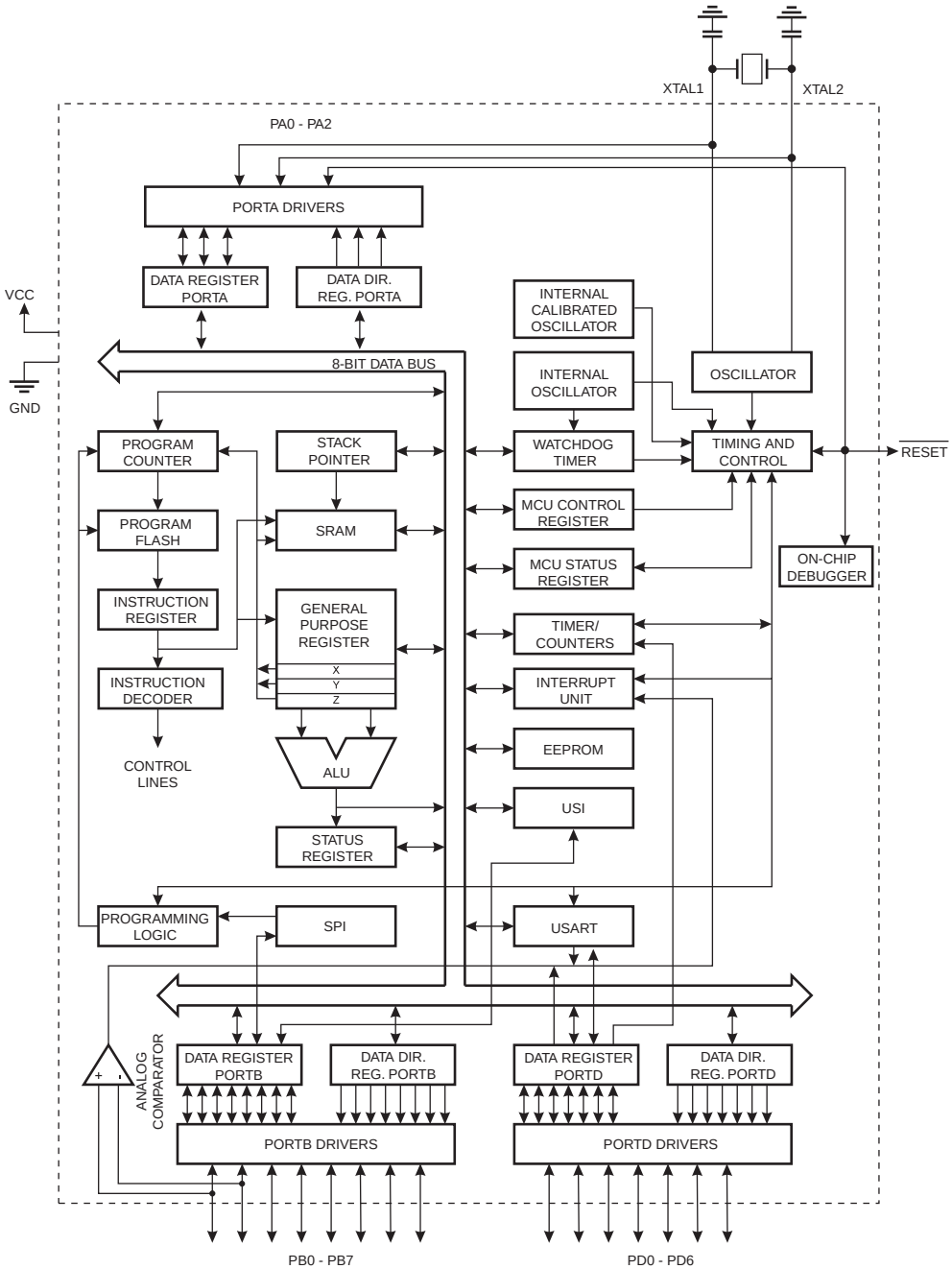
Output from the inverting Oscillator amplifier. XTAL2 is an alternate function for PA1.

2. Overview

The ATtiny2313A/4313 is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny2313A/4313 achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block Diagram

Figure 2-1. Block Diagram



10.2.1 Alternate Functions of Port A

The Port A pins with alternate function are shown in Table 10-3.

Table 10-3. Port A Pins Alternate Functions

Port Pin	Alternate Function
PA0	XTAL1: Crystal Oscillator Input CLKI: External Clock Input PCINT8: Pin Change Interrupt 1, Source 8
PA1	XTAL2: Crystal Oscillator Output PCINT9: Pin Change Interrupt 1, Source 9
PA2	$\overline{\text{RESET}}$: Reset pin dW: debugWire I/O PCINT10: Pin Change Interrupt 1, Source 10

- **Port A, Bit 0 – XTAL1/CLKI/PCINT8**
  - XTAL1: Chip Clock Oscillator pin 1. Used for all chip clock sources except internal calibratable RC oscillator. When used as a clock pin, the pin can not be used as an I/O pin. When using internal calibratable RC Oscillator as a chip clock source, PA0 serves as an ordinary I/O pin.
  - CLKI: Clock Input from an external clock source, see “External Clock” on page 27.
  - PCINT8: Pin Change Interrupt source 8. The PA0 pin can serve as an external interrupt source for pin change interrupt 1.

- **Port A, Bit 1 – XTAL2/PCINT9**
  - XTAL2: Chip Clock Oscillator pin 2. Used as clock pin for all chip clock sources except internal calibratable RC Oscillator and external clock. When used as a clock pin, the pin can not be used as an I/O pin. When using internal calibratable RC Oscillator or External clock as a Chip clock sources, PA1 serves as an ordinary I/O pin.
  - PCINT9: Pin Change Interrupt source 9. The PA1 pin can serve as an external interrupt source for pin change interrupt 1.

- **Port A, Bit 2 – $\overline{\text{RESET}}$/dW/PCINT10**
  - $\overline{\text{RESET}}$: External $\overline{\text{Reset}}$ input is active low and enabled by unprogramming (“1”) the RSTDISBL Fuse. Pullup is activated and output driver and digital input are deactivated when the pin is used as the $\overline{\text{RESET}}$ pin.
  - dW: When the debugWIRE Enable (DWEN) Fuse is programmed and Lock bits are unprogrammed, the debugWIRE system within the target device is activated. The RESET port pin is configured as a wire-AND (open-drain) bi-directional I/O pin with pull-up enabled and becomes the communication gateway between target and emulator.
  - PCINT10: Pin Change Interrupt source 10. The PA2 pin can serve as an external interrupt source for pin change interrupt 1.

Table 10-4 relates the alternate functions of Port A to the overriding signals shown in Figure 10-5 on page 60.

Table 10-4. Overriding Signals for Alternate Functions in PA2..PA0

Signal Name	PA2/RESET/dW/PCINT10	PA1/XTAL2/PCINT9	PA0/XTAL1/PCINT8
PUOE	$\overline{\text{RSTDISBL}}$[1] + DEBUGWIRE_ENABLE[2]	EXT_OSC[3]	EXT_CLOCK[4] + EXT_OSC[3]
PUOV	1	0	0
DDOE	$\overline{\text{RSTDISBL}}$[1] + DEBUGWIRE_ENABLE[2]	EXT_OSC[3]	EXT_CLOCK[4] + EXT_OSC[3]
DDOV	DEBUGWIRE_ENABLE[2] • $\overline{\text{debugWire Transmit}}$	0	0
PVOE	$\overline{\text{RSTDISBL}}$[1] + DEBUGWIRE_ENABLE[2]	EXT_OSC[3]	EXT_CLOCK[4] + EXT_OSC[3]
PVOV	0	0	0
PTOE	0	0	0
DIEOE	$\overline{\text{RSTDISBL}}$[1] + DEBUGWIRE_ENABLE[2] + PCINT10 • PCIE1	EXT_OSC[3] + PCINT9 • PCIE1	EXT_CLOCK[4] + EXT_OSC[3] + (PCINT8 • PCIE1)
DIEOV	DEBUGWIRE_ENABLE[2] + ($\overline{\text{RSTDISBL}}$[1] • PCINT10 • PCIE1)	$\overline{\text{EXT\_OSC}}$[3] + PCINT9 • PCIE1	(EXT_CLOCK[4] • $\overline{\text{PWR\_DOWN}}$) + ($\overline{\text{EXT\_CLOCK}}$[4] • $\overline{\text{EXT\_OSC}}$[3] • PCINT8 • PCIE1)
DI	dW/PCINT10 Input	PCINT9 Input	CLKI/PCINT8 Input
AIO		XTAL2	XTAL1

Notes:
1. RSTDISBL is 1 when the fuse is “0” (Programmed).
2. DebugWIRE is enabled when DWEN Fuse is programmed and Lock bits are unprogrammed.
3. EXT_OSC = crystal oscillator or low frequency crystal oscillator is selected as system clock.
4. EXT_CLOCK = external closk is selected as system clock.

10.2.2 Alternate Functions of Port B

The Port B pins with alternate function are shown in Table 10-5.

Table 10-5. Port B Pins Alternate Functions

Port Pin	Alternate Function
PB0	AIN0: Analog Comparator, Positive Input PCINT0: Pin Change Interrupt 0, Source 0
PB1	AIN1: Analog Comparator, Negative Input PCINT1: Pin Change Interrupt 0, Source 1
PB2	OC0A:: Timer/Counter0 Compare Match AOutput PCINT2: Pin Change Interrupt 0, Source 2
PB3	OC1A: Timer/Counter1 Compare Match A Output PCINT3: Pin Change Interrupt 0, Source 3

Table 10-5. Port B Pins Alternate Functions

Port Pin	Alternate Function
PB4	OC1B: Timer/Counter1 Compare Match B Output PCINT4: Pin Change Interrupt 0, Source 4
PB5	DI: USI Data Input (Three Wire Mode) SDA: USI Data Input (Two Wire Mode) PCINT5: Pin Change Interrupt 0, Source 5
PB6	DO: USI Data Output (Three Wire Mode) PCINT6: Pin Change Interrupt 0, Source 6
PB7	USCK: USI Clock (Three Wire Mode) SCL : USI Clock (Two Wire Mode) PCINT7: Pin Change Interrupt 0, Source 7

- **Port B, Bit 0 – AIN0/PCINT0**
  - AIN0: Analog Comparator Positive input. Configure the port pin as input with the internal pull-up switched off to avoid the digital port function from interfering with the function of the Analog Comparator.
  - PCINT0: Pin Change Interrupt Source 0. The PB0 pin can serve as an external interrupt source for pin change interrupt 0.

- **Port B, Bit 1 – AIN1/PCINT1**
  - AIN1: Analog Comparator Negative input. Configure the port pin as input with the internal pull-up switched off to avoid the digital port function from interfering with the function of the analog comparator.
  - PCINT1: Pin Change Interrupt Source 1. The PB1 pin can serve as an external interrupt source for pin change interrupt 0.

- **Port B, Bit 2 – OC0A/PCINT2**
  - OC0A: Output Compare Match A output. The PB2 pin can serve as an external output for the Timer/Counter0 Output Compare A. The pin has to be configured as an output (DDB2 set (one)) to serve this function. The OC0A pin is also the output pin for the PWM mode timer function.
  - PCINT2: Pin Change Interrupt Source 2. The PB2 pin can serve as an external interrupt source for pin change interrupt 0.

- **Port B, Bit 3 – OC1A/PCINT3**
  - OC1A: Output Compare Match A output: The PB3 pin can serve as an external output for the Timer/Counter1 Output Compare A. The pin has to be configured as an output (DDB3 set (one)) to serve this function. The OC1A pin is also the output pin for the PWM mode timer function.
  - PCINT3: Pin Change Interrupt Source 3: The PB3 pin can serve as an external interrupt source for pin change interrupt 0.

- **Port B, Bit 4 – OC1B/PCINT4**
  - OC1B: Output Compare Match B output: The PB4 pin can serve as an external output for the Timer/Counter1 Output Compare B. The pin has to be configured as an output (DDB4 set

(one)) to serve this function. The OC1B pin is also the output pin for the PWM mode timer function.

- PCINT4: Pin Change Interrupt Source 4. The PB4 pin can serve as an external interrupt source for pin change interrupt 0.

- **Port B, Bit 5 – DI/SDA/PCINT5**
  - DI: Three-wire mode Universal Serial Interface Data input. Three-wire mode does not override normal port functions, so pin must be configured as an input. SDA: Two-wire mode Serial Interface Data.
  - PCINT5: Pin Change Interrupt Source 5. The PB5 pin can serve as an external interrupt source for pin change interrupt 0.

- **Port B, Bit 6 – DO/PCINT6**
  - DO: Three-wire mode Universal Serial Interface Data output. Three-wire mode Data output overrides PORTB6 value and it is driven to the port when data direction bit DDB6 is set (one). However the PORTB6 bit still controls the pull-up enabling pull-up, if direction is input and PORTB6 is set (one).
  - PCINT6: Pin Change Interrupt Source 6. The PB6 pin can serve as an external interrupt source for pin change interrupt 0.

- **Port B, Bit 7 – USCK/SCL/PCINT7**
  - USCK: Three-wire mode Universal Serial Interface Clock.
  - SCL: Two-wire mode Serial Clock for USI Two-wire mode.
  - PCINT7: Pin Change Interrupt source 7. The PB7 pin can serve as an external interrupt source for pin change interrupt 0.

Table 10-6 and Table 10-7 relate the alternate functions of Port B to the overriding signals shown in Figure 10-5 on page 60. SPI MSTR INPUT and SPI SLAVE OUTPUT constitute the MISO signal, while MOSI is divided into SPI MSTR OUTPUT and SPI SLAVE INPUT.

Table 10-6. Overriding Signals for Alternate Functions in PB7..PB4

Signal Name	PB7/USCK/ SCL/PCINT7	PB6/DO/PCINT6	PB5/SDA/ DI/PCINT5	PB4/OC1B/ PCINT4
PUOE	USI_TWO_WIRE	0	0	0
PUOV	0	0	0	0
DDOE	USI_TWO_WIRE	0	USI_TWO_WIRE	0
DDOV	(USI_SCL_HOLD+ $\overline{\text{PORTB7}}$)•DDB7	0	($\overline{\text{SDA}}$ + $\overline{\text{PORTB5}}$)• DDB5	0
PVOE	USI_TWO_WIRE • DDB7	USI_THREE_WIRE	USI_TWO_WIRE • DDB5	OC1B_PVOE
PVOV	0	DO	0	0OC1B_PVOV
PTOE	USI_PTOE	0	0	0
DIEOE	(PCINT7•PCIE) +USISIE	(PCINT6•PCIE)	(PCINT5•PCIE) + USISIE	(PCINT4•PCIE)
DIEOV	1	1	1	1
DI	PCINT7 Input USCK Input SCL Input	PCINT6 Input	PCINT5 Input SDA Input DI Input	PCINT4 Input
AIO	–	–	–	–

Table 10-7. Overriding Signals for Alternate Functions in PB3..PB0

Signal Name	PB3/OC1A/ PCINT3	PB2/OC0A/ PCINT2	PB1/AIN1/ PCINT1	PB0/AIN0/ PCINT0
PUOE	0	0	0	0
PUOV	0	0	0	0
DDOE	0	0	0	0
DDOV	0	0	0	0
PVOE	OC1A_PVOE	OC0A_PVOE	0	0
PVOV	OC1A_PVOV	OC0A_PVOV	0	0
PTOE	0	0	0	0
DIEOE	(PCINT3 • PCIE)	(PCINT2 • PCIE)	(PCINT1 • PCIE)	(PCINT0 • PCIE)
DIEOV	1	1	1	1
DI	PCINT7 Input	PCINT6 Input	PCINT5 Input	PCINT4 Input
AIO	–	–	AIN1	AIN0

10.2.3 Alternate Functions of Port D

The Port D pins with alternate functions are shown in Table 10-8..

Table 10-8. Port D Pins Alternate Functions

Port Pin	Alternate Function
PD0	RXD: UART Data Receiver PCINT11:Pin Change Interrupt 2, Source 11
PD1	TXD: UART Data Transmitter PCINT12:Pin Change Interrupt 2, Source 12
PD2	INT0: External Interrupt 0 Input XCK: USART Transfer Clock CKOUT: System Clock Output PCINT13:Pin Change Interrupt 2, Source 13
PD3	INT1: External Interrupt 1 Input PCINT14:Pin Change Interrupt 2, Source 14
PD4	T0: Timer/Counter0 Clock Source PCINT15:Pin Change Interrupt 2, Source 15
PD5	OC0B: Timer/Counter0 Compare Match B output T1: Timer/Counter1 Clock Source PCINT16:Pin Change Interrupt 2, Source 16
PD6	ICPI: Timer/Counter1 Input Capture Pin PCINT17:Pin Change Interrupt 2, Source 17

- **Port D, Bit 0 – RXD/PCINT11**
  - RXD: UART Data Receiver.
  - PCINT11: Pin Change Interrupt Source 11. The PD0 pin can serve as an external interrupt source for pin change interrupt 2.
- **Port D, Bit 1 – TXD/PCINT12**
  - TXD: UART Data Transmitter.
  - PCINT12: Pin Change Interrupt Source 12. The PD1 pin can serve as an external interrupt source for pin change interrupt 2.
- **Port D, Bit 2 – INT0/XCK/CKOUT/PCINT13**
  - INT0: External Interrupt Source 0. The PD2 pin can serve as en external interrupt source to the MCU.
  - XCK: USART Transfer Clock used only by Synchronous Transfer mode.
  - CKOUT: System Clock Output.
  - PCINT13: Pin Change Interrupt Source 13. The PD2 pin can serve as an external interrupt source for pin change interrupt 2.
- **Port D, Bit 3 – INT1/PCINT14**
  - INT1: External Interrupt Source 1. The PD3 pin can serve as an external interrupt source to the MCU.
  - PCINT14: Pin Change Interrupt Source 14. The PD3 pin can serve as an external interrupt source for pin change interrupt 2.

- **Port D, Bit 4 – T0/PCINT15**
  - T0: Timer/Counter0 External Counter Clock input is enabled by setting (one) the bits CS02 and CS01 in the Timer/Counter0 Control Register (TCCR0).
  - PCINT15: Pin Change Interrupt Source 15. The PD4 pin can serve as an external interrupt source for pin change interrupt 2.

- **Port D, Bit 5 – OC0B/T1/PCINT16**
  - OC0B: Output Compare Match B output: The PD5 pin can serve as an external output for the Timer/Counter0 Output Compare B. The pin has to be configured as an output (DDD5 set (one)) to serve this function. The OC0B pin is also the output pin for the PWM mode timer function.
  - T1: Timer/Counter1 External Counter Clock input is enabled by setting (one) the bits CS02 and CS01 in the Timer/Counter1 Control Register (TCCR1).
  - PCINT16: Pin Change Interrupt Source 16. The PD5 pin can serve as an external interrupt source for pin change interrupt 2.

- **Port D, Bit 6 – ICPI/PCINT17**
  - ICPI: Timer/Counter1 Input Capture Pin. The PD6 pin can act as an Input Capture pin for Timer/Counter1.
  - PCINT17: Pin Change Interrupt Source 17. The PD6 pin can serve as an external interrupt source for pin change interrupt 2.

Table 10-9 and Table 10-10 relates the alternate functions of Port D to the overriding signals shown in Figure 10-5 on page 60.

Table 10-9. Overriding Signals for Alternate Functions PD6..PD4

Signal Name	PD6/ICPI/PCINT17	PD5/OC1B/T1/PCINT16	PD4/T0/PCINT15
PUOE	0	0	0
PUOV	0	0	0
DDOE	0	0	0
DDOV	0	0	0
PVOE	0	OC1B_PVOE	0
PVOV	0	OC1B_PVOV	0
PTOE	0	0	0
DIEOE	ICPI Enable + PCINT17	T1 Enable + PCINT16	T0 Enable + PCINT15
DIEOV	PCINT17	PCINT16	PCINT15
DI	ICPI Input/PCINT17	T1 Input/PCINT16	T0 Input/PCINT15
AIO	–	–	AIN1