Iteration	Week	Date	SYS.2 Sistem Requirements Analysis	SWE.1 Sofware Requirements Analysis
1	36-37	[03 - 14 Sep 2018]	DC Motor Velocity Control by means of a square signal whose pulse with varies trough time and presents a constant frequency fo = 10 KHz.	Configure the necessary pin for PWM signal generation with a fixed frequency of 10KHz.
2	38-39	[17 - 28 Sep 2018]	Hall Efect Sensor coupled with motor rotor outputs 15 pulses per each 360° turn around.	Communication interface development to capture the Hall Efect Sensor pulses.
3	40-41	[01 - 12 Oct 2018]	DC Motor Power Supply is 12 Volts.	GPIO Configuration to allow motor clockwise or anticlockwise rotation. (If necessary).
4	42-43	[15 - 26 Oct 2018]	The reference value or "Set-Point" shoulg be defined by the use of a variable resistor.	Configure the necessary pin for Analog input voltage adquisition as well as ADC configuration for raw data reading.
5	44-45	[29 - 09 Nov 2018]	The system should allow the user to set the Desired velocity by using the potentiometer.	Velocity Control Module Development.
6	46-47	[12 - 23 Nov 2018]	The LCD Display or Graphical Interface must show the motor velocity and "Set-Point" (both in RPM's), as well as the PWM Duty Cycle percentage (%).	Human Machine Interface Development. "Project Name: DC Motor Velocity Control", "Duty cycle: XXX%", "Speed: XXXX RPM", "SW Version: X.X" "HW Version: CESEQ-C001/CESEQ-P001". Embedded Software Engineers: Last Name, Name.
7	48-49	[26 - 07 Dec 2018]	OS configuration during boot-up	1. EEPROM Memory 2. Timer by interruption avery XXms (User defined). 3. Watchdog timer.
8	50-51	[10 - 21 Dec 2018]	The system should be able to detect: Battery and Earth short circuit	Diagnostics Module Development, Store values in EEPROM.

9	52-01	[24 - 04 Jan 2019]	The system should keep track of Internal Memory corruption.	Diagnostics Module Development, Button in short circuit
10	02-03	[07 - 18 Jan 2019]	Throghput Analysis and Tasks Management should be monitored in order to n.	Tasks could be monitored with a resolution of at least 10 TIC's. Furthermore, they should be stored in integer type variables. If the Throughput is greater than 70% the CPU use, Software design must be reconsidered. It will be necessary to divide states/tasks/subrutines in order to satify the desired Throughput.
11	04-05	[21 - 01 Feb 2019]	Cyclomatic Complexity Analysis and Conventions and Standards.	Complexity through the CCCC, which must less than < 19.