EE4363 / CSci 4203 – Computer Architecture
Machine Problem 1

Description

- Figure C.5.15 on page C-37 in Appendix-C-Computer-Organization.pdf contains Verilog code for a MIPS ALU. (**NOTE: The Appendix C referred to here is not from our textbook. Please refer to the Appendix-C-Computer-Organization.pdf available on Canvas.**)
- Study the Verilog code to determine how it works. Enter the Verilog code into a file called MIPSALU.v.
- Compile the Verilog code for the MIPS ALU. Suggestions for free Verilog compilation and simulation tools can be found in the text file **Verilog_tools.rtf** on Canvas.
- Use the testbench test_mipsalu.v to simulate operation of the MIPS ALU Verilog module. Modify the testbench to experiment with all available operations for four different values of the 32-bit A and B operands. Verify that the correct results are produced by the ALU.
- Summarize your observations in a report.

Report Format

- Provide a brief summary of your experiment.
- Include waveforms for your simulation showing all ports of the ALU (as a function of simulated time).
- Attach your Verilog code for the MIPS ALU and testbench with your submission.
- Submit a tarball or zip file of your files through Canvas.

Reference Materials (available on Canvas)

- Appendix-C-Computer-Organization.pdf – The Basics of Hardware Design
- Appendix-D-Computer-Organization.pdf – Mapping control to Hardware
- Section-4.12-Computer-Organization.pdf – An introduction to digital design using a hardware language to describe and model a pipeline and more pipelining illustrations