EE4363 / CSci 4203 – Computer Architecture Machine Problem 2

ALEX LEMA

Lemac001

We want to support hazard detection; therefore, we must add stall as bellow: ECMEMStall & IFIDStall new pipelines stall.

Feeding NOP instructions to the execution stage:

```
//new added****************************

ifidstall = nop;

EXMEMStall = nop;

//ExMemstall: EXMem_STALL <= '0';

//Ifidstall: Ifid_STALL <= '0';
```

Iqual to zero:

```
//new added*****************************

iFIDStall = 0;

EXMEMStall = 0;

//EXMEMStall: EXMEM_STALL <= '0';

//IFIdStall: IFId_STALL <= '0';
```

Tests for MIPS pipeline Verilog module

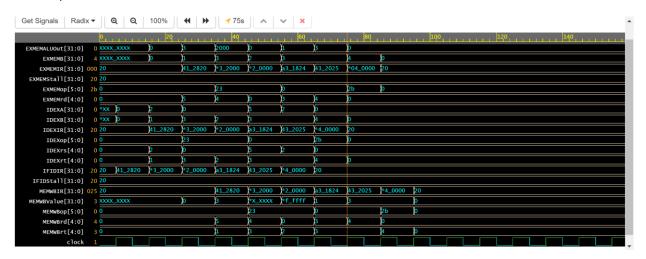
```
51
                                          // Initialize pipeline data
52
                                           // test some instructions
                                          for (i=0; i \le 31; i=i+1) Regs[i] = i; // initialize registers
53
54
55
56
57
                                         // IMemory[0] = 32'h8c210003;
                                          // IMemory[1] = 32'hac020000;
                                         // IMemory[2] = 32'h00642820;
58
59
                                         for (j=0; j<=1023; j=j+1) IMemory[j] = nop;
60
                                         // DMemory[0] = 32'h00000000;
61
                                         // DMemory[1] = 32'hffffffff;
62
63
64
65
66
                                         for (k=0; k<=1023; k=k+1) DMemory [k] = 0;
                                           //new define*************
67
                                         define RTYPE(Op, RD, RS, RT, funct) \setminus (Op << (26)) \mid (RS << (21)) \mid (RT << (16)) \mid (RD << (11)) \mid (funct) \mid (func)
68
                                               define IMRTYPE(Op, RD, IM)\(IM << (11))|(RD << (16))|(Op << (26))
                                             define IMMITYPE(OP, RD, IM)/(IM << (11))//
IMEMORY[0] = RTYPE(ALUOP, 5, 2, 1, 32);
IMEMORY[1] = IMRTYPE(LW, 3, 4);
IMEMORY[2] = IMRTYPE(LW, 2, 0);
IMEMORY[3] = RTYPE(ALUOP, 3, 5, 3, 36);
IMEMORY[4] = RTYPE(ALUOP, 4, 2, 3, 37);
IMEMORY[5] = IMRTYPE(SW, 4, 0);</pre>
69
70
71
72
73
74
75
76
77
                                         DMemory[0] = 32'hffffffff;
                                          DMemory[4] = 32'hffffffff;
```

With these we complete the Verilog code for your MIPS processor. I have modify the code to support ADD, OR, & AND instructions.

```
104 //AND , OR//
105 36: EXMEMALUOUT <= Ain & Bin; // and operation
106 37: EXMEMALUOUT <= Ain | Bin; // or operation
107
```

In the output we can see the instructions don't depend on completion of data access by a previous instruction compare with the incomplete code given in canvas for this exercise.

With nop:



Without nop:

