EE4363 / CSci 4203 – Computer Architecture Machine Problem 4

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- **Provide a brief summary of your code modifications.**

I use Edaplayground.com to compile the Verilog code for the MIPS processor. The given code is for the MIPS 5-stage pipeline. I test the given code than I was able to analyze each line and command. The analysis is hard we must know the pipelining woks. We have a 5-stage pipeline: IF ID EX MEM WB.

In the modifications, I have incorporated the basic logic for branches and control hazards. The given code statically predicts that a branch is not taken. Now, It implements the branch hazard by detecting a taken branch in ID and using that signal to squash the instruction in IF, in addition the PC is assigned to the branch target.

```
104  IFIDIR <= nop;
105  PC <= PC + ({{16{IFIDIR[15]}}, IFIDIR[15:0]}<<2);
106  end
```

```
60   //assign stall = 0;
61    assign stall = (MEMWBIR[31:26]==LW) && // source instruction is a load
62    ((((IDEXop==LW)|(IDEXop==SW)) && (IDEXrs==MEMWBrd)) | // stall for address calc
63   ((IDEXop==ALUop) && ((IDEXrs==MEMWBrd)|(IDEXrt==MEMWBrd)))); // ALU use
64   // Signal for a taken branch: instruction is BEQ and registers are equal
65    assign takebranch = (IFIDIR[31:26]==BEQ) && (Regs[IFIDIR[25:21]]== Regs[IFIDIR[20:16]]);
66
```

At the given code I see that the writeback happens at the 13th cycle.

```
clock cycle = 13 (time = 130)
IF/ID registers
        IF/ID.PC+4 = 0000002c, IF/ID.IR = 00000020

ID/EX registers
        ID/EX.rs =  0, ID/EX.rt =  0
        ID/EX.A = 00000000, ID/EX.B = 00000000
        ID/EX.op = 00

EX/MEM registers
        EX/MEM.rs =  0, EX/MEM.rt =  0
        EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
        EX/MEM.op = 00

MEM/WB registers
        MEM/WB.rd = 12, MEM/WB.rt = 1
        MEM/WB.value = 0000000c
        EX/MEM.op = 00
```

After several experiments the best output was as bellow:

```
clock cycle =  1 (time = 10)
IF/ID registers
        IF/ID.PC+4 = 00000004, IF/ID.IR = 8ca30002

ID/EX registers
        ID/EX.rs =  0, ID/EX.rt =  0
        ID/EX.A = 00000000, ID/EX.B = 00000000
        ID/EX.op = 00

EX/MEM registers
        EX/MEM.rs =  0, EX/MEM.rt =  0
        EX/MEM.ALUOut = xxxxxxxx, EX/MEM.ALUout = xxxxxxxx
        EX/MEM.op = 00

MEM/WB registers
        MEM/WB.rd =  0, MEM/WB.rt = 0
        MEM/WB.value = xxxxxxxx
        EX/MEM.op = 00



clock cycle =  2 (time = 20)
IF/ID registers
        IF/ID.PC+4 = 00000008, IF/ID.IR = 8c620007

ID/EX registers
        ID/EX.rs =  5, ID/EX.rt =  3
        ID/EX.A = 00000005, ID/EX.B = 00000003
        ID/EX.op = 23

EX/MEM registers
        EX/MEM.rs =  5, EX/MEM.rt =  3
        EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
        EX/MEM.op = 00

MEM/WB registers
        MEM/WB.rd =  0, MEM/WB.rt = 0
        MEM/WB.value = xxxxxxxx
        EX/MEM.op = 00



clock cycle =  3 (time = 30)
IF/ID registers
        IF/ID.PC+4 = 0000000c, IF/ID.IR = 10200003

ID/EX registers
        ID/EX.rs =  3, ID/EX.rt =  2
        ID/EX.A = 00000003, ID/EX.B = 00000002
        ID/EX.op = 23

EX/MEM registers
        EX/MEM.rs =  3, EX/MEM.rt =  2
        EX/MEM.ALUOut = 00000007, EX/MEM.ALUout = 00000003
        EX/MEM.op = 23

MEM/WB registers
        MEM/WB.rd =  0, MEM/WB.rt = 0
        MEM/WB.value = 00000000
        EX/MEM.op = 00
```

```
clock cycle =  4 (time = 40)
IF/ID registers
        IF/ID.PC+4 = 00000010, IF/ID.IR = 8c0b0010

ID/EX registers
        ID/EX.rs =  1, ID/EX.rt =  0
        ID/EX.A = 00000001, ID/EX.B = 00000000
        ID/EX.op = 04

EX/MEM registers
        EX/MEM.rs =  1, EX/MEM.rt =  0
        EX/MEM.ALUOut = 0000000a, EX/MEM.ALUout = 00000002
        EX/MEM.op = 23

MEM/WB registers
        MEM/WB.rd =  0, MEM/WB.rt = 1
        MEM/WB.value = 0000000d
        EX/MEM.op = 23



clock cycle =  5 (time = 50)
IF/ID registers
        IF/ID.PC+4 = 00000014, IF/ID.IR = ad6f0009

ID/EX registers
        ID/EX.rs =  0, ID/EX.rt = 11
        ID/EX.A = 00000000, ID/EX.B = 0000000b
        ID/EX.op = 23

EX/MEM registers
        EX/MEM.rs =  0, EX/MEM.rt = 11
        EX/MEM.ALUOut = 0000000a, EX/MEM.ALUout = 00000000
        EX/MEM.op = 04

MEM/WB registers
        MEM/WB.rd =  0, MEM/WB.rt = 0
        MEM/WB.value = 00000000
        EX/MEM.op = 23



clock cycle =  6 (time = 60)
IF/ID registers
        IF/ID.PC+4 = 00000014, IF/ID.IR = ad6f0009

ID/EX registers
        ID/EX.rs =  0, ID/EX.rt =  0
        ID/EX.A = 00000000, ID/EX.B = 0000000b
        ID/EX.op = 00

EX/MEM registers
        EX/MEM.rs =  0, EX/MEM.rt =  0
        EX/MEM.ALUOut = 00000010, EX/MEM.ALUout = 0000000b
        EX/MEM.op = 23

MEM/WB registers
        MEM/WB.rd =  0, MEM/WB.rt = 0
        MEM/WB.value = 00000000
        EX/MEM.op = 04
```

```
clock cycle =  7 (time = 70)
IF/ID registers
        IF/ID.PC+4 = 00000018, IF/ID.IR = 10210001

ID/EX registers
        ID/EX.rs = 11, ID/EX.rt = 15
        ID/EX.A = 0000000b, ID/EX.B = 0000000f
        ID/EX.op = 2b

EX/MEM registers
        EX/MEM.rs = 11, EX/MEM.rt = 15
        EX/MEM.ALUOut = 0000000b, EX/MEM.ALUout = 0000000b
        EX/MEM.op = 00

MEM/WB registers
        MEM/WB.rd =  0, MEM/WB.rt = 1
        MEM/WB.value = 00000003
        EX/MEM.op = 23



clock cycle =  8 (time = 80)
IF/ID registers
        IF/ID.PC+4 = 0000001c, IF/ID.IR = 00000020

ID/EX registers
        ID/EX.rs =  0, ID/EX.rt =  0
        ID/EX.A = 0000000b, ID/EX.B = 0000000f
        ID/EX.op = 00

EX/MEM registers
        EX/MEM.rs =  0, EX/MEM.rt =  0
        EX/MEM.ALUOut = 0000000c, EX/MEM.ALUout = 0000000f
        EX/MEM.op = 2b

MEM/WB registers
        MEM/WB.rd =  0, MEM/WB.rt = 0
        MEM/WB.value = 0000000b
        EX/MEM.op = 00



clock cycle =  9 (time = 90)
IF/ID registers
        IF/ID.PC+4 = 00000020, IF/ID.IR = 8c0b0010

ID/EX registers
        ID/EX.rs =  0, ID/EX.rt =  0
        ID/EX.A = 00000000, ID/EX.B = 00000000
        ID/EX.op = 00

EX/MEM registers
        EX/MEM.rs =  0, EX/MEM.rt =  0
        EX/MEM.ALUOut = 0000001a, EX/MEM.ALUout = 0000000f
        EX/MEM.op = 00

MEM/WB registers
        MEM/WB.rd =  0, MEM/WB.rt = 1
        MEM/WB.value = 0000000b
        EX/MEM.op = 2b



clock cycle = 10 (time = 100)
IF/ID registers
        IF/ID.PC+4 = 00000024, IF/ID.IR = 002b6020
```

```
ID/EX registers
        ID/EX.rs =  0, ID/EX.rt = 11
        ID/EX.A = 00000000, ID/EX.B = 0000000b
        ID/EX.op = 23

EX/MEM registers
        EX/MEM.rs =  0, EX/MEM.rt = 11
        EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
        EX/MEM.op = 00

MEM/WB registers
        MEM/WB.rd =  0, MEM/WB.rt = 0
        MEM/WB.value = 0000001a
        EX/MEM.op = 00



clock cycle = 11 (time = 110)
IF/ID registers
        IF/ID.PC+4 = 00000028, IF/ID.IR = 00000020

ID/EX registers
        ID/EX.rs =  1, ID/EX.rt = 11
        ID/EX.A = 00000001, ID/EX.B = 0000000b
        ID/EX.op = 00

EX/MEM registers
        EX/MEM.rs =  1, EX/MEM.rt = 11
        EX/MEM.ALUOut = 00000010, EX/MEM.ALUout = 0000000b
        EX/MEM.op = 23

MEM/WB registers
        MEM/WB.rd =  0, MEM/WB.rt = 0
        MEM/WB.value = 00000000
        EX/MEM.op = 00



clock cycle = 12 (time = 120)
IF/ID registers
        IF/ID.PC+4 = 0000002c, IF/ID.IR = 00000020

ID/EX registers
        ID/EX.rs =  0, ID/EX.rt =  0
        ID/EX.A = 00000000, ID/EX.B = 00000000
        ID/EX.op = 00

EX/MEM registers
        EX/MEM.rs =  0, EX/MEM.rt =  0
        EX/MEM.ALUOut = 0000000c, EX/MEM.ALUout = 0000000b
        EX/MEM.op = 00

MEM/WB registers
        MEM/WB.rd =  0, MEM/WB.rt = 1
        MEM/WB.value = 00000003
        EX/MEM.op = 23



clock cycle = 13 (time = 130)
IF/ID registers
        IF/ID.PC+4 = 0000002c, IF/ID.IR = 00000020

ID/EX registers
        ID/EX.rs =  0, ID/EX.rt =  0
```

```
        ID/EX.A = 00000000, ID/EX.B = 00000000
        ID/EX.op = 00

EX/MEM registers
        EX/MEM.rs =  0, EX/MEM.rt =  0
        EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
        EX/MEM.op = 00

MEM/WB registers
        MEM/WB.rd = 12, MEM/WB.rt = 1
        MEM/WB.value = 0000000c
        EX/MEM.op = 00



clock cycle = 14 (time = 140)
IF/ID registers
        IF/ID.PC+4 = 00000030, IF/ID.IR = 00000020

ID/EX registers
        ID/EX.rs =  0, ID/EX.rt =  0
        ID/EX.A = 00000000, ID/EX.B = 00000000
        ID/EX.op = 00

EX/MEM registers
        EX/MEM.rs =  0, EX/MEM.rt =  0
        EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
        EX/MEM.op = 00

MEM/WB registers
        MEM/WB.rd =  0, MEM/WB.rt = 0
        MEM/WB.value = 00000000
        EX/MEM.op = 00



clock cycle = 15 (time = 150)
IF/ID registers
        IF/ID.PC+4 = 00000034, IF/ID.IR = 00000020

ID/EX registers
        ID/EX.rs =  0, ID/EX.rt =  0
        ID/EX.A = 00000000, ID/EX.B = 00000000
        ID/EX.op = 00

EX/MEM registers
        EX/MEM.rs =  0, EX/MEM.rt =  0
        EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
        EX/MEM.op = 00

MEM/WB registers
        MEM/WB.rd =  0, MEM/WB.rt = 0
        MEM/WB.value = 00000000
        EX/MEM.op = 00



clock cycle =  0 (time = 160)
Done
```