EE4363 / CSci 4203 – Computer Architecture Machine Problem 3

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The file mipspipe_mp3.v contains an incomplete behavioral Verilog description of a MIPS processor. • Study the Verilog code to determine how it works.

I use Edaplayground.com to compile the Verilog code for the MIPS processor. The given code is for the MIPS 5-stage pipeline. I notice that it ignores branch and data hazards. I test the given code than I was able to analyze each line and command. The analysis is hard we have to know the pipelining woks.

We have a 5-stage pipeline: IF ID EX MEM WB

At the given code I see that the writeback happens at the 13th cycle.

```
clock cycle = 13 (time = 130)
IF/ID registers
         IF/ID.PC+4 = 00000034, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd = 12, MEM/WB.rt = 11
         MEM/WB.value = 0000000c
         EX/MEM.op = 00
```

```
clock cycle = 15 (time = 150)
IF/ID registers
         IF/ID.PC+4 = 0000003c, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = 00000000, EX/MEM.ALUout = 00000000
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = 00000000
         EX/MEM.op = 00
```

Next, modify the hardware description to add support for forwarding.

The Forwarding Unit is designed to solve the data hazards in pipelined MIPS Processor. The correct data at the output of the ALU is forwarded to the input of the ALU when data hazards are detected.

```
clock cycle = 13 (time = 130)
IF/ID registers
         IF/ID.PC+4 = 00000030, IF/ID.IR = 00000020

ID/EX registers
         ID/EX.rs =  0, ID/EX.rt =  0
         ID/EX.A = 00000000, ID/EX.B = 00000000
         ID/EX.op = 00

EX/MEM registers
         EX/MEM.rs =  0, EX/MEM.rt =  0
         EX/MEM.ALUOut = 0000000e, EX/MEM.ALUout = 0000000b
         EX/MEM.op = 00

MEM/WB registers
         MEM/WB.rd =  0, MEM/WB.rt =  0
         MEM/WB.value = 00000000
         EX/MEM.op = 00
```

The final result pipeline diagram with forwarding must be like graph below:

Instr.	1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	IF	ID	EX	MEM	WB									
2		IF				WB								
3			IF				WB							
4				IF				WB						
5					IF				WB					
6						IF				WB				
7							IF				WB			
8								IF				WB		
9									IF				WB	
10										IF	ID	EX	MEM	WB

In conclusion with no forwarding are required stall, with forwarding no stalls are required.