HW/SW Entwurfssprachen am Beispiel System-C

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November 1, 2014

1 HW/SW Design Languages

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2 What is SystemC

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2.1 History

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2.2 Benefits

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2.3 Drawbacks

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2.4 SysC vs. C

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2.5 SysC vs. VHDL

3 Automatic Partitioning

3.1 What is Partitioning?

Partitioning means the separation of hardware and software parts with focus on hardware/software co-design. Traditionally the hardware part of an embedded system is written in VHDL *(more present in Europe)* or Verilog *(more present in*

the USA) while the software part is written in *assembly*, *C* or *C++*. The common design-flow (depicted in Figure 1) shows that partitioning splits the design in hardware and software. The software part is the shorter one of this two paths because it needs only an compiler to translate it to machine-code. Therefore, the hardware part is the much longer way because of the hardware design-flow which is necessary for every chip-design. If the hardware and software parts

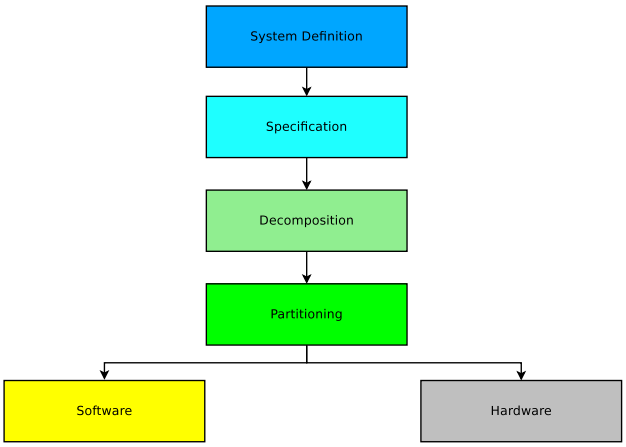

Figure 1: Design flow *(c.f. Hardware Modelling VO)*.

should be modified because of, e.g., performance reasons, these two parts must be modified or completely redesigned in order to fit the specifications. This leads to an much higher and probably expensive procedure for the hardware part, thus its design-flow is much longer and every change in the *VHDL/Verilog* code leads to a new compilation, technology-mapping and place and route.

4 Tools

4.1 LegUP

LegUP is an open source high level synthesis tool for fpga based systems. It takes an standart C program as input and implements the hardware fitting part to hardware and the software fitting part to software. LegUP uses an MIPS soft core and uses a standard bus interface for communication between the hardware parts and the processor. **Automatic Partitioning? - Yes in a way.**

5 Creators

5.1 Accellera

Accellera Systems Initiative is a non-profit organisation composed of an broad range of members which aims to create system-level standards for the worldwide

electronics industry. One of the IEEE[1] standards ratified by accellera was IEEE 1666 SystemC.

6 Users

6.1 ARM

Figure 2: ARM Ltd.

ARM (Advanced RISC Machines) Ltd. has an active community[2] and there are many informations about tools and IP cores available. SystemC is used by many chip designers and they use the systemC-IP-cores from ARM Ltd. to simulate their designs.

6.2 AMD

6.3 Intel

[1] This standards organisation also ratified VHDL, Verilog and SystemVerilog
[2] http://community.arm.com