

Linear Programming Control LPC 2148 microcontrollers

[ARM7 + 16-bit THUMB mode
+ JTAG Debug
+ fast Multiplier
+ enhanced ICE
synthesizable core]

- * microcontrollers are based on 16-bit/32-bit ARM7TDMI-S CPU
 - with real time emulation & embedded trace support
 - embedded high speed flash mem. ranging from 32 KB to 512 KB.
 - 128-bit wide memo interface
 - a unique accelerator architecture enabled 32-bit code execution at max. clk rate.
 - For critical code size appns
 - alternative 16-bit THUMB mode reduces code by more than 30% with minimal performance penalty.
- * LPC2148 are small in size & consume less power so are ideal for appns where miniaturization is key requirement viz access control etc.
- * Also serial comm interfaces ranging from USB 2.0 full speed device, multiple UARTs, SPI, SSP to I²C-bus & On-chip SRAM of 8KB to 40KB makes these devices well suited for comm gateways & protocol converters, soft modems, voice recognition & low end imaging, providing both large buffer size & high processing power.
- * Various 32-bit timers, single or Dual 10-bit ADC(s), 10-bit DAC, PWM channels, 45 fast GPIO lines, external interrupt pins make these controllers suitable for industrial control & medical systems

Definitions : -①

- * LQPF64 package : Low profile Quad Flat Package:
surface-mount integrated ckt. package
pins are mounted on surface

- * Static RAM → is a type of semiconductor RAM that uses Bistable latching circuitry (F/F) to store each bit.

DRAM

- uses 2 Transistors
- refreshed periodically
- used in computer's main mem.

- SRAM is faster & more expensive than DRAM (uses 6 Transistors)
- used in CPU cache
- is volatile
- Reliability / more reliable
- low idle power consumption

- * Flash memory : → is a non-volatile mem. chip used for storage & for transferring data bet. a personal computer & digital devices.

- It has the ability to be electronically reprogrammed & erased.
- It is found in USB flash drives, MP3 players, digital cameras & solid state drives.

- * Accelerator → h/w dedicated to perform func's faster than CPU.

- 128-bit wide mem. interface & a unique accelerator architecture enable 32-bit code execution at max clk. rate.

- * In-System Programming (ISP) also called in-circuit serial programming (ICSP)

- It is the ability of some programmable logic devices, microcontrollers & other embedded devices to be programmed while installed in a complete system rather than requiring the chip to be programmed prior to installing it, into the system.
- It allows firmware updates to be delivered to the on-chip memory of microcontrollers & related processors without requiring specialist programming circuitry on the circuit board & simplifies design work.

Definitions -②

* In-Application Programming: means that the appn. itself can ~~re-run~~ re-program the On-chip Flash ROM.

In Circuit Emulation

* Embedded ICE RT and Embedded Trace interfaces

Offer real time debugging with On-chip RealMonitor software as well as high-speed real-time tracing of instr. execution.

→ enables breakpoints & watch points. ISR's can continue to execute while the foreground task is debugged with the On-chip RealMonitor s/w.

* USB 2.0 Full speed compliant Device controller

→ consists of a register interface, serial interface engine, endpoint buffer & DMA controller.

* Timers / external event counters : → is designed to count cycles of the peripheral clk (PCLK) or an externally supplied clk & optionally generate interrupt or perform other actions at specified timer values based on 4 match registers.

- It also has 4 capture i/p's to trap the timer value when an i/p signal transitions occurs, optionally generating an interrupt.

* watch dog Timer :-

- the purpose is to reset uc within a reasonable amt. of time if it enters an erroneous state.

- when enabled, the watchdog will generate a system reset if the user pgm fails to reload the watchdog within a predetermined amt of time.

JTAG → (Joint Test Action Group) is industry standard for verifying designs & testing PCB after manufacture.

LPC 2148 Functional Description :-

- (1) ARM7TDMI-S is a general purpose
- 32-bit microcontroller ; offers high performance & low power consumption
 - RISC architecture ie instr. set & related decode mechanism simplicity results in high instr. throughput & impressive real-time interrupt response.
 - Pipeline techs are employed so that all parts of the processing & mem. systems can operate continuously.
 - It employs a unique architectural strategy known as THUMB, which makes it suitable to high-volume apps with mem. restrictions or apps where code density is an issue.
 - Essentially ARM7TDMI-S processor has 2-instr. sets :
 - ① 32-bit ARM set
 - ② 16-bit THUMB set
 - the particular flash implementation in LPC2148 allows full speed execution also in ARM mode.

(2) On-chip Flash program memory :-

- it incorporates a 32KB, 64KB, 128KB, 256KB & 512KB flash mem. system resp.
- ~~it~~ it can be used for both code & data storage.
- it may be programmed in system via the serial port.

- the appln program may also erase and/or pgm the flash while the appln is running, allowing a great degree of flexibility for data storage field firmware upgrades etc.
- Due to architectural soln chosen for an on-chip boot loader, flash mem. available for user's code on LPC2148 is 32KB, 64KB, 128KB, 256KB & 500KB resp.
- LPC2148 flash mem. provides a minimum of 1,00,000 erase/write cycles & 20 yrs of data retention.

③ on-chip static RAM:

- it may be used code and/or data storage.
- SRAM may be accessed as 8-bit, 16-bit & 32-bit.
- 8KB SRAM block is available as USR can also be used as a general purpose RAM for data storage & code storage & execution.

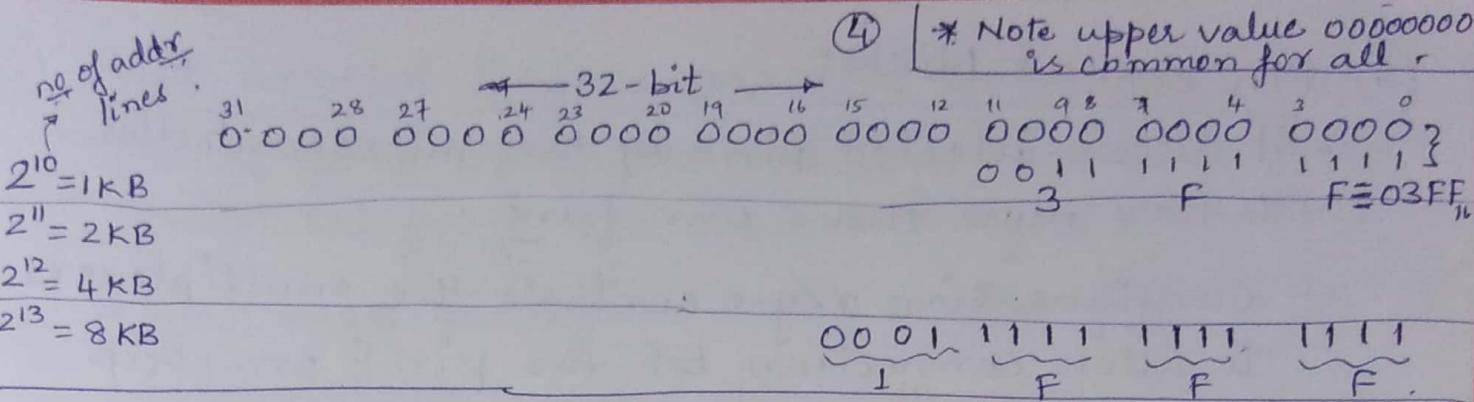
④ Memory map: - incorporates several distinct regions, shown in Figure.

- In addition, the CPU interrupt vectors may be remapped to allow them to reside in either flash mem. or on-chip static RAM.

LPC 2141/42/44/46/48 Memory map

- * In addition, the CPU interrupt vectors may be remapped to allow them to reside in either flash mem. or on-chip static RAM.

4.0GB	AHB Peripherals	0xFFFF FFFF
3.75GB	VPB peripherals	0xF000 0000
3.5GB	VPB peripherals	0xED00 0000
3.0GB	Reserved addr. space	0xC000 0000 0x8000 0000
2.0GB	BOOT Block (12 KB Remapped from on-chip flash mem.)	0x7FFF FFFF 0x7FFF D000 0x7FFF CFFF
	Reserved addr. space	0x7FD0 2000 0x7FD0 1FFF
	8 KB On-chip USB DMA RAM (LPC2146/48)	0x7FD0 0000 0x7FCF FFFF
	Reserved addr. space	0x4000 8000 0x4000 7FFF
	32 KB On-chip Static RAM (LPC2146/48)	0x4000 4000 0x4000 3FFF
	16 KB On-chip Static RAM (LPC2142/44)	0x4000 2000 0x4000 1FFF
	8 KB On-chip Static RAM (LPC2141)	0x4000 0000 0x3FFF FFFF
1.0GB	Reserved addr. space	0x0008 0000 0x0007 FFFF
	Total of 512KB Onchip nonvolatile mem (LPC2148)	0x0004 0000 0x0003 FFFF
	Total of 256KB On-chip non-volatile mem (LPC2146)	0x0002 0000 0x0001 FFFF
	Total of 128KB On-chip non-volatile mem (LPC2144)	0x0001 0000 0x0000 FFFF
	Total of 64KB On-chip non-volatile mem (LPC2142)	0x0000 8000 0x0000 7FFF } 64KB
0.0GB	Total of 32KB On-chip non-volatile mem (LPC2141)	0x0000 0000 } 32KB



In memory map the starting mem. addr. is different.
You need to find the mem. addr. (ending or higher)
with respect to that.

(5) Interrupt controller :-

- the vectored Interrupt controller (VIC) accepts all of the interrupt request i/p's and categorizes them as Fast Interrupt request (FIQ)
 - ↳ vectored Interrupt Request (IRQ)
 - ↳ non-vectored IRQ
- as defined by programmable settings.
- the programmable assignment scheme means that priorities of interrupt from the various peripherals can be dynamically assigned & adjusted.
- FIQ → highest priority
 - ↳ if more than 1 request is assigned to FIQ, the VIC combines the request to produce FIQ signal to ARM processor.
- Vectored IRQs → middle priority
 - ↳ 16 of the interrupt requests can be assigned to this category
 - ↳ Any of the interrupt req's can be assigned to any of the 16 vectored IRQ slots [slot 0 → highest, slot 15 → lowest priority]
- Non-vectored IRQ → least priority
- VIC combines the req's from all vectored & non-vectored IRQs to produce IRQ signal to ARM up.

⑥ Pin connect block:

- it allows selected pins of the microcontroller to have more than one func.
- Configuration reg's controls the multiplexers to allow connection bet the pin & on-chip peripherals.
- Peripherals should be connected to appropriate pins prior to being activated, & prior to any related interrupt(s) being enabled.
- Pin control module with its pin select registers defines the functionality of the microcontroller in a given h/w environment.
- After reset all pins of Port 0 & Port 1 are configured as I/O with following exceptions :
 - ① If debug is enabled, JTAG pins will assume their JTAG functionality .
 - ② If trace is enabled , Trace pins will assume their trace functionality .
 - ③ the pins associated with I²C0 & I²C1 interface are open drain.

⑦ Fast General Purpose parallel I/O (GPIO) :-

- Device pins which are not connected to a specific peripheral func. are controlled by GPIO registers.
- Pins may be dynamically configured as i/p's or o/p's.
- Separate reg.s allow setting or clearing any no. of o/p simultaneously.
- The value of o/p reg. may be read back, as well as the current state of the port pins.
- GPIO reg.s are relocated to the ARM local bus for the fastest possible I/O timing.
- Mask reg.s allow treating sets of port bits as a group, leaving other bits unchanged.
- All GPIO reg.s are byte addressable.
- Entire port value can be written in one inst.
- Bit level set & clear reg.s allow a single inst to set or clear any no. of bits in 1 port.
- Direction control of individual bits.
- Separate control of o/p set & clear.
- All I/O default to i/p's after reset.

⑧ 10-bit ADC's

- LPC2148 has 2 ADC \rightarrow single 10-bit successive approx. A/D converters.
- ADC0 has 6 channels ; ADC1 has 8 channels.
- LPC2148 has 14 ADC_{i/p} pins
- Measurement range of 0V to V_{REF} ($2.5V \leq V_{ref} \leq V_{DDA}$)
- Each converter is capable of performing more than 4,00,000 10-bit samples/sec.
- Every analog i/p has a dedicated result reg. to reduce the interrupt overhead.
- Global start command for both converters.

⑨ 10-bit DAC:

- 1 10-bit DAC to generate variable analog o/p.
- max DAC o/p voltage = V_{REF} .
- Buffered o/p.
- Selectable speed versus power.

⑩ USB 2.0 device controller:-

- USB is a 4-wire serial bus which supports comm bet a host & no. of peripherals (127 max.)
- The host controller allocates the USB bandwidth to attached devices through a token based protocol.
- All transactions are initiated by host controller.
- LPC2148 is equipped with a USB controller which enables 12 Mbit/sec data exchange with USB host controller.
- It consists of a register interface, serial interface engine, endpoint buffer & DMA controller.
- serial interface engine decodes the USB data stream & writes data to appropriate end point buffer mem. The status of a completed USB transfer or error condition is indicated via status registers.
- The DMA controller can transfer data bet. an endpoint buffer & USB RAM.
- Allows dynamic switching bet CPU controlled & DMA modes.

(11) UARTs :- Universal Asynchronous Receiver/Transmitter (UART0, UART1)

- LPC2148 contains 2 UARTs; which provide 2 transmit & receive lines.
- UART1 provides a full modem control handshake interface.
- Both UARTs have baud rates of 115200 with any crystal freq. above 2 MHz.
- 16 Bytes Receive /Transmit FIFOs.
- Receive FIFO trigger pts at 1B, 4B, 8B & 14B.
- Built-in fractional Band rate generator covering wide range of baud rates without a need for external crystals of particular values.
- Transmission FIFO control enables implementation of S/W (XON/XOFF) flow control on both UARTs.

(12) I²C-bus serial I/o controller :- [Inter-Integrated Circuit]

- I²C bus controllers.
 - I²C is bidirectional, for inter-IC control using only 2 wires: Serial Clock Line (SCL) & a Serial DATA line (SDA).
 - Each device is recognized by a unique address & can operate as either a receiver-only device (Ex:- LCD driver or Transmitter with a capability to both send & receive information ie. Memory)
 - Transmitters and/or Receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed.
 - I²C is a multi-master bus, it can be controlled by more than one bus master connected to it.
 - I²C-bus implemented in LPC2148 supports bit-rates upto 400 Kbits/sec
- [synchronous, multi-master, multi-slave, packet switched, single ended serial computer bus → by NXP semiconductors]

Applns of I²C bus:

- It is appropriate for peripherals where simplicity & low manufacturing cost are more important than speed.

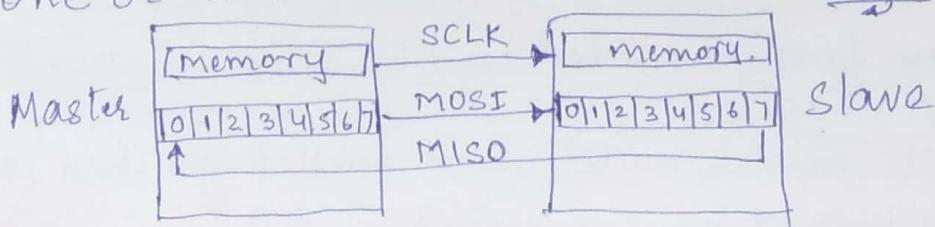
Appln Exs

- ① Accessing Real time clocks
- ② Accessing low speed DACs & ADCs.
- ③ changing contrast, hue & color balance settings in Monitors
- ④ Reading h/w monitors & diagnostic sensors ex a fan's speed.

* - A particular strength of I²C is the capability of the microcontroller to control a network of device chips with just two General purpose IO pins & software.

(13) SPI serial I/O controllers: (developed by Motorola)

- Serial Peripheral Interface (SPI) is a synchronous serial communication interface specification used for short distance comm viz embedded systems.
- Typical applns Secure Digital cards & Liquid Crystal Displays.
- SPI devices comm in full duplex mode using a Master-Slave architecture with a single master. The master device originates the frame for reading & writing.
- SPI bus specifies 4 logic signals:
 - ① SCLK → serial clk. (O/p from master)
 - ② MOSI → Master O/p Slave i/p
 - ③ MISO → Master i/p Slave O/p
 - ④ SS → Slave select
- SPI bus can operate with single master & with one or more slave devices.



Ex:-

Slave

- LPC2148 has 1 SPI controller
- SPI is full duplex serial interface
- Only a single master & a single slave can communicate on the interface during a given data transfer.
- Maximum data bit rate : $1/8^{\text{th}}$ of i/p clk rate .

(14) SSP serial I/o controller :

- **Synchronous Serial Port :** is a controller that supports the SPI , 4-wire Synchronous serial interface(SSI) & Micro wire serial busses .
- It uses a master-slave paradigm to communicate across its connected bus . (\rightarrow master \rightarrow slave for a given data transfer)
- The peripherals may be serial EEPROMs , shift reg's display drivers , A/D converters etc .
- It supports full duplex transfers , with data frames of 4-bits to 16-bits of data flowing from master to slave & from slave to master .
- 8-frame FIFO's for both transmit & receive .

(15) General Purpose Timers/ External Event counters :

- Timer/counter is designed to count cycles of the peripheral clock (PCLK) or externally supplied clock & optionally generate interrupt or perform other actions at specified timer values based on 4 match reg's .
- It also includes 4 capture i/p's to trap the timer value when an i/p signal transitions occur, optionally generating an interrupt .
- It can count external events on one of the capture i/p's if minimum external pulse is equal or longer than a period of PCLK .

- 4 32-bit capture channels per timer/counter that can take a snapshot of the timer value when an I/O signal transition occurs.
 - A capture event may also optionally generate an interrupt.
- 4 32-bit match registers which allow:
 - continuous operation with optional interrupt generation on match.
 - stop timer on match with optional interrupt generation
 - Reset timer on match with optional interrupt generation.
- 4 external ops per timer/counter corresponding to match reg.s with following capabilities:
 - Set LOW on match
 - Set HIGH on match
 - Toggle on match
 - Do nothing on match

⑯ Watchdog Timer:-

- The purpose of watchdog is to reset the microcontroller within a reasonable amount of time if it enters an erroneous state.
- When enabled, the watchdog will generate a system reset if the user program fails to "feed" (or reload) the watchdog within a predetermined amount of time.

Features:

- Internally resets chip if not periodically reloaded
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect/incomplete feed sequence causes reset/interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 32-bit timer with internal pre-scales.

(17) Real-time clock (RTC) :

- (8)
- It is designed to provide a set of counters to measure time when normal or idle operating mode is selected.
 - It is used to use little power, making it suitable for battery powered systems where CPU is not running continuously.

Features:

- Measures the passage of time to maintain a calendar & clock.
- Ultra-low power design to support battery powered systems.
- Provides seconds, Minutes, Hours, Day of the month, month, Year, day of the week & Day of the year.
- Dedicated power supply pin can be connected to a battery or the main 3.3V.

(18) Pulse Width Modulator (PWM) :-

- It is based on standard timer block & inherits all of its features.
- The timer is designed to count cycles of the peripheral clk (PCLK) & optionally generate interrupts or perform other actions when specified timer values occur, based on 7 match reg's.
- The ability to separately control rising & falling edge locations allows the PWM to be used for more applns.

(19) System control :-

(19.1) crystal oscillator :

- On chip oscillator operates with external crystal in range of 1 MHz to 25 MHz.
- Oscillator o/p freq. $\rightarrow f_{osc}$
- ARM processor clk freq $\rightarrow CCLK$.

(19.2) PLL \rightarrow Phase Locked Loop is a control system that generates an o/p signal whose phase is related to phase of i/p signal.

- PLLs are widely used for synchronization purposes.
- PLLs are clock multipliers in microprocessors which allow internal processor elements to run faster than external connections, while maintaining precise timing relationship.
- PLL accepts i/p clk freq. in the range of 10MHz to 25MHz. The i/p freq. is multiplied up into the range of 10MHz to 60MHz with a Current Controlled Oscillator (CCO)

(19.3) Reset & wake-up timer :-

- Reset has 2 sources: the RESET pin & watchdog.
- RESET pin is a Schmitt trigger i/p pin.
- Assertion of chip reset by any source starts the wake up timer, causing the internal chip reset to remain asserted until the external reset is de-asserted, the oscillator is running, a fixed no. of clocks have passed, & the on-chip flash controller has completed its initialization.
- When internal reset is removed, the processor begins executing at address 0, (reset vector). At that point, all the processor & peripheral registers

have been initialized to predetermined values. (9)

- the wake-up timer ensures that the oscillator & other analog functions required for chip operations are fully functional before the processor is allowed to execute instrs.
- Wake-up timer monitors the crystal oscillator as the means of checking whether it is safe to begin code execution.

19.4 BrownOut Detector : (BOD)

- LPC2148 include 2-stage monitoring of the voltage on V_{DD} pins.
1st stage If this voltage falls below 2.9V, the (BOD) BrownOut Detector asserts an interrupt signal to the Vectored Interrupt Controller (VIC).
2nd stage the 2nd stage of low voltage detection asserts reset to inactivate the LPC2148 when voltage on V_{DD} pins fall below 2.6V.

19.5 Code Security :

- this feature of LPC2148 allows an application to control whether it can be debugged or protected from observation.
- If after reset on-chip boot loader detects a valid checksum in flash & reads 0x87654321 from address 0x1Fc in flash, debugging will be disabled & thus the code in flash will be protected from observation.
- Once debugging is disabled, it can be enabled only by performing a full chip erase using the ISP.

19.6 External interrupt pins:

- LPC2148 has 4 independent interrupt signals.

19.7 Memory mapping control:

- It alters the mapping of interrupt vectors that appear beginning at address 0x0000 0000
- Vectors may be mapped to the bottom of the on-chip flash memory or to the on-chip Static RAM.

19.8 Power Control:

- LPC2148 supports two reduced power modes:
Idle mode & Power down mode
 - * In Idle mode execution of instrs is suspended until either a reset or interrupt occurs.
 - Peripheral func^s continue operation during Idle mode & may generate interrupt to cause the processor to resume execution.
 - Idle mode eliminates power used by the processor itself, memory systems & related controllers & internal buses.
- * In Power-down mode, the oscillator is shut down & the chip receives no internal clocks.
 - the processor state & registers, peripheral registers & the internal SRAM values are preserved throughout Power-down mode and the logic levels of chip I/O pins remain static.
 - the power-down mode can be terminated and normal operation resumed by either a reset or certain specific interrupts which are able to function without clocks.

19.9 APB Bus :- (ARM Peripheral Bus)

- the APB divider determines the relationship between the processor clock (CCLK) & the clock used by peripheral devices (PCLK).
- APB divider serves 2 purposes:
 - ① 1st is to provide peripherals with the desired PCLK via APB, so that they can operate at the speed chosen for ARM processor.
 - ② 2nd purpose of APB divider is to allow power savings when an application does not require any peripherals to run at full processor rate.

20 Emulation & Debugging :-

- LPC2148 support emulation & Debugging via a JTAG serial port.
- A trace port allows tracing program execution.
- Debugging and trace functions are multiplexed only with GPIO on Port 1. This implies that all communication, timer & interface peripherals residing on Port 0 are available during the development & debugging phase as they are when the app is run in embedded system itself.
- * RealMonitor: is a configurable s/w module (by ARM) which enables real-time debug. It is programmed in flash memory.