

HW08: Implementing Column Amplification and Cleaning up the Project

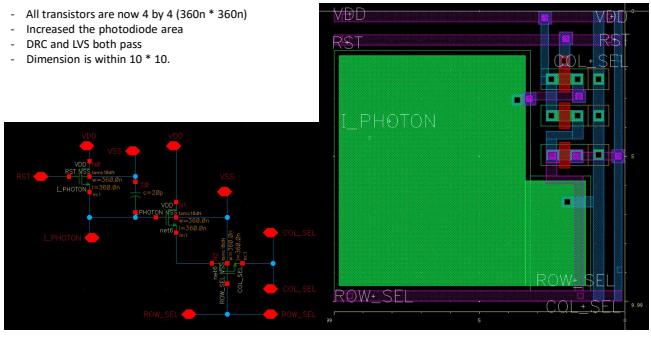
Huanying Yeh 05/08/2022



- Need:
 - Change the clock delays from 440us to about 50us so that the readouts are a bit earlier
 - Figure out why the current can't be in the 1-10 pA range.
 - Redo the big pixel array (col and row sel on the side, use C2MOS to make pulses, VSS and VDD busses, maybe something on the top of the pixels for connection)
 - If have time to flex in the paper, extract layout design and simulate
 - Pixel layout needs fixing
 - Column Amplification stage.

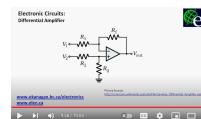
Change Pixel Layout

- All transistors are now 4 by 4 ($360n \times 360n$)
 - Increased the photodiode area
 - DRC and LVS both pass
 - Dimension is within 10×10 .



Notes: Column Amplifier

- https://www.youtube.com/watch?v=7zUYqQ6wUhA&ab_channel=ElectronXLab



Differential Amplifier (continues)

$$V_{out} = \frac{R_{f1}}{R_1} V_1 - \frac{R_{f2}}{R_2} V_2$$

Assumptions: ideal op-amp:
 $V_{in} = V_{in}$
 $V_{out} = V_{out}$

No 2nd order noise terms assumed.

$20 \text{ dB} = 20 \log \left| \frac{V_{out}}{V_{in}} \right|$
 $20 \text{ dB} = 20 \log \left| \frac{R_{f1}}{R_1} \cdot V_1 - \frac{R_{f2}}{R_2} \cdot V_2}{V_1} \right|$

Superposition principle:

Q1 Short V_2 : $V_{out} = 20 \text{ dB}$

Q2 Short V_1 : $V_{out} = V_{out} = \frac{R_{f1}}{R_1 + R_{f1}} \cdot V_2 = 20 \text{ dB}$

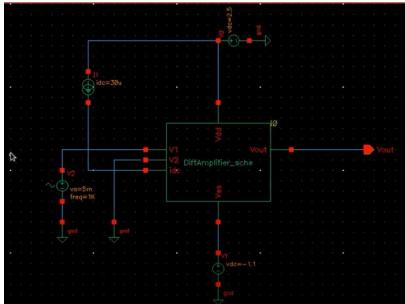
Q3 Short V_1 & V_2 : $V_{out} = 0 \text{ dB}$

negative amplifier



Notes: Column Amplifier

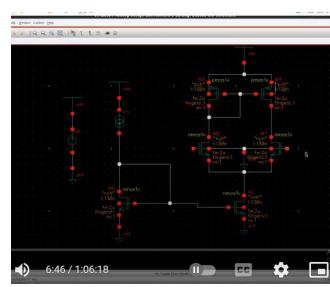
- https://www.youtube.com/watch?v=l7t6wH1QbnU&ab_channel=PraveenAKS



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Notes: Column Amplifier

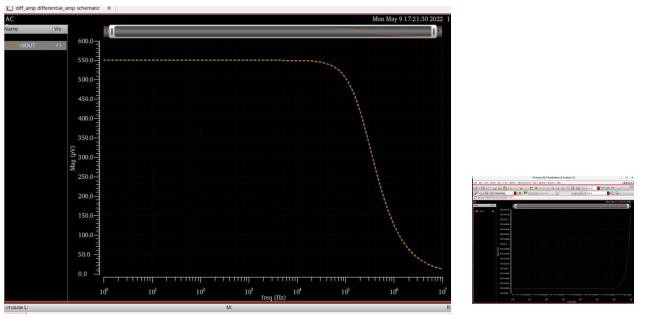
- <https://www.youtube.com/watch?v=uZ2rWwFFa70&t=118s>
ab_channel=AH



The circuit diagram shows a differential pair with two input nodes, V_{IN1} and V_{IN2} , connected to the gates of transistors Q_1 and Q_2 respectively. The drains of Q_1 and Q_2 are connected to the gates of transistors Q_3 and Q_4 respectively. The drains of Q_3 and Q_4 are connected to a common output node V_{OUT} . The source of Q_3 is connected to a voltage source $+V$, and the source of Q_4 is connected to a voltage source $-V$. A feedback node V_f is connected between the drain of Q_1 and the gate of Q_3 . A load resistor r_{load} is connected between the output node V_{OUT} and the feedback node V_f .

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Notes: Column Amplifier



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The diff_amp library (Updated 05/11)

Some params to tune

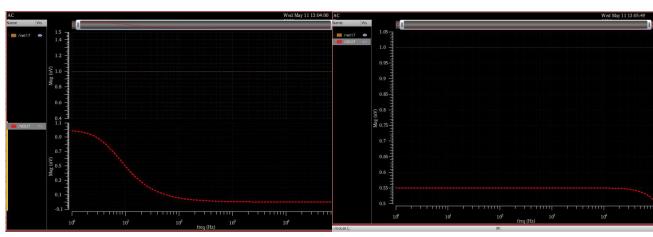
- Vin amplitude
 - Vin2 amplitude
 - How does their difference affect the gain?
 - Do a DC analysis and compare the amplitudes between Vin1 and Vout. What's the amplitude gain?
 - What happens if vin and vout are pulse waves?

Make a diff-amp symbol

- Re-open the big array test with the 16 outputs. Plug in a diff-amp and see how the output changes.

Experiment: Smaller Voffset

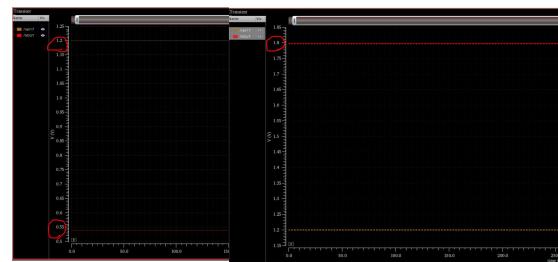
- Offset voltages of Vin1 and Vin2 went from 1.2V to 0.2V
 - Seems to make the frequency response decay faster
 - 0.2V, 0.2V 1.2V, 1.2V
 - Higher starting point, faster decay lower starting point, slower decay.



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Exp: Transient Analysis (0.05ms)

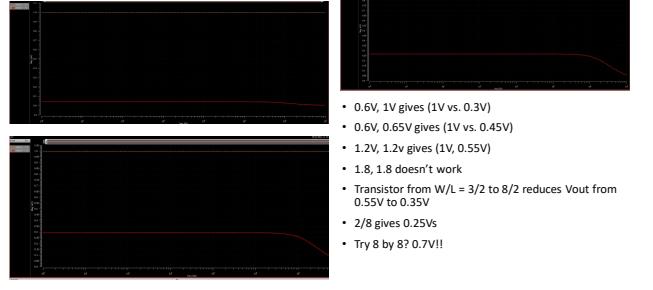
- Time duration doesn't matter
 - $V_{in1} = 1.2V$, $V_{in2} = 1.2V$
 - $V_{out} = 0.53V$
 - Time duration doesn't matter
 - $V_{in1} = 1.2V$, $V_{in2} = 0.6V$
 - $V_{out} = 1.8V$



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Different Vin1, Vin2, and W/L

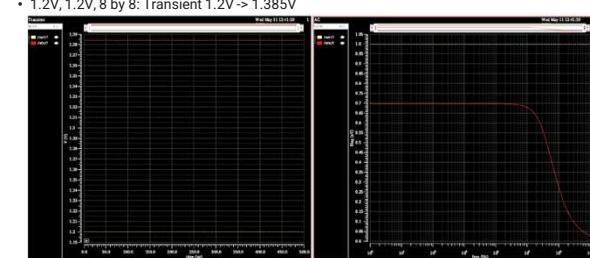
- But for 12.V, 0.6V, the AC gain seems to drop again
 - (1V vs. 0.1V)



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Template

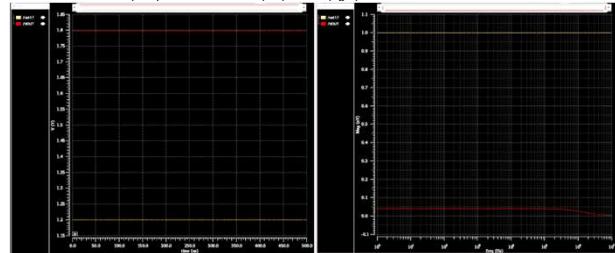
- Transient analysis gives time domain waveforms which are plots of voltage or current versus time. AC analysis gives the voltage or current versus frequency in a linearized version of the circuit.



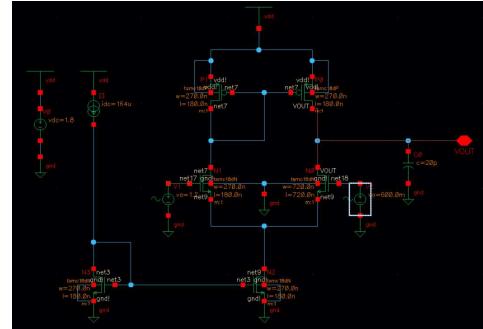
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Template

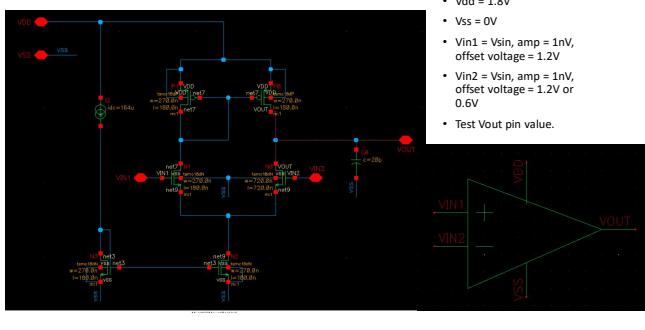
- 1.2V, 0.6V, 8 by 8
- Can't tell what the disparity between transient (left) and AC (right) means



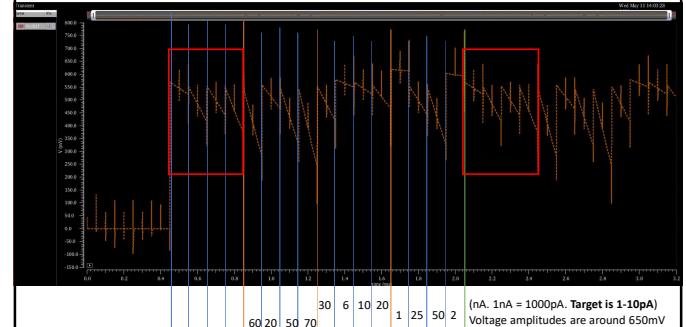
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Make a symbol!! Keep the Transistor at 8 by 8.

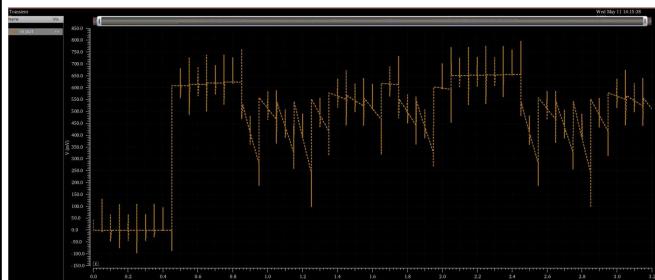
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Schematic and Symbol

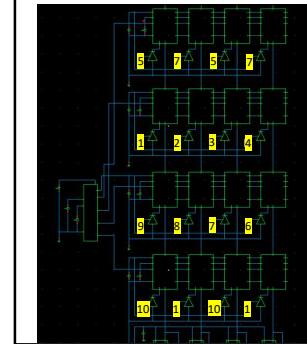
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Open the test array and run simulation again: higher I_PHOTON == steeper voltage leak, as expected

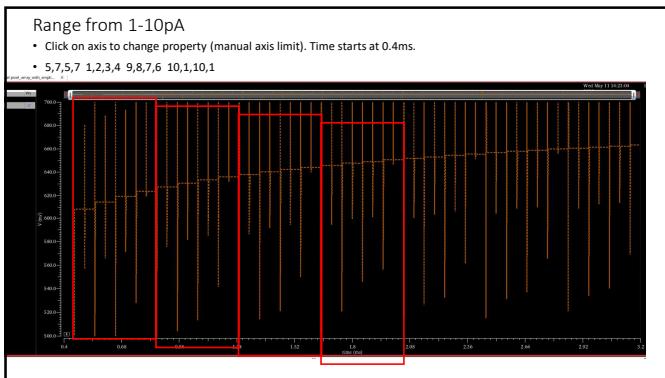
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Adjust to 1-10 pA

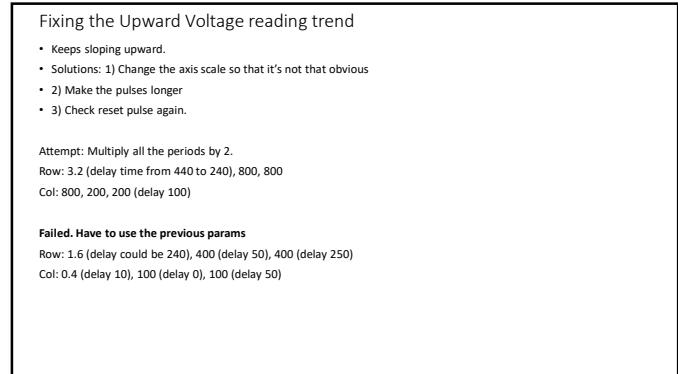
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Pixel Array: New Pattern

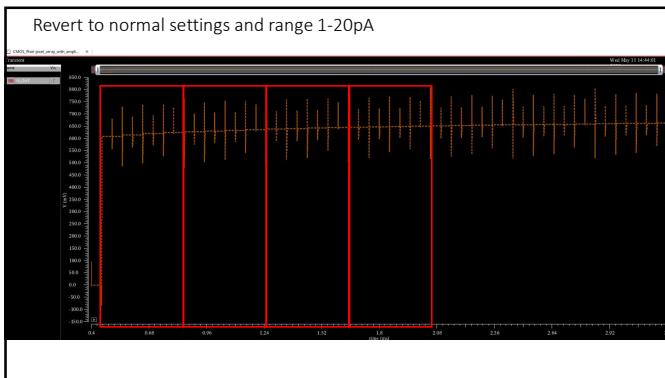
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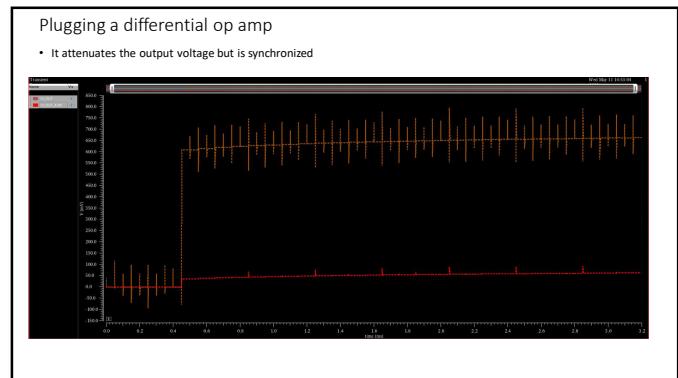
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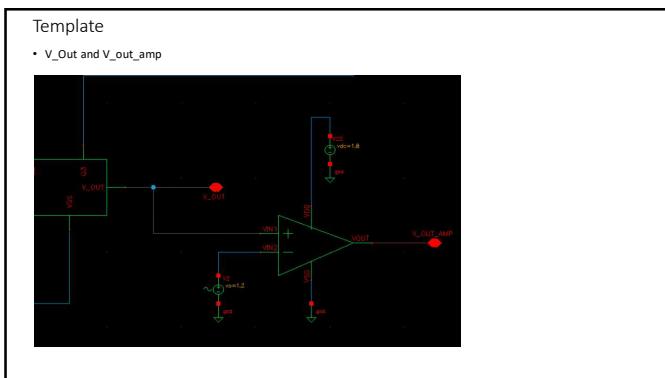
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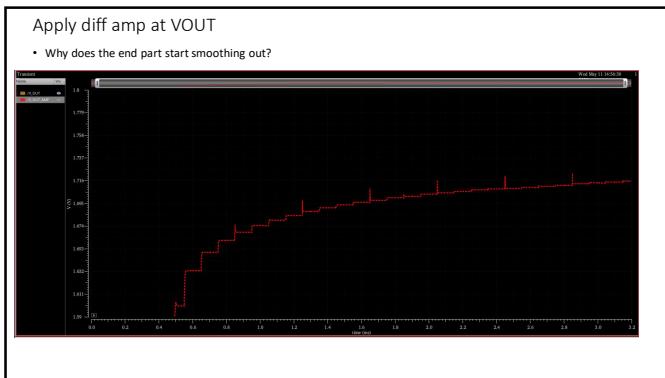
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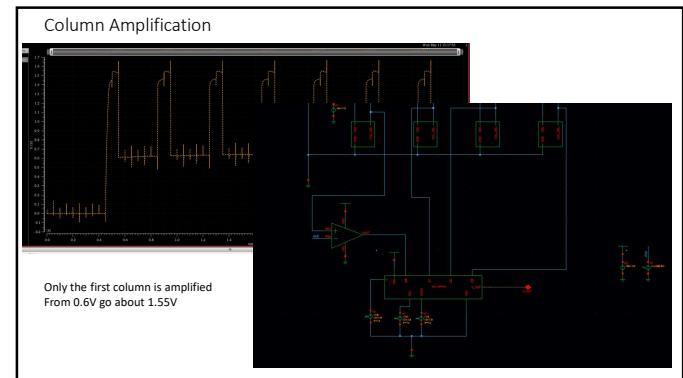
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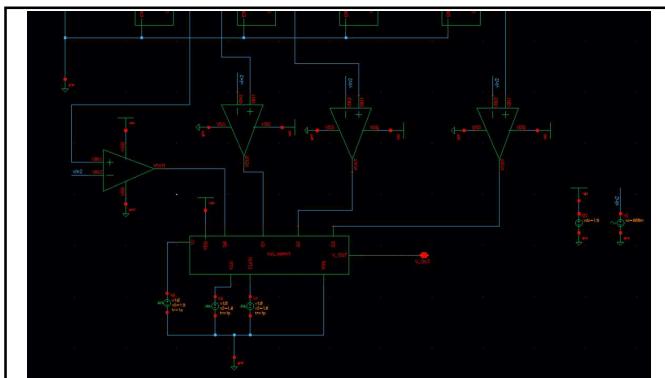
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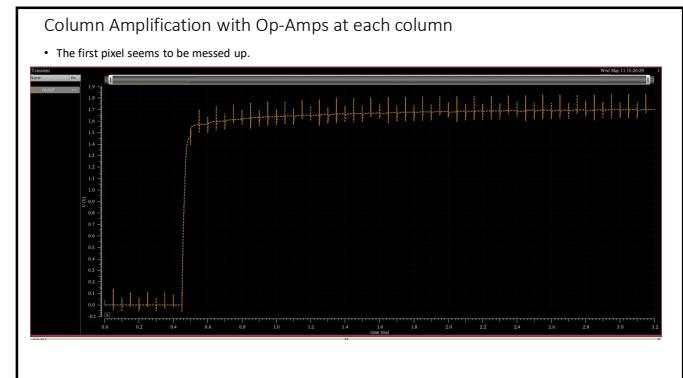
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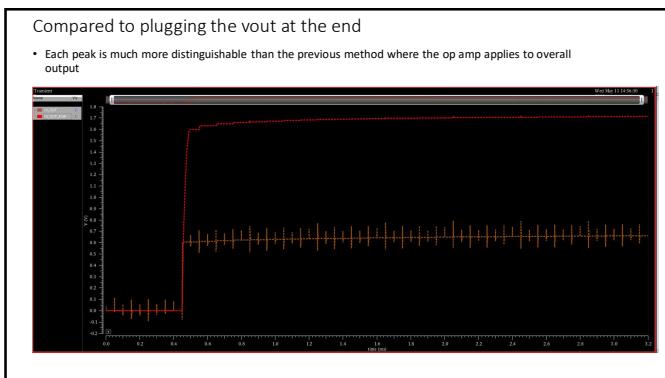
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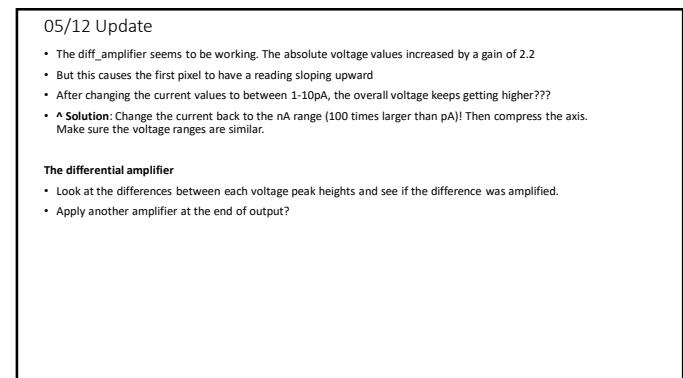
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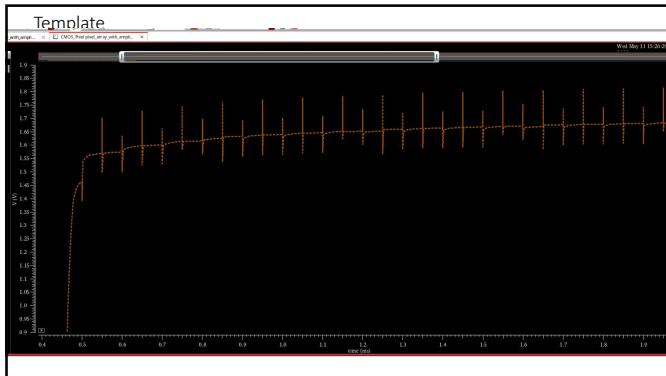
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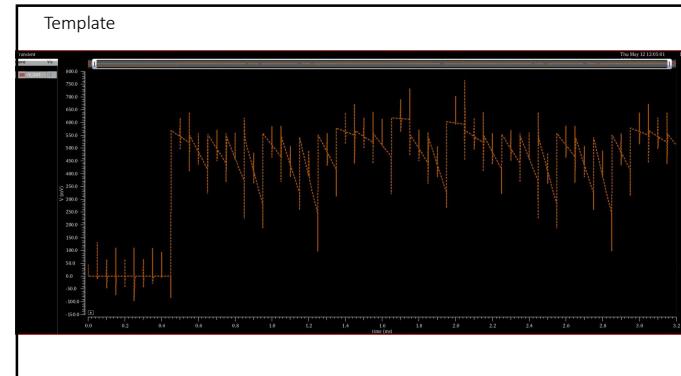
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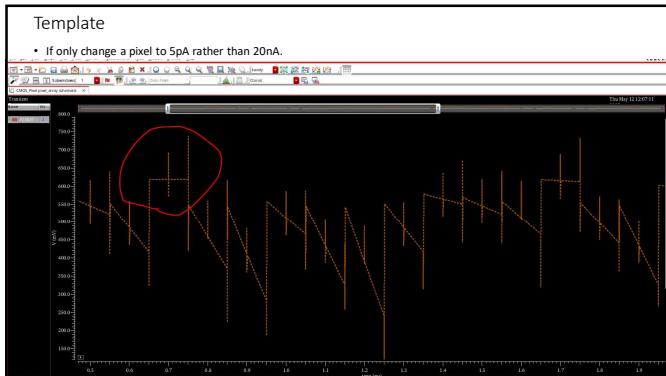
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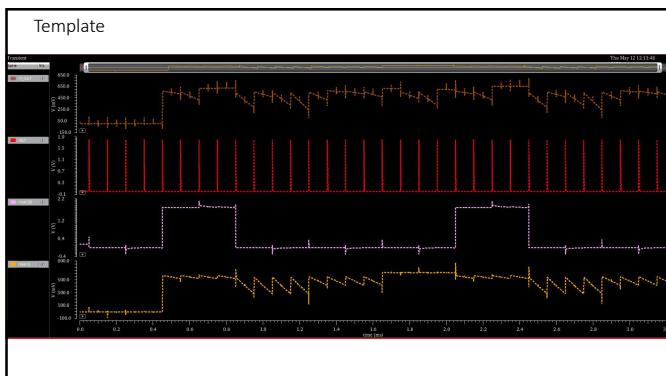
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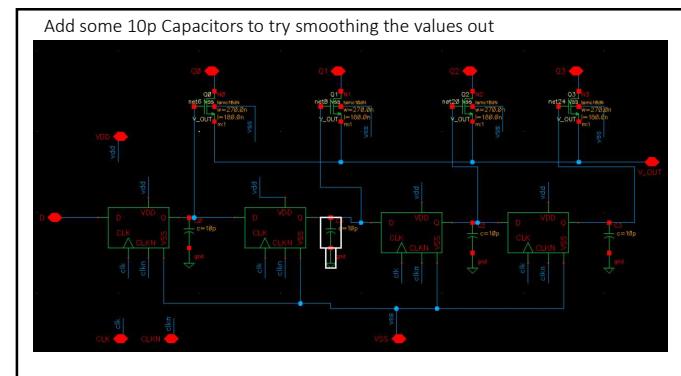
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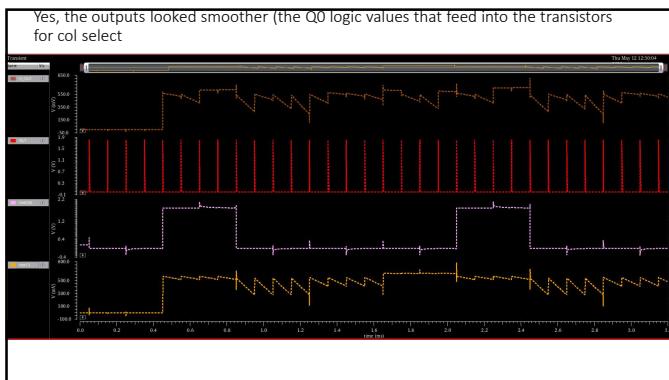
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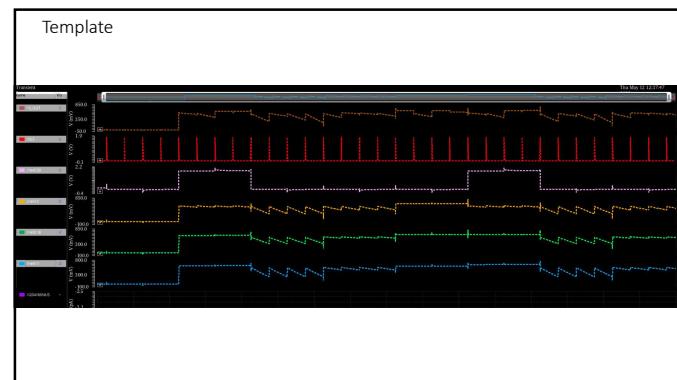
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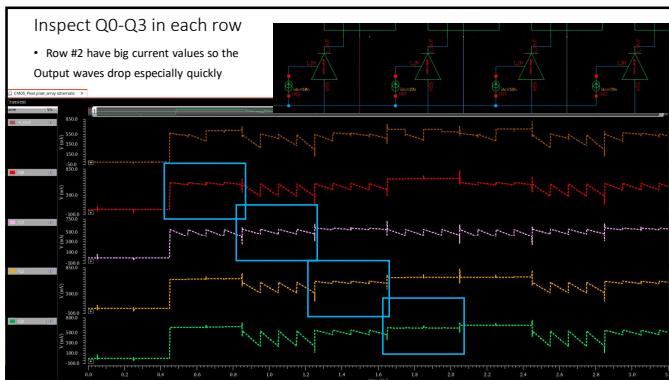
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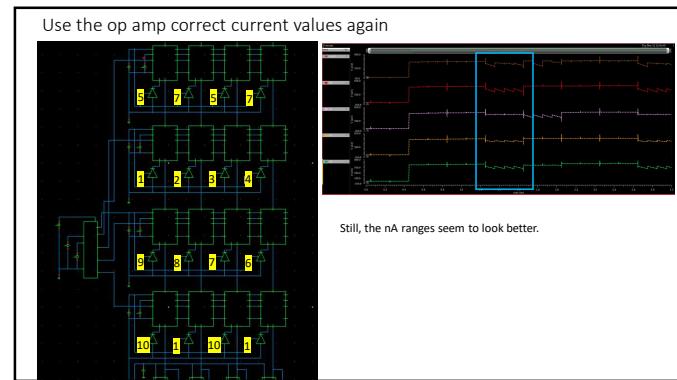
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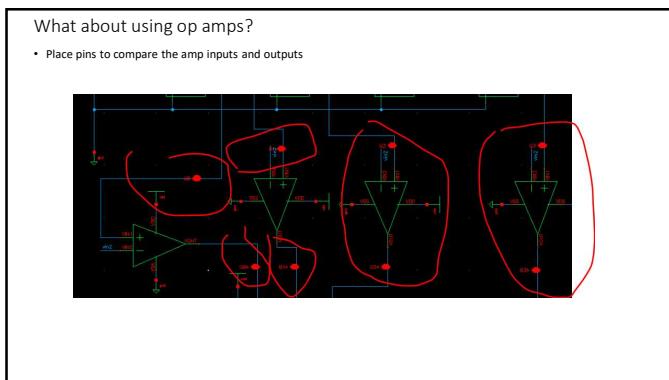
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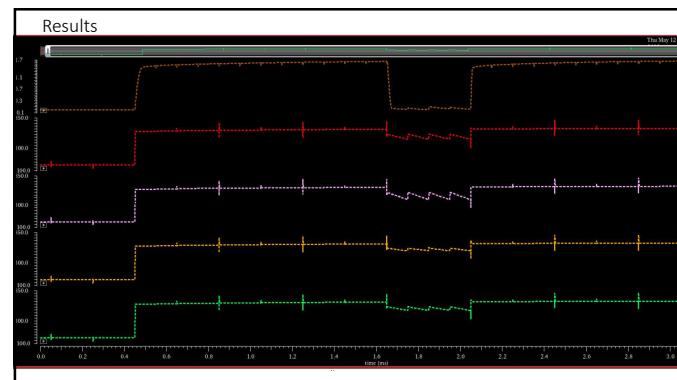
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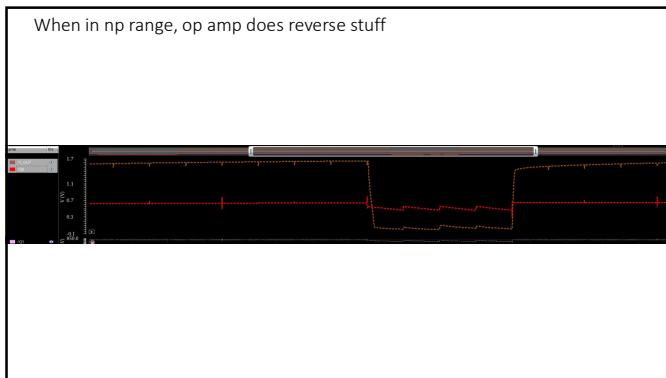
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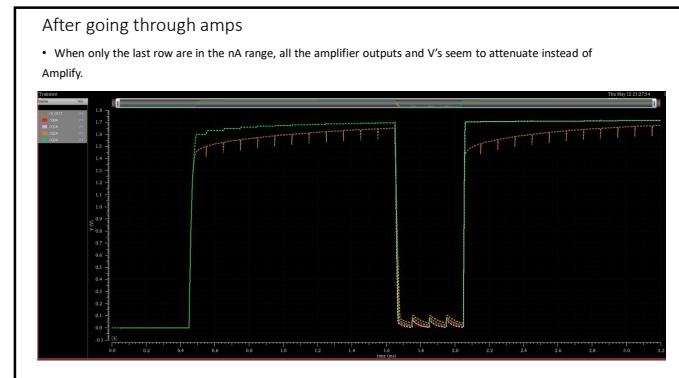
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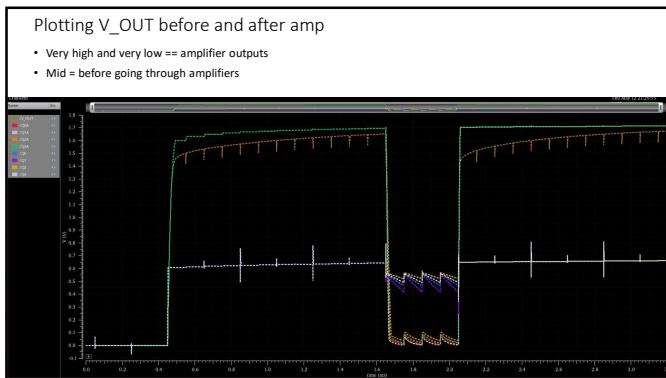
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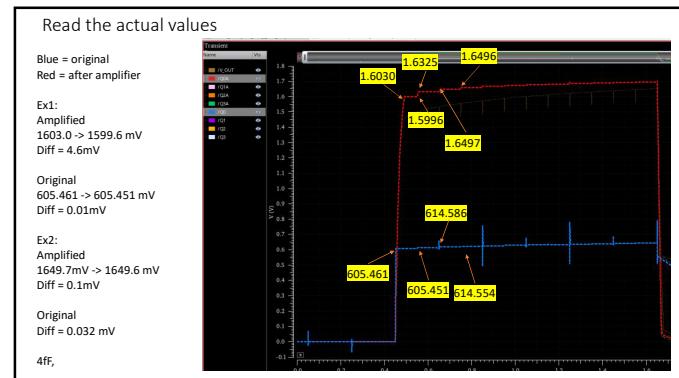
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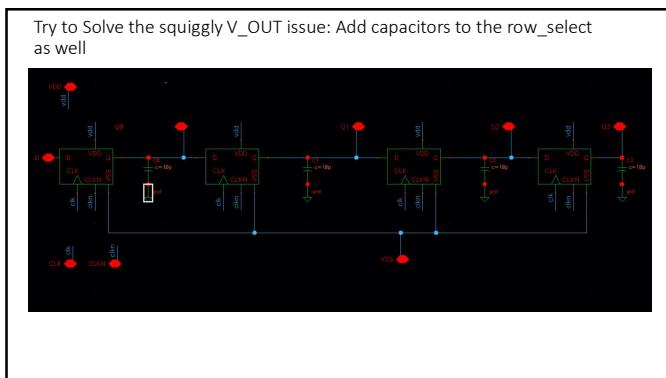
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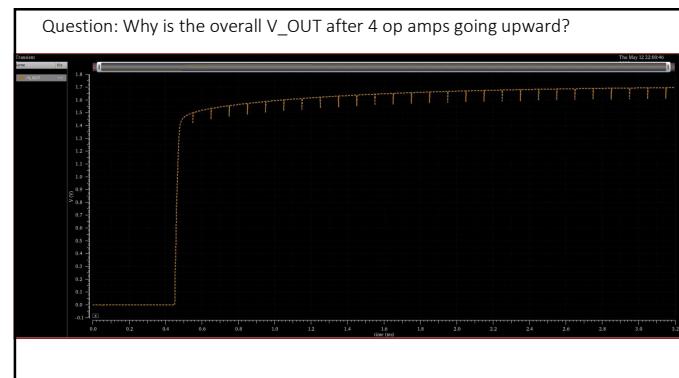
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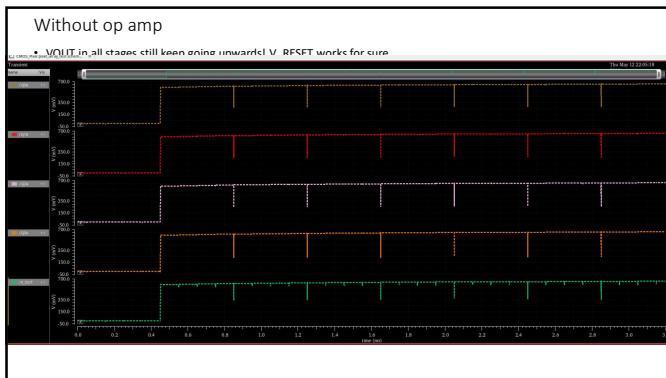
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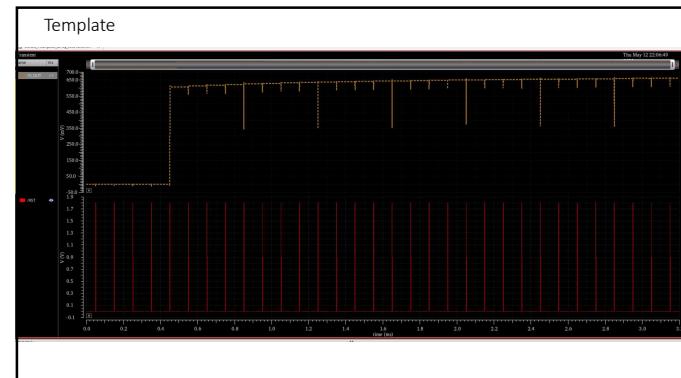
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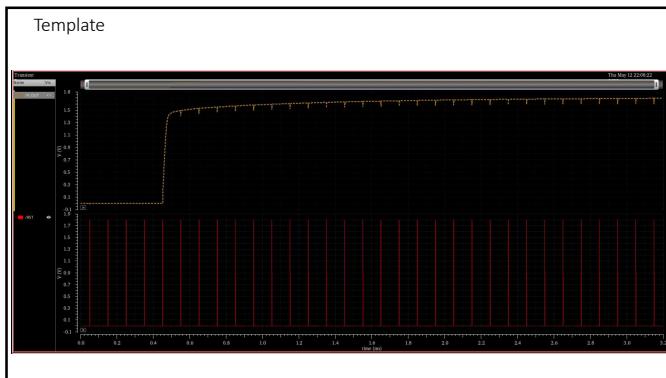
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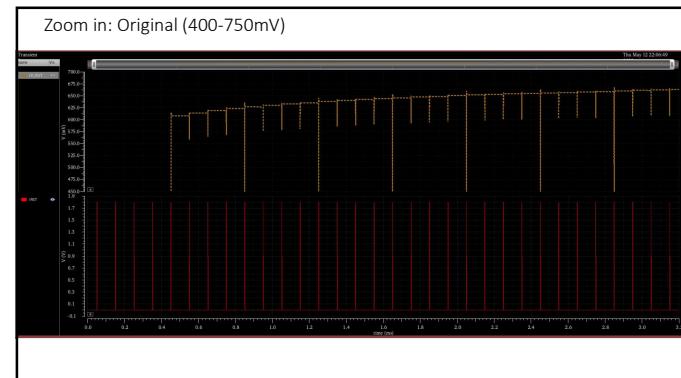
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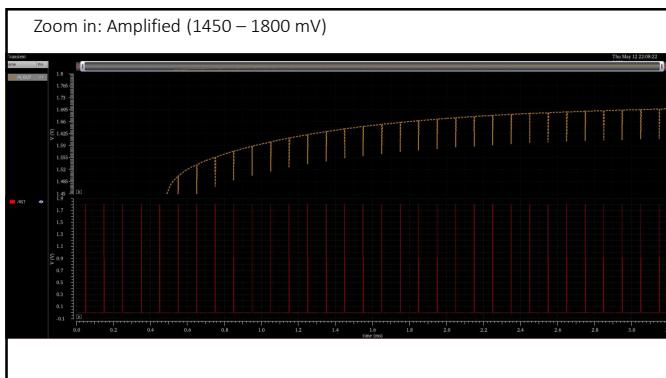
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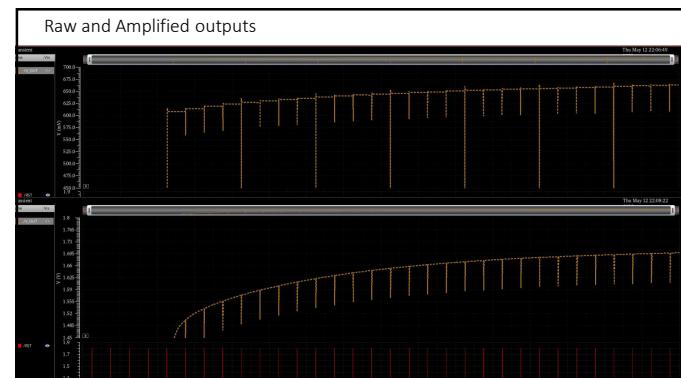
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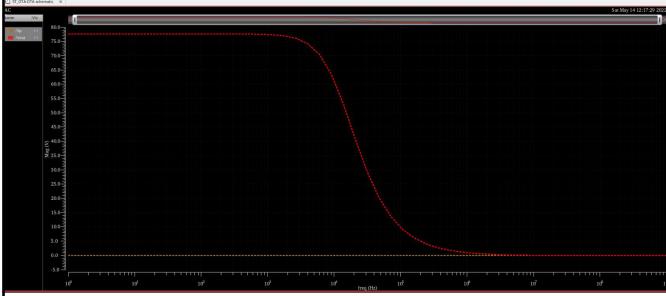
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Updated 05/14: Design the 5T_OTA

- Gain goes up to $75V/1V = 75!!$ Used optimized parameters in this video:
- https://www.youtube.com/watch?v=2kAUN_xBGuc&ab_channel=SpeedyZebra



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Template

Hi,
The m is the multiplication factor.

In Layout XL, for transistors, the m from the schematic is used to create multiple layout instances with common parameters.

i.e. for eg., a schematic instance M0 with total_width=6u, length=1u, fingers=3 finger_width=2u m=5

will result in 5 layout instances:

M0.0: total_width=6u, length=1u, fingers=3 finger_width=2u

M0.5: total_width=6u, length=1u, fingers=3 finger_width=2u

M0.2: total_width=6u, length=1u, fingers=3 finger_width=2u

M0.3: total_width=6u, length=1u, fingers=3 finger_width=2u

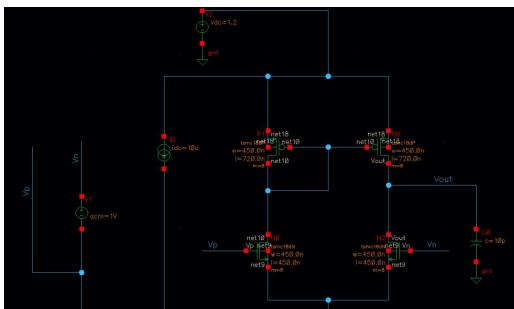
M0.4: total_width=6u, length=1u, fingers=3 finger_width=2u

Rgds,

Vikram

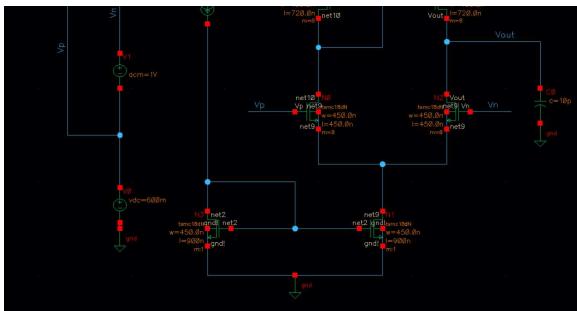
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Template



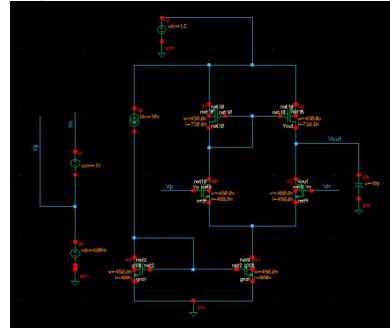
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Template



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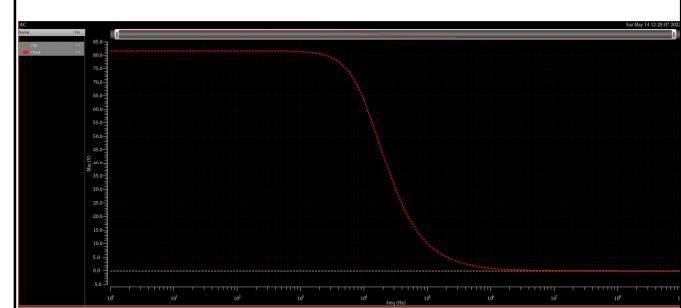
Template



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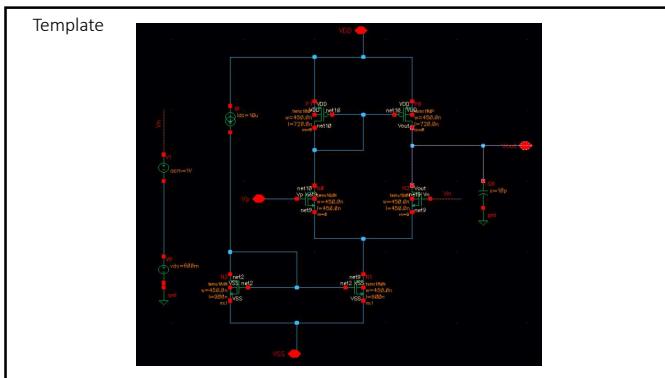
Template

- Gain is up to 82

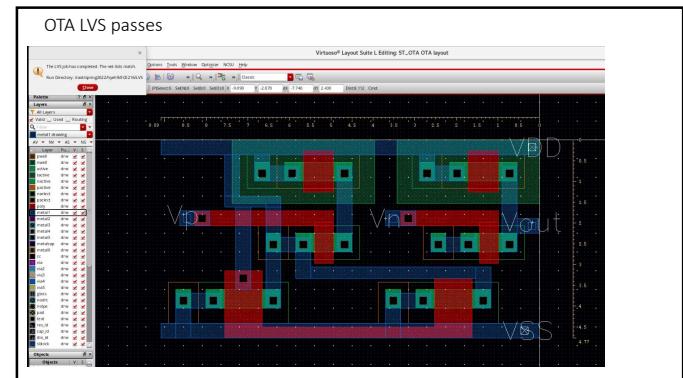


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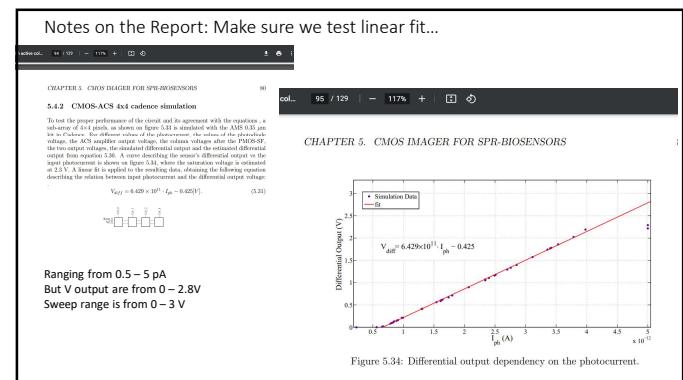
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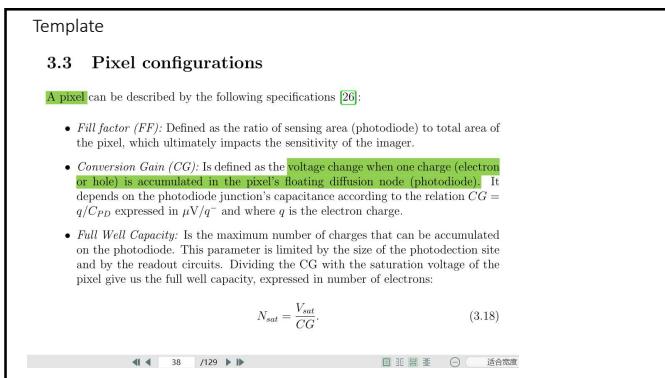
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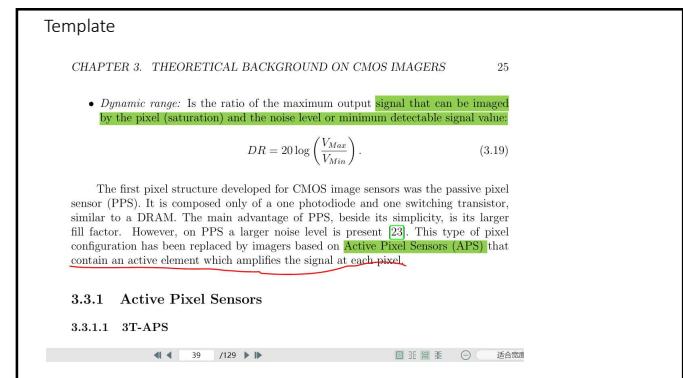
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65



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Template

3.5.3.3 Delta Double Sampling (DDS)

The Delta Double Sampling (DDS) noise suppression circuit was introduced to eliminate the charge transfer mismatch between the two signal paths in a differential FPN suppression circuit. It consists of two parallel S/H blocks, one for the V_{GS} signal and one for the V_{DS} signal, and averages the difference of the output signals. It is used to improve the corresponding noise performance of the sensor. This technique is also known as double sampling or CDS or NCDS. In fact this technique cannot be implemented by itself without the use of one of these two techniques [1]. Figure 3.13 shows a simplified schematic of the DDS noise suppression circuit. The two parallel S/H blocks have two parallel switches, M_{S1} and M_{S2} , and two parallel capacitors, C_{S1} and C_{S2} , sample the signals V_{GS} and V_{DS} respectively. When the i -th column is selected, two parallel switches, M_{S3} and M_{S4} , connect the two parallel S/H blocks to the inverter and the S/H output is connected to V_{OUT} and V_{REF} . When the i -th column is selected, two parallel switches, M_{S3} and M_{S4} , connect the two parallel S/H blocks to the inverter and the S/H output is connected to V_{OUT} and V_{REF} . When the i -th column is selected, two parallel switches, M_{S3} and M_{S4} , connect the two parallel S/H blocks to the inverter and the S/H output is connected to V_{OUT} and V_{REF} . When the i -th column is selected, two parallel switches, M_{S3} and M_{S4} , connect the two parallel S/H blocks to the inverter and the S/H output is connected to V_{OUT} and V_{REF} .

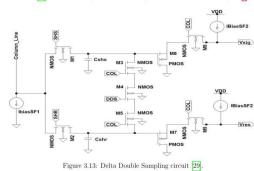
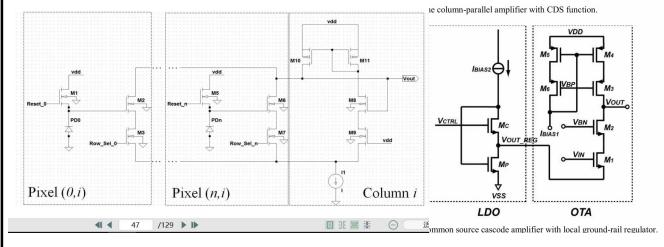


Figure 3.13: Delta Double Sampling circuit

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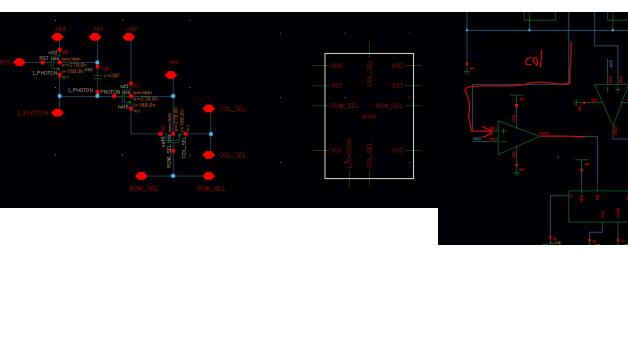
Template

the column-parallel amplifier with CDS function.



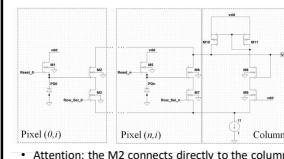
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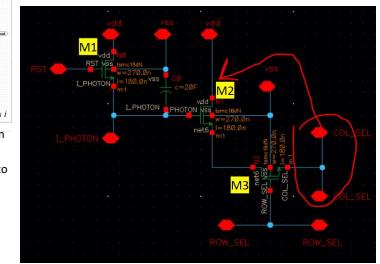


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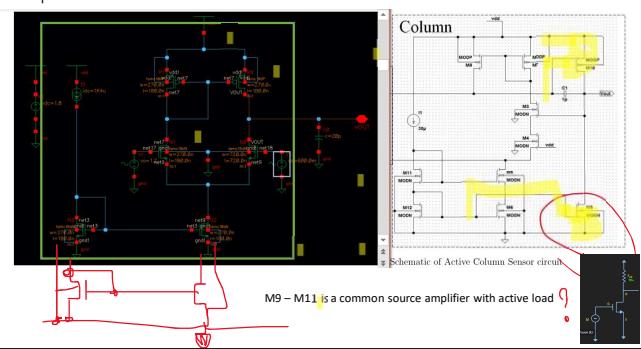


- Attention: the M2 connects directly to the column output instead of VDD.
- M3 connects to the bottom half of the amplifier to go to column select (?) and GND (?)
- When a column is selected, only one of the ROW_SELS are on. So the output



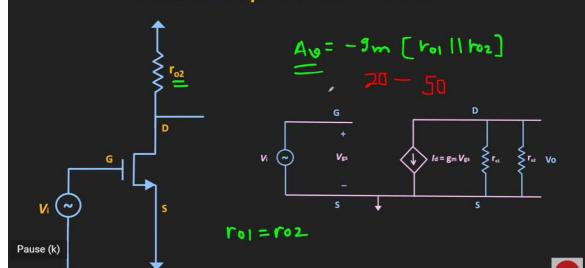
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Template



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Template

MOSFET Amplifier with Active Load

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Template

Table 5.8: Final ACS op-amp performance characteristics

Open loop gain	55 dB
Cut-off frequency	11.2 KHz
Gain bandwidth (GB)	6.31 MHz
Phase margin	85.6°
PSRR	56.5 dB
CMRR	56.5 dB
ICMR	0.15 V - 3 V
Output Swing	0.21 V - 3.1 V
Slew rate (positive)	23.0 V/μs
Slew rate (negative)	9.6 V/μs
Slew rate (average)	16.3 V/μs

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Template

$$dB = 20 \log_{10} \left[\frac{V_{OUT}}{V_{IN}} \right]$$

$$55dB = 20 \log_{10} [V_{out}/V_{in}]$$

$$55 = 20 \log_{10} (V_{out})$$

$$2.75 = \log_{10} (V_{out})$$

$$V_{out} = 10^{2.75} = 562.34132519 V$$

$$-10 = 20 \log_{10} \left[\frac{V_{OUT}}{12} \right]$$

Voltage gain is about 562 times
A .01 mV difference becomes 5.62 mV difference?

$$-0.5 = \log_{10} \left[\frac{V_{OUT}}{12} \right]$$

$$0.3162 = \frac{V_{OUT}}{12}$$

$$\therefore V_{OUT} = 0.3162 \times 12 = 3.79 \text{ Volts}$$

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