Signals and Systems
Lab with Opamps

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Overview

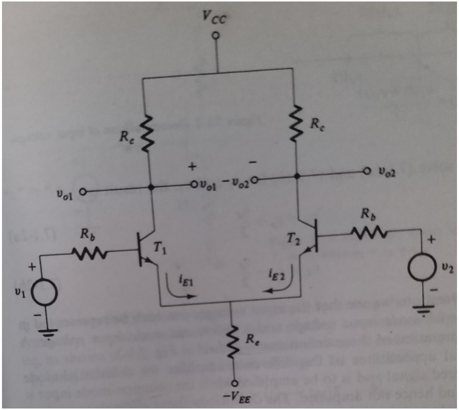
1. Operational Amplifier basics
   - Multiple transistor IC
   - Opamp circuit analysis
   - Practical considerations of opamp

2. Opamp - linear operations in time domain
   - Realizing linear functions
   - Response of PID controllers

Multiple BJT circuits in IC

- small size, low power consumption, high reliability
- very stable amplifier performance over wide range of applications
- linear and nonlinear operations can be realized by adding external components

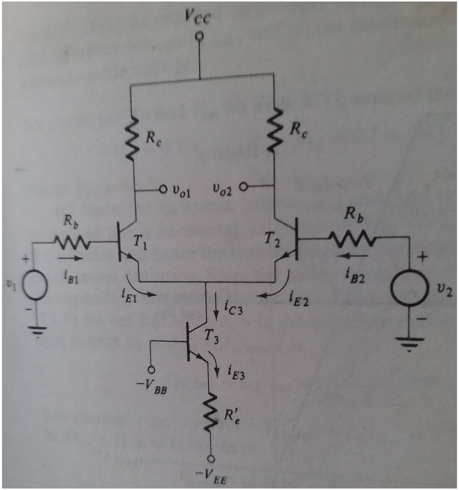
Basic transistor based difference amplifier



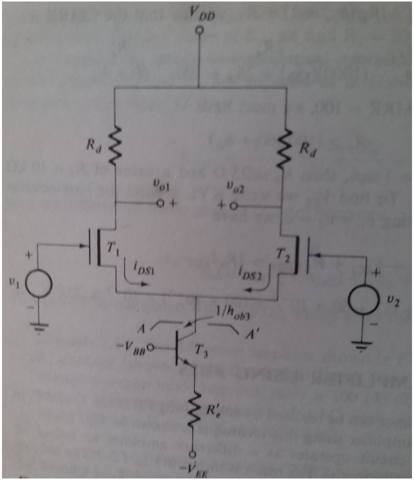
Multiple BJT circuit analysis

- Difference mode signal is $v_d = v_2 - v_1$
- Common mode signal is $v_a = \frac{v_2+v_1}{2}$
- So $v_2 = v_a + \frac{v_d}{2}$ and $v_1 = v_a - \frac{v_d}{2}$
- Applying KVL, KCL appropriately and noting the amplification factors (h_{fe}, h_{ib}) of individual transistors, output can be solved.
- Difference mode gain is $A_d = \frac{R_c/2}{h_{ib}+R_b/(h_{fe}+1)}$
- Common mode gain is $A_a = \frac{R_c}{2R_e+h_{ib}+R_b/(h_{fe}+1)}$
- Output signals can be written as $v_{o1} = A_d v_d - A_a v_a$ and $v_{o2} = -A_d v_d - A_a v_a$.
- Now the common mode rejection ratio $(CMRR = \frac{A_d}{A_a})$ can be evaluated from practice $2R_e >> h_{ib} + R_b/h_{fe}$ hence $CMRR >> \frac{v_a}{v_d}$.
- Other variants like constant current source, FET based, Darlington amplifiers are shown for conception. Details not covered.

Difference amplifier with constant current source

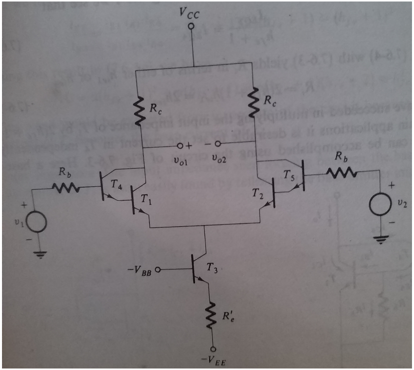


Field effect transistor based difference amplifier



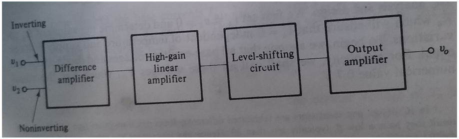
With FET as device, performance improves.

Darlington transistor based difference amplifier



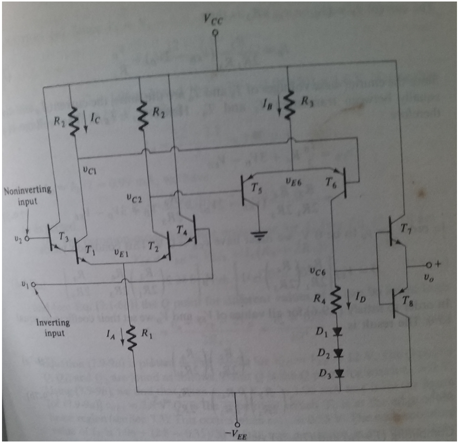
Such configuration enhances overall h_{fe} so that performance is better.

Overall block diagram of the opamp

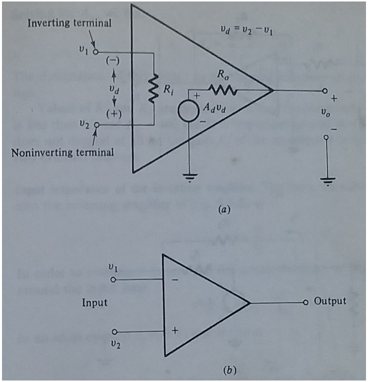


- Here the output is $v_o = -A_d(v_1 - v_2) - \frac{A_a(v_1+v_2)}{2}$.
- Typical values are $A_d = 10^5$ and $A_a = 1 \therefore CMRR \approx 100dB$.
- When $v_2 = 0$ the output v_o is opposite in phase to input v_1.
- When $v_1 = 0$ the output v_o is in phase with input v_2.
- Hence v_2 is noninverting input and v_1 is inverting input.
- When both inputs are zero, output remains zero in spite of power supply and temperature variations due to design.

Full blown IC internals of opamp



Operational Amplifier Equivalent Circuit Model

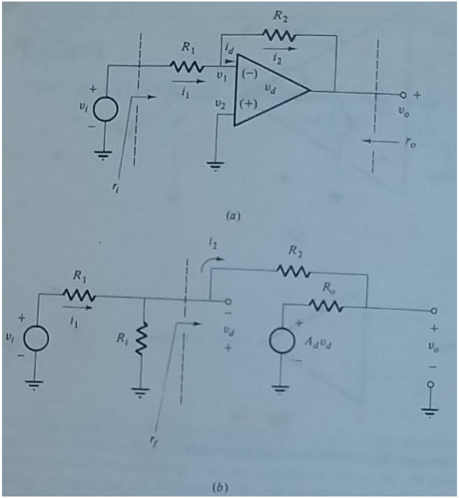


Input impedance R_i connected between input terminals v_1 and v_2. Output circuit is controlled voltage source $A_d v_d$ in series with output impedance R_o connected between output terminal and ground.

Ideal opamp assumptions

- Voltage gain A_d is very large (infinite), practically of the order of 10^5 compared to overall gain of the circuit.
- Input impedance R_i is very high, typically $100K\Omega$ compared to external resistances connected with system.
- Output impedance is very low, typically 100Ω and may be neglected.
- The differential input voltage $v_d = v_1 - v_2 \approx 0$ since $v_d = \frac{v_0}{A_d}$ and with infinite A_d this follows. Thus input of opamp is virtual short circuit.
- Now that $v_1 \approx v_2$ together with very large R_i, no current enters into the opamp.

Linear Inverting Amplifier Circuit



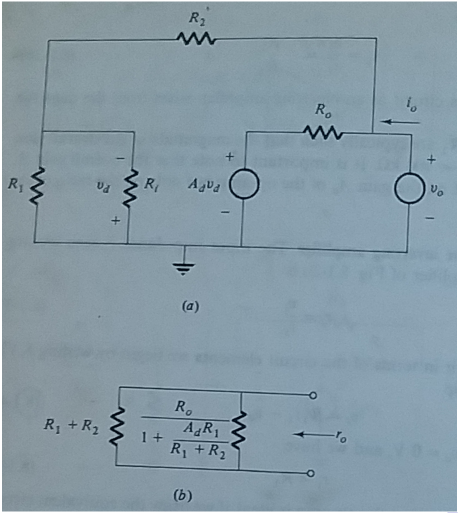
Voltage gain of the inverting opamp

- Overall voltage gain can be found from ideal opamp assumptions. Then $i_1 = i_2$ is possible.
- Now $i_1 - \frac{v_i + v_d}{R_1} = i_2 = \frac{-v_d - v_o}{R_2}$. Since v_d can be ignored, $\frac{v_i}{R_1} = -\frac{v_o}{R_2}$
- Then overall gain is $A_v = \frac{v_o}{v_i} = -\frac{R_2}{R_1}$.
- Should keep $R_2 < 100K\Omega$ and overall gain within the range of 50.

Input impedance of the inverting opamp

- Looking into the inverting amplifier, $r_i = \frac{v_i}{i_1}$
- Using KVL around the input loop, $v_i = R_1 i_1 - v_d$. From ideal opamp assumptions. Then $r_i = R_1$ since $v_d \approx 0$.
- If not ideal, $r_i = R_1 + R_i || r_f$ where $r_f = -\frac{v_d}{i_2}$.
- Now writing KVL by including R_2, we have $-v_d = R_2 i_2 + R_o i_2 + A_d v_d$ so that $r_f = -\frac{R_2 + R_o}{1 + A_d}$.
- $r_f << R_i$ and also $r_f << R_1$ so that $r_i \approx R_1$ even for non-ideal conditions.

Linear Inverting Amplifier Output impedance equivalent Circuit



Output impedance of the inverting opamp

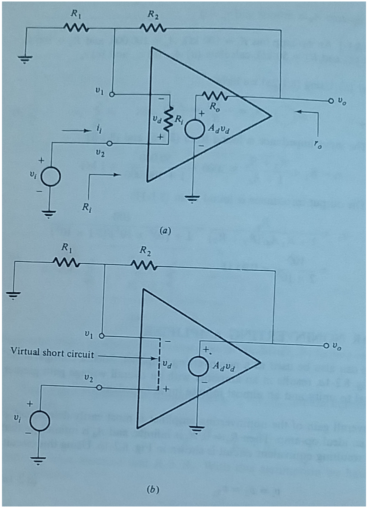
- Looking out of the inverting amplifier, $r_o = \frac{v_o}{i_o}$ with $i_o = \frac{v_o - A_d v_d}{R_o} + \frac{v_o}{R_1+R_2}$.
- Due to assumption of $R_i >> R_1$, further $-v_d = \frac{R_1}{R_1+R_2} v_o$
- Manipulating above gives $\frac{1}{r_o} = \frac{i_o}{v_o} = \frac{1+R_1 A_d/(R_1+R_2)}{R_o} + \frac{1}{R_1+R_2}$.
- This has two admittances, and for practical purposes $R_1 + R_2 >> 1 + R_1 A_d/(R_1 + R_2)$.
- Hence $r_o \approx \frac{R_o}{1+R_1 A_d/(R_1+R_2)}$.
- For ideal opamp, A_d is infinite so that $r_o = 0$.

Example problem

In the problem, $R_2 = 50k\Omega$, $R_1 = 1.0k\Omega$ are connected to opamp which has $R_o = 100\Omega$, $R_i = 100k\Omega$ and $A_d = 100000$.

- Gain $A_v = -\frac{R_2}{R_1} = -50$.
- Input impedance $r_i = 1000 + \frac{50000+100}{1+100000} \approx 1k\Omega$.
- Output impedance $r_o \approx \frac{100}{1+(10^3 x 10^5)/(5.1 x 10^4} \approx \frac{100}{2x10^3} = 0.05\Omega$.

Noninverting Amplifier Circuit



Noninverting Amplifier Circuit analysis

- Gain with ideal opamp assumptions. $R_o = 0$, $R_i = \infty$, $A_d = \infty$ so that $v_d \approx 0$.
  Now $v_i = v_2 = v_1$ and $v_1 = \frac{R_1}{R_1+R_2} v_o$, so that
  $A_v = \frac{v_o}{v_i} = \frac{R_1+R_2}{R_1} = 1 + \frac{R_2}{R_1}$.
- Input impedance $r_i = \frac{v_i}{i_i}$ with $i_i = \frac{v_d}{R_i} = \frac{v_o}{A_d r_i}$ Since $v_o = (1 + \frac{R_2}{R_1})v_i$ we have $i_i = \frac{1+R_2/R_1}{A_d R_i} v_i$. Hence $r_i = \frac{A_d R_i}{1+R_2/R_1}$ remains very large.
- Output impedance Calculations are similar to inverting case.
  $\frac{1}{r_o} = \frac{i_o}{v_o} = \frac{1+R_i A_d/(R_1+R_2)}{R_o} + \frac{1}{R_1+R_2}$ remains very small.

Feedback Amplifier Circuit analysis

- The resistances feed back portion of output voltage to opamp inverting circuit.
- When feedback connection is made to inverting input, it is negative feedback.
- When feedback connection is made to noninverting input, it is positive feedback.
- When $i_d = -v_d/R_i$ is the difference $i_2 - i_1 = i_d$ in inverting case, this difference current is forced to zero by the feedback.
- When $v_2 - v_1 = v_d$ in non-inverting case, this difference voltage is forced to zero by the feedback.
- Advantage of feedback is that the gain becomes independent of the opamp characteristics or parameters.

Datasheet specifications of opamps

- **Supply voltage:** Two supplies are often required $\pm 15v$ typical. Some require single supply $+15v$ only.
- **Power dissipation:** Maximum power the IC can dissipate without destruction, typically $0.5W$.
- **Operating temperature:** Ambient temperature is generally $0^o C$ to $70^o C$ for commercial grade, military operations may range from $-55^o C$ to $+125^o C$.
- **Maximum input difference or common mode voltage:** When input difference exceeds v_d specified by manufacturer, or excessive common mode voltage as well, can destroy the opamp. Typically $\pm 30V$ is specified.

Electrical characteristics of opamps

- **Input offset voltage** - value of v_d that makes v_o zero. Typically $1mV$ needed.
- **Input offset current** - difference in current that makes v_o zero with offset voltage. typically $1nAmp$.
- **Input bias current** - needed to operate input transistors, typically $300nA$.
- **Temperature coefficient of offset voltage** - typically varies by $5\mu V/^oC$.

Gain characteristics of opamps

- **Large signal voltage gain** - typically 100000 and same as A_d.
- **Common mode rejection ratio** - ratio of difference mode gain to common mode gain. $A_d/A_a = 100dB$.
- **Supply voltage rejection ratio** - Output voltage should not vary with supply voltage. When supply is $V_{cc} + \Delta V_{cc}$, required input offset becomes $V_{io} + \Delta V_{io}$ so that $\frac{\Delta V_{io}}{\Delta V_{cc}}$ defines the term and is typically $-100dB$.

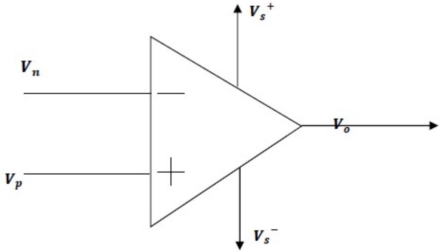
Frequency characteristics of opamps

- **Frequency compensation** - transient oscillations due to presence of stray capacitance must be compensated for.
- **Unity gain bandwidth** - Frequency range from dc to the frequency at which amplifier gain reduces to unity, typically $1MHz$.
- **Slew rate and settling time** - For large step input, output rises with a finite slope called slew rate. There is often overshoot and then undershoot before the output settles. This is due to saturation and cutoff of inbuilt transistors.

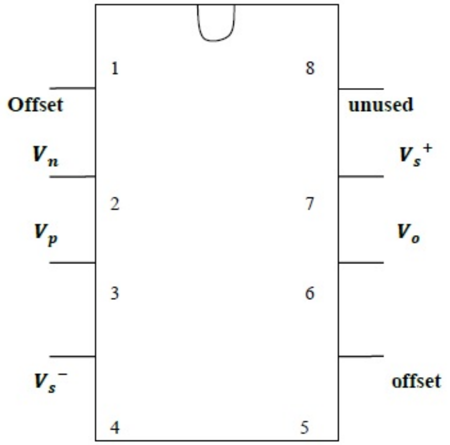
Different types of opamps

- **General purpose** - 741 will be used for the basic experiments.
- **High frequency, high slew rate** - needed for sampling at high frequencies
- **High voltage, high power, single supply** - needed for power electronics applications
- **Low input offset voltage and drift** - needed when there are issues with operating temperature
- **Programmable opamp** - there is more control on the electrical characteristics.
- The 741 is chosen because it has internal frequency compensation, unity gain bandwidth of $1MHz$ and slew rate of $0.5V/\mu S$.

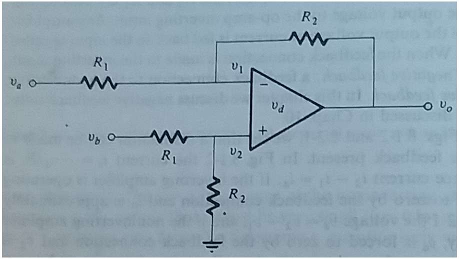
741 Opamp Pinout based circuit connectivity



741 Opamp Pinout basics



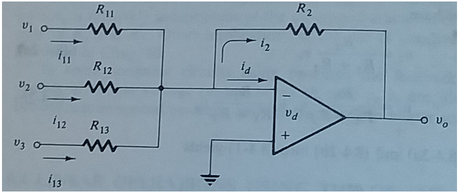
Difference Amplifier Circuit



Difference amplifier analysis

- Output is $v_o = -A_d(v_2 - v_1) - A_a\frac{v_2+v_1}{2}$
- Now $v_2 = \frac{R_2}{R_1+R_2}v_b$ and $v_1 = \frac{R_2}{R_1+R_2}v_a + \frac{R_1}{R_1+R_2}v_o$.
- Putting back and solving, $v_o = \frac{-A_d\frac{R_2}{R_1+R_2}(v_b-v_a)-A_a\frac{R_1}{R_1+R_2}((v_b+v_a)/2)}{1-A_d\frac{R_1}{R_1+R_2}+A_a\frac{R_1}{2(R_1+R_2)}}$
- Using approximations like $A_d >> A_a$ and $A_d >> 1 + R_2/R_1$ gives $v_o = \frac{R_2}{R_1}(v_b - v_a) + \frac{A_a}{A_d}\frac{v_b+v_a}{2}$
- First term is difference mode, amplified by inverting amplifier gain. Second term is common mode, attenuated by inverse of CMRR (common mode rejection ratio). Hence called difference amplifier.

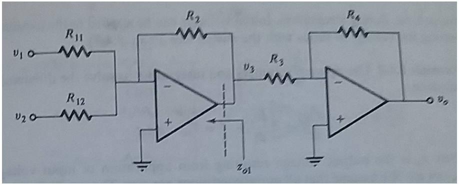
Sum Amplifier Circuit



Summing amplifier analysis

- Current equation from KCL is $i_{11} + i_{12} + i_{13} = i_2$ since $v_d = i_d = 0$.
- Now $i_{11} = \frac{v_1}{R_{11}}$, $i_{12} = \frac{v_2}{R_{12}}$, $i_{13} = \frac{v_3}{R_{13}}$. $i_2 = -\frac{v_2}{R_2}$.
- Hence $v_o = -(\frac{R_2}{R_{11}} v_1 + \frac{R_2}{R_{12}} v_2 + \frac{R_2}{R_{13}} v_3)$.
- Each input voltage is thus multiplied with a scale factor and added to produce the output voltage.

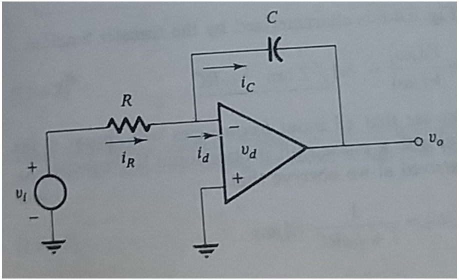
Designed output Amplifier Circuit



Designed output amplifier analysis

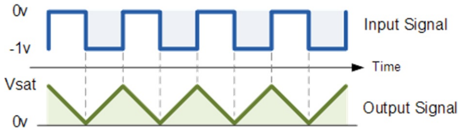
- Two opamps are used here. First opamp does the necessary voltage scaling while second one only changes the sign.
- Choose $R_2 = R_3 = R_4 = 10k\Omega$
- Choose $R_{11} = 5k\Omega$ and $R_{12} = 2k\Omega$.
- Neglect $z_{o1} < 1\Omega$.
- Can be shown that the Designed output $v_o = 2v_1 + 5v_2$.

Integrator opamp Circuit

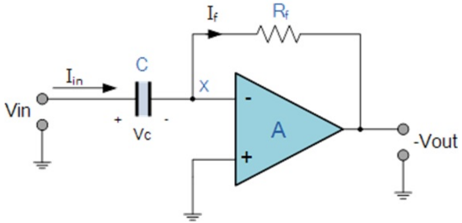


Integrator opamp analysis

- With ideal opamp assumptions, Current equation from KCL gives $i_R = \frac{v_i}{R} = i_C = -C\frac{dv_o}{dt}$.
- Hence
$$v_o = -\frac{1}{RC}\int^t v_i(\tau)d\tau$$
which implies integration of the input signal at the output.
- Swapping the position of resistance and capacitance, we get the derivative opamp circuit. Check it out.

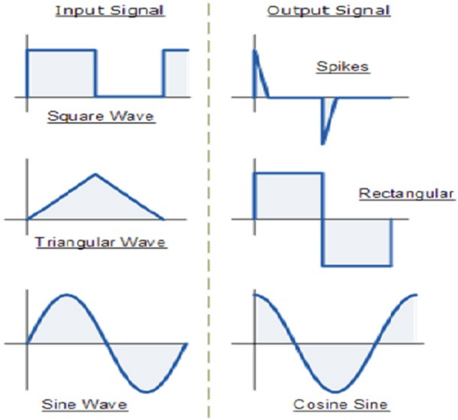


Differentiator opamp Circuit analysis

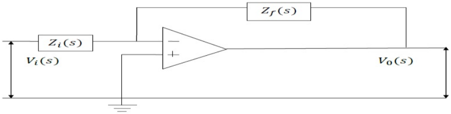


- With ideal opamp assumptions, Current equation from KCL gives $I_f = -\frac{V_{out}}{R_f} = I_{in} = C\frac{dV_{in}}{dt}$.
- Hence $V_{out} = -RC\frac{dV_{in}}{dt}$ which implies differentiation of the input signal at the output.

Differentiator opamp Output



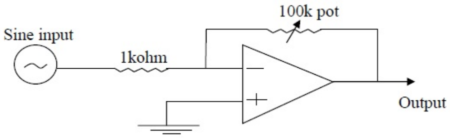
Opamp based basic linear PID like circuit



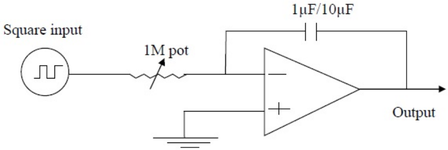
Opamp based circuit options tabulated

Controller	Z_f	Z_i	Transfer Function G(s)
P	R_f	R_i	$-\dfrac{R_f}{R_i}$
PI	$R_f + \dfrac{1}{sC_f}$	R_i	$-\left[\dfrac{R_f}{R_i} + \dfrac{1}{sC_f R_i}\right]$
PD	R_f	$\dfrac{R_i}{sC_i R_i + 1}$	$-\left[\dfrac{R_f}{R_i}\left(sC_i R_i + 1\right)\right]$
PID	$R_f + \dfrac{1}{sC_f}$	$\dfrac{R_i}{\left(sC_i R_i + 1\right)}$	$-\left[\dfrac{\left(sC_i R_i + 1\right)\left(sC_f R_f + 1\right)}{\left(sC_f R_i\right)}\right]$

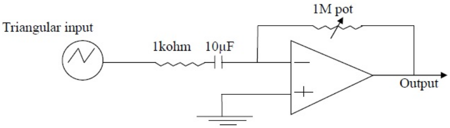
Opamp based proportional circuit



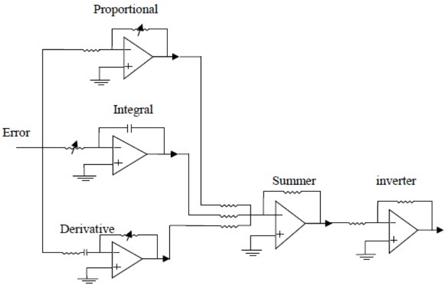
Opamp based PI circuit



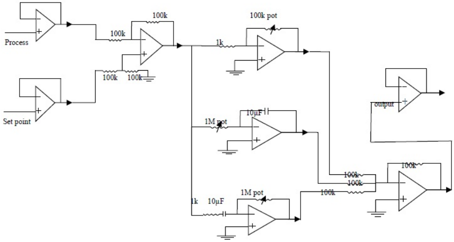
Opamp based PD circuit



Opamp based cascaded PID circuit



741 Opamp based complete PID circuit



Effect of increasing PID coefficients

Parameter	Rise Time	Overshoot	Settling Time	Steady-State Error	Stability
k_p	Decrease	Increase	Small Change	Decrease	Degrade
k_i	Decrease	Increase	Increase	Elimination	Degrade
k_d	Minor Change	Decrease	Decrease	No effect in theory	Improve if k_d is small