INDIAN INSTITUTE OF ENGINEERING SCIENCE AND TECHNOLOGY, SHIBPUR

B.E. 3rd SEMESTER (CS) MID TERMINAL EXAMINATION, 2016

Digital logic (CS301)

FULL MARKS: 50 *TIME: 2 Hrs*

1. (a) Simplify the following Boolean expressions to a minimum number of literals.
   (i) ABC+A′B+ABC′ (ii) (BC′+A′D).(AB′+CD′)
   (b) Reduce the followings
   (i) A′C′+ABC+AC′ to three literals
   (ii) (A′+C)(A′+C′)(A+B+C′D) to four literals [4+6]

2. (a) Find the complement of (i) (AB′+C)D′+E (ii) (X+Y′+Z)(X′+Z′)(X+Y)
   (b) Simplify F=XY′Z+X′Y′Z+W′XY+WX′Y+WXY using K-map. Realize the simplified logic function using two input NAND gate. [4+6]

3. (a) Find the essential prime implicants of the function
   F(W, X, Y, Z)=∑(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)
   (b) Simplify F together with the don't care condition. Realize the simplified expression using two NOR gates assuming that all the normal and complement inputs are available.
   F(A, B, C, D) = ∑(0, 1, 2, 9, 11), d(A, B, C, D)=∑(8, 10, 14,15)
   (c) A logic circuit has 4 inputs and 1 output. The output is equal to 1 when all the inputs are 1 or none of the inputs are equal to 1 or an odd number of inputs are 1. Find the simplified output function in SOP. [2+5+3]

4. (a) Design one full adder using two half adder and one OR gate.
   (b) Design full adder using two 4:1 MUX.
   (c) Discuss about the advantages and disadvantages of ripple carry adder and carry look ahead adder? [2+4+4]

5. (a) Draw the circuit and explain the operation of CMOS inverter.
   (b) In a DTL circuit voltage across conducting diode is 0.7 volt, cut in voltage of the diode is 0.6 volt, cut in voltage of the transistor is 0.5 volt, V_{CEsat}=0.2 volt, V_{BEsat}=0.8 volt, β=30. Find the logic 0 and logic 1 noise margin.
   (c) Draw Venn diagram illustration of X.(Y+Z). [4+4+2]

INDIAN INSTITUTE OF ENGINEERING SCIENCE AND TECHNOLOGY, SHIBPUR

B.E. 3rd SEMESTER (CS) FINAL EXAMINATION, 2016

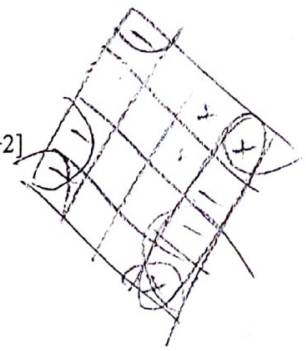
Digital logic (CS301)

FULL MARKS: 70 TIME: 3 Hrs

(Answer any five)

1. (a) Find the 9's complement of the following 8-digit decimal numbers.
(i)12349876 (ii) 00980100 (iii) 90009951 (iv) 67543218
(b) Perform subtraction with the following unsigned decimal numbers by taking the 10's complement of the subtrahend.
(i) 5250-1321 (ii) 1753-8640 (iii) 20-100 (iv) 1200-250
(c) In a DTL circuit voltage across conducting diode is 0.7 volt, cut in voltage of the diode is 0.6 volt, cut in voltage of the transistor is 0.5 volt, V_{CEsat}=0.2 volt, V_{BEsat}=0.8 volt, β=30. Find the logic 0 and logic 1 noise margin.
(d) The state of a 12-bit register is 010110010111. What is the content of the register in BCD and in excess-3 code? [2+6+4+2]

2. (a) Prove that xy+x′z+yz = xy+x′z
(b) Simplify the following Boolean expressions to a minimum number of literals.
(i) x′yz+xz (ii) xy+x(wz+wz′)
(c) Find the complement of F = x+yz. Show that F.F′=0 and F+F′=1
(d) Convert the following expressions into SOP and POS.
(i) (AB+C)(B+C′D) (ii) x′+x(x+y′)(y+z′)
(e) Show that dual of Exclusive-OR is its complement. [1+3+4+4+2]



3. (a) Simplify the following Boolean function using K-map.
(i) F(A, B, C, D) = ∏(0, 1, 2, 3, 4, 10, 11)
(b) Find the essential prime implicants of the following Boolean function.
F(W, X, Y, Z) = ∑(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)
(c) Simplify F together with the don't care condition.
F(A, B, C, D) = ∑(0, 1, 2, 9, 11), d(A, B, C, D)=∑(8, 10, 14,15)
(d) Simplify the following Boolean functions using K-map and implement them using 3-level NOR gate.
(i) F(W, X, Y, Z)=WX′+Y′Z′+W′YZ′ (ii) F(W, X, Y, Z) = ∑(5, 6, 9, 10) [2+2+3+7]

4. (a) Design a combinational circuit with three inputs (A, B, C) and one output (Y). The output is equal to 1 when the binary value of the input is less than 3. Otherwise the output is 0.
(b) Design a combinational circuit that adds one to a 4-bit binary number ($A_3A_2A_1A_0$) using four half adders.
(c) Prove the followings:
(i) x′⊕ y =x⊕ y′=(x⊕y)′= xy+x′y′ (ii) x⊕1=x′and x⊕0=x (iii) x⊕y=x+y if xy=0
(d) Define the following terms.
(i) Fan out (ii) Propagation delay (iii) Noise margin [2+2+2+1+1+6]

5. (a) Implement the following Boolean function using 8x1 MUX.
F(A, B, C, D) = ∑(0, 3, 5, 6, 8, 9, 14, 15)
(b) Draw the block diagram of a 5x32 decoder using four 3x8 decoders with enable input and one 2x4 decoder.
(c) Design a combinational circuit that compares two 4-bit numbers A and B to check if they are equal. The output of the circuit (X) is 1 if A=B and 0 if A≠B.
(d) Draw and explain the operation of a CMOS NAND. [4+5+2+3]

circuit of a 4-bit binary up ripple counter using negative edge triggered J-K flip flop.

(b) A flip flop has 10 ns propagation delay. What is the maximum delay of a 10-bit binary ripple counter and synchronous counter using such flip flops?

(c) How many clock pulses are required to shift 8-bit data through a 4-bit shift register?

(d) Write the output of the circuit in figure 1 for six clock pulses. Assume that the initial value of Q is 0.

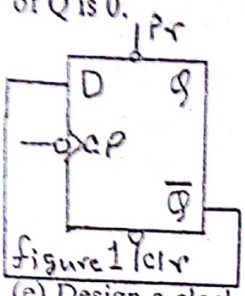


figure 1

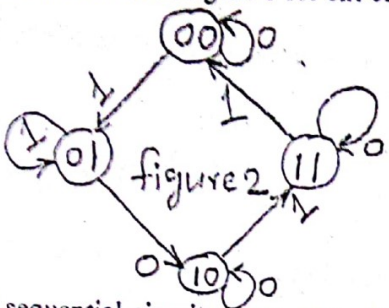


figure 2

(e) Design a clocked sequential circuit whose state diagram is shown in figure 2. Design the circuit using J-K flip flop. [3+2+1+2+6]

7. (a) What is the content of the shift register in figure 3 after 3 clock pulses? Assume that the initial content of the register is 0110.

(b) The characteristic table of X-Y flip flop is given below. Implement it using J-K flip flop.

X	Y	Q_{n+1}
0	0	1
0	1	Q_n
1	0	Q_n'
1	1	0

(c) What is the mod value of an-bit ring counter and switch-tail counter?

(d) Draw the block diagram of a 16x4 RAM. Explain the read and write operation.

(e) Find the mod value of the counter in figure 4. [3+2+2+4+3]

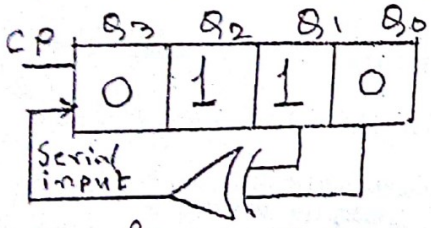


figure 3

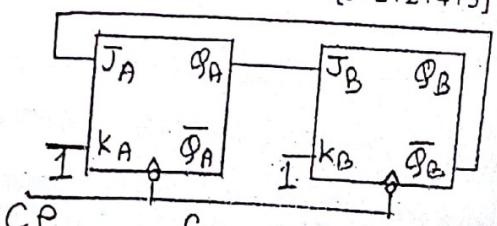


figure 4

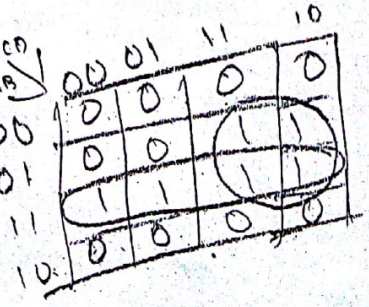
$xy + x'z + yz = xy + x'z$

$xy + x'z + yz(x + x')$

$= xy + x'z + xyz + x'yz$

$= xy(1 + z) + x'z(1 + y)$

$= xy + x'z$



1010 0100 0001 1000 0110 0011 1011 1010