Indian Institute of Engineering Science and Technology, Shibpur

BTech (CST) 5th Semester Mid Semester Examination, December 2020

Computer Architecture and Organization II (CS-502)

Full Marks: 30 Time: 45 Minutes

Answer all questions

1A) Let the content of registers (in hex) R1 = 20, R2 = 1F and the content (in hex) of memory location MEM1 = 11, MEM2 = 05. Consider execution of program segment of five instructions I1, I2, I3, I4, I5 (in sequence) in a 4-stage (IF, ID, OF, EX) conventional instruction pipeline. Assume instruction fetch is done from I-cache and memory data access is from D-cache.

a) If I1: LOAD R2, MEM2; I2: LOAD R1, MEM1; I3: R1 = R1 + R2; I4: R1 = 2R1, I5: R2 = R1-R2, then

Show the snapshot of pipeline stages occupied by the instructions in different clock cycles during execution of the program segment when data hazard is not addressed. Find content of R1 (in hex) at the end of clock cycle 6 and 7; and the content of R1 and R2 (in hex) at the end of execution of this program segment. 5

b) If I1: LOAD R2, MEM2; I2: LOAD R1, MEM1; I3: R1 = R1 + R2; I4: R1 = 2R1, I5: R2 = R1-R2, then

Show the snapshot of pipeline stages occupied by the instructions in different clock cycles during execution of the program segment avoiding data hazards. Assume data forwarding is allowed. Find the content of R1 (in hex) at the end of clock cycle 6 and 7; and the content of R1 and R2 (in hex) at the end of program segment execution. 5

B) A program, consisting of two consecutive loops L1 and L2 (as shown in Fig, 1), is executed in CPU_{iiest}. L1 and L2 iterate 2 and 3 times respectively. The CPU_{iiest} implements 2-bit history (counter) for loop branch prediction. The counter is initialized to ”00” before execution of L1. Determine count value of the 2-bit history counter after each iteration of the loops L1 and L2. 3

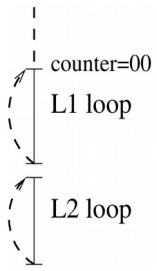

Fig. 1

2A) Define compulsory and conflict misses in a cache system with examples. A CPU has I-cache and D-cache. The D-cache is of 32 KB and direct mapped. The main memory (MM) block size is 128-byte. Suppose A, a two-dimensional 256x256 array, is stored in MM in row major order. Each A[*i,j*] is of *eight* bytes. The blocks for A are consecutive in MM. Consider the following C code segment

```
for (i = 0; i<256; i++) {
    for (j =0; j<256; j++) {
        y+ = A[j][i];

 } }
```

a) Find the maximum number of MM blocks that can be accommodated in D-cache at a time.
b) Find the number of blocks compete for the same place in D-cache.
c) Find number of compulsory and conflict misses in D-chace, experienced by the program segment.
d) Show whether the loop interchange technique can reduce/increase the cache miss rate. 6

B) Define the 4 states of MESI protocol. Let a bus based shared memory (MM) multiprocessor system consists of three processors P1, P2 and P3. P1 is having a cache C1, P2 is having C2, and P3 is having cache C3. Each of the caches can accommodate *one* block at a time. The shared memory MM stores *two* blocks block1 & bblock2 and the variable *x* & *y* are in block1. The variable *z* is in block2. Initial values of the variables in MM are $x = 10$, $y = 20$, and $z = 40$. The system follows snoopy based MESI protocol, and write-invalidate scheme for cache coherence. Initially, the caches are empty and then the following events occur in sequence

(1) P2 reads *x*, (2) P1 reads *x*, (3) P1 updates $y = y+50$, (4) P3 reads *x*,
(5) P2 updates $x = x-20$, (6) P3 reads *y*, (7) P1 updates $y = 10$, (8) P2 reads *y*.

i) Show the values of *x*, *y* and *z* variables in MM after each event.
ii) Show the states of cached blocks in C1, C2 and C3 after each event.
iii) Denote the cases of false sharing misses.

Mention assumptions taken. 6

C) `False sharing miss normally occurs in a system realizing the large block size and write-invalidate scheme for cache coherence' – Explain. 3

D) Define the relationship between regular hit time and pseudo-hit time. 2