B-Tech 4th Semester

Mid-Term Examination

April 2021

Subject: Computer Architecture and Organization - I

[CS 2202]

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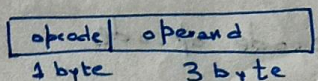
Q1) given single address 32-bit μ-processor

32 bit address bus.

32 bit data bus

Instruction: 

a) PC: 3 byte = 24 bit

DR: 32 bit

AR: 5 bit

IR: ~~1~~ 8 bit

b) 16-bit memory module.

max. no. of address space: $\frac{2^{32}}{2^{16}} = 2^{28}$

c) Assuming Fetch Cycle already done.

~~LOAD X~~

~~I) LOAD X~~

0: Activate CPU

1: Transfer PC content of AR

AR ← PC

2: Read Memory to DR

DR ← M(AR)

3) a) IR ← DR (opcode) [opcode = LOAD]

b) PC ← PC + 1

~~then~~ 4) decode opcode

LOAD

5) AR ← DR (address)

or

AR ← DR(x)

6) DR ← M(AR)

7) AC ← DR

8) Goto Step 1

STORE

5) AR ← DR (x)

6) DR ← AC

7) M(AR) ← DR

8) Goto Step 1

d) Assuming initial PC value 1

1) AR ← PC

AR: 1
PC: 1

2) DR ← M(AR)

DR = M(01)
= 01h AB000000h

3) a) IR ← DR (opcode)

IR = 01h

b) PC ← PC+1
PC = 2

4) decode 01h, found LOAD

5) AR ← DR (address)

AR = AB000000h

6) DR ← M(AR)

DR = M(AB000000h) [let it be α]
= α

7) AC ← DR

AC = α

8) ~~go again to step 1~~ go to Fetch Cycle.

9) AR ← PC

AR: 2

10) DR ← M(AR)

DR = M(02)

= 02h AB000001h

11) a) IR ← DR(opcode)

IR = 02h

b) PC ← PC+1

PC = 3

12) decode 02h, found STORE

13) AR ← DR(address)

∴ AR = AB000001h

14) DR ← AC

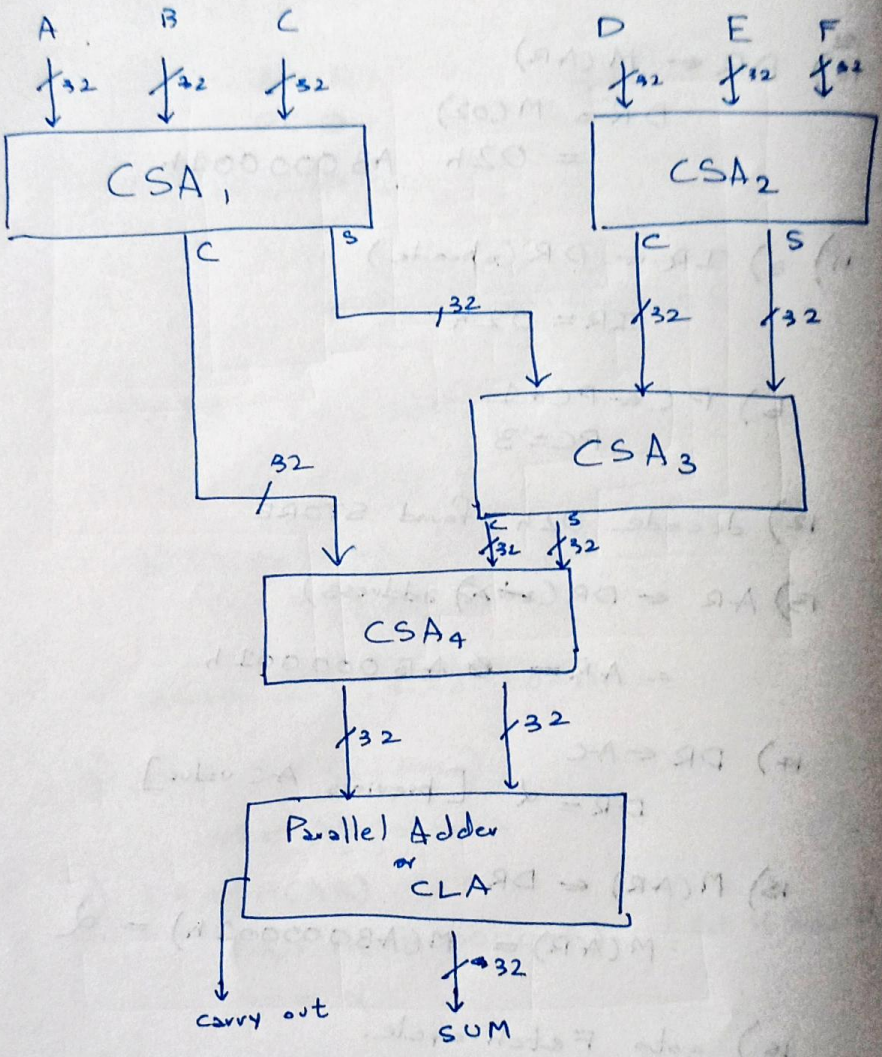
DR = α [previous AC value]

15) M(AR) ← DR

M(AR) = M(AB000001h) = α

16) goto Fetch cycle.

(Q2) a) let the six no. be A, B, C, D, E, F



b) given. $y = 0101 = M = 5$

$x = 1010 = Q = -6$ [n = 4]

Booth's Multiplication

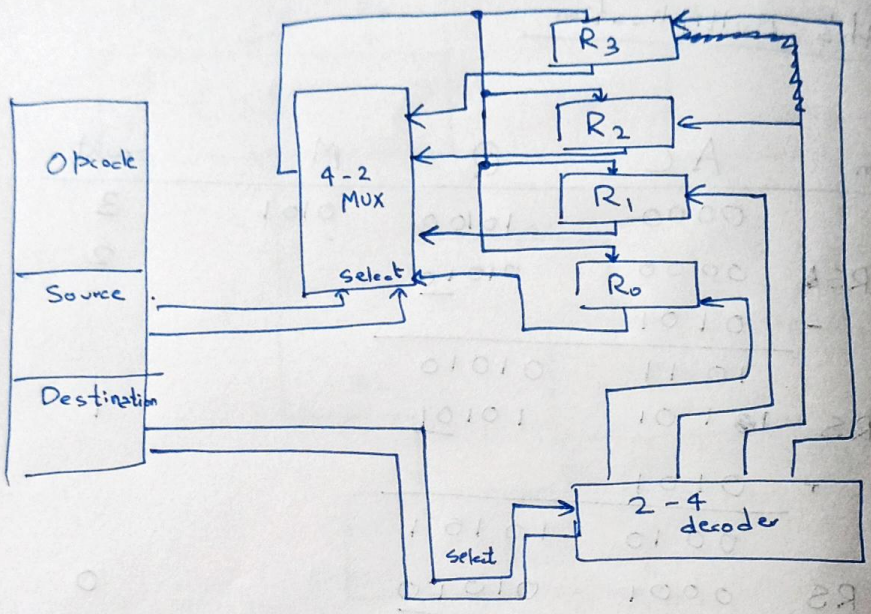
Action	AC	Q	M	count
	0000	10100	0101	3
RSA	0000	01010		2
−	0101			
	1011	01010		
RS	1101	10101		1
+	0101			
	0010	10101		
RS	0001	01010		0
−	0101			
	1100	01010		
RS	1110	00101		

Ans = 1110 0010 = −30

If y = 1010
x = 0101

No. of addition / subtraction required. = 4

3) a) given 4 Register R0, R1, R2, R3, data movement between them



b) Horizontal Format

$L_{\mu\text{-inst}} = 24$ bit

Control Field	Branch Addr Field	Condition select
13 bit	A	S

→ 8 status bits input to MUX for which S is mode

i) $\therefore S = 3$

$A = 24 - 13 - 3$

$= 8$

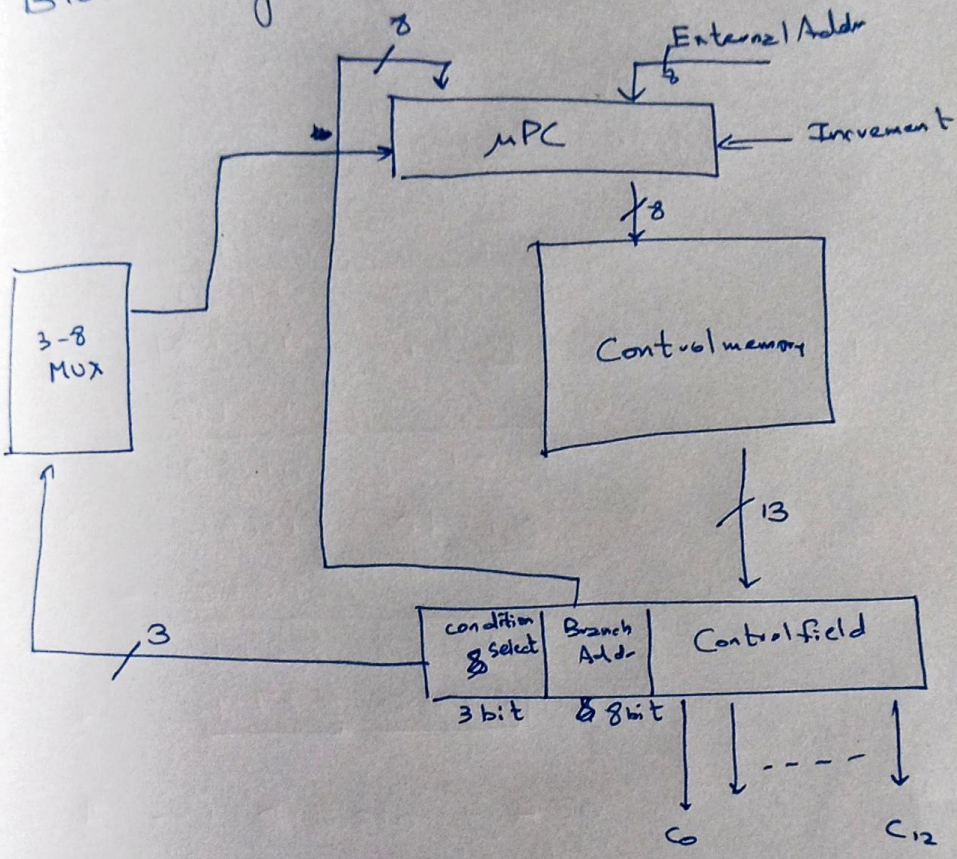
$\therefore A = 8$ bit

$S = 3$ bit

ii) no. of words in control memory = 2^8

no. of control signal = 13

iii) Block Diagram



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