Computer Architecture and Organization Laboratory

Department of Computer Science and Technology, IIEST

Experiment No: 1 (Organization of $(m \times d)$ memory with latches)

Objective: To design memory module with the features of Read/Write, using RS latch, considering
(a) m = 1, d = 1, (b) m = 2, d = 1
(c) m = 2, d = 2 - using the design resulted out of (b)

Utilize the following:

1. RS latch (For physical lab, 74279),
2. Tri-state logic (For physical lab, 74367)
3. Triple-input NAND (For physical lab, 7410),
4. Inverter (For physical lab, 7404)

Realize the logic circuits shown in Figure and verify the designs as per the following tables.

TABLE I
VERIFICATION FOR DESIGN (a)

Sl no	Select	R/$\overline{W}$	Data in [supply]	Data out [verify]	Activity
1	1	0	1	-	Write 1 in Loc-1
2	1	1	-	1	Read 1 from Loc-1
3	0	x	-	-	No operation
4	1	0	0	-	write 0 in Loc-1
5	1	1	-	0	Read 0 from Loc-1

TABLE II
VERIFICATION FOR DESIGN (b)

No	Select	R/$\overline{W}$	D_{in}	D_{out}	Verify
1	1	0	1 (d_1)	-	Write 1 in Loc-1
2	0	0	1 (d_2)	-	Write 1 in Loc-0
3	1	1	-	1 (d_1)	Read 1 from Loc-1
4	0	1	-	1 (d_2)	Read 1 from Loc-0
5	1	0	0	-	Write 0 in Loc-1
6	0	0	1	-	Write 1 in Loc-0
7	1	1	-	0	Read 0 from Loc-1
8	0	1	-	1	Read 1 from Loc-0
9	1	0	1	-	Write 1 in Loc-1
10	0	0	0	-	Write 0 in Loc-0
11	1	1	-	1	Read 1 from in Loc-1
12	0	1	-	0	Read 0 from Loc-0

TABLE III
VERIFICATION FOR DESIGN (c)

No	Select	R/$\overline{W}$	D1$_{in}$	D0$_{in}$	D1$_{out}$	D0$_{out}$	Verify
1	1	0	1	0	-	-	Write 10 in Loc-1
2	0	0	0	1	-	-	Write 01 in Loc-0
3	1	1	-	-	1	0	Read 10 from Loc-1
4	0	1	-	-	0	1	Read 01 from Loc-0
5	1	0	0	0	-	-	Write 00 in Loc-1
6	0	0	1	1	-	-	Write 11 in Loc-0
7	1	1	-	-	0	0	Read 00 from Loc-1
8	0	1	-	-	1	1	Read 11 from Loc-0

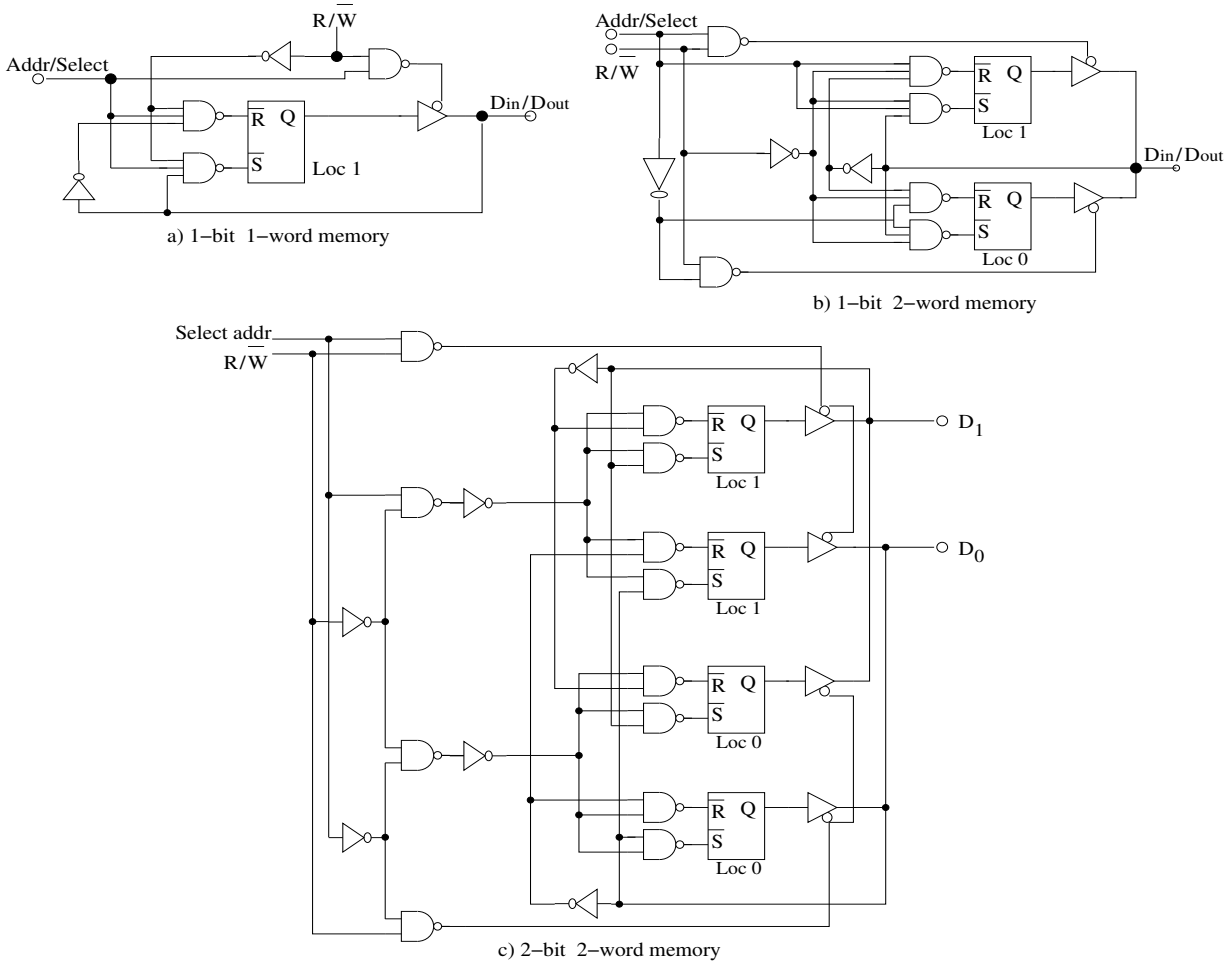

Fig. 1. Circuit diagram