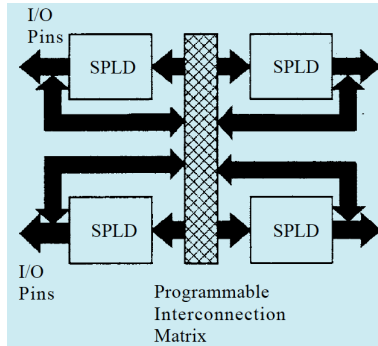

Complex Programmable Logic Devices (CPLDs)

Complex Programmable Logic Devices (CPLDs)

- Another way to extend the density of SPLDs
- A number of SPLD blocks sharing a common programmable interconnection matrix or switch
- Contains a bunch of I/O pins whose I/O are connected together by the interconnection matrix
- Methods to make the connections between logic blocks:
 - Fuses or anti-fuses: one-time programmable (OTP) CPLDs
 - Pass transistors: EPROM or EEPROM based CPLDs (user can erase it and then place it in a special programmer socket and reprogram it)
 - Static RAM or Flash bits: In-circuit reconfigurable or in-circuit programmable CPLDs
- Xilinx offers CPLD products in two categories: XC9500TM and CoolRunnerTM devices

Complex Programmable Logic Devices (CPLDs)

A generic CPLD architecture



Complex Programmable Logic Devices (CPLDs)

CPLD Manufacturers



Lucent Technologies
Bell Labs Innovations



CPLD Product Portfolio

Xilinx's CPLD Product Portfolio



- **1.8V RealDigital core**
- 1.5V - 3.3V I/O
- SSTL, HSTL, LVC MOS, LVTTTL
- Lower power
 - DataGATE
- Clocking features
 - Clock Divide
 - CoolCLOCK
 - DualEDGE
- I/O banking



- **2.5V core**
- 1.8V - 3.3V I/O
- LVC MOS, LVTTTL
- I/O banking

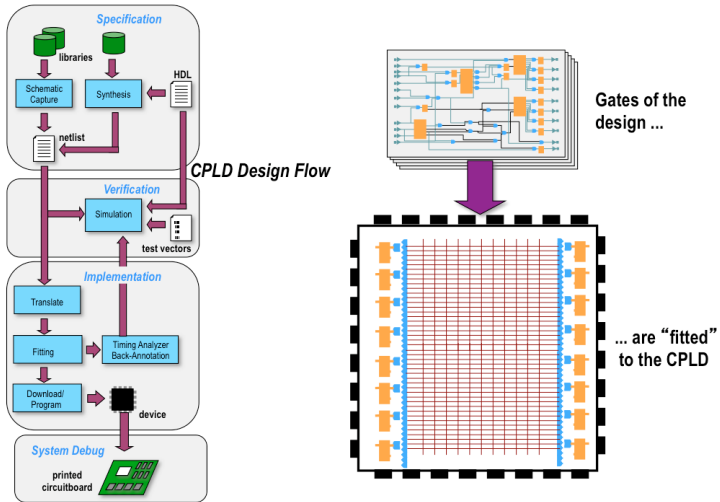


- **3.3V core**
- 2.7V - 5V I/O
- LVC MOS, LVTTTL
- Low power
 - Fast Zero Power

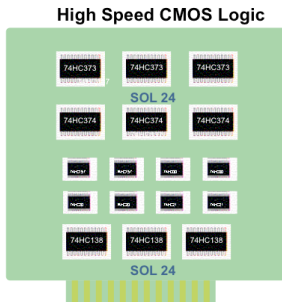


- **3.3V core**
- 2.5V - 5.0V I/O
- LVC MOS, LVTTTL

CPLD Design Flow

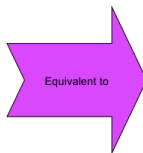


CPLD Advantage over Discrete Logic



Discrete Part No.	Function	Qty
74HC373	Octal D-type transparent latch	3
74HC374	Octal D-Type Flip Flop	3
74HC157	Quad 2-input multiplexer	2
74HC00	Quad 2 input NAND	2
74HC21	Dual 4 input AND	2
74HC20	Dual 4 input NAND	2
74HC138	3 to 8 line decoder	3

XPLA™ Architecture



TQFP 100



XCR3128XL

Or XCR3064 XL

3.3V parts in the same package
bridging two densities for added
design flexibility

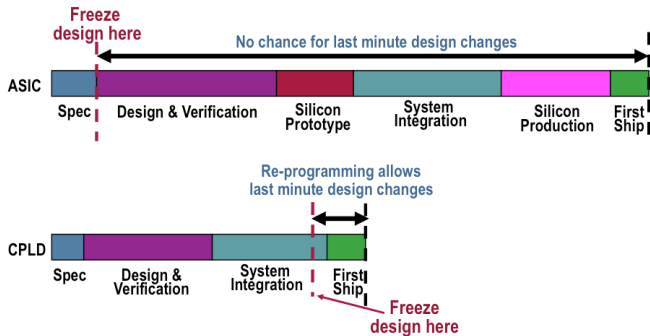
Real design example: Aircraft Passenger Handset

- Smaller PCB with less layers (lower cost) - 7 to 3 layers!
- One part to purchase & stock, less inventory
- One part to pick and place in manufacture, saving time
- Design can be changed and enhanced without PCB re-layout - even in the field
- Stock and purchase one part instead of 17 in this example!

ASIC Development Take Too Long!

- ASIC: Application Specific Integrated Circuit
- Product life cycles maybe shorter than ASIC development time
 - Multiple ASIC spins may miss the market window
 - Smaller than expected run rates may not justify the ASIC development cost
- Long ASIC development times do not allow last minute design revision changes
 - Revisions leave little time to run in production
 - Programmable logic allow customers to address market changes quicker

ASICs Give Designers Only ONE Chance



- CPLD flexibility allow performance analysis and late HW/SW changes meeting customer needs and improves **Time To Market with faster, lower risk designs**

Source: Xilinx

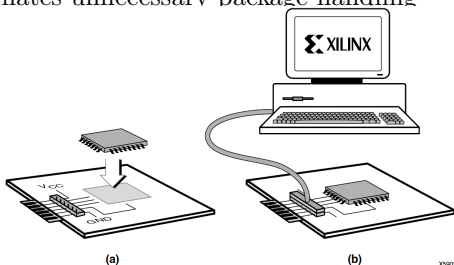
CPLD: XC9500 Family

- High-performance: 5 *ns* pin-to-pin logic delays on all pins
- Large density range
 - 36 to 288 macrocells with 800 to 6,400 usable gates
- 5V In-System Programmable
 - Endurance of 10,000 program/erase cycles
 - Programerase over full commercial voltage and temperature range
- Flexible 36V18 Function Block
 - 90 product terms drive any or all of 18 macrocells within Function Block
 - Global and product term clocks, output enables, set and reset signals
 - Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
 - 3.3V or 5V I/O capability
 - Advanced CMOS 5V FastFLASHTM technology
 - Supports parallel programming of multiple XC9500 devices

CPLD: XC9500 Family

■ Benefits of ISP:

- No need for costly device programmers
- Less scrap and re-work
- Reduces design and development time scales
- Enables field upgrades
- Eliminates unnecessary package handling



In-System Programming Operation (a) Solder Device to PCB and (b) Program Using Download Cable

Source: Xilinx

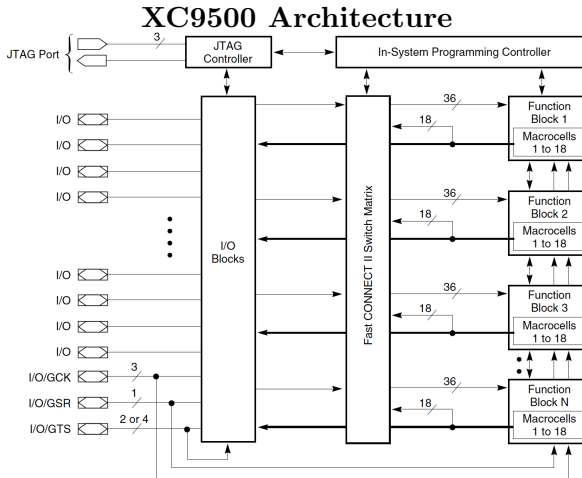
CPLD: XC9500 Family

■ Benefits of JTAG:

- Improved testability
- Higher system reliability
- Cheaper test equipment
- Shorter test time
- Reduced spare board inventories
- Reduces device handling

Source: Xilinx

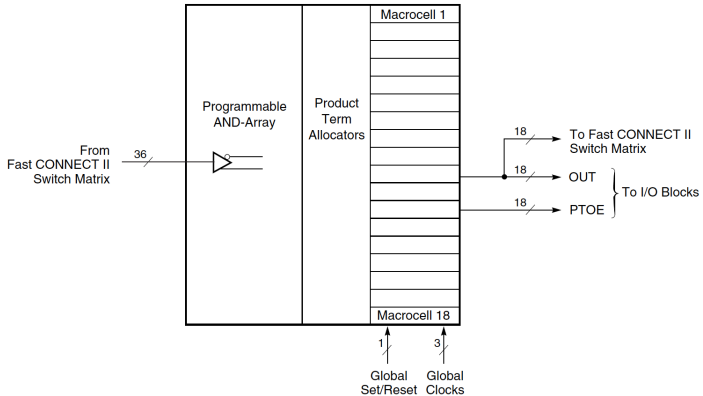
CPLD: XC9500 Family



Note: Function block outputs (indicated by the bold lines) drive the I/O blocks directly.

CPLD: XC9500 Family

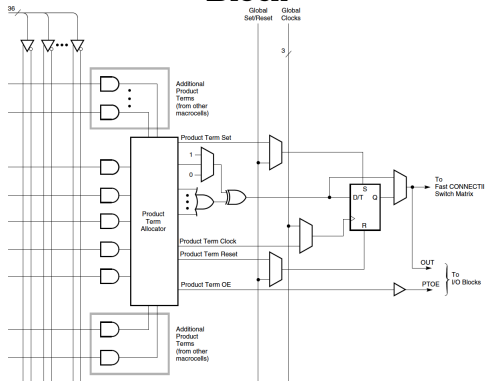
XC9500 Architecture: Function Block



Source: Xilinx

CPLD: XC9500 Family

XC9500 Architecture: Macrocell Within Function Block



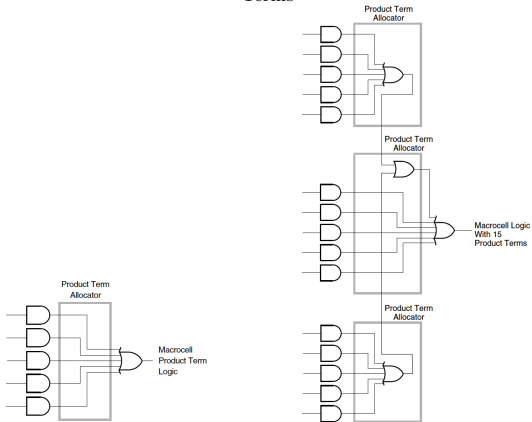
Source: Xilinx

CPLD: XC9500 Family

XC9500 Architecture: Macrocell Within Function Block

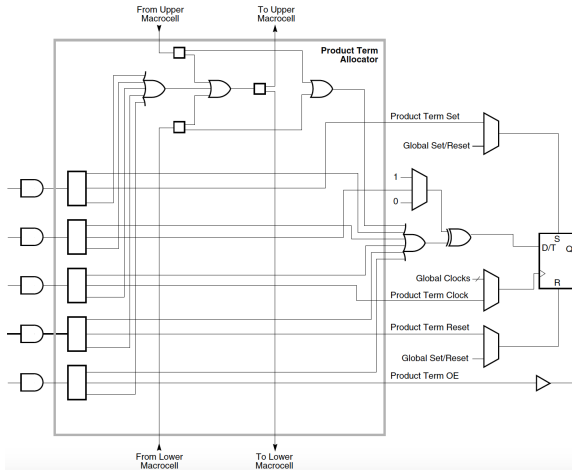
Macrocell Logic Using Direct Product Term

Product Term Allocation With 15 Product Terms



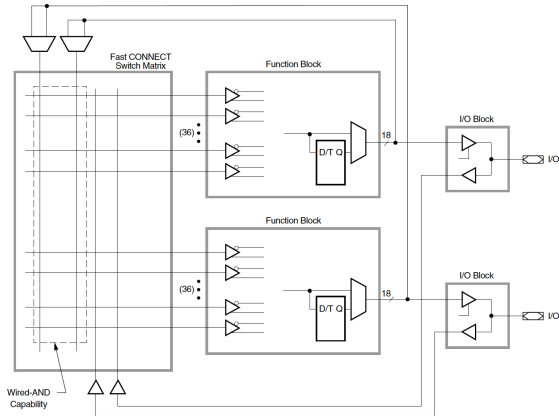
CPLD: XC9500 Family

XC9500 Architecture: Product Term Allocator Logic



CPLD: XC9500 Family

XC9500 Architecture: Fast CONNECT Switch Matrix



Source: Xilinx

CPLD: XC9500 Family

- Motherboards for PCs and servers
- PC peripherals and add-on cards
 - DVD players/controller cards
 - Graphics cards
- Automotive
 - Engine control
 - Automotive navigation systems (GPS)
- Consumer
 - LAN / DSLAM
 - Video Games/Toys

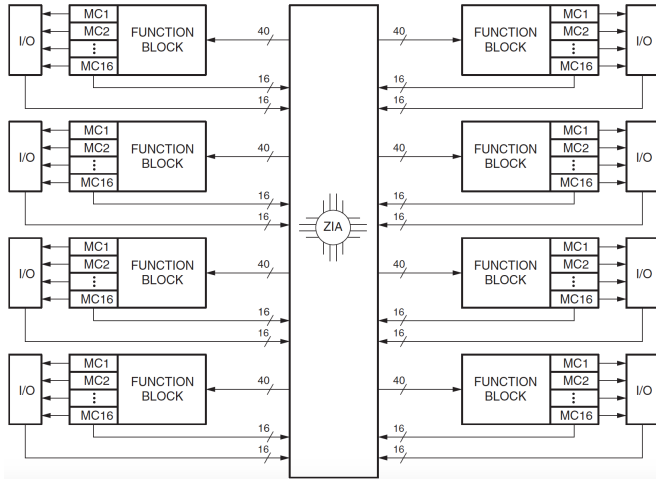
Source: Xilinx

CPLD: CoolRunner XPLA3 Family

- Fast Zero Power (FZP) design technique provides ultra-low power and very high speed
- Combines high speed with extreme flexibility
- 3V, In-System Programmable (ISP) using JTAG IEEE 1149.1 interface
 - Full Boundary-Scan Test (IEEE 1149.1)
 - Fast programming times
- Support for complex asynchronous clocking
 - 16 product term clocks and four local control term clocks per function block
 - Four global clocks and one universal control term clock per device
- Foldback NAND for synthesis optimization
- Innovative Control Term structure provides:
 - Asynchronous macrocell clocking
 - Asynchronous macrocell register preset/reset
 - Clock enable control per macrocell
 - Four output enable controls per function block

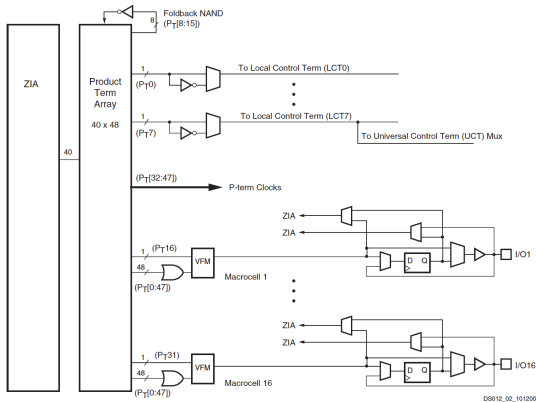
CPLD: CoolRunner XPLA3 Family

CoolRunner XPLA3 Architecture



CPLD: CoolRunner XPLA3 Family

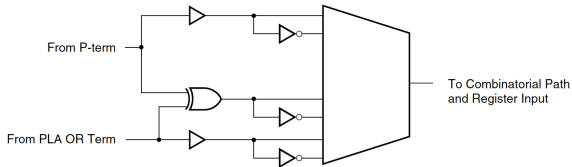
CoolRunner XPLA3 Architecture: Function Block



Source: Xilinx

CPLD: CoolRunner XPLA3 Family

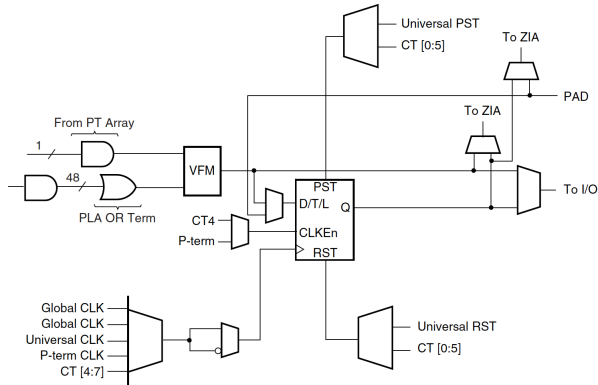
CoolRunner XPLA3 Architecture: Variable Function Multiplexer



Source: Xilinx

CPLD: CoolRunner XPLA3 Family

CoolRunner XPLA3 Architecture: Macrocell Architecture



Source: Xilinx

CPLD: CoolRunner II

Features of Xilinx's CoolRunner-II CPLD Family

- Industry's fastest low power CPLD
- Densities from 32 to 512 macrocells
- Optimized architecture for effective logic synthesis
- Multi-voltage I/O operation - 1.5V to 3.3V
- Fastest in system programming: 1.8V ISP using IEEE 1532 (JTAG) interface
- On-The-Fly Reconfiguration (OTF)
- Multiple I/O banks on all devices
- Flexible clocking modes
 - Optional DualEDGE triggered registers
 - Clock divider (\div 2,4,6,8,10,12,14,16)
- Global signal options with macrocell control
 - Multiple global output enables and Global set/reset
- Mixed I/O voltages compatible with 1.5V, 1.8V, 2.5V, and 3.3V logic levels on all parts

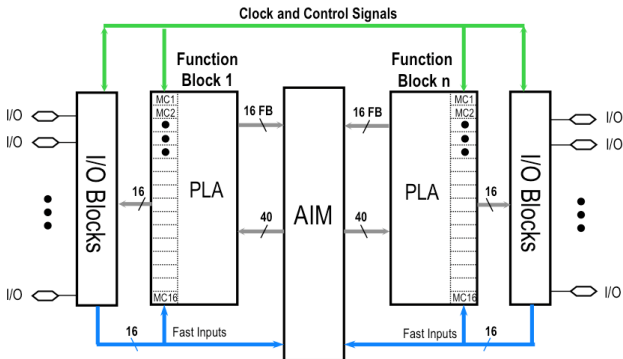
CPLD: CoolRunner II

Features of Xilinx's CoolRunner-II CPLD Family

- PLA architecture
 - Superior pinout retention
 - 100% product term routability across function block
- Wide package availability including fine pitch:
 - Chip Scale Package (CSP) BGA, Fine Line BGA, TQFP, PQFP, VQFP, and QFN packages
 - Pb-free available for all packages
- Design entry/verification using Xilinx and industry standard CAE tools
- Free software support for all densities using Xilinx WebPACK tool
- Industry leading nonvolatile 0.18 micron CMOS process
 - Guaranteed 1,000 program/erase cycles
 - Guaranteed 20 year data retention

CPLD: CoolRunner II

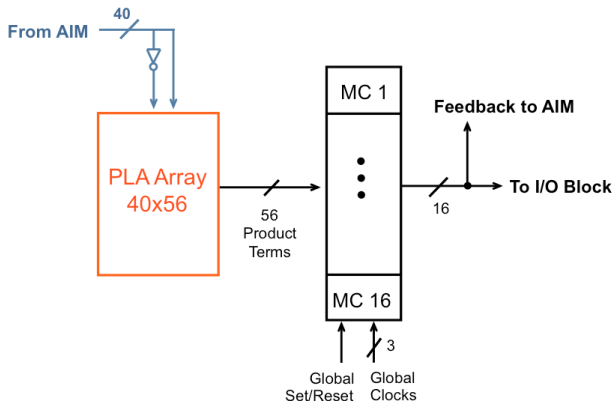
High Level Architecture



Source: Xilinx

CPLD: CoolRunner II

Functional Block Architecture



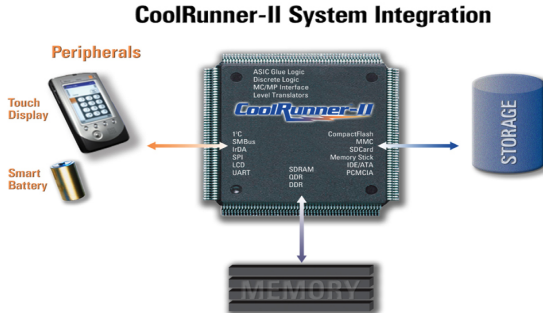
Source: Xilinx

Micro Cell Architecture



CPLD: CoolRunner II

System Integration Advantage



Source: Xilinx

CPLD: CoolRunner II

System Level Savings

- High volume economies of scale
 - Single chip for multiple system solutions
 - ▶ Increase volume means reduction in all related costs
- Reference designs
 - Minimize risk and shorten design cycle
- Lowest cost per I/O
- On The Fly (OTF) reconfiguration
 - Two devices for the price of one

Source: Xilinx

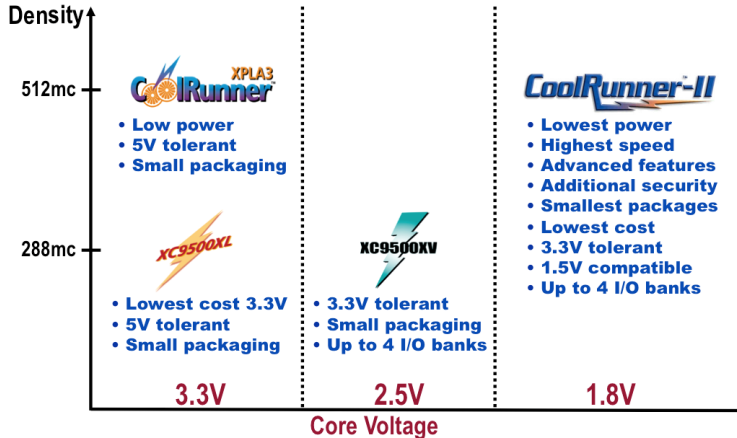
CPLD: CoolRunner II

CoolRunner Reference Designs

- Shorten design cycle time
 - Eliminate code porting costs for next design cycle
 - ▶ Re-use of HDL is reliable and stable
- Minimize design risk by using reference designs
 - Availability of reference designs prepares you for unexpected system changes
 - ▶ Update main processor but it does not incorporate correct bus interface
- Further improve customer's **Time To Market**
 - Proven designs for quick turn requirements

Source: Xilinx

Industrial and Automotive CPLDs



Source: Xilinx

Xilinx CPLD Summary

■ XC9500/XL/XV fast, higher voltage, low-cost

- For mainstream 5v, 3.3v & 2.5v designs
- Great architectural features (ISP, JTAG, pin-locking)



■ CoolRunner XPLA3 low power

- Pioneering low power 3.3v product with 5v tolerant I/O
- Lowest power 3.3v CPLD - 3x better than nearest 3.3v competitor



■ CoolRunner-II High Performance and Low Power

- Higher Performance & High Speed (385MHz) at 1.8V
- Enhanced clocking & I/O feature set
- Lowest power consumption
- Higher system reliability & system security



Source: Xilinx