Indian Institute of Engineering Science and Technology, Shibpur

BTech (CST) 5th Semester Mid Semester Examination, October 2021

Computer Architecture and Organization II (CS-3103)

Full Marks: 30 Time: 45 Minutes

Answer all questions

1A) Compare the schemes direct mapped, 2-way set associative, and fully associative in terms of number of misses when the Block access sequence is 0, 8, 0, 6, 8. The system is having 4-frames in its cache. 5

B) `False sharing miss normally occurs in a system realizing the large block size and write-invalidate scheme for cache coherence' – Explain. 4

C) Let a bus based shared memory (MM) multiprocessor system consists of three processors P1, P2 and P3 with caches C1, C2, and C3 respectively. Each of the caches can accommodate *one* block at a time. The MM stores *two* blocks B1 and B2. The variables *x and y* are in B1. The variable *z* is in B2. Initially in MM $x = 100$, $y = 200$, and $z = 400$. The system follows snoopy based MESI protocol, and write-invalidate scheme for cache coherence. Initially, C1, C2, and C3 are empty. Now, following events occur in sequence

(1) P1 reads *x*, (2) P2 reads *x*, (3) P2 updates $y = y+500$, (4) P3 reads *x*,
(5) P1 updates $x = x-200$, (6) P3 reads *y*, (7) P2 updates $y = 100$, (8) P1 reads *y*.

i) Show the values of *x, y* and *z* in MM after each event.
ii) Show the states of cached blocks in C1, C2 and C3 after each event.

Mention assumptions taken if any. 6

2A) Let consider execution of the following code segment in a 5-stage (IF, ID/OF, EX, MEM, and WB) instruction pipeline. 6

R1 ← M(R2)
R3 ← R1 * R4
R4 ← R1 v R5
R6 ← R1 . R7

a) Clearly indicate the data dependencies and their type in the code segment.
b) If data forwarding is not implemented in this pipelined processor, then indicate possible data hazards and show stalls introduced to eliminate those hazards.
c) Show stalls introduced to eliminate those hazards when data forwarding is implemented.

B) A program consists of two nested loops, with only single branch instruction at the end of each loop. The outer loop is executed 10 times and the inner loop 20 times. Determine the accuracy of following branch prediction strategies: 4

a) Always predict taken,
b) Use 1-bit of history (history for each loop is initialized to "taken").

C) Consider the following code fragment 5

```
I1: Load R1, X          //R1 = M(X)
I2: Decrement R2, 1
I3: BrZero R2, I5       //Jump to I5 if R2==0
I4: Add R3, R4          //R3 = R3 + R4
I5: Sub R5, R6          //R5 = R5 - R6
```

Modify the original program by moving an instruction into branch delay slot considering
a) The instruction that is appeared before branch instruction,
b) The instruction that is at the target address of the branch,

Evaluate options (a) and (b) considering the “predict taken” scheme.