28-4-16

INDIAN INSTITUTE OF ENGINEERING SCIENCE AND TECHNOLOGY, SHIBPUR

B.E. 4th SEMESTER (CS) FINAL EXAMINATION, 2016

Computer Architecture and Organization – I (CS402)

FULL MARKS: 70 TIME: 3 Hrs

(Answer any five)

1. (a) Show the multiplication of (-7x3) and (-7x-3) using booth's algorithm.
   (b) Show the division of (-7÷-3) using division algorithm
   (c) What is the advantage of using carry save adder in multiplier circuit? [4+4+4+2]
2. (a) A two level memory consisting of cache memory and main memory. The cache memory is 5 times faster than main memory, hit ratio is 80%. If average access time is increased by 20% from 50 ns, what is the approximate change in hit ratio?
   (b) Consider a 2-way set associative cache memory with 4 sets and total of 8 cache blocks (0-7). What memory blocks will be present in the cache memory after the following sequence of memory block reference if least recently used policy is used for cache block replacement?

   0, 5, 3, 9, 7, 0, 16, 55

   (c) What are the advantages of using virtual memory? What is CAM? What is DRO? [4+4+6]
3. (a) A CPU has only 4 instructions I1, I2, I3, I4. The following signals are used in time steps T1 – T5 by these four instructions.

	T1	T2	T3	T4	T5
I1	S1, S3, S5	S2, S4, S6	S1, S7	S10	S3, S8
I2	S1, S3, S5	S8, S9, S10	S5, S6, S7	S6	S10
I3	S1, S3, S5	S7, S8, S10	S2, S6, S9	S10	S1, S3
I4	S1, S3, S5	S2, S6, S7	S5, S10	S6, S9	S10

   Write down the logic functions to generate hardwired control for the signal S5 and S10.
   (b) An instruction set of a processor has 125 signals which can be divided into 5 groups of mutually exclusive signals as follows:
   Group1: 20 signals, Group2: 70 signals, Group3: 2 signals, Group4: 10 signals, Group5: 23 signals. How many bits of the control word can be saved by using vertical microprogramming over horizontal microprogramming?
   (c) Why control memory optimization is required for microprogrammed control unit? Determine the minimum width of the control memory word for the following set of microinstructions and set of control signals activated by them. [4+4+6]

Microinstruction	Control signals
I1	a, b, c, g
I2	a, c, e, h
I3	a, d, f
I4	b, c, f

4. (a) Compare the performance of daisy-chaining, polling and independent requesting with respect to communication reliability in the event of hardware failure.
   (b) Explain the followings: (i) Programmed IO (ii) Interrupt driven IO (iii) IO mapped IO
   (c) A magnetic disk has 1024 number of tracks, 512 number of sectors per track, 512 bytes per sector, 7200 rpm disk rotational speed and 9 msec seek time. Find data transfer rate and average access time of the disk. [3+6+5]

5. (a) Compare the performance of base scalar processor, superscalar processor and superpipelined processor in the context of speedup.
(b) A pipeline has 4 stages with time delays 60 ns, 50 ns, 90 ns and 80 ns. The interface latch has a delay of 10 ns. Find clock frequency of the pipeline.
(c) How nonlinear pipeline differs from linear pipeline? Define the following terms in the context of nonlinear pipeline: (i) Forbidden latency (ii) Latency sequence (iii) Latency cycle (iv) Constant latency
(d) How speedup, efficiency and throughput of a pipeline are related with each other?
(e) What is the maximum speedup factor of a n stage pipeline?
(f) A pipeline has 2 stages, one stage is for multiplication and the other stage is for addition. Each stage takes 10 ns. How much time is required to complete the following code segment?
for i = 1 to 100 do A[i]=B[i]*C[i]+D[i] [3+1+2+4+1+1+2]

6. (a) Define addressing mode.
(b) The word 20 of main memory contains 40, word 30 of main memory contains 50, word 40 of main memory contains 60 and word 50 of main memory contains 70. What values do the following instructions load into the accumulator?
(i) LOAD IMMEDIATE 20 (ii) LOAD DIRECT 30 (iii) LOAD INDIRECT 30
(c) A set of 5 instructions along with their probability of occurrence is given in TABLE below.

Instruction	Probability of occurrence
I1	0.5
I2	0.3
I3	0.08
I4	0.06
I5	0.06

Describe the Huffman's method to minimize the average opcode length for the given set of instructions.
(d) Consider the followings:
- PC contains address X1
- Instruction stored in X1 has an address part as operand address = X2
- Operand needed to execute the instruction is stored in the memory word with address X3
- An index register contains the value X4

What is the relationship between X1, X2, X3, X4 if the addressing mode of the instruction is direct, indirect, indexed and relative (PC based)? [1+3+4+6]

7. (a) Describe the followings:
(i) RISC and CISC
(ii) Fetch cycle and execution cycle
(iii) Zero address machine and one address machine
(iv) Handshaking, master unit, slave unit, wait state, tristate in the context of bus design
(v) Synchronous and asynchronous modes of data transfer [2+2+2+5+3]