Computer Architecture and Organization Laboratory

Department of Computer Science and Technology, IIEST

Experiment No: 6 (Design of sequence counter for processor control unit)

Objective: To build a mod-8 sequence counter for generation of control signals of a processor ALU.

The design

The instruction cycle of a CPU is shown in Figure 1. Assuming that each step is performed in an appropriately chosen clock period. A control unit CU for this CPU can be build around a modulo-8 sequence counter.

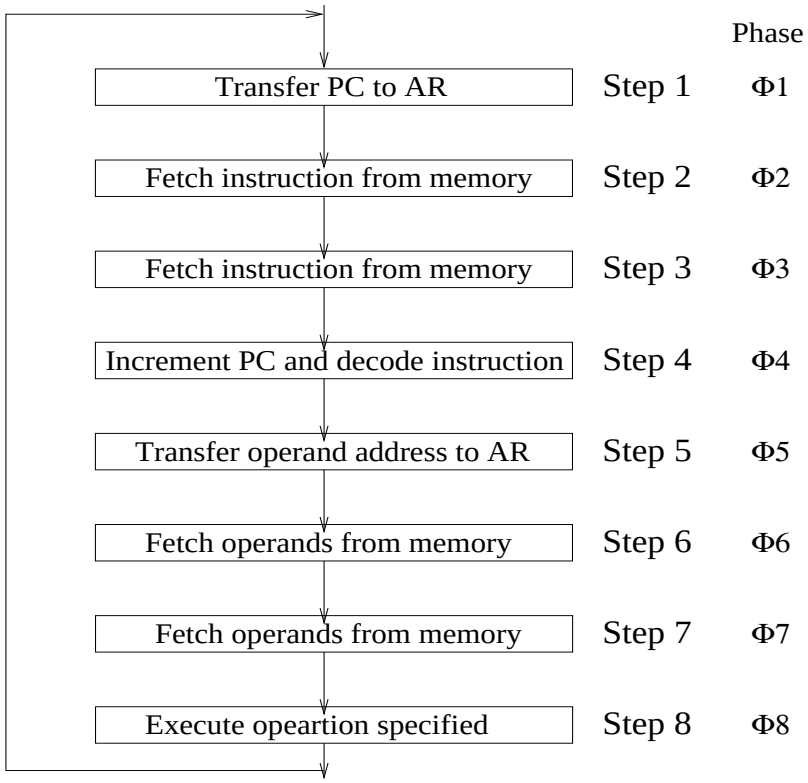

Fig. 1. Instruction cycle

A modulo-8 counter counts input clock pulses from 000 to 111 and then sets to 000. The modulo-8 sequence counter can be designed with a modulo-8 counter and an 1 of 8 decoder as shown in Figure 2.

Task

1. Design Modulo-8 sequence counter
2. Design a combinational logic that takes the phase signals $(\phi_1, \phi_2, \phi_3, \phi_4, \phi_5, \phi_6, \phi_7, \phi_8)$ as the input and generates a sequence of signals to control the primitive operations of the ALU.

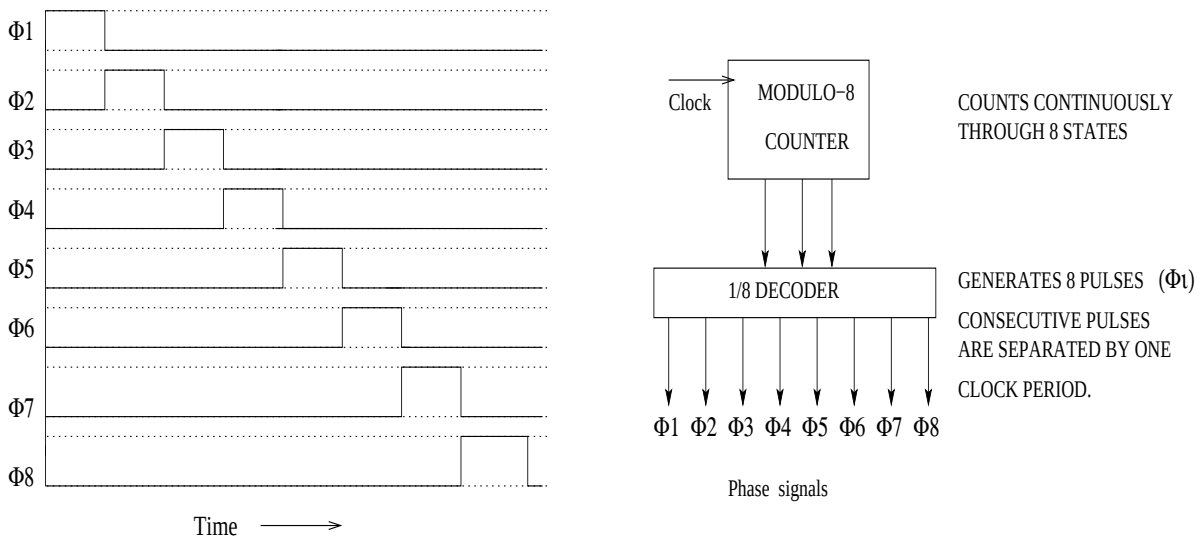

Fig. 2. Modulo-8 sequence counter