Digital Logic

Practical

Lab Report

Latches and Flip Flops

Student:

Abhiroop Mukherjee

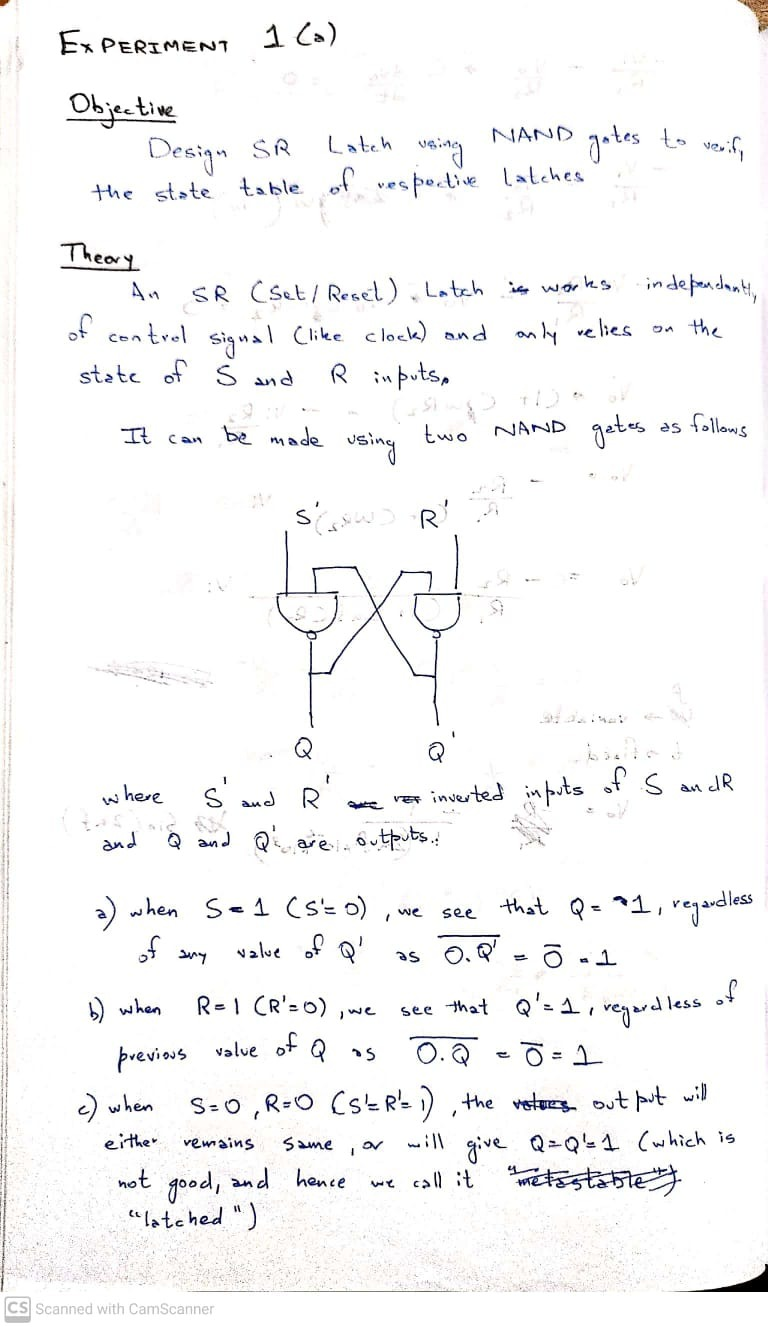
Teacher:

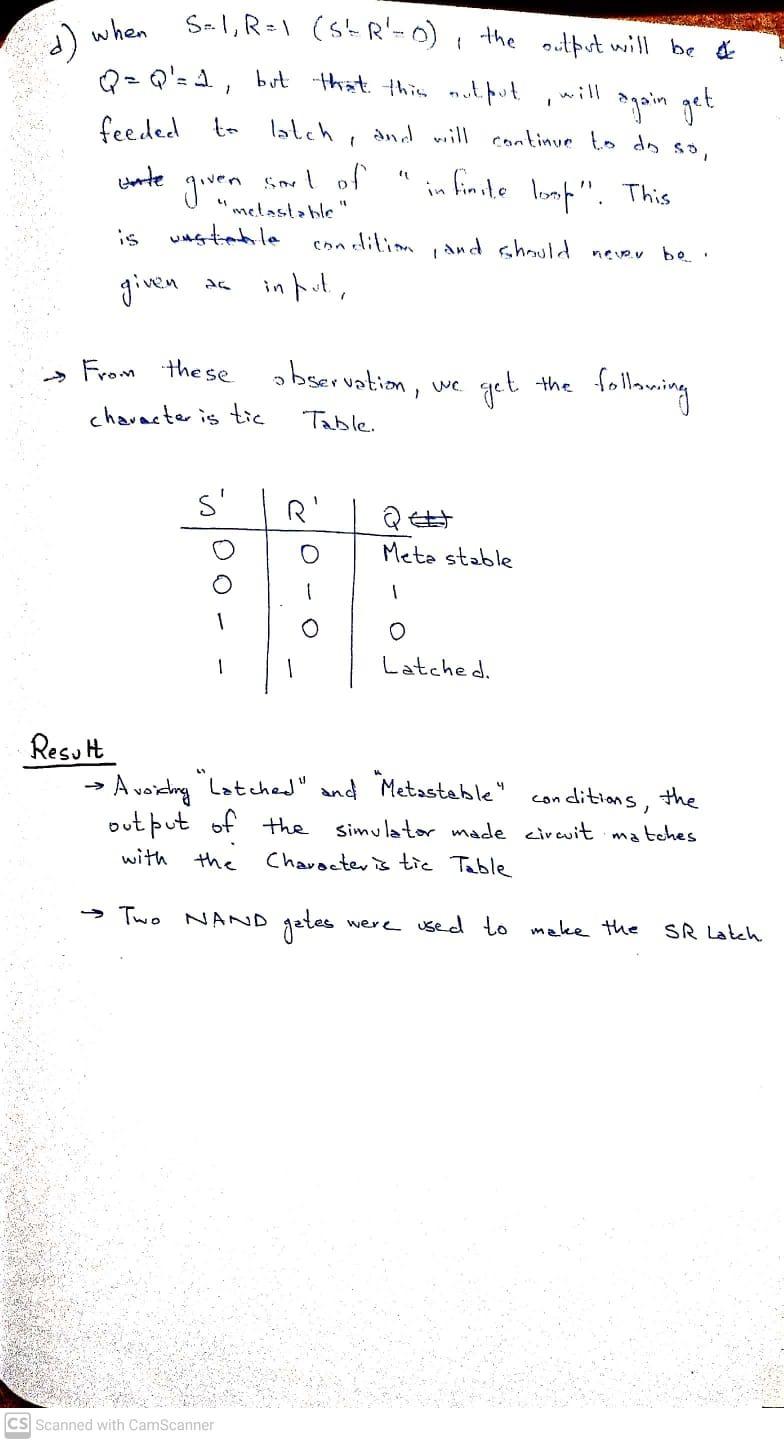
Prof. Surajeet Ghosh

Prof. Sekhar Mandal

Course:

Digital Logic Laboratory (CS351)





## Inputs / Outputs:

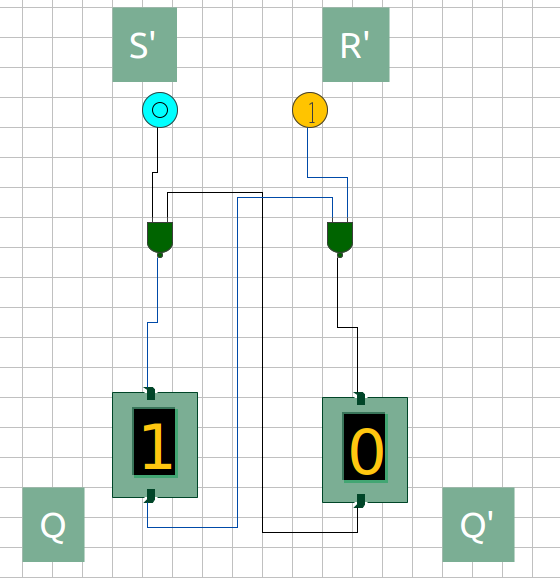
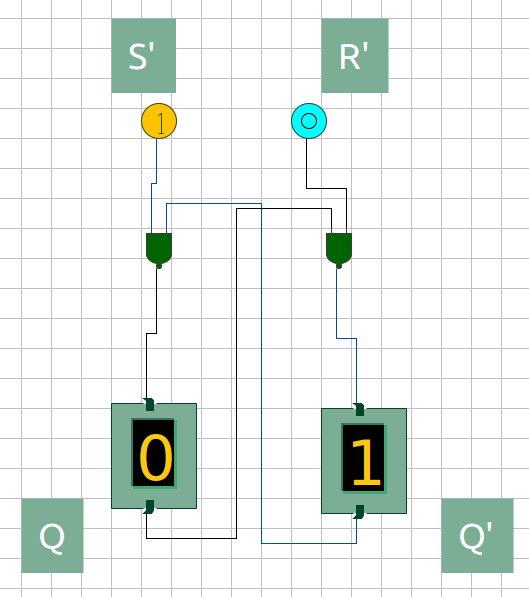
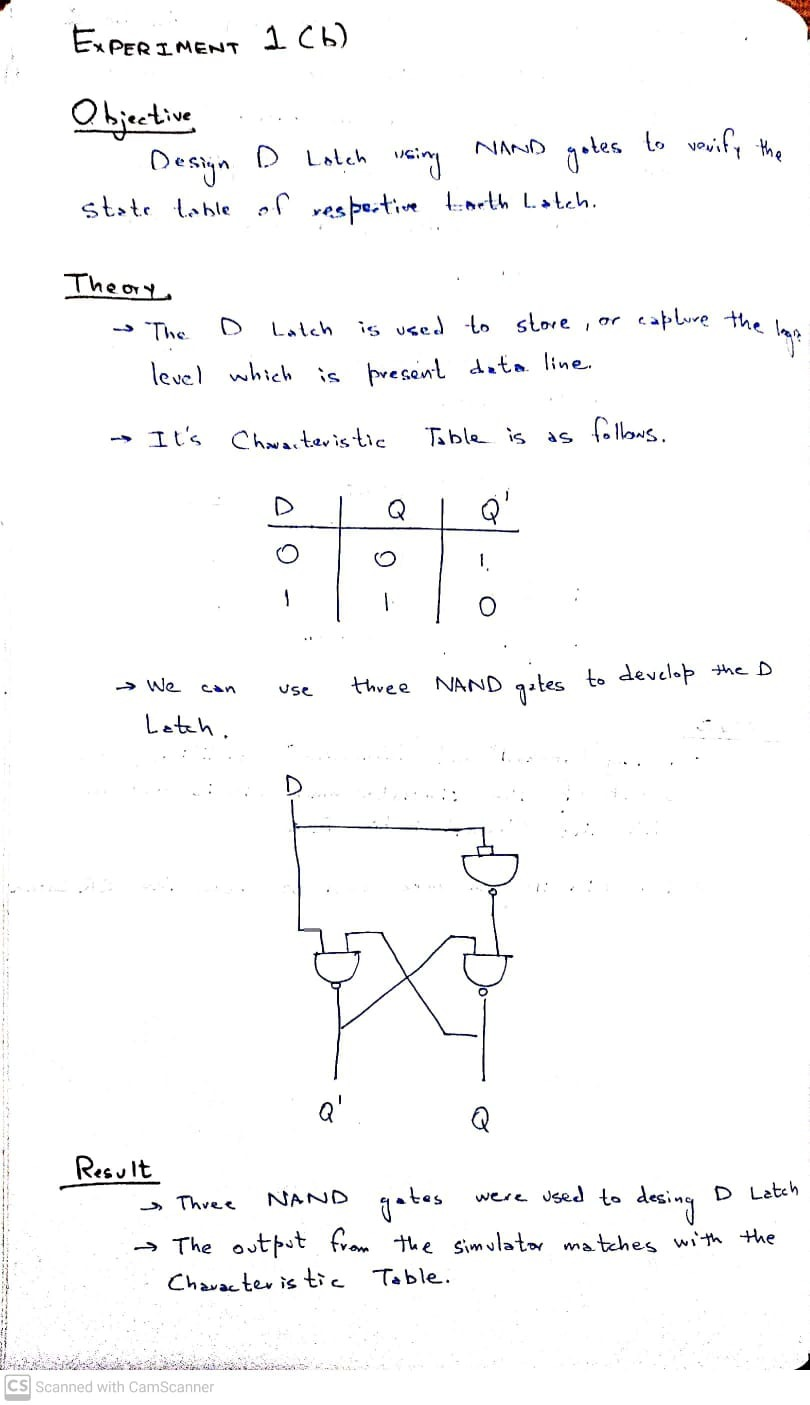
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Figure 1: S’ = 0, R’ = 1; Q = 1, Q’ = 0

Figure 2: S’ = 1, R’ = 0; Q = 0, Q’ = 1



## Inputs / Outputs:

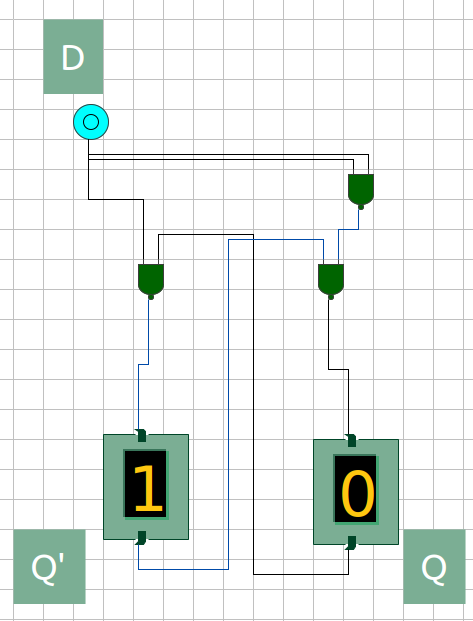
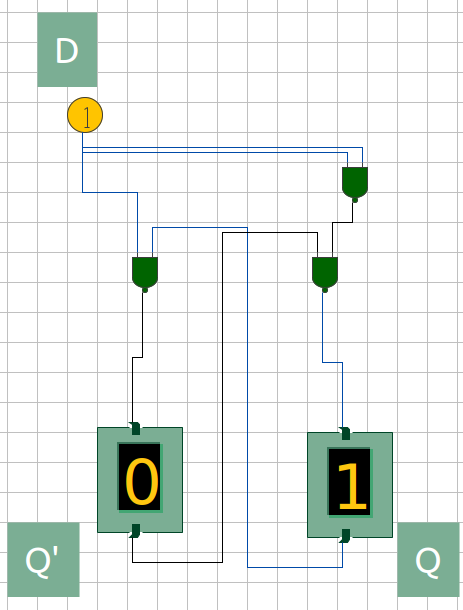
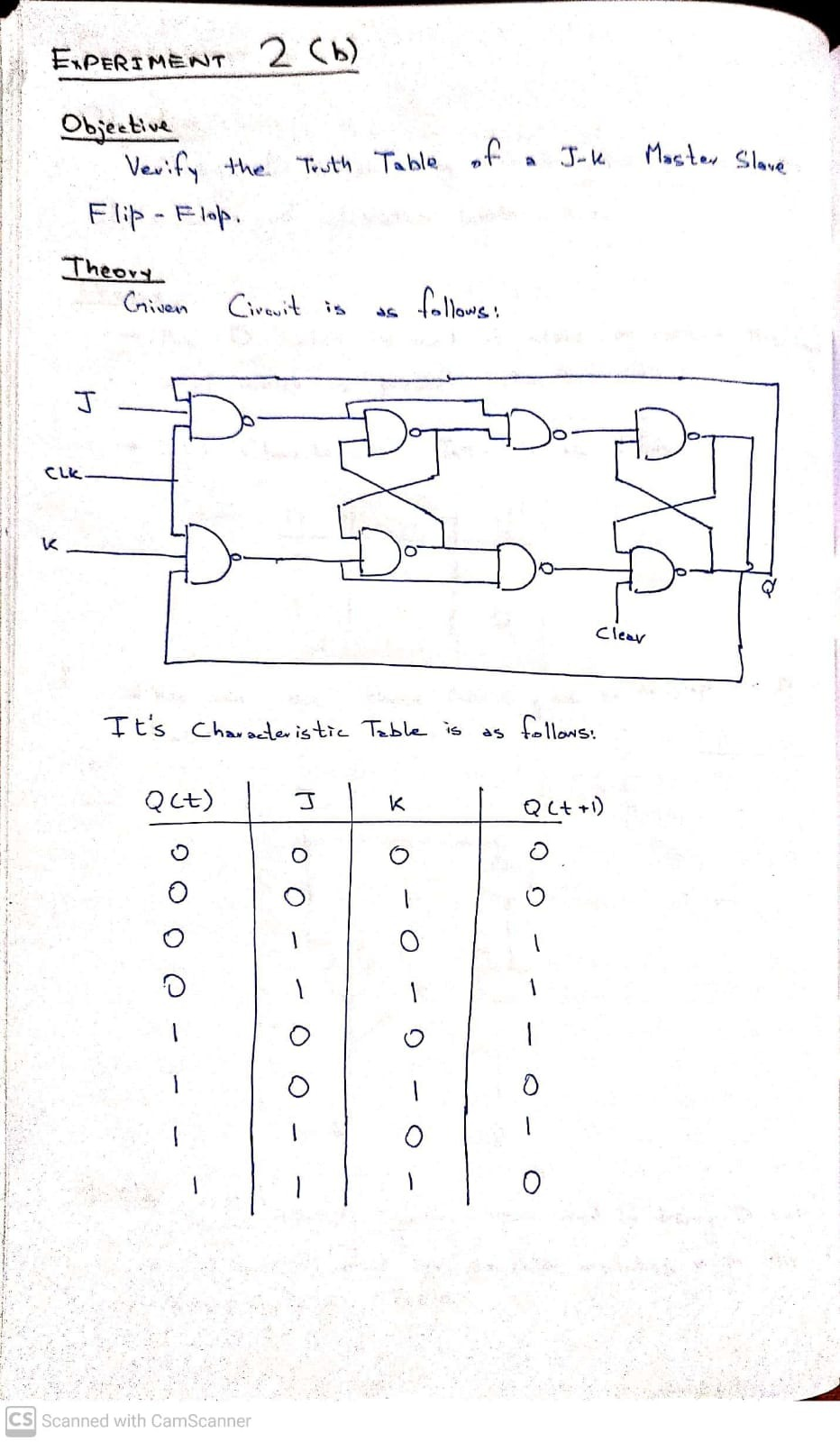
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Figure 1: D = 0; Q = 1, Q’ = 0

Figure 2: D = 1; Q = 0, Q’ = 1





## Inputs / Outputs:

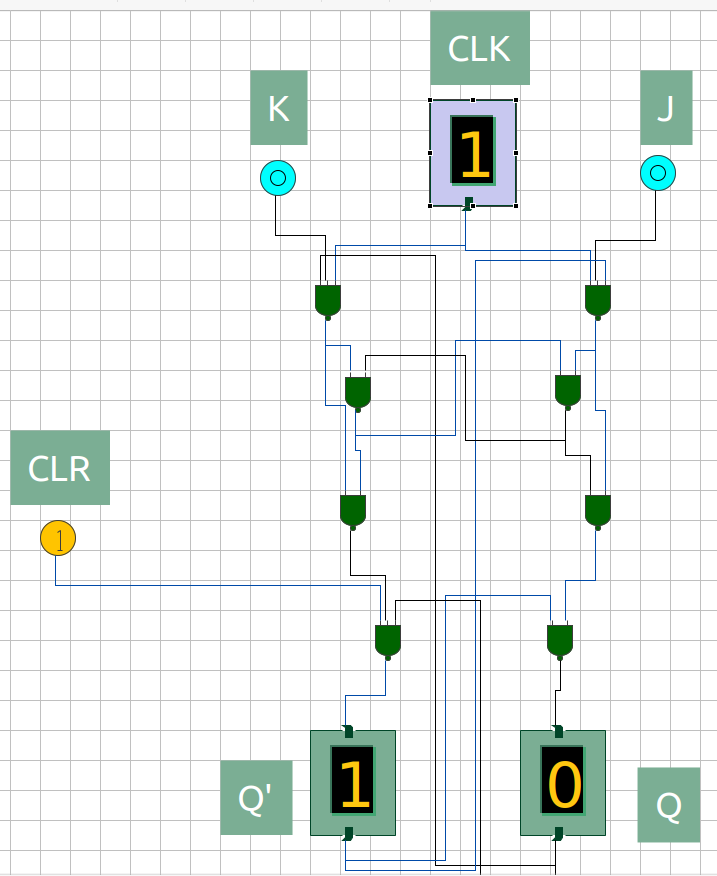
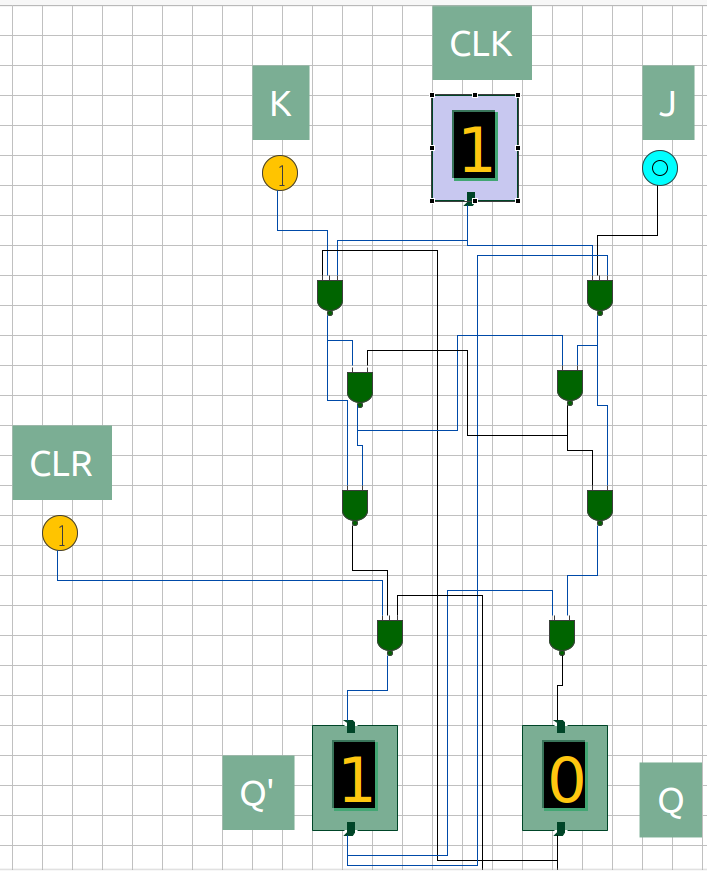
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Figure 1: Q(t) = 0, J = 0, K = 0; Q(t+1) = 0

Figure 2: Q(t) = 0, J = 0, K = 1; Q(t+1) = 0

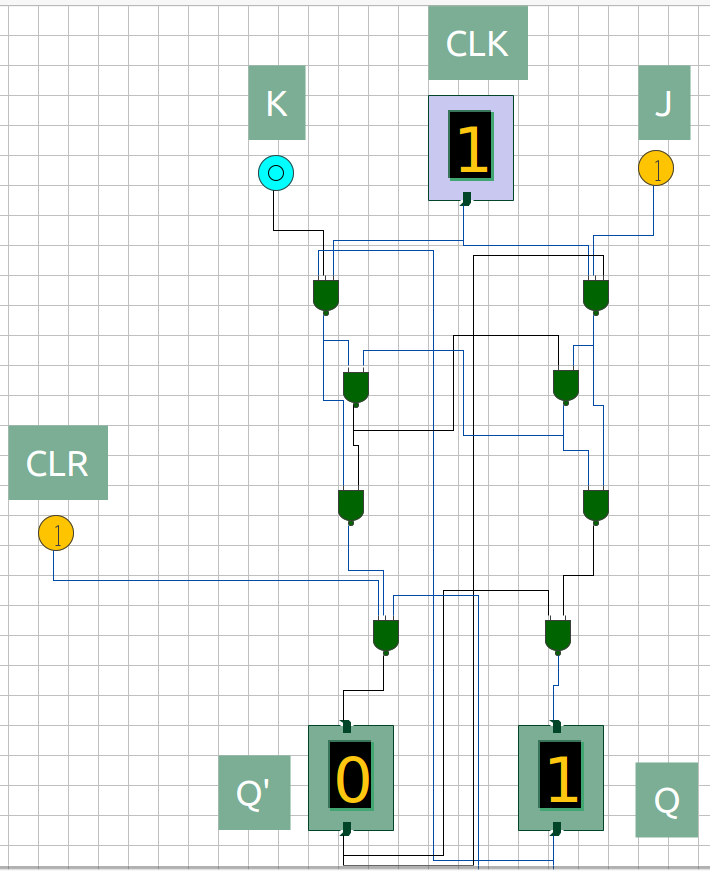
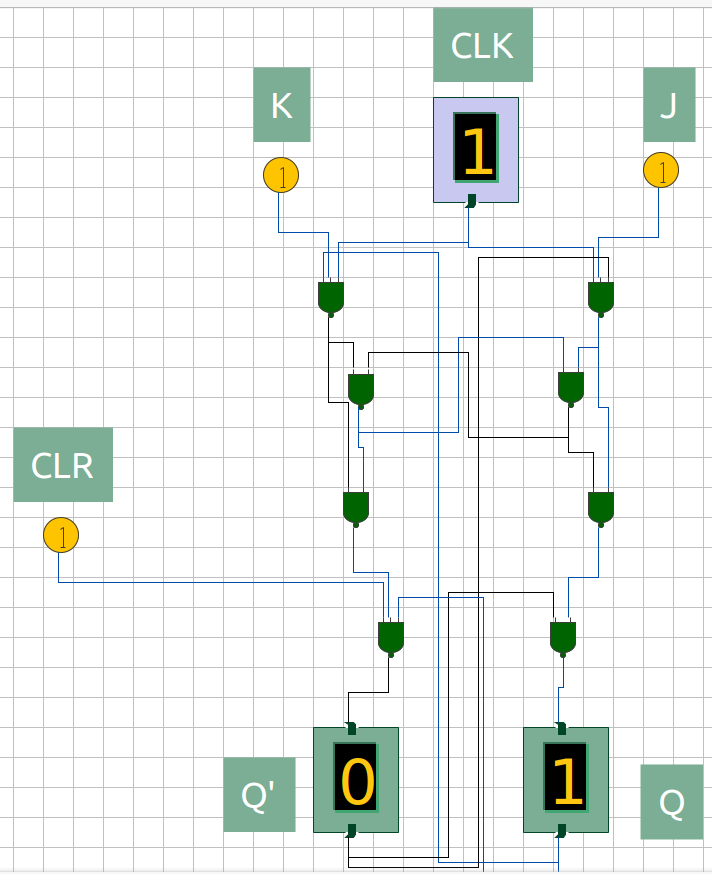


Figure 4: Q(t) = 0, J = 1, K = 1; Q(t+1) = 1

Figure 3: Q(t) = 0, J = 1, K = 0; Q(t+1) = 1

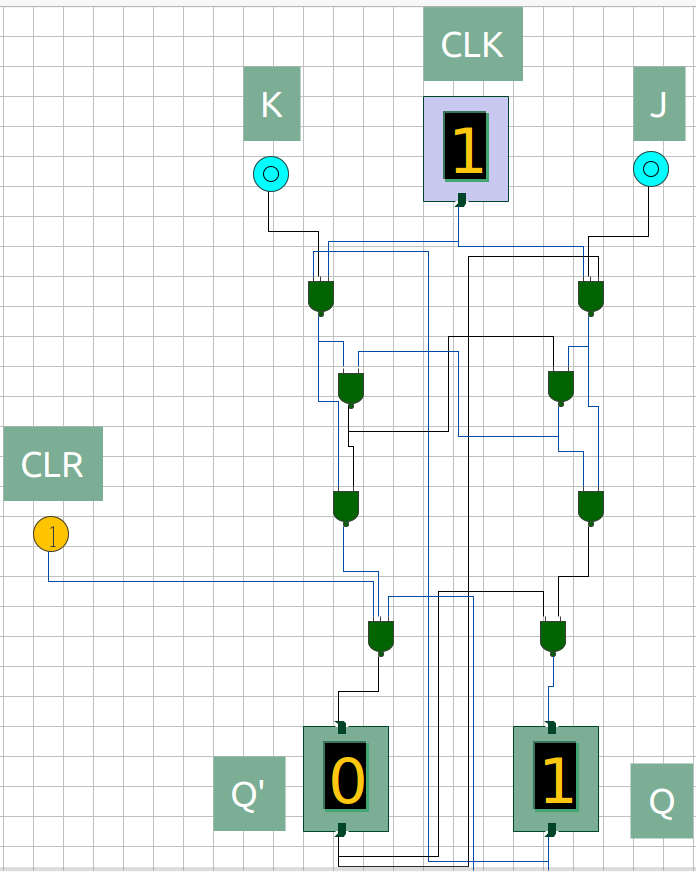
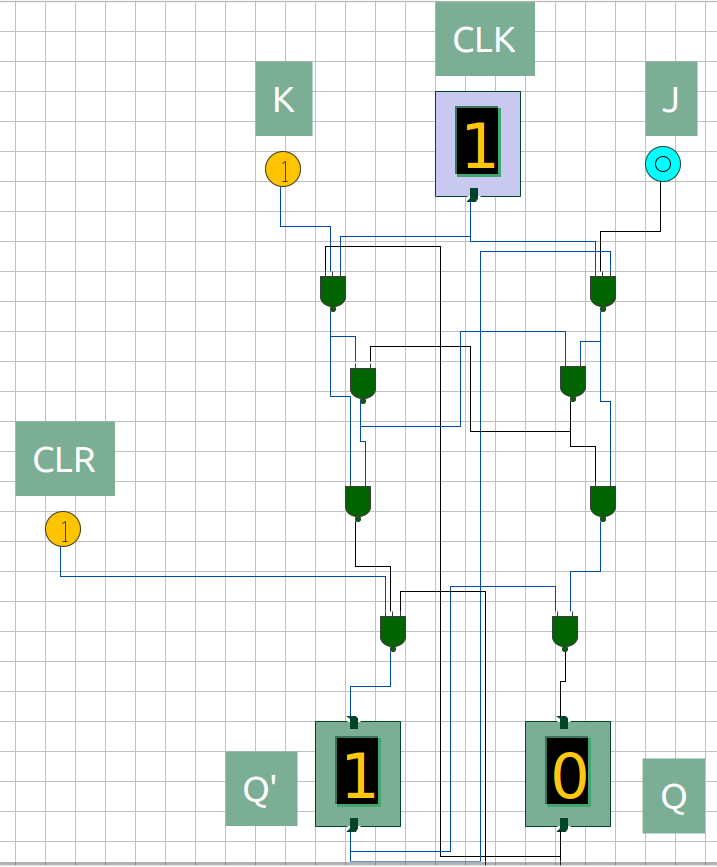


Figure 5: Q(t) = 1, J = 0, K = 0; Q(t+1) = 1

Figure 6: Q(t) = 1, J = 0, K = 1; Q(t+1) = 0

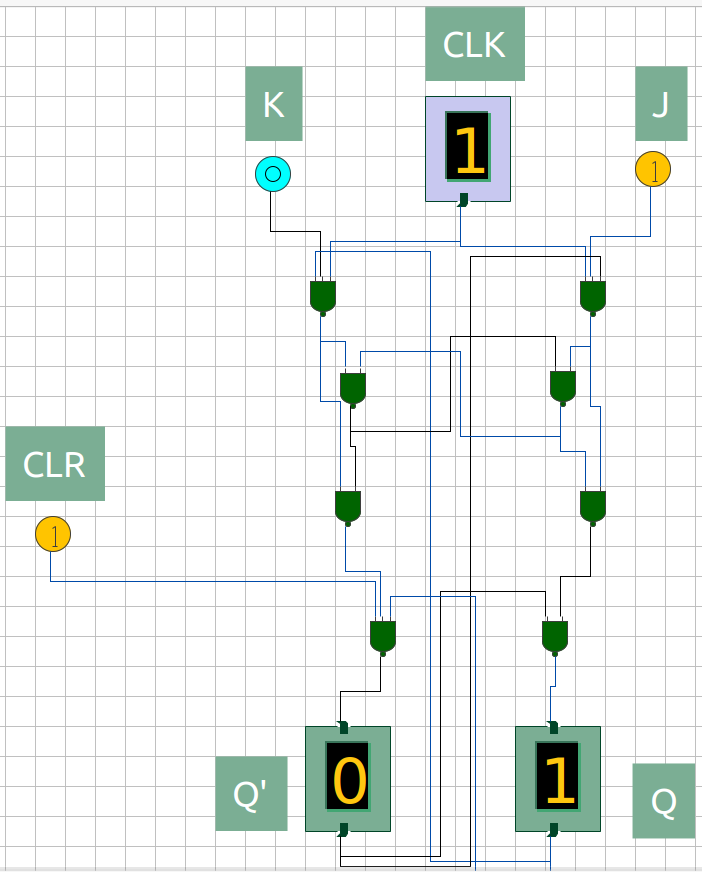
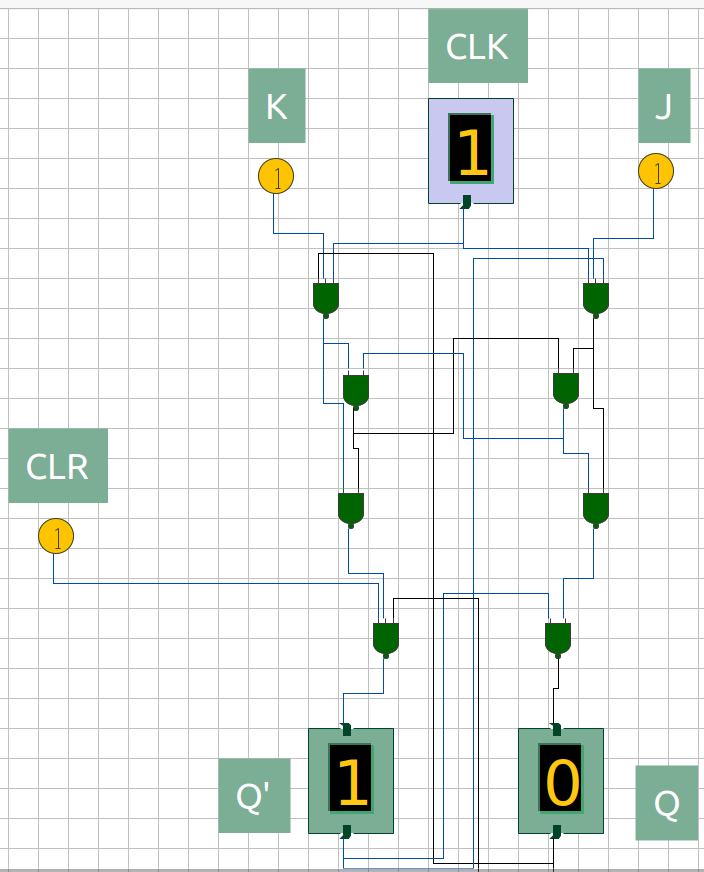
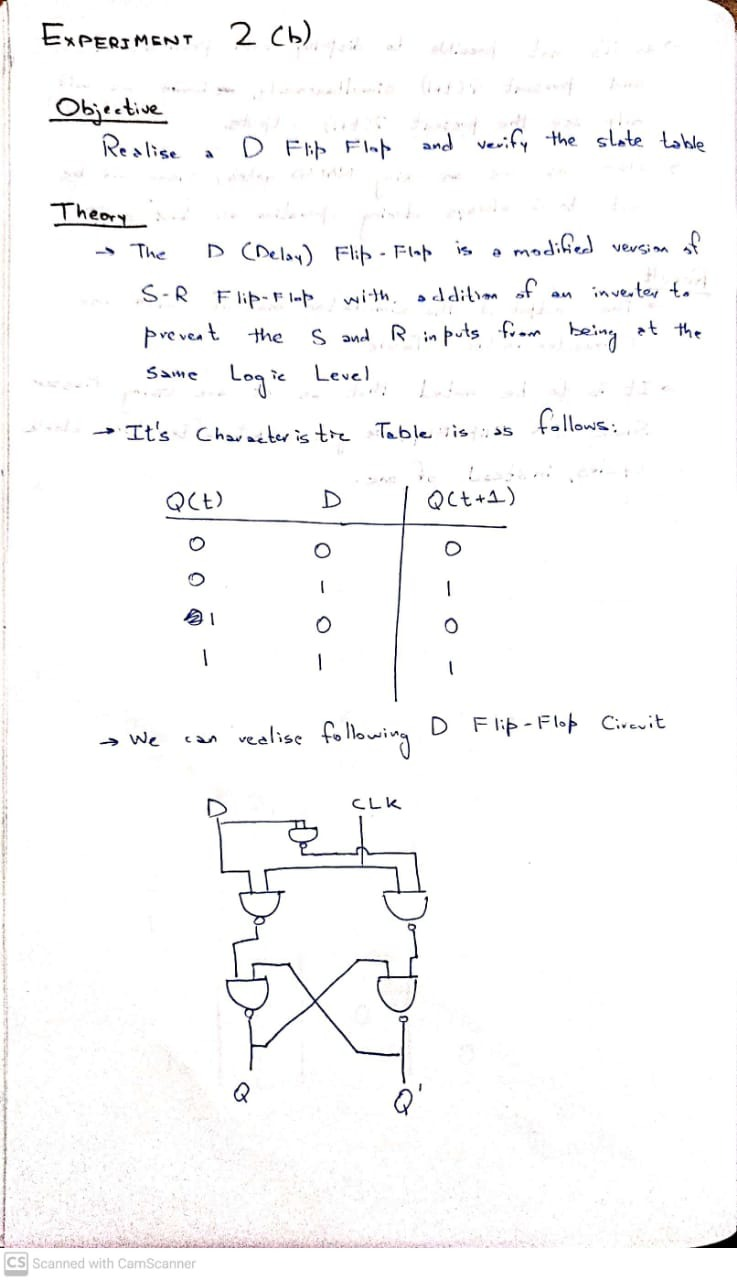
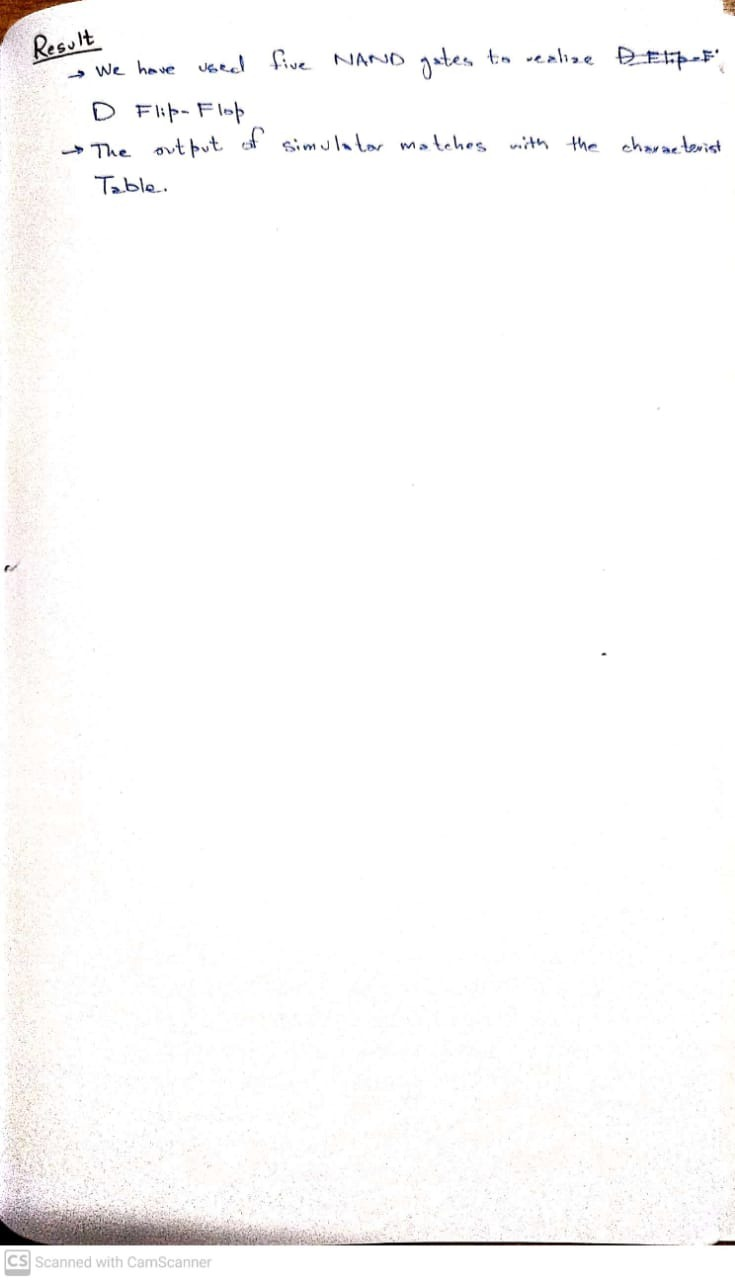


Figure 7: Q(t) = 1, J = 1, K = 0; Q(t+1) = 1

Figure 8: Q(t) = 1, J = 1, K = 1; Q(t+1) = 0





## Inputs / Outputs:

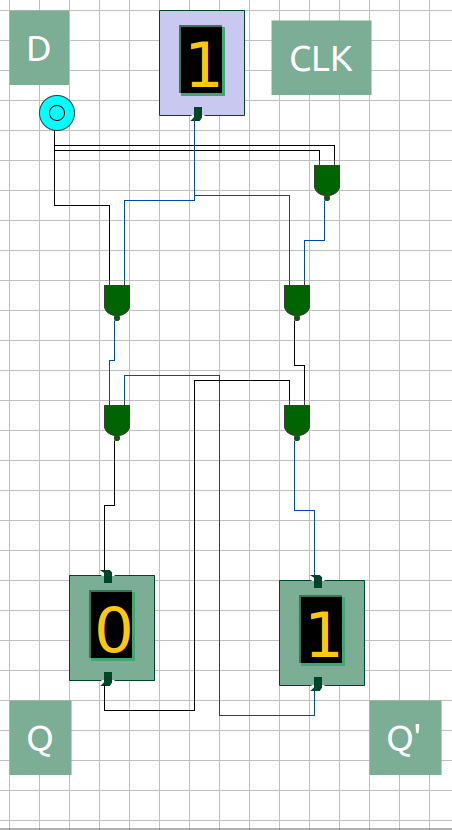
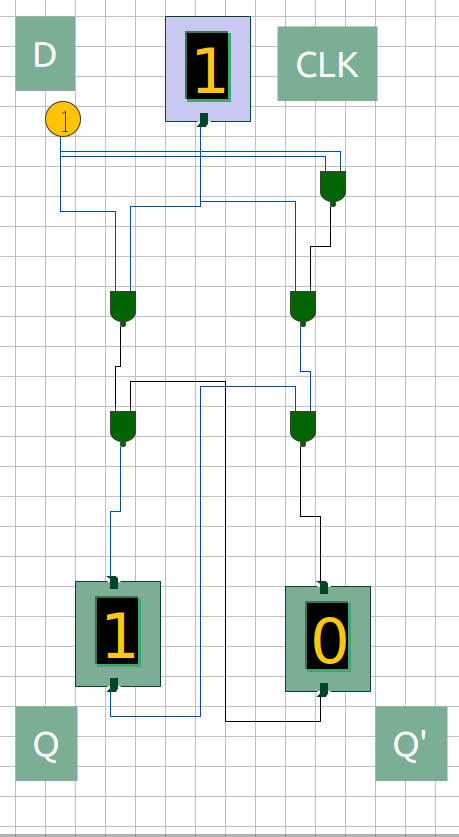
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Figure 1: Q(t) = 0, D = 0; Q(t+1) = 0

Figure 2: Q(t) = 0, D = 1; Q(t+1) = 1

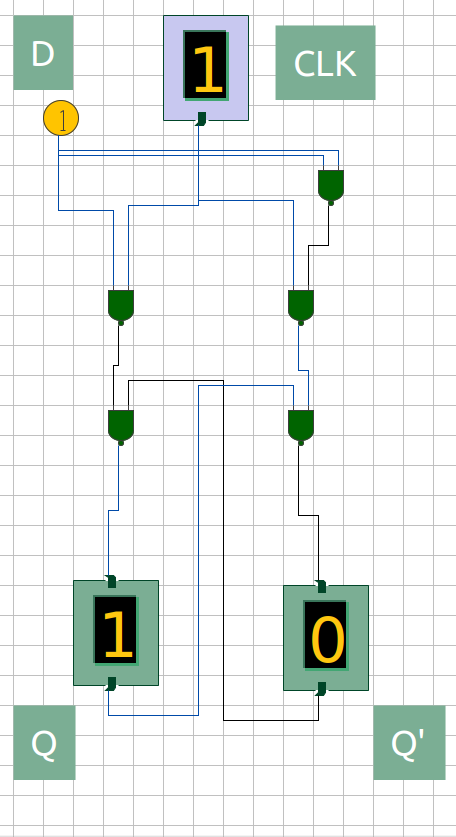
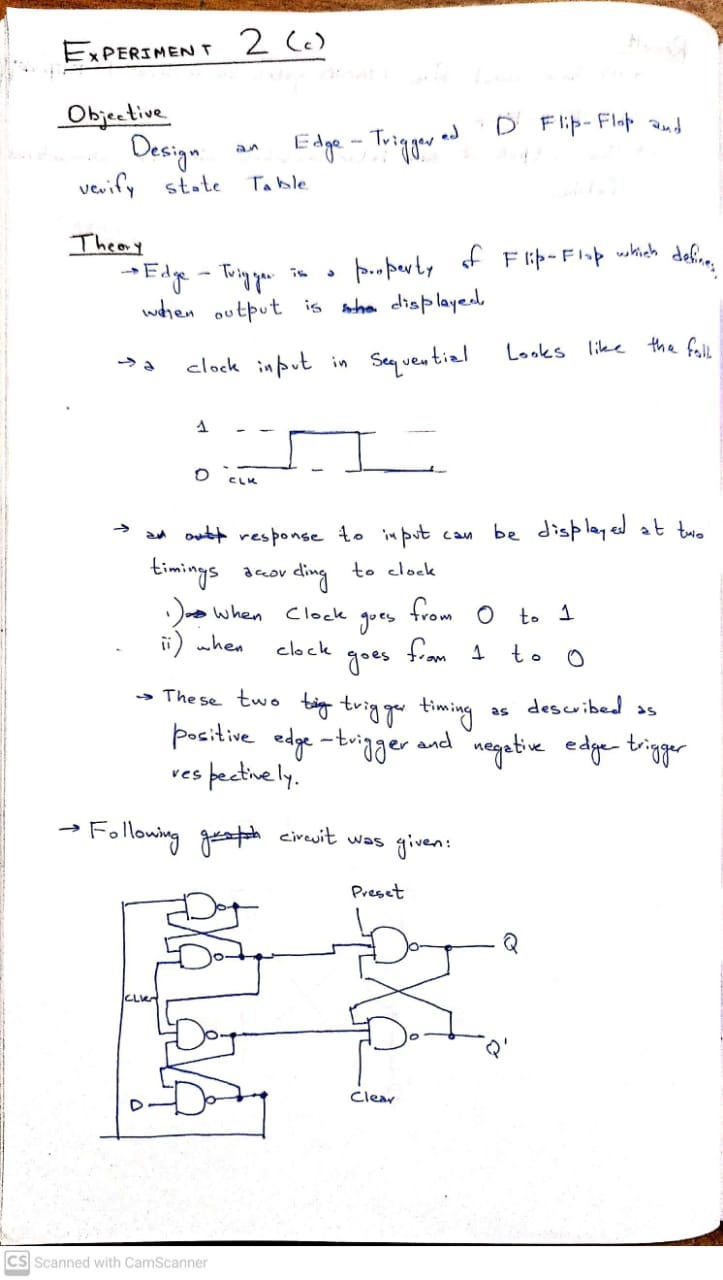
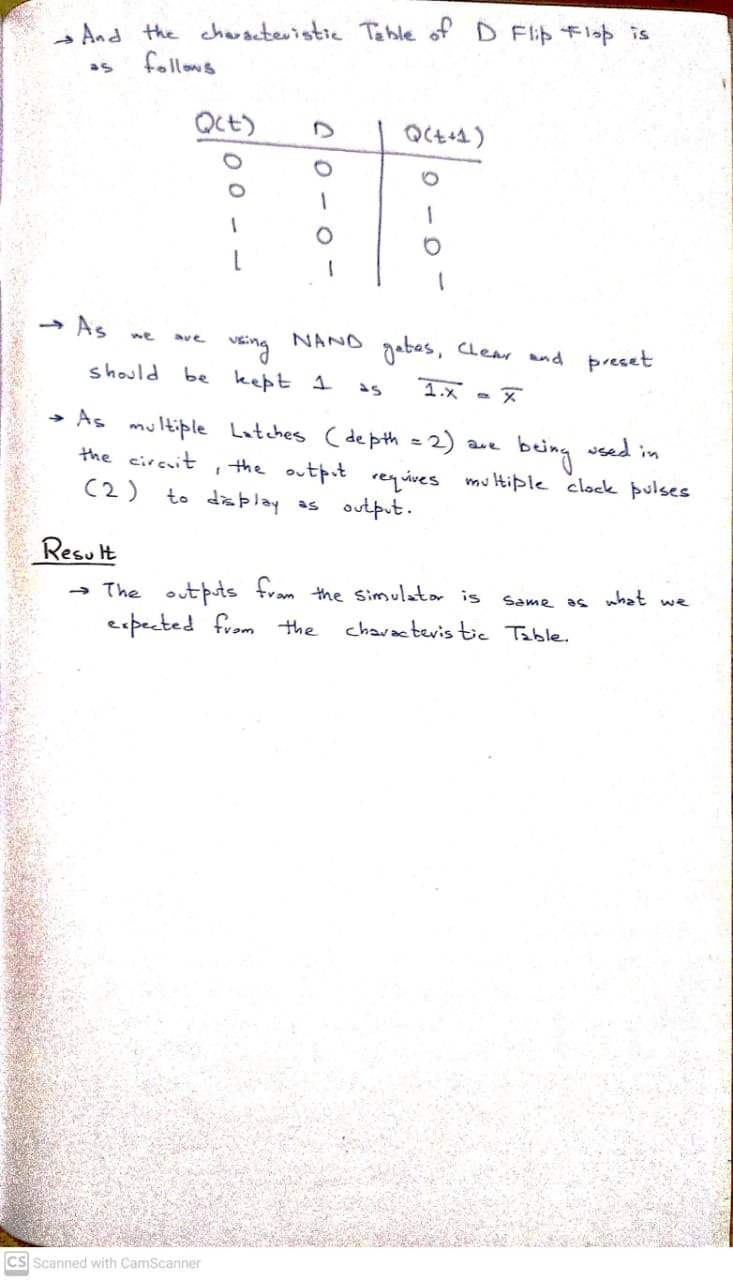


Figure 3: Q(t) = 1, D = 0; Q(t+1) = 0

Figure 4: Q(t) = 1, D = 1; Q(t+1) = 1





## Inputs / Outputs:

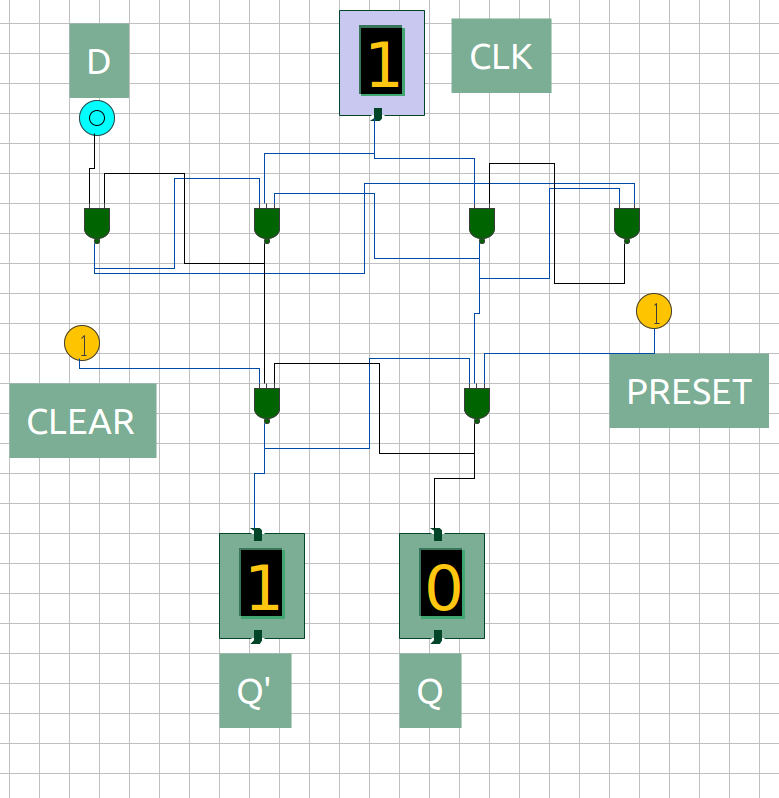
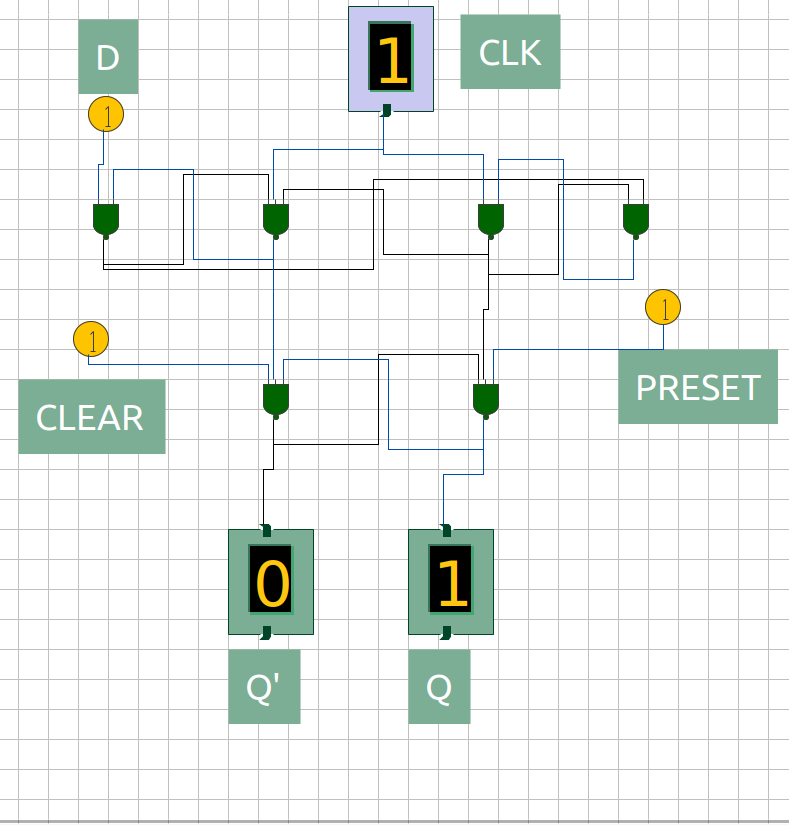
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Figure 1: Q(t) = 0, D = 0; Q(t+1) = 0

Figure 2: Q(t) = 0, D = 1; Q(t+1) = 1

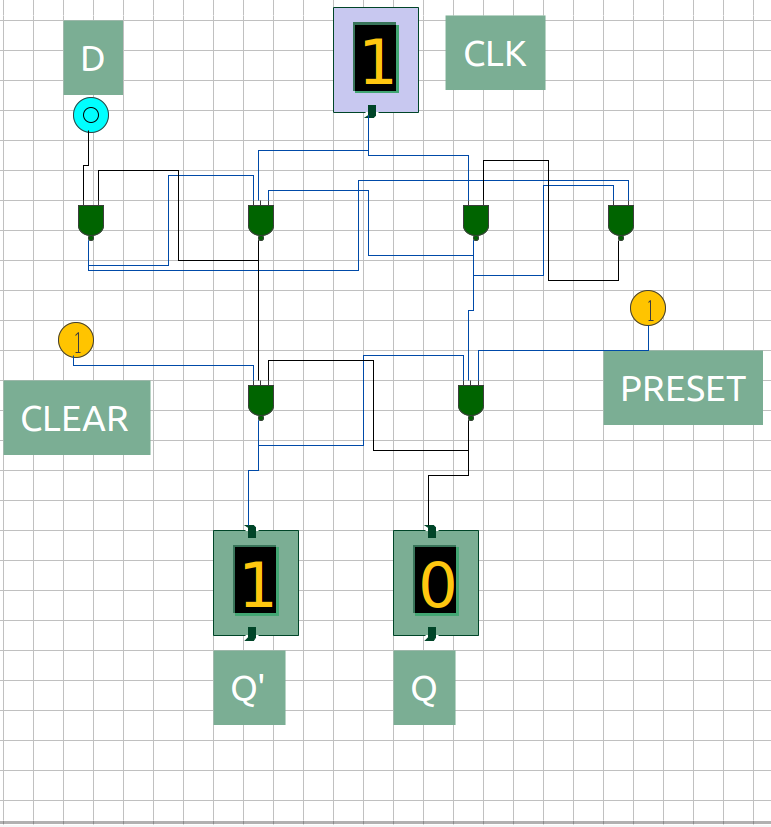
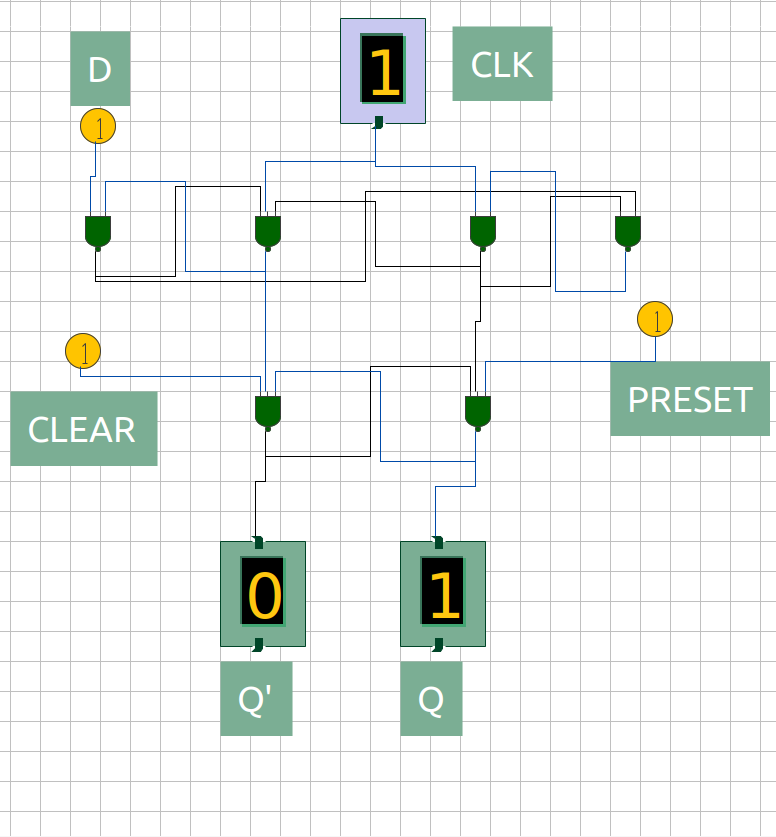


Figure 3: Q(t) = 1, D = 0; Q(t+1) = 0

Figure 4: Q(t) = 1, D = 1; Q(t+1) = 1