4

Programming Technology

CONTENTS

Programming Technology

4.1 Introduction

The logic cells within PLDs are configured using a programming technology. There are two classes of programming technology:

- One-time programmable (OTP): This programming is accomplished during manufacturing and is irreversible. This non-volatility prevents undesirable reprogramming. These attributes are particularly attractive in specific aerospace applications.
- Re-programmable: This kind of programming technology supports repeated programming features. In this programming method, the devices require removing or erasing switching content from the device before programming again.

The use of non-volatile components and devices indicates one-time usage, mainly utilizing fuse technology. If errors are discovered, the production of a new board or device is likely to be required, and for complex systems where extensive testing is needed, this can be cost-prohibitive. On the other hand, for

critical military and aerospace missions that must be carried out irrespective of evolving conditions, the advantages of antifuse technology may be well worth the additional costs. However, various PLD devices use programming technologies based on application areas, cost, and performance.

4.2 Fuse Technology

Fuse programming technology is a one-time programming process where re-programming can not be done. If any changes or development is required, then a new PLD device must be considered for programming.

- This was the original programmable link technology. It is still used in some SPLDs.
- The fuse is a metal link that connects a row and a column in the interconnection matrix. Before programming, there is a fused connection at each intersection.
- To program a PLD device, the selected fuses are opened by passing a current through them sufficient to "blow" the fuse and break the connection. The intact fuses remain and provide a connection between the rows and columns.
- Programmable logic devices that use fuse technology are one-time programmable (OTP).

Figure 4.1 depicts a conceptual illustration of fuse technology. In Figure 4.1(a), a fuse links two lines before programming. For programming the device, a current is passed through the fuse to break the tiny connection between the links (Figure 4.1(b)). Figure 4.1(c) shows the disconnection after programming the device. This disjoint connection can not be reversible. That is, the fuse link can not connect the same lines in the future.

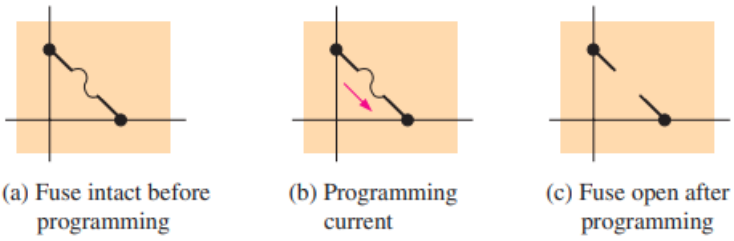

FIGURE 4.1
Conceptual representation of fuse programming method.

4.3 Antifuse Technology

An antifuse is the opposite of a regular fuse — an antifuse is normally an open circuit until applying a programming current through it (about 5 mA).

Normally two types of Antifuses are used:

- Poly-diffusion antifuse (Actel)
- Metal-metal antifuse (Quick Logic)

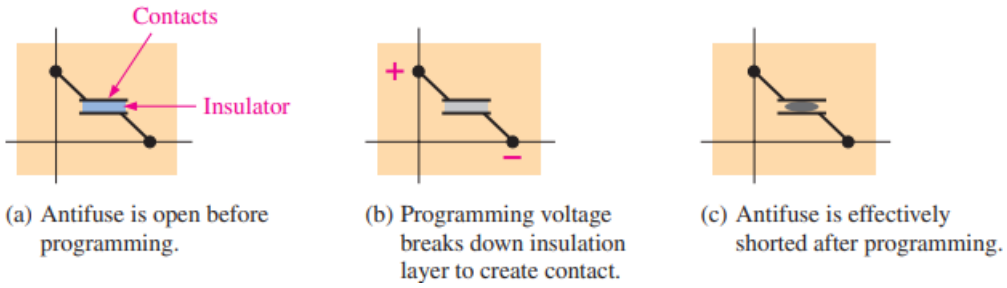

FIGURE 4.2
Conceptual representation of antifuse programming method.

4.3.1 Poly-diffusion antifuse

In a poly–diffusion antifuse, the high current density causes a significant power dissipation in a small area, which melts a thin insulating dielectric between polysilicon and diffusion electrodes and forms a thin (about 20 nm in diameter), permanent, and resistive silicon link. The programming process also drives dopant atoms from the polysilicon and diffusion electrodes into the link, and the final doping level determines the link's resistance value. Actel calls its antifuse a programmable low-impedance circuit element (PLICE).

Figure 4.3 shows a poly–diffusion antifuse with an oxide–nitride–oxide (ONO) dielectric sandwich of silicon dioxide (SiO_2) grown over the n-type antifuse diffusion, a silicon nitride (Si_3N_4) layer, and another thin SiO_2 layer. The layered ONO dielectric results in a tighter spread of blown antifuse resistance values than using a single-oxide dielectric. The effective electrical thickness is equivalent to 10 nm of SiO_2 (Si_3N_4 has a higher dielectric constant than SiO_2, so the actual thickness is less than 10 nm). Sometimes this device is called a fuse even though it is an antifuse, and both terms are often used interchangeably.

Advantage: Small area overhead (size of the antifuse switching element is very small in comparison with size of SRAM cell).

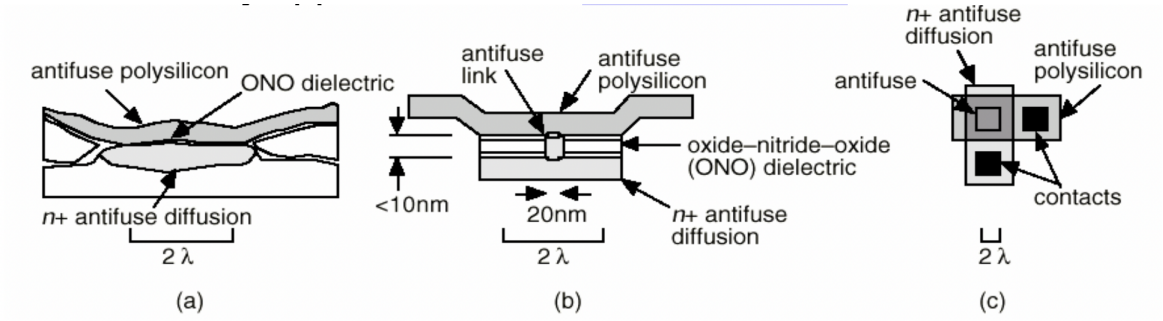

FIGURE 4.3
Actel antifuse. (a) A cross section. (b) A simplified drawing. The ONO (oxide–nitride–oxide) dielectric is less than 10 nm thick, so this diagram is not to scale. (c) From above, an antifuse is approximately the same size as a contact.

Disadvantage: Antifuse technology are one-time programmable.

The fabrication process and the programming current control the average resistance of a blown antifuse. In a particular technology, a programming current of 5 mA may result in an average blown antifuse resistance of about 500 W. Increasing the programming current to 15 mA might reduce the average antifuse resistance to 100 W. Antifuses separate interconnect wires on the chip, and the programmer blows an antifuse to make a permanent connection. Once an antifuse is programmed, the process cannot be reversed. This is an OTP technology (and radiation hard). The number of antifuse switches used in an ACTEL FPGA is significant; for example, Actel 1010 contains 112,000 antifuses.

4.3.2 Programming Process

Designers iterate between design entry and simulation to design and program Actel antifuses. When they are satisfied that the design is correct, they plug the chip into a socket on a special programming box, called an Activator, that generates the programming voltage. A PC downloads the configuration file to the Activator, instructing it to blow the necessary antifuses on the chip. When programmed, it may be removed from the Activator without harming the configuration data and the chip assembled into a system. One disadvantage of this procedure is that modern packages with hundreds of thin metal leads are susceptible to damage when they are inserted and removed from sockets. The advantage of other programming technologies is that PLD chips may be programmed after they have been assembled on a printed-circuit board—a feature known as in-system programming (ISP).

4.3.3 Metal–Metal Antifuse

Figure 4.4 shows a QuickLogic metal–metal antifuse (ViaLink). The link is an alloy of tungsten, titanium, and silicon with a bulk resistance of about 500 mW cm.

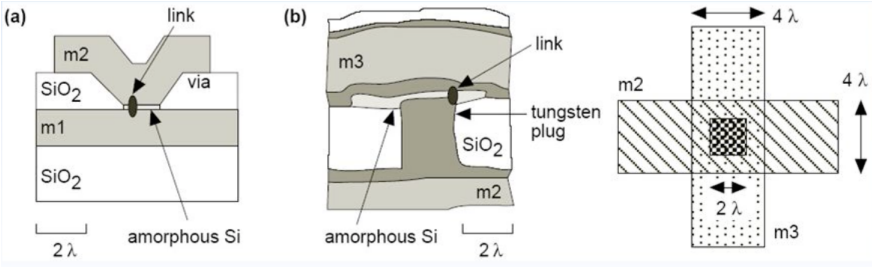

FIGURE 4.4
Metal–metal antifuse. (a) An idealized (but to scale) cross section of a QuickLogic metal–metal antifuse in a two-level metal process. (b) A metal–metal antifuse in a three-level metal process that uses contact plugs. The conductive link usually forms at the corner of the via where the electric field is highest during programming.

There are two advantages of a metal–metal antifuse over a poly–diffusion antifuse. The first is that connections to a metal–metal antifuse are direct to metal–the wiring layers. Connections from a poly-diffusion antifuse to the wiring layers require extra space and create additional parasitic capacitance. The second advantage is that the direct connection to the low-resistance metal layers makes it easier to use larger programming currents to reduce the antifuse resistance.

The size of an antifuse is limited by the resolution of the lithography equipment used to produce ICs. The Actel antifuse connects diffusion and polysilicon, and both these materials are too resistive for use as signal interconnects. To connect the antifuse to the metal layers requires contacts that take up more space than the antifuse itself, reducing the advantage of the small antifuse size. However, the antifuse is so small that it is normally the contact and metal spacing design rules that limit how closely the antifuses may be packed rather than the size of the antifuse itself.

4.3.4 Antifuse Technology Advantages

- **Reliability:** The internal connectivity of antifuse components and networks is practically impossible to break without the destruction of the device, board or component. This makes printed circuit board assemblies

that employ this technology highly reliable. Due to their increased reliability and security, antifuse-based PLDs are great for mission-critical space applications in order to perform various functions such as command and data handling, altitude and orbit control, and spacecraft environmental and power controls.

- **Security:** Antifuse technology can protect PLDs from being reverse engineered since they are OTP (One-Time Programmable) and since they are pre-programmed when shipped to the end-user and they do not have a data/bitstream that can be intercepted. It is very difficult, virtually impossible, to determine the digital state (0 or 1) of the programmed Antifuse PLD. Antifuse PLDs are even more reliable than ASICs.
- **Minimal power and size requirements:** Antifuse technology packages are almost identical in size to their counterparts that do not employ the technology as the antifuse substrate is smaller than the distance between conductors. Moreover, there are no significant power consumption issues since minimal energy is required to read One-Time Programmable Non-Volatile Memory (OTP NVM). This energy efficiency makes devices that employ this technology great for battery-powered operation.

4.4 EPROM / EEPROM

- Non-volatile and reprogrammable
- Generally used in product-term type of PLDs.
- An EPROM (or EEPROM) cell looks like a normal MOS transistor except that it has a second, floating, gate.
- To program an EPROM (or EEPROM) cell, apply a high voltage to the drain of the transistor. It results in electrons trapped in the floating gate and consequently increasing the the threshold voltage.
- To erase an EPROM cell, expose the chip to UV light.
- To erase an EEPROM cell, electrical field is used to remove electrons from the floating gate.
- Good for FSM, less good for arithmetic circuits.

An EPROM transistor looks like a normal MOS transistor except it has a second, floating, gate (gate1 in Figure 4.5(a)). Applying a programming voltage V_{PP} (usually greater than 12 V) to the drain of the n-channel EPROM

transistor programs the EPROM cell. A high electric field causes electrons flowing toward the drain to move so fast they "jump" across the insulating gate oxide where they are trapped on the bottom, floating, gate. We say these energetic electrons are hot and the effect is known as hot-electron injection or avalanche injection. EPROM technology is sometimes called floating-gate avalanche MOS (FAMOS).

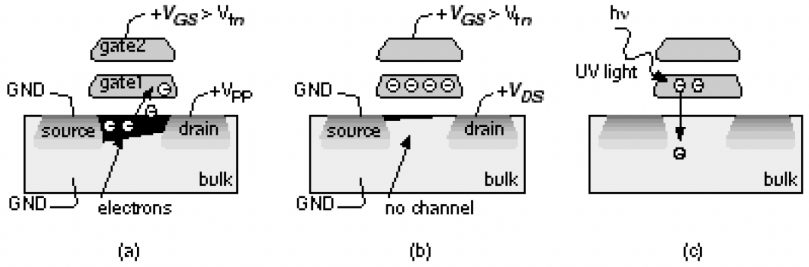

FIGURE 4.5
An EPROM transistor. (a) With a high ($> 12\ V$) programming voltage, V_{PP} , applied to the drain, electrons gain enough energy to "jump" onto the floating gate (gate1). (b) Electrons stuck on gate1 raise the threshold voltage so that the transistor is always off for normal operating voltages. (c) Ultraviolet light provides enough energy for the electrons stuck on gate1 to "jump" back to the bulk, allowing the transistor to operate normally.

Electrons trapped on the floating gate raise the threshold voltage of the n-channel EPROM transistor (Figure 4.5(b)). Once programmed, an n-channel EPROM device remains off even with VDD applied to the top gate. An unprogrammed n- channel device will turn on as normal with a top-gate voltage of V_{DD} . The programming voltage is applied either from a special programming box or by using on-chip charge pumps. Exposure to an ultraviolet (UV) lamp will erase the EPROM cell (Figure 4.5(c)). An absorbed light quantum gives an electron enough energy to jump from the floating gate. To erase a part we place it under a UV lamp. The manufacturer provides a software program that checks to see if a part is erased. You can buy an EPROM-based PLD part in a windowed package for development, erase it, and use it again, or buy it in a non-windowed package and program (or burn) the part once only for production. The packages get hot while they are being erased, so that windowed option is available with only ceramic packages, which are more expensive than plastic packages.

Programming an EEPROM transistor is similar to programming an UV-erasable EPROM transistor, but the erase mechanism is different. In an EEPROM transistor an electric field is also used to remove electrons from the floating gate of a programmed transistor. This is faster than using a UV lamp

and the chip does not have to be removed from the system. If the part contains circuits to generate both program and erase voltages, it may use ISP.

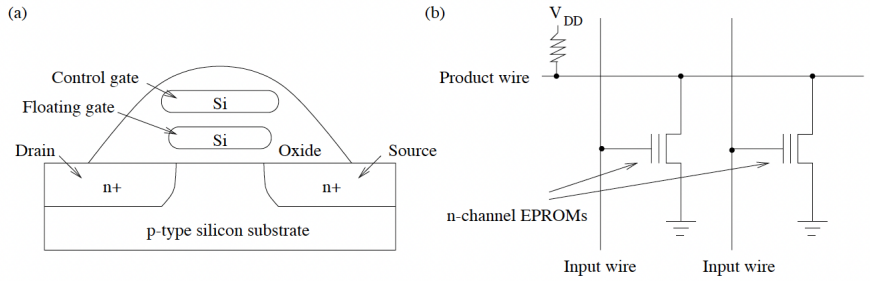

FIGURE 4.6
(a) A n-channel EPROM transistor. (b) A section of an EPROM-based device.

4.5 Static RAM (SRAM) Based Programming Technology

- Use SRAM cells to control pass transistors or multiplexers by the bit-content in the SRAM cells.
- Advantage: re-programmable.
- Disadvantage: occupy more space, volatile and generally consumes high power

4.5.1 SRAM-Controlled Programmable Switch: An Example

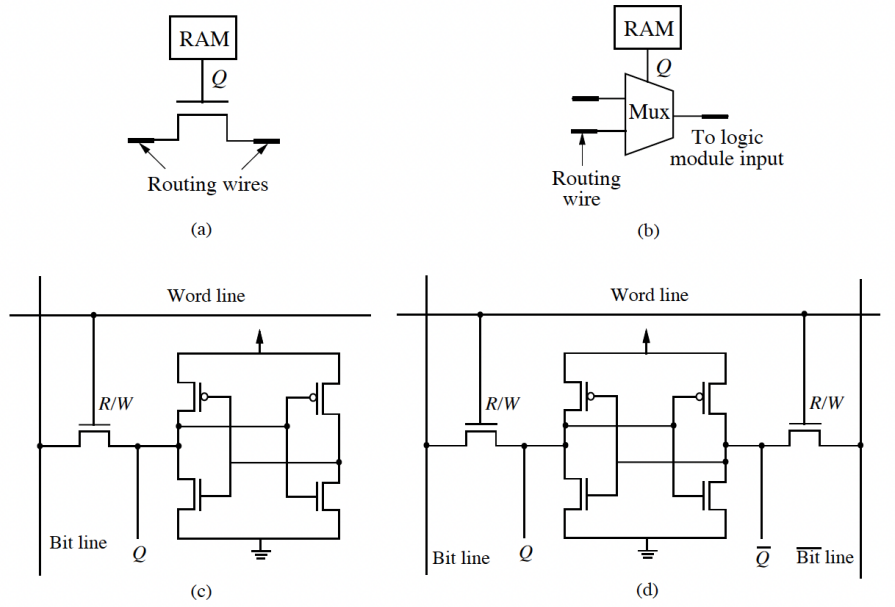

FIGURE 4.7
(a)(b) A pass-transistor switch/multiplexer switch controlled by a RAM cell.
(c)(d) SRAM cells implemented using five/six transistors.

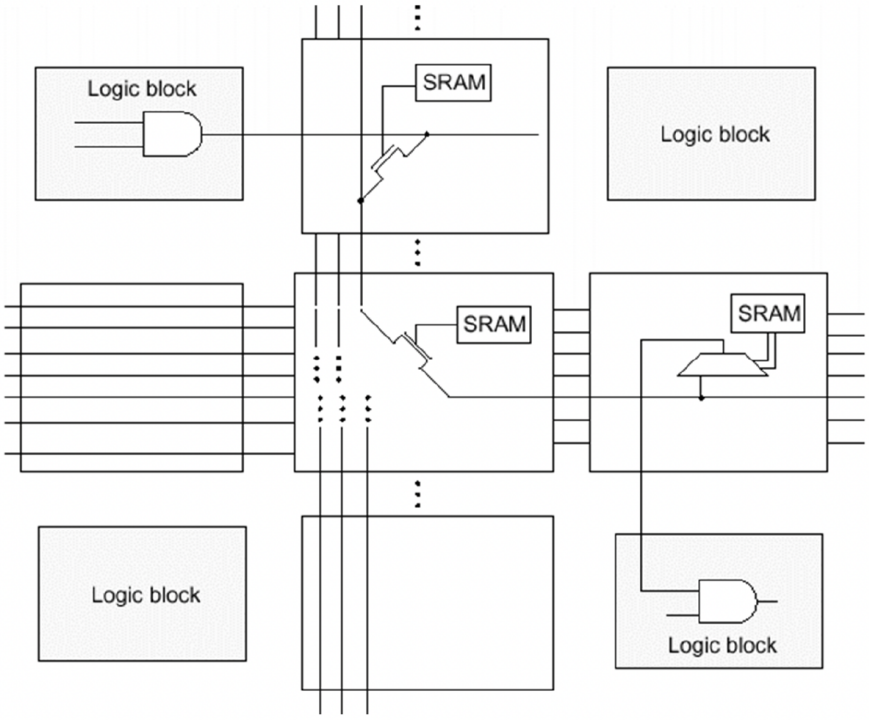

FIGURE 4.8
Example of SRAM-Controlled Programmable Switch.