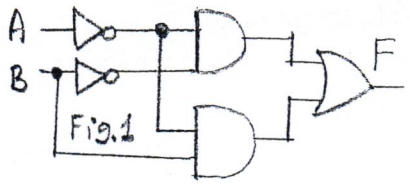
5/12/17

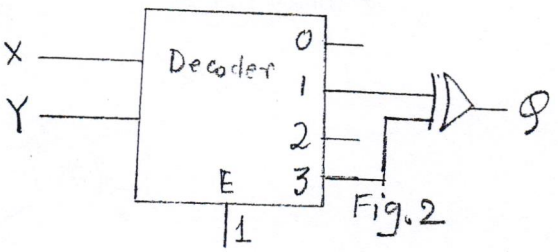
Indian Institute of Engineering Science and Technology, Shibpur
Five year Dual Degree (B.Tech-M.Tech) 3rd Semester
Examination <Year>
<Digital logic> < CS 301>

Full marks: 70 Time: 3 hours

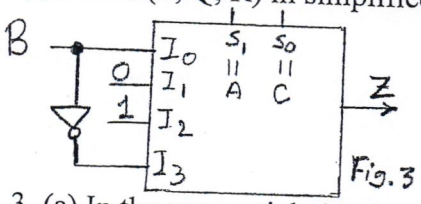
(Answer any five)

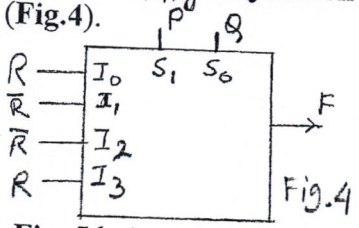
1. (a) Realize NAND gate using NOR gate.
   (b) Prove that the following circuit (**Fig.1**) is same as NOT i.e. negation of a Boolean variable A.



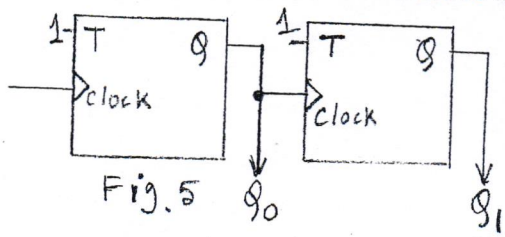


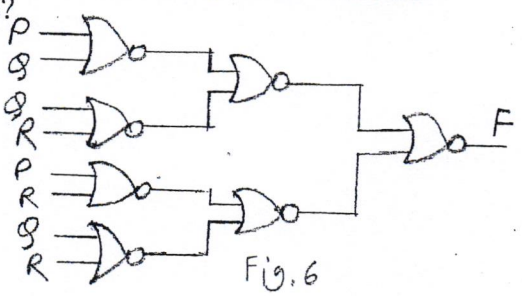
   (c) Prove that A[AB+C(D′+A)+B] = AB+AC
   (d) Find Dual of x+x′y = x+y
   (e) Prove that AB+ABC+ABCD+ABCDE+ABCDEF = AB
   (f) A Boolean function Q(x, y) is implemented using a 2x4 decoder (**Fig.2**). What is Q(x, y)?
   (g) Find Z(A, B, C), the output of **Fig.3**.
   (h) Draw Karnaugh map for F(A, B, C) = A′+B+C [2+2+2+1+1+2+2+2]
2. (a) How many adjacent cells in a Karnaugh map must be circled to eliminate 3 variables?
   (b) Simplify F(A, B, C, D) = ∑ (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14) using Karnaugh map and find the number of literals in the simplified equation of F.
   (c) What is hazard? How hazard can be avoided?
   (d) How many clock pulses are counted by n-bit Ring and Johnson counter?
   (e) Find F(P, Q, R) in simplified form (**Fig.4**). [1+4+(1+3)+2+3]





3. (a) In the sequential circuit shown in **Fig. 5** below the initial output Q_1Q_0 is 00. What are the values of Q_1Q_0 at the consecutive four clock pulses?





   (b) Find F in simplified form (**Fig.6**).
   (c) Express the Boolean function F=xy+x′z in POS form.
   (d) Draw the OR-AND circuit of the simplified Boolean function F(A, B, C, D) = ∑(0, 1, 2, 5, 8, 9, 10) assuming that the complement inputs are available. [4+4+2+4]
4. (a) Obtain 9's and 10's complement of the following decimal numbers.

(i) 13579 (ii) 09900 (iii) 90090

(b) Perform the following subtraction using 9's complement

(i) 5250-321 (ii) 753-864 (iii) 20-1000 (iv) 1753-8640 [6+8]

5. (a) Design the binary synchronous counter having the following repeated binary sequence using T flip flops. (i) 0, 1, 2, 0 (ii) 0, 3, 2, 0

(b) Draw and explain the operation of NAND and NOR gate using CMOS. [8+6]

6. (a) Design a clocked sequential circuit whose state diagram is given in **Fig.7** using T flip flop.

(b) How many clock pulses are required to shift 8 bit data through a 4-bit shift register and why?

(c) Draw the circuit of a Mod-10 ripple counter using negative edge triggered J-K flip flop. Find the repetition rate of this counter when the clock time is T_c. [6+2+4+2]

7. (a) Compare the performance of DTL, TTL, CMOS logic on the basis of power dissipation and propagation delay.

(b) Find the fan out of a RTL gate for I_{Csat}=5.31 mA and h_{FE}>7.

(c) What is the propagation delay time of open collector TTL, totem pole TTL and schottky TTL? [6+5+3]

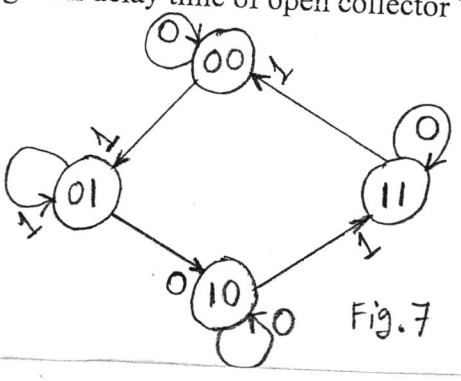


Fig.7