Digital Logic

Practical

Lab Report

Multiplexer and Decoder/Demultiplexer

Student:

Abhiroop Mukherjee

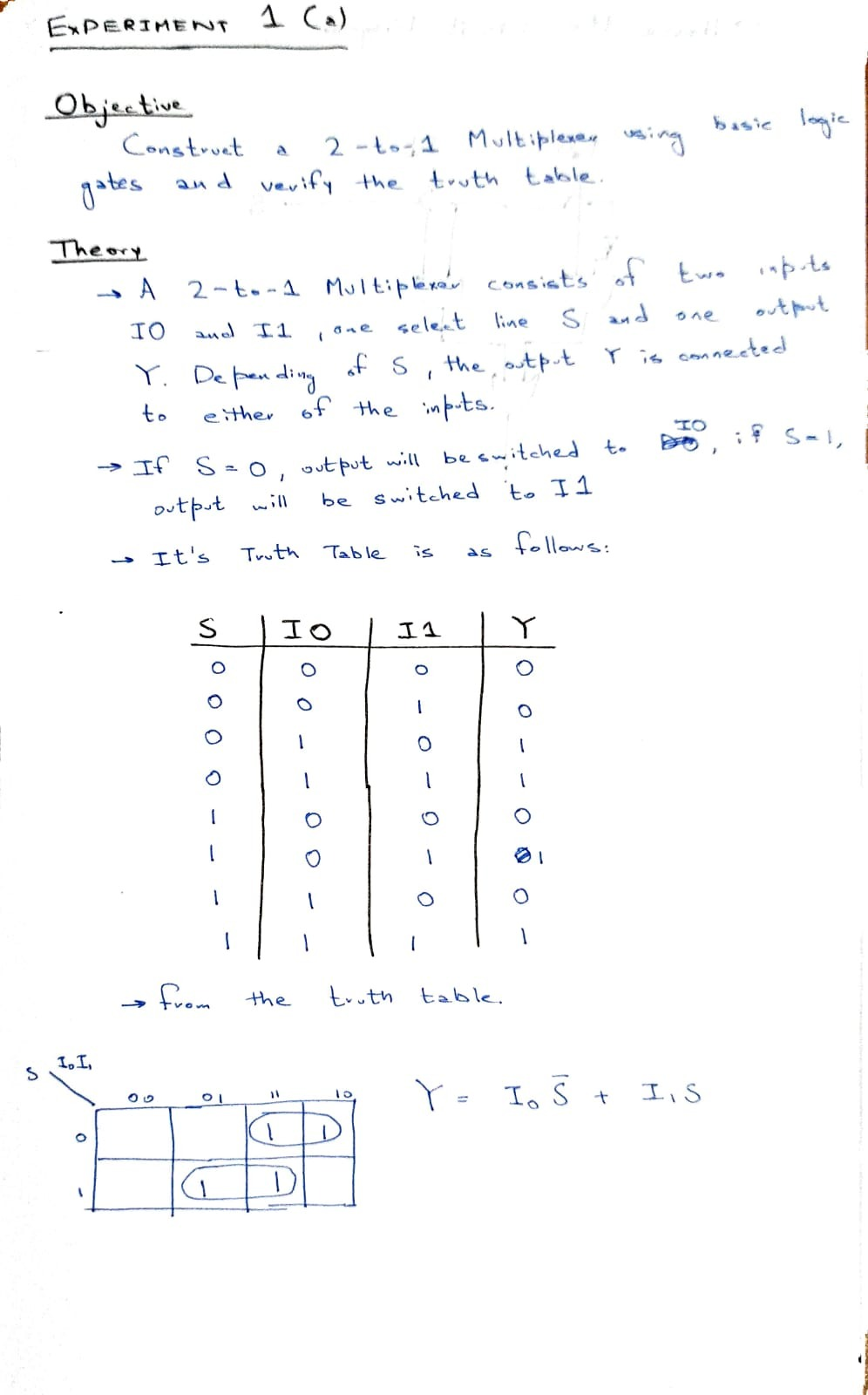
Teacher:

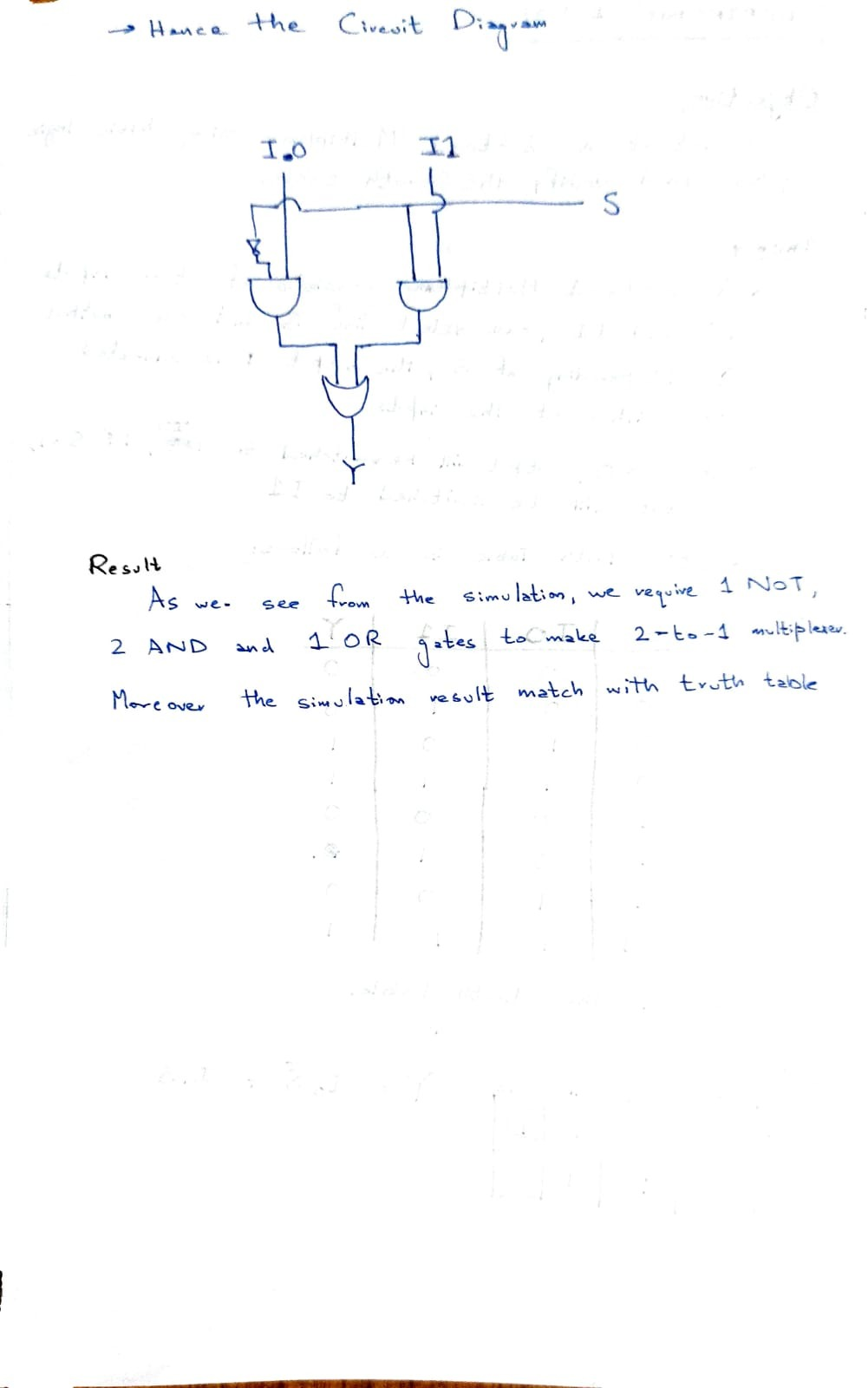
Prof. Surajeet Ghosh

Prof. Sekhar Mandal

Course:

Digital Logic Laboratory (CS351)





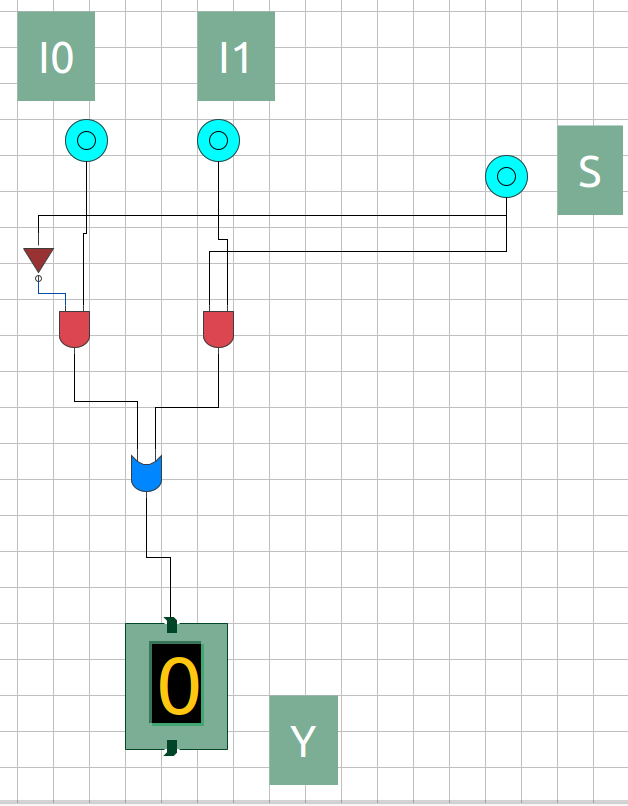
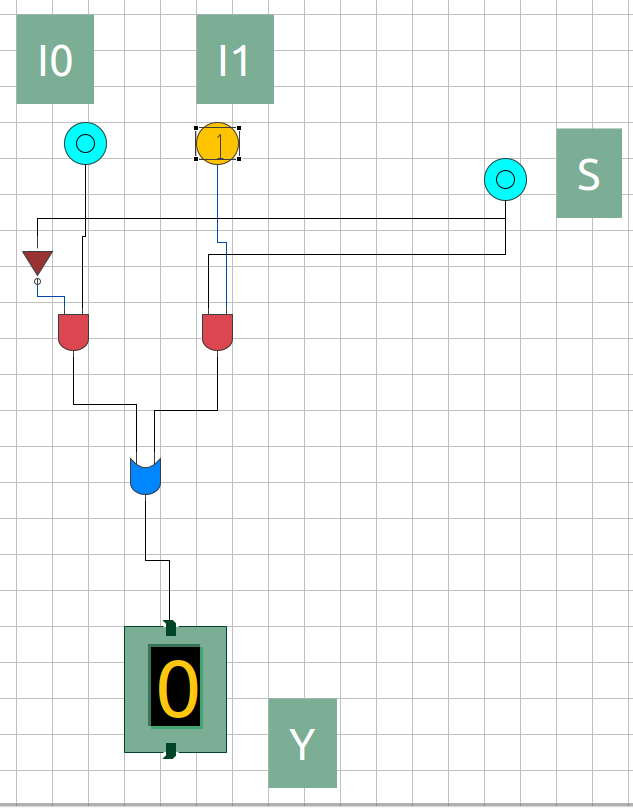
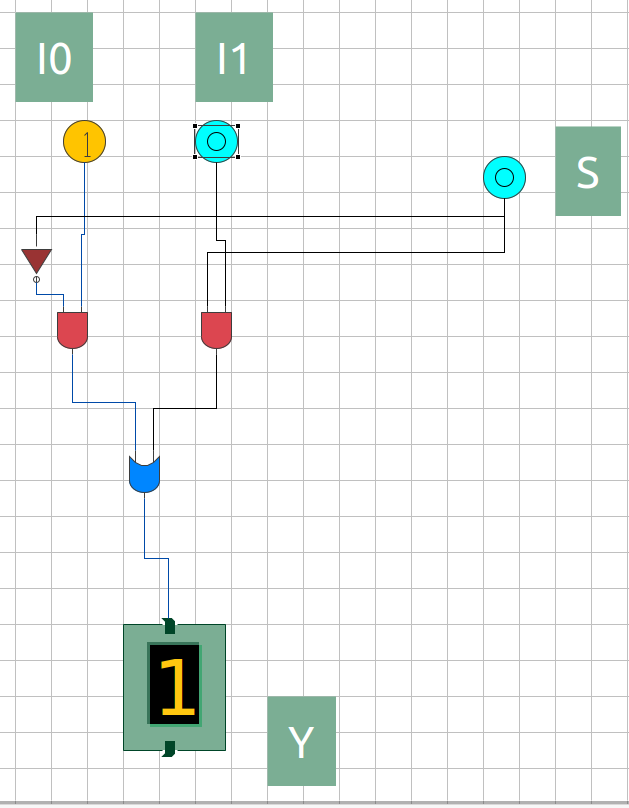
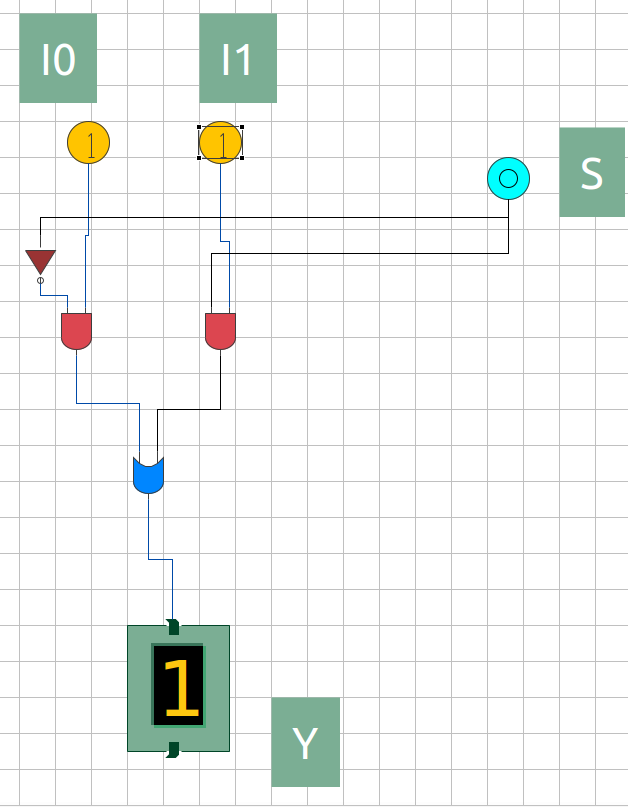
## Inputs / Outputs:

Figure 1: S = 0, I0 = 0, I1 = 0; Y=0

Figure 2: S = 0, I0 = 0, I1 = 1; Y=0

Figure 3: S = 0, I0 = 1, I1 = 0; Y=1

Figure 4: S = 0, I0 = 1, I1 = 1; Y=1



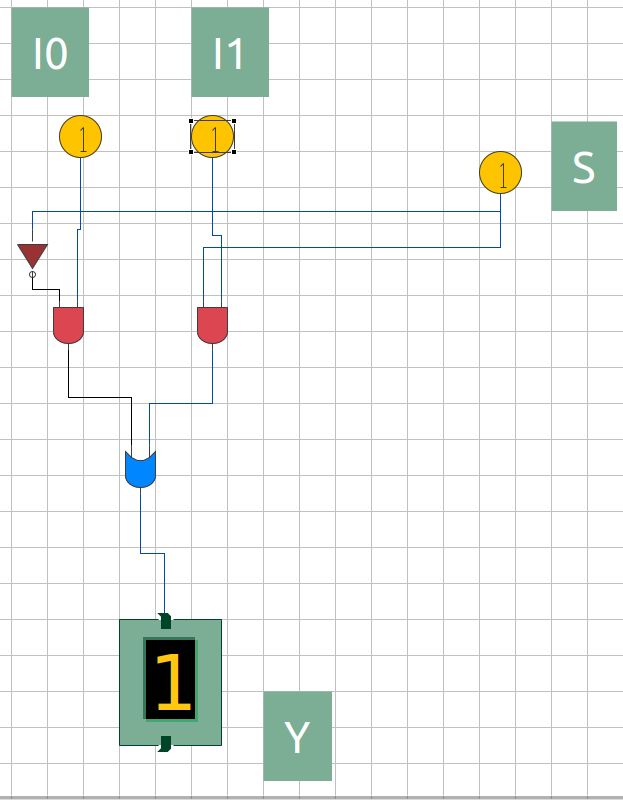
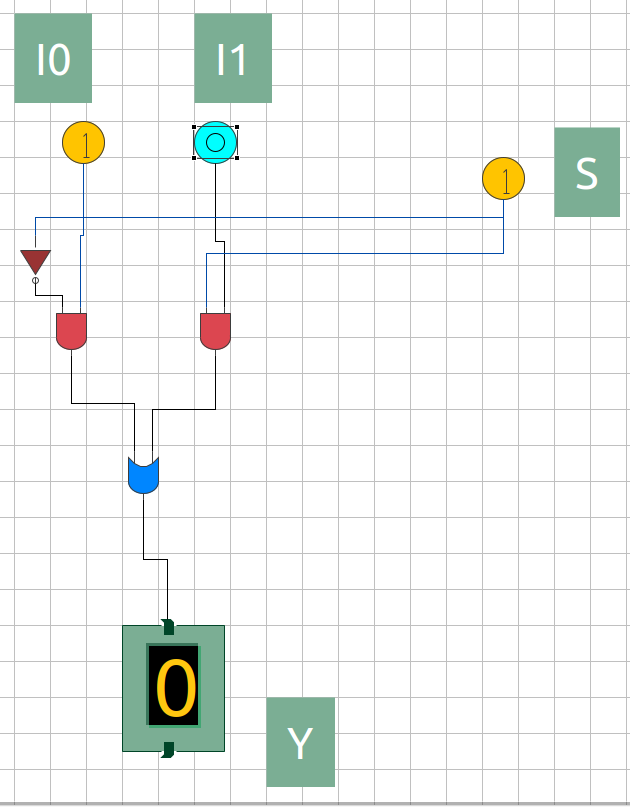
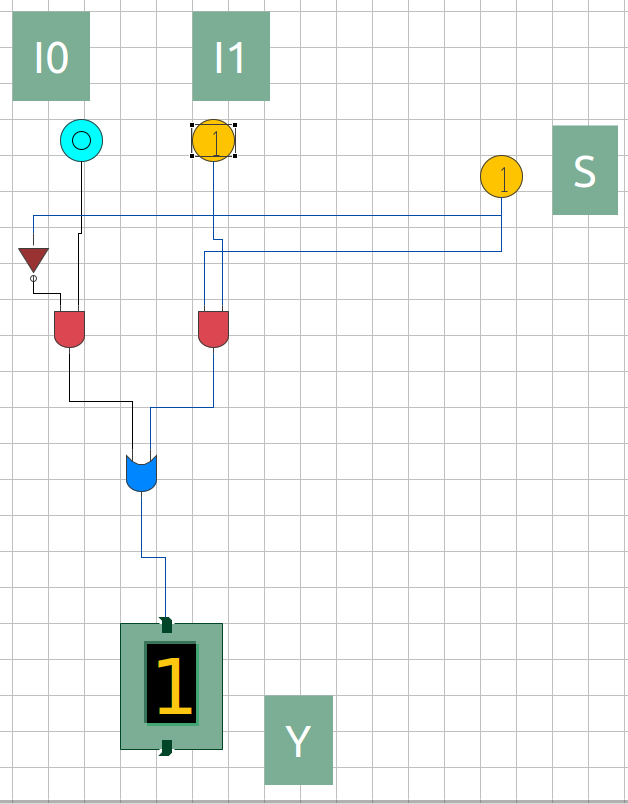
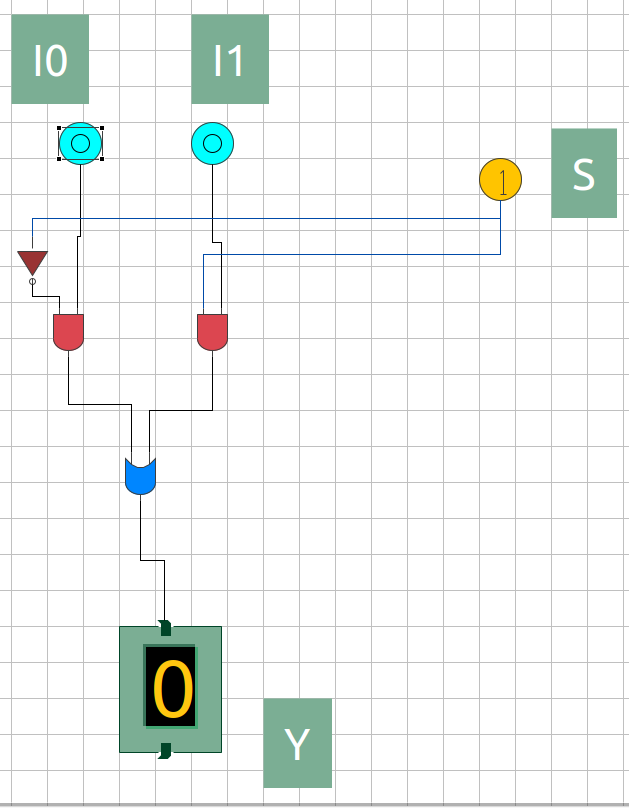


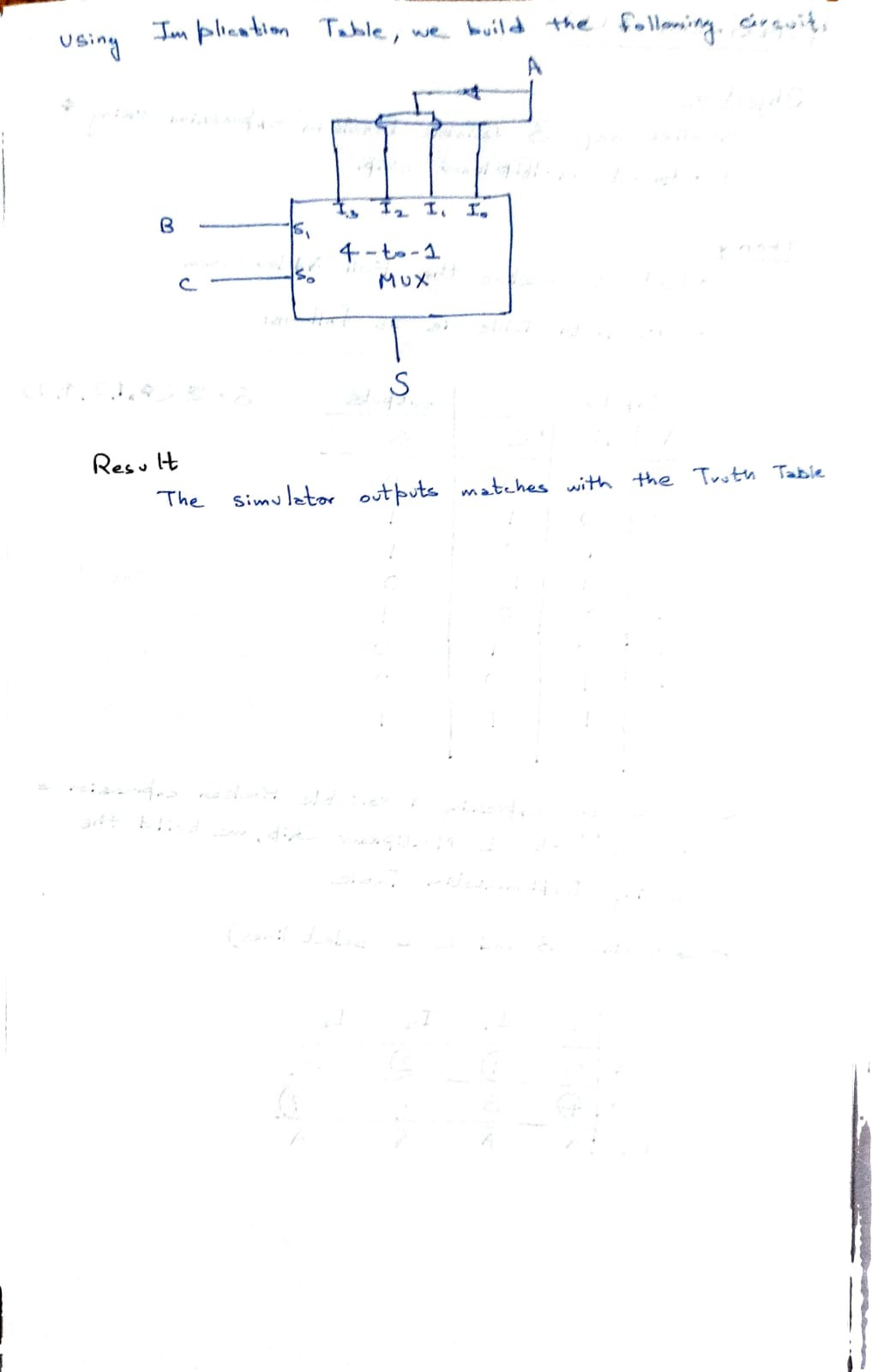
Figure 5: S = 1, I0 = 0, I1 = 0; Y=0

Figure 6: S = 1, I0 = 0, I1 = 1; Y=1

Figure 7: S = 1, I0 = 1, I1 = 0; Y=0

Figure 8: S = 1, I0 = 1, I1 = 1; Y=1

## 



## Inputs / Outputs:

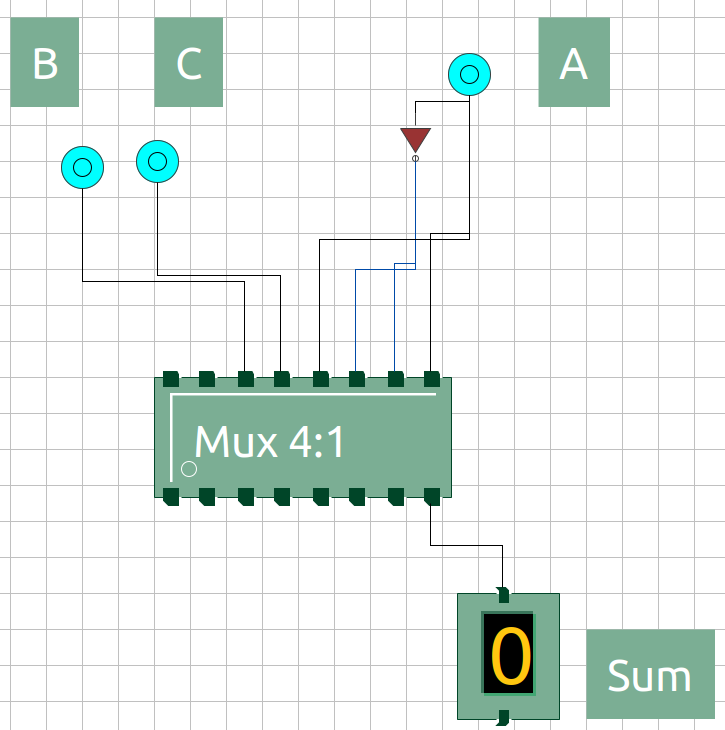
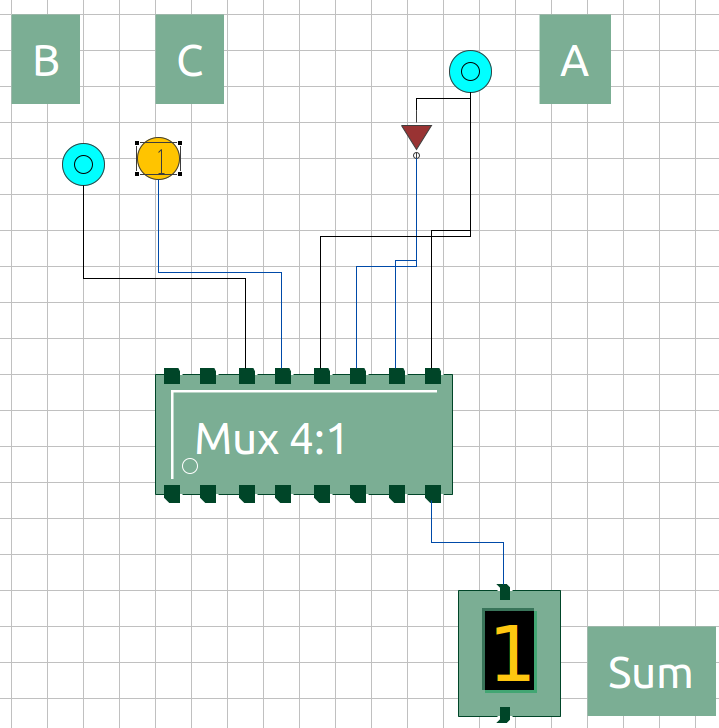
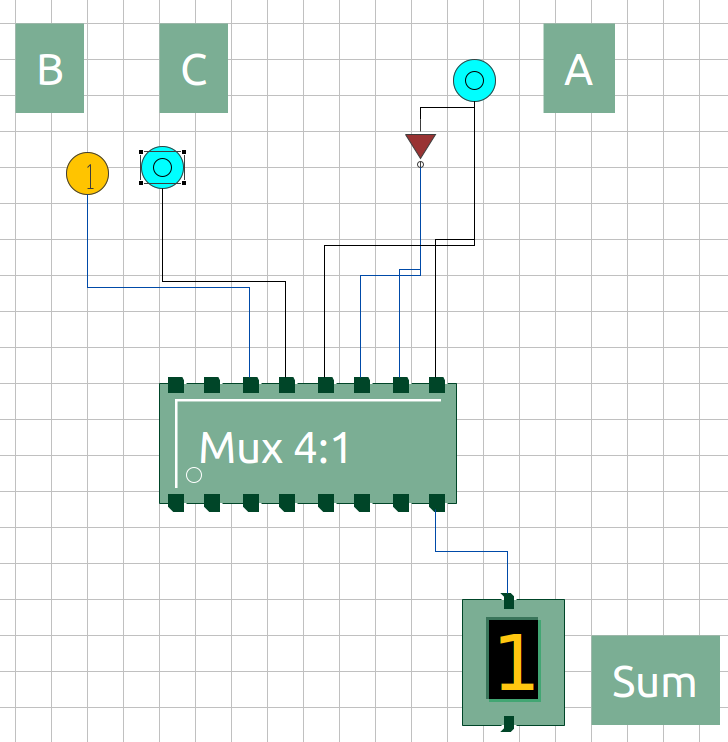
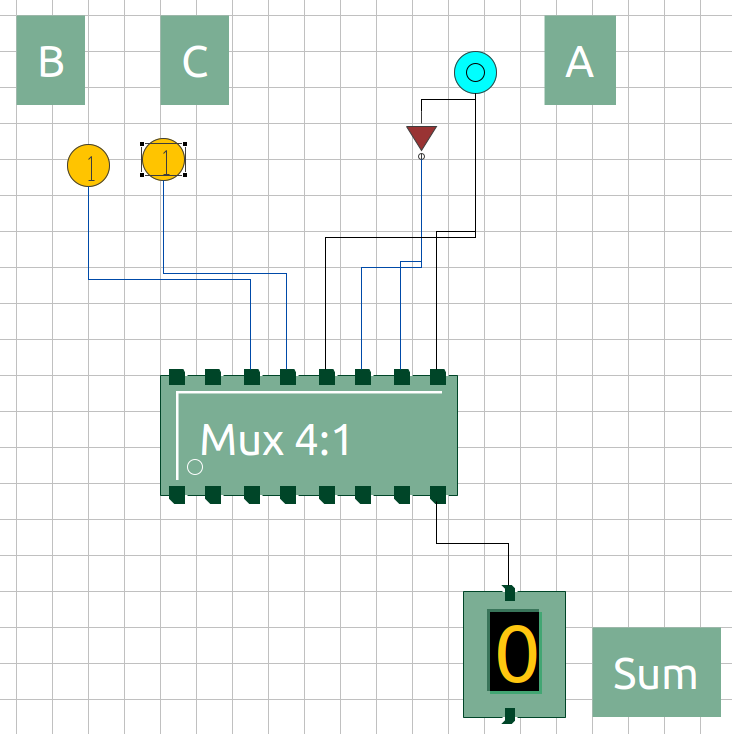


Figure 3: A = 0, B = 1, C = 0; S=1

Figure 4: A = 0, B = 1, C = 1; S=0

Figure 1: A = 0, B = 0, C = 0; S=0

Figure 2: A = 0, B = 0, C = 1; S=1

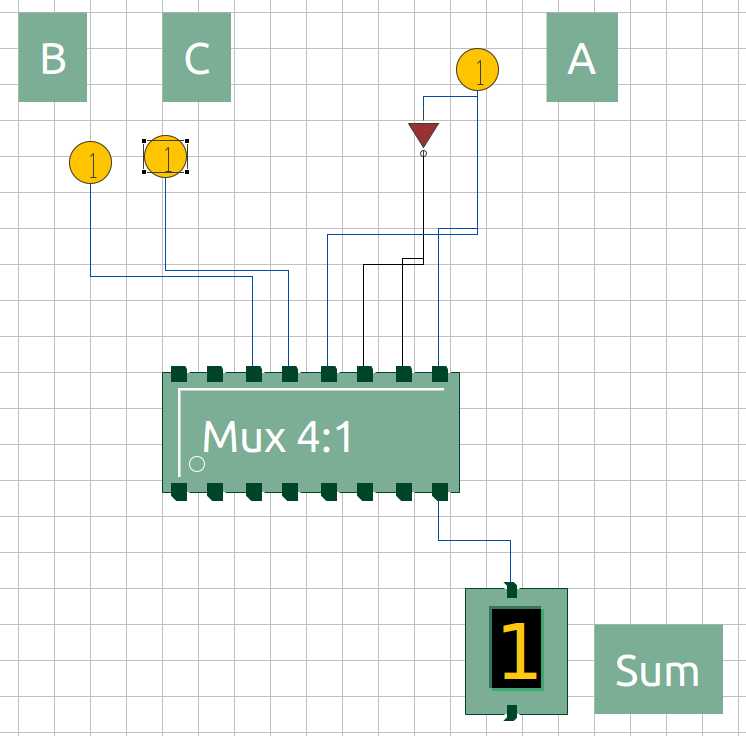
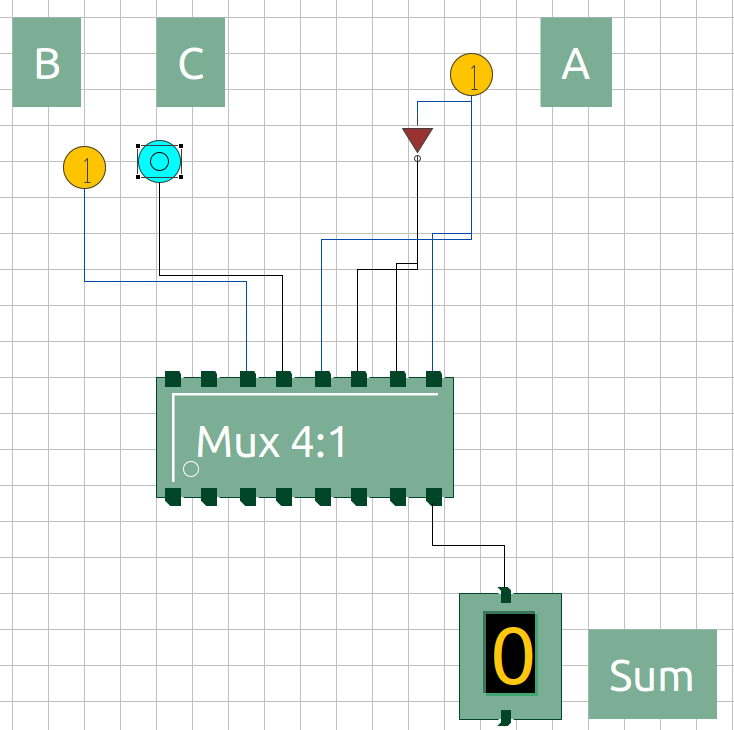
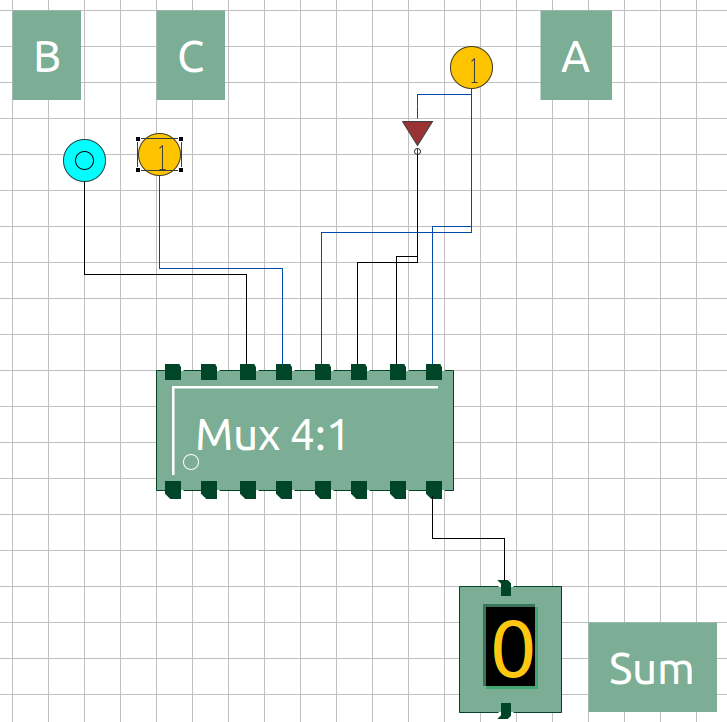
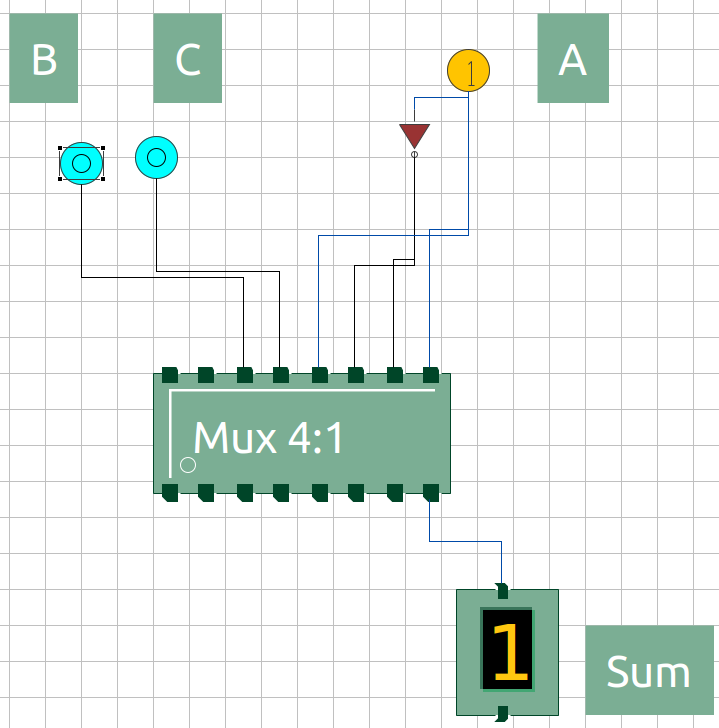
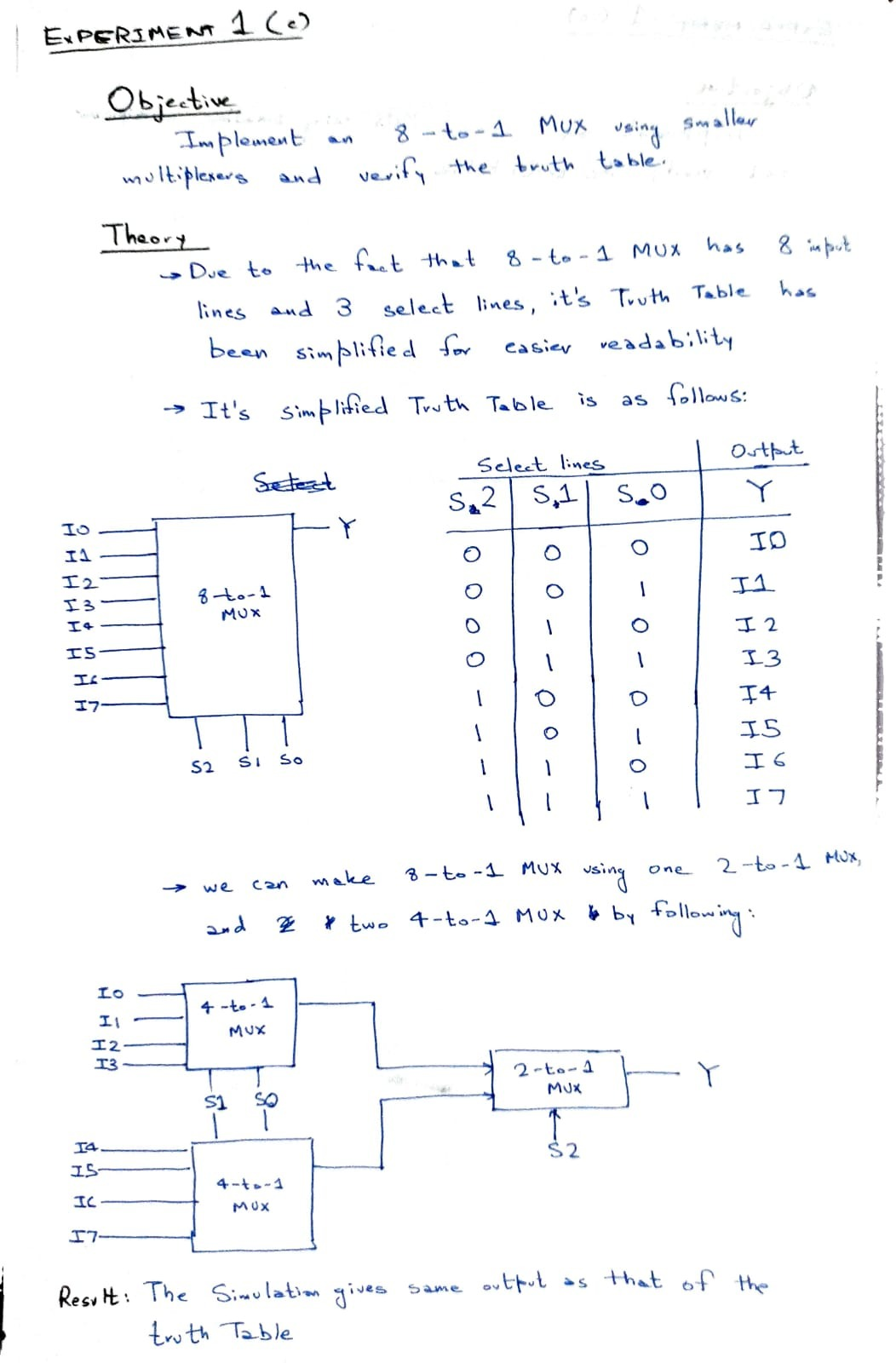


Figure 5: A = 1, B = 0, C = 0; S=1

Figure 6: A = 1, B = 0, C = 1; S=0

Figure 7: A = 1, B = 1, C = 0; S=0

Figure 8: A = 1, B = 1, C = 1; S=1



## Inputs / Outputs:

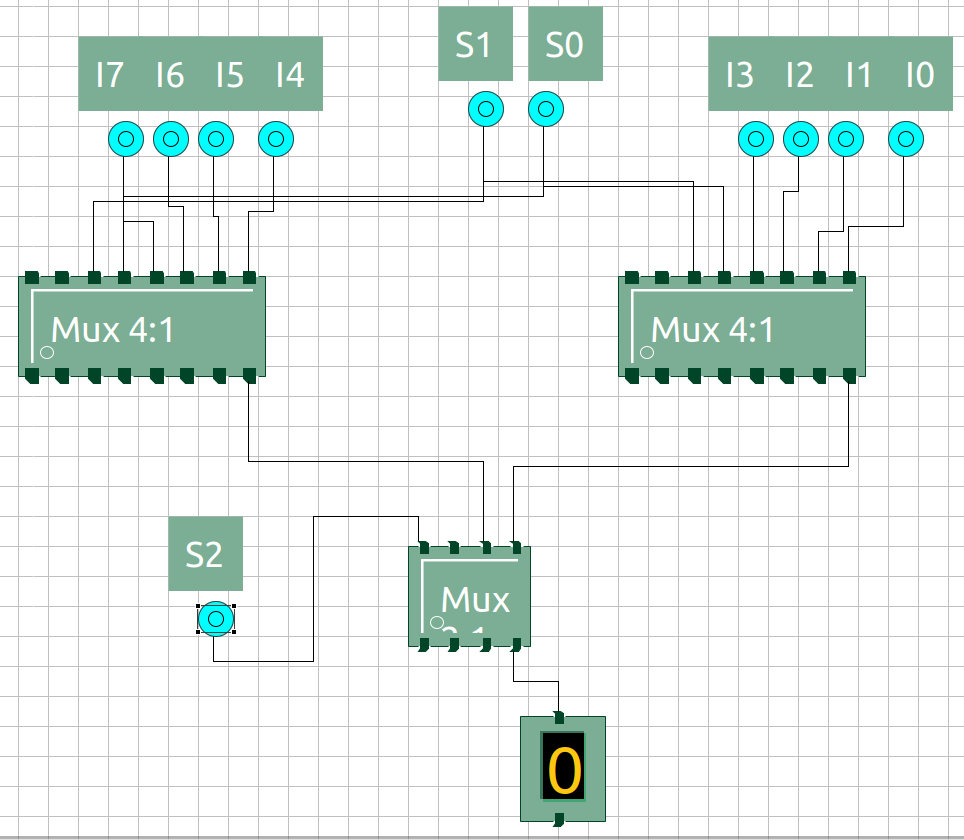
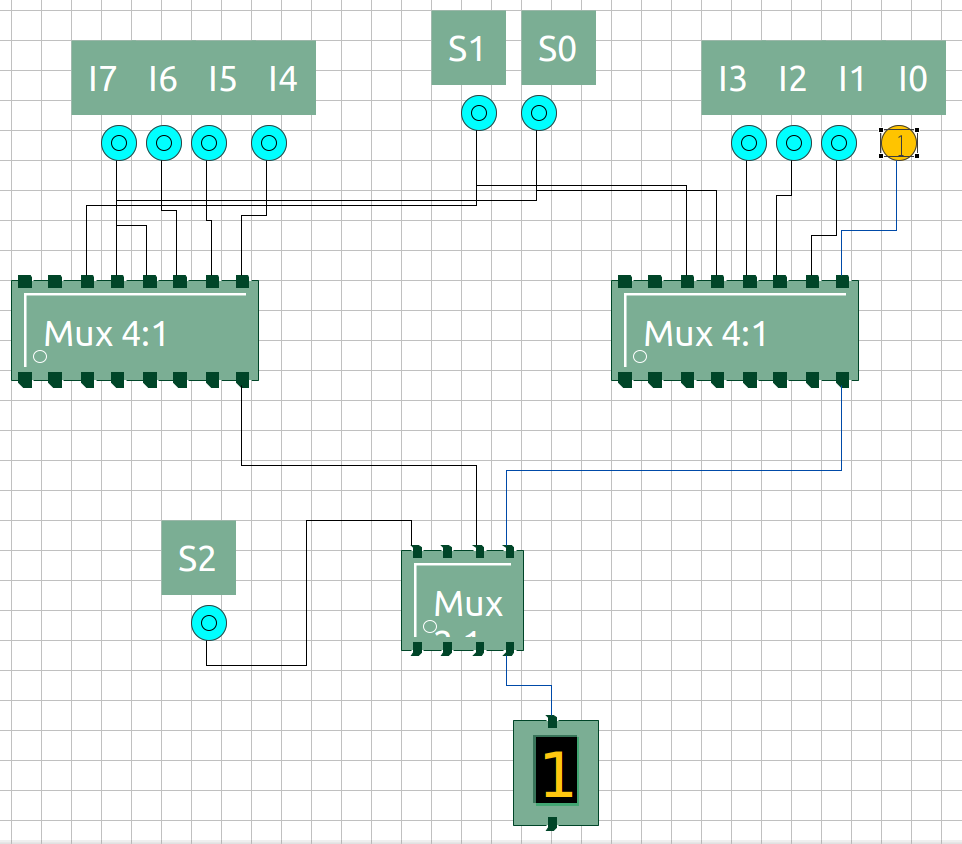
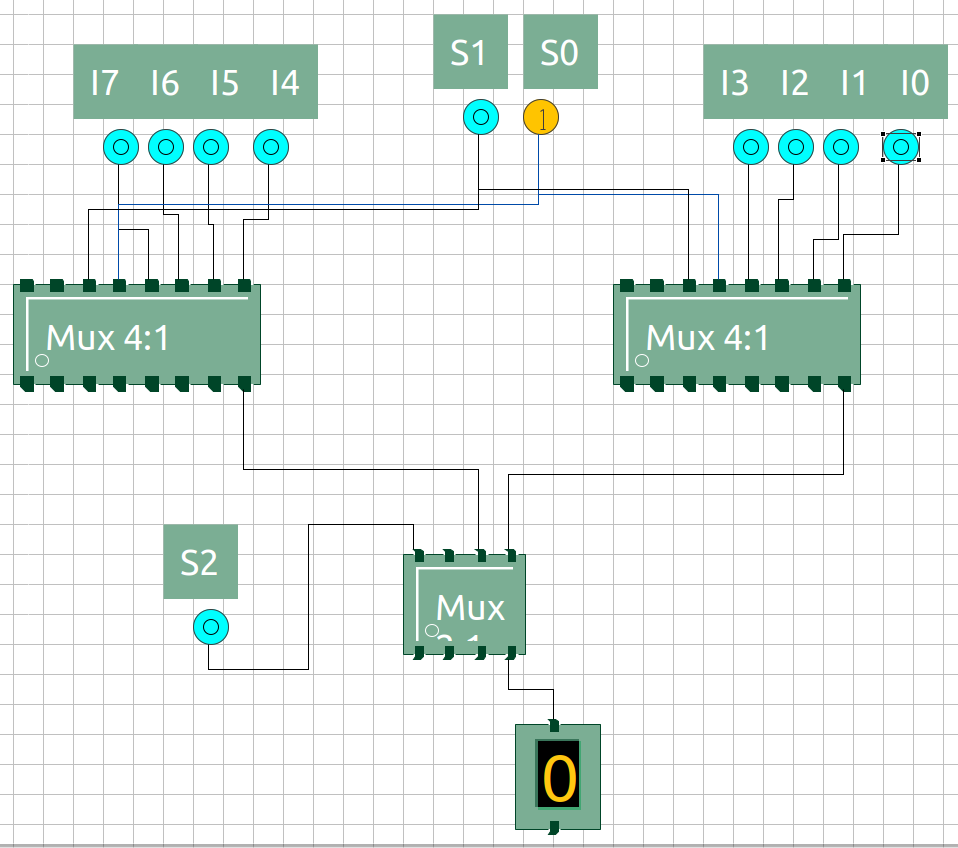
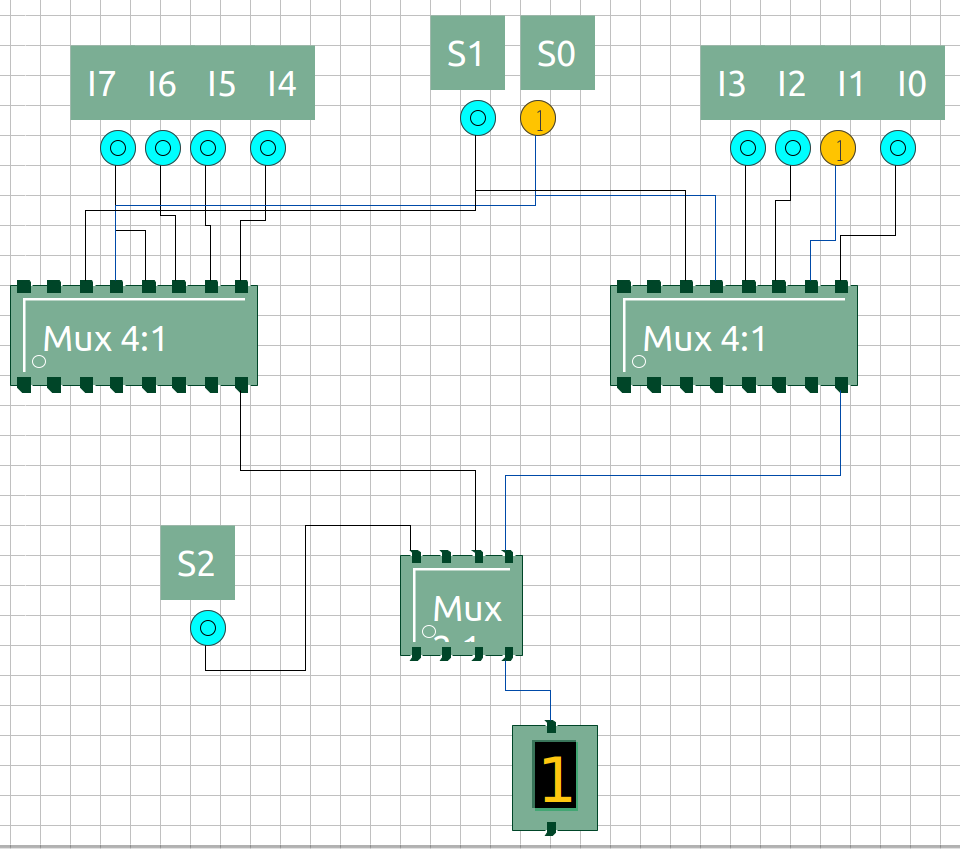


Figure 3: S2 = 0, S1 = 0, S0 = 1, I1 = 0; Y=0

Figure 4: S2 = 0, S1 = 0, S0 = 1, I1 = 1; Y=1

Figure 2: S2 = 0, S1 = 0, S0 = 0, I0 = 1; Y=1

Figure 1: S2 = 0, S1 = 0, S0 = 0, I0 = 0; Y=0

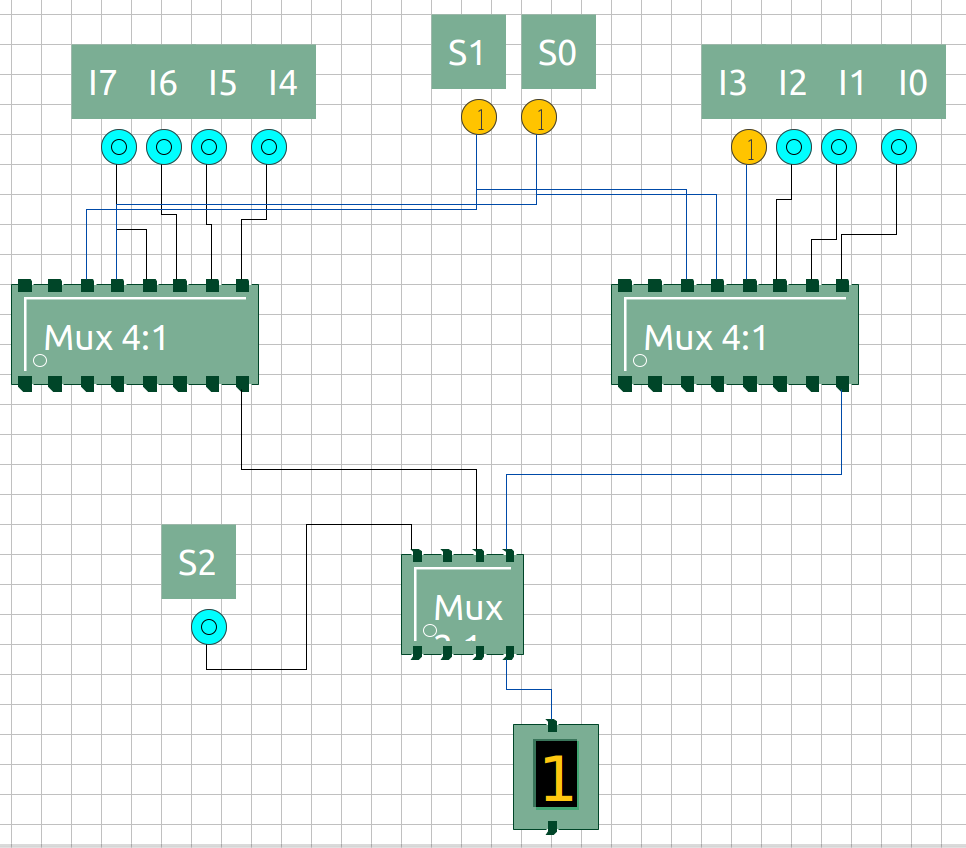
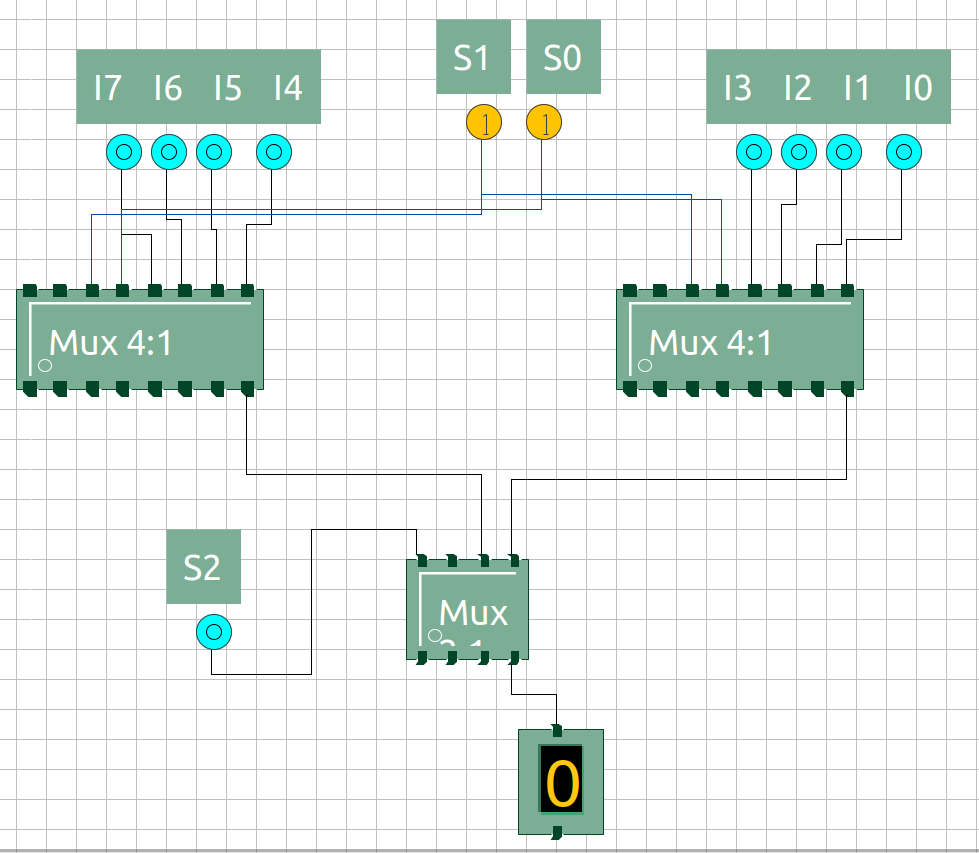
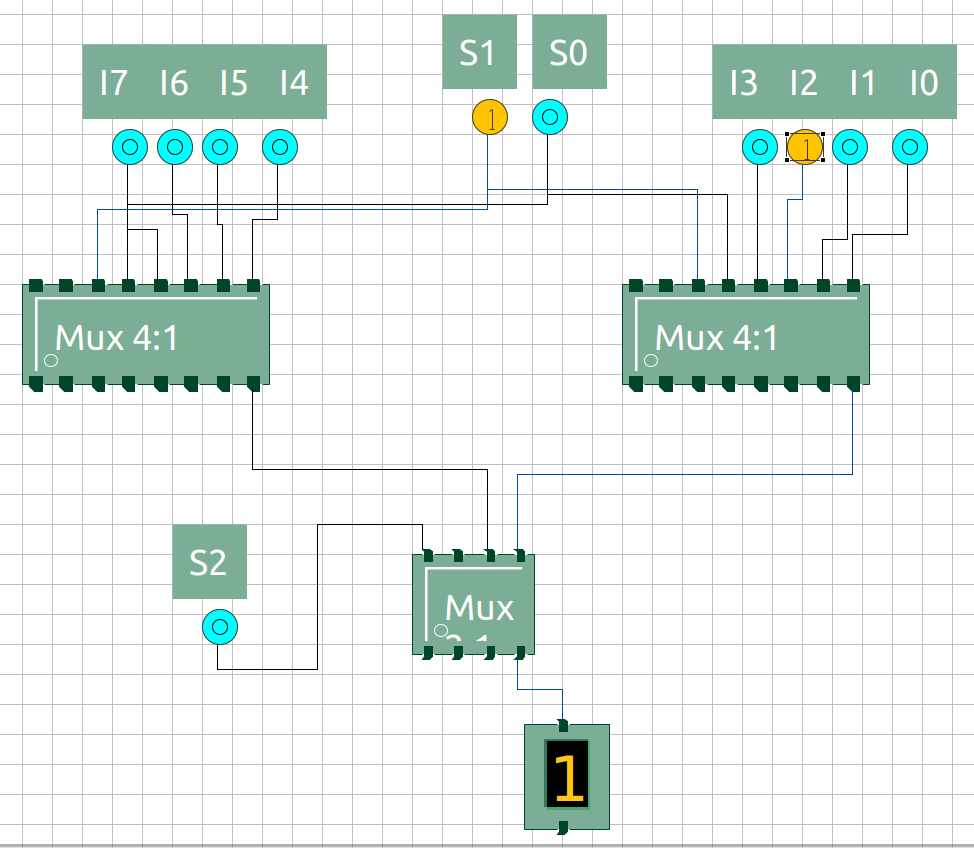
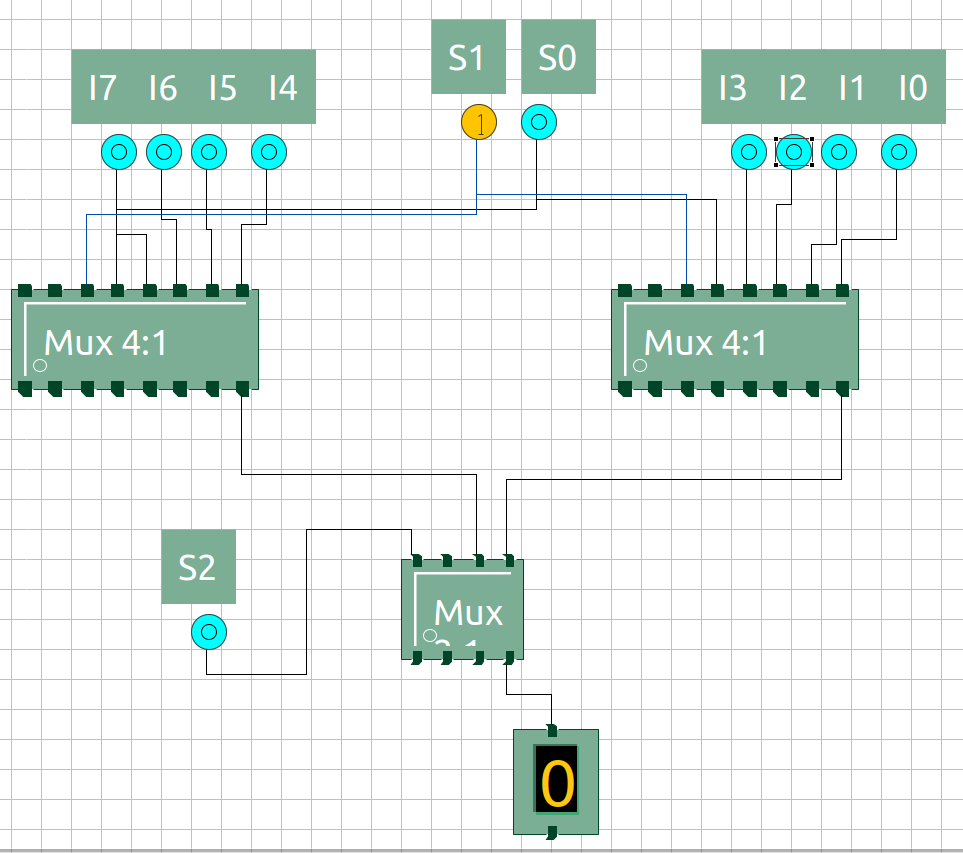


Figure 5: S2 = 0, S1 = 1, S0 = 0, I2 = 0; Y=0

Figure 6: S2 = 0, S1 = 1, S0 = 0, I2 = 1; Y=1

Figure 7: S2 = 0, S1 = 1, S0 = 1, I3 = 0; Y=0

Figure 8: S2 = 0, S1 = 1, S0 = 1, I3 = 1; Y=1

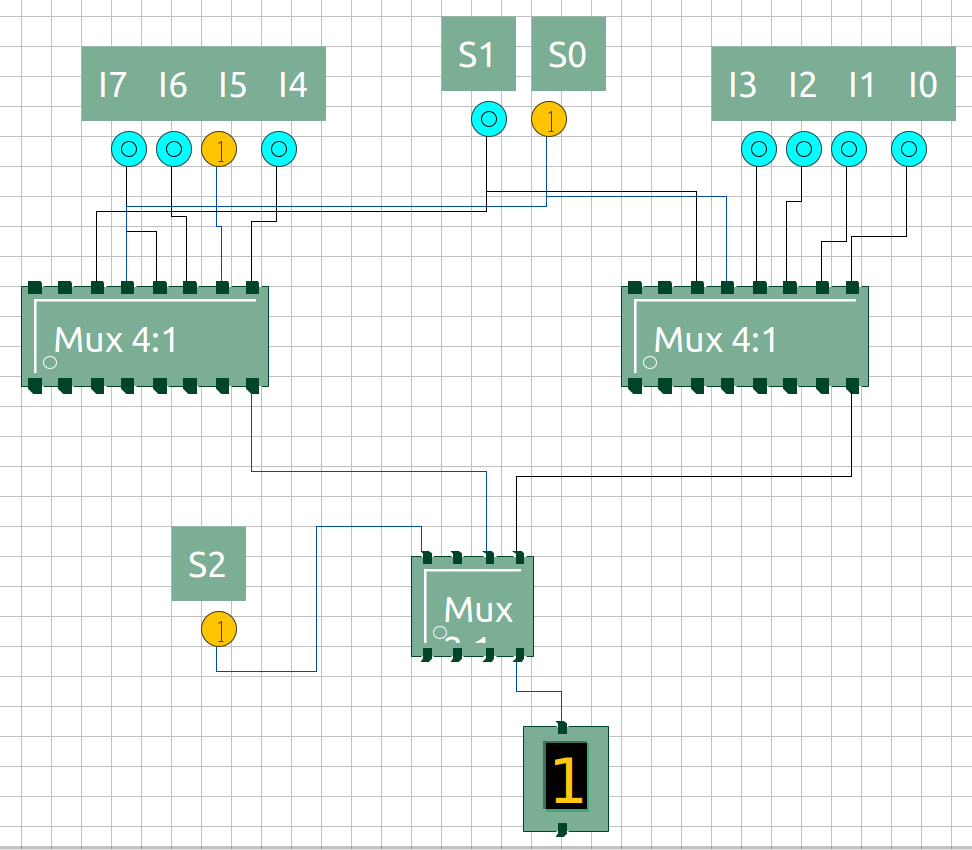
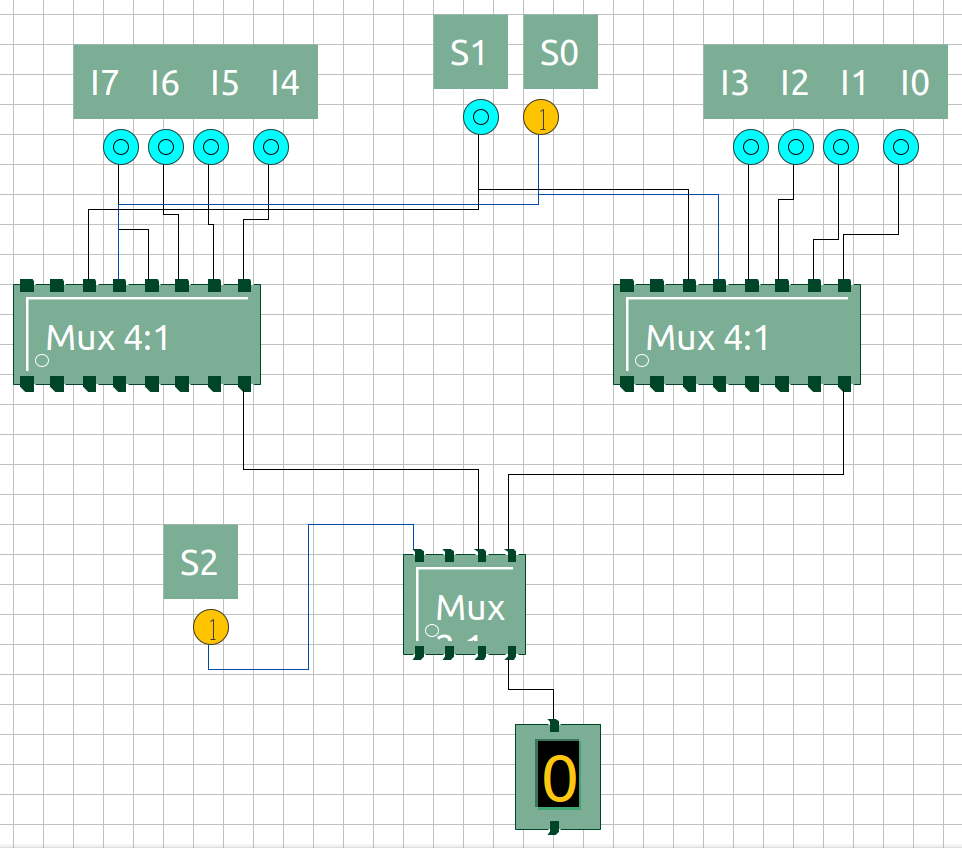
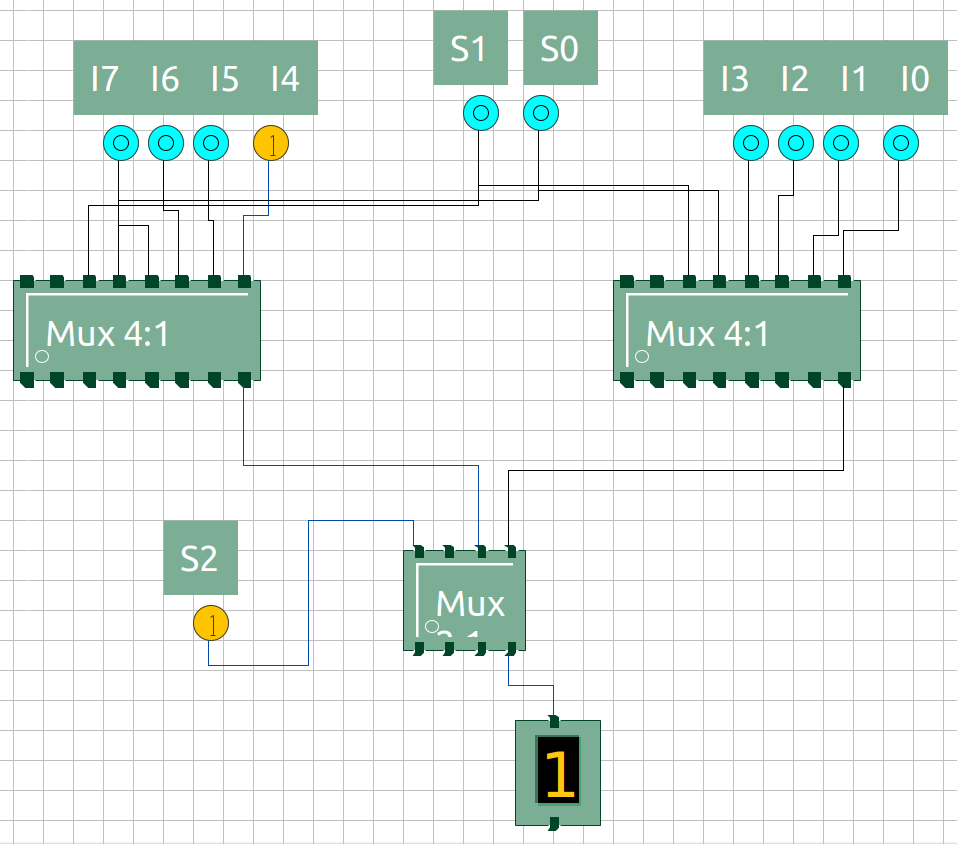
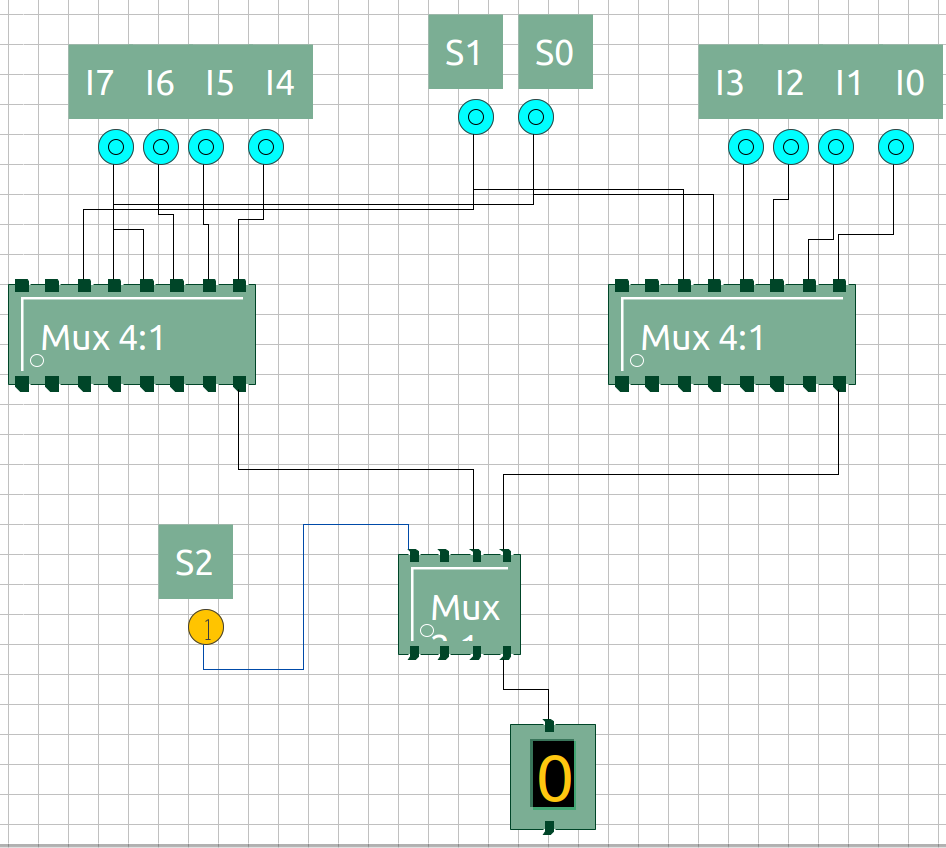


Figure 9: S2 = 1, S1 = 0, S0 = 0, I4 = 0; Y=0

Figure 10: S2 = 1, S1 = 1, S0 = 0, I4 = 1; Y=1

Figure 11: S2 = 1, S1 = 0, S0 = 1, I5 = 0; Y=0

Figure 12: S2 = 1, S1 = 0, S0 = 1, I5 = 1; Y=1

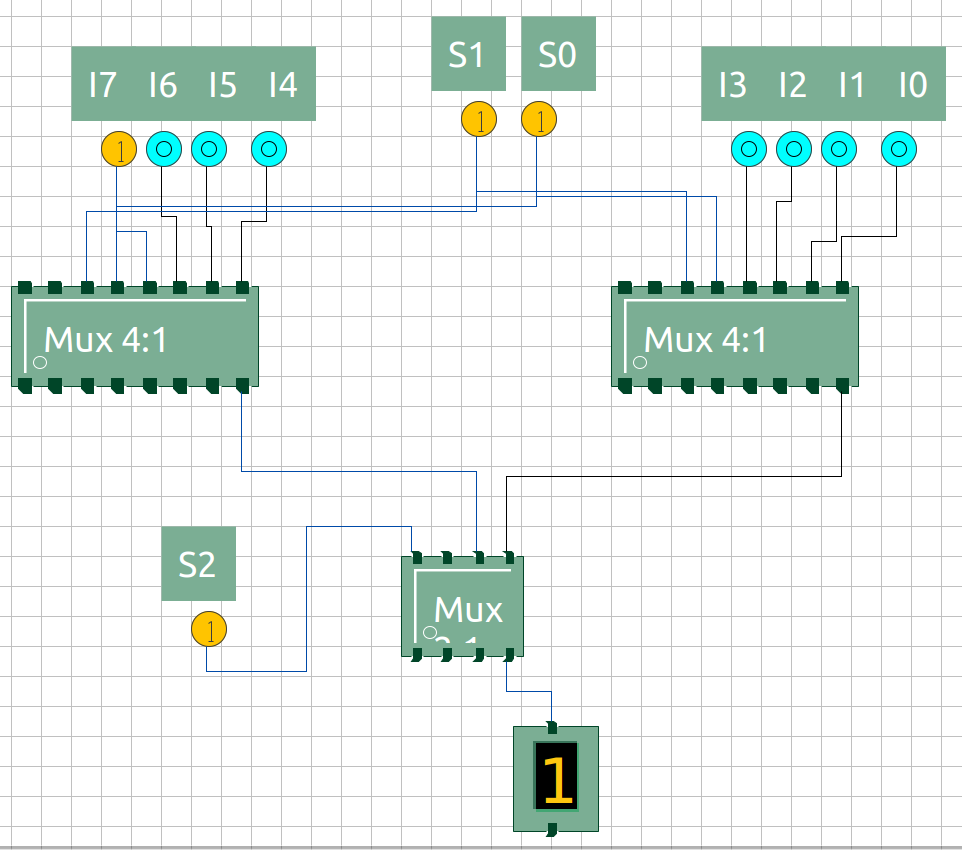
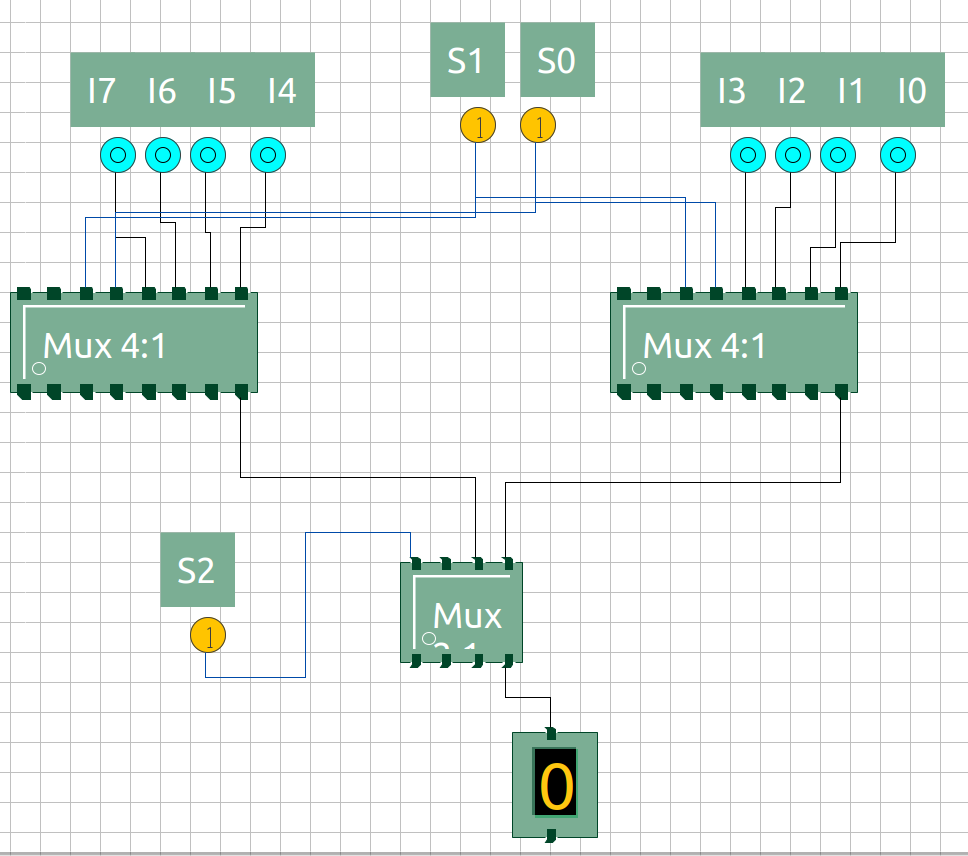
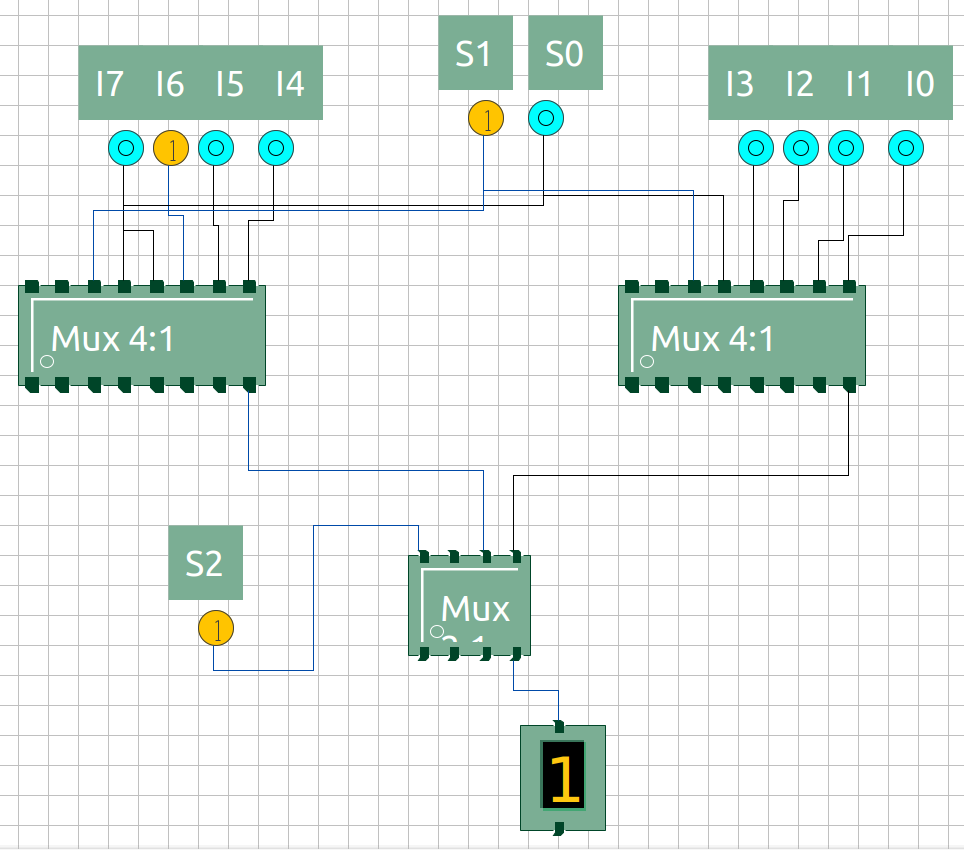
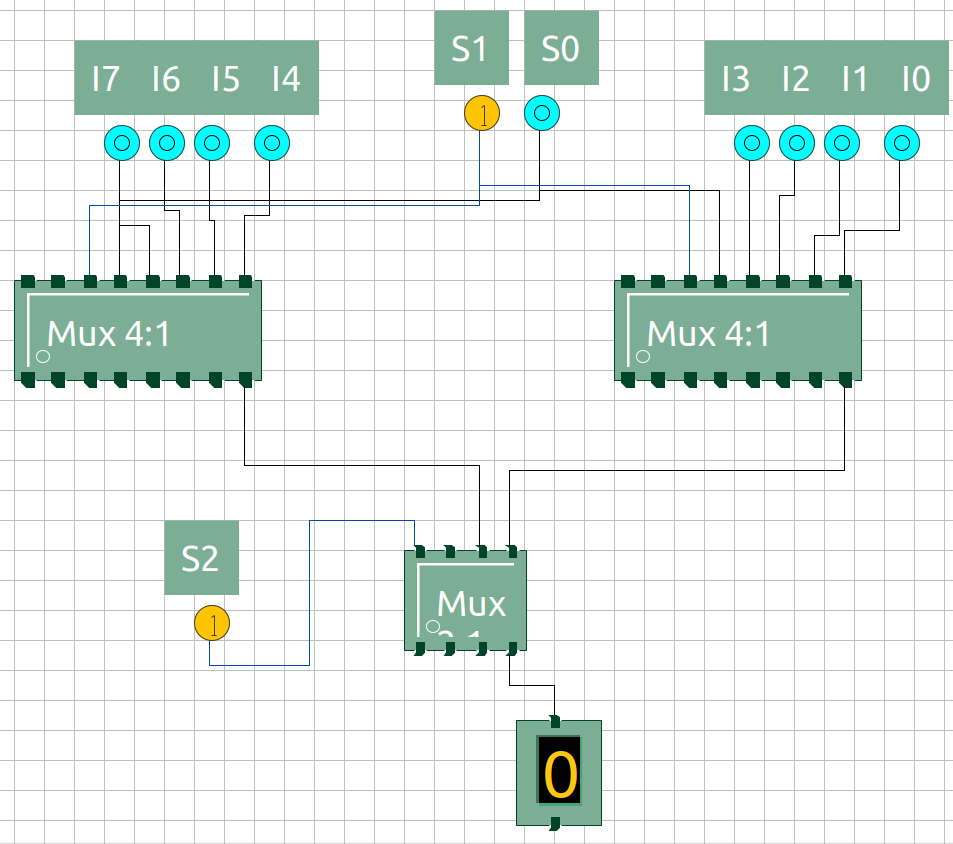
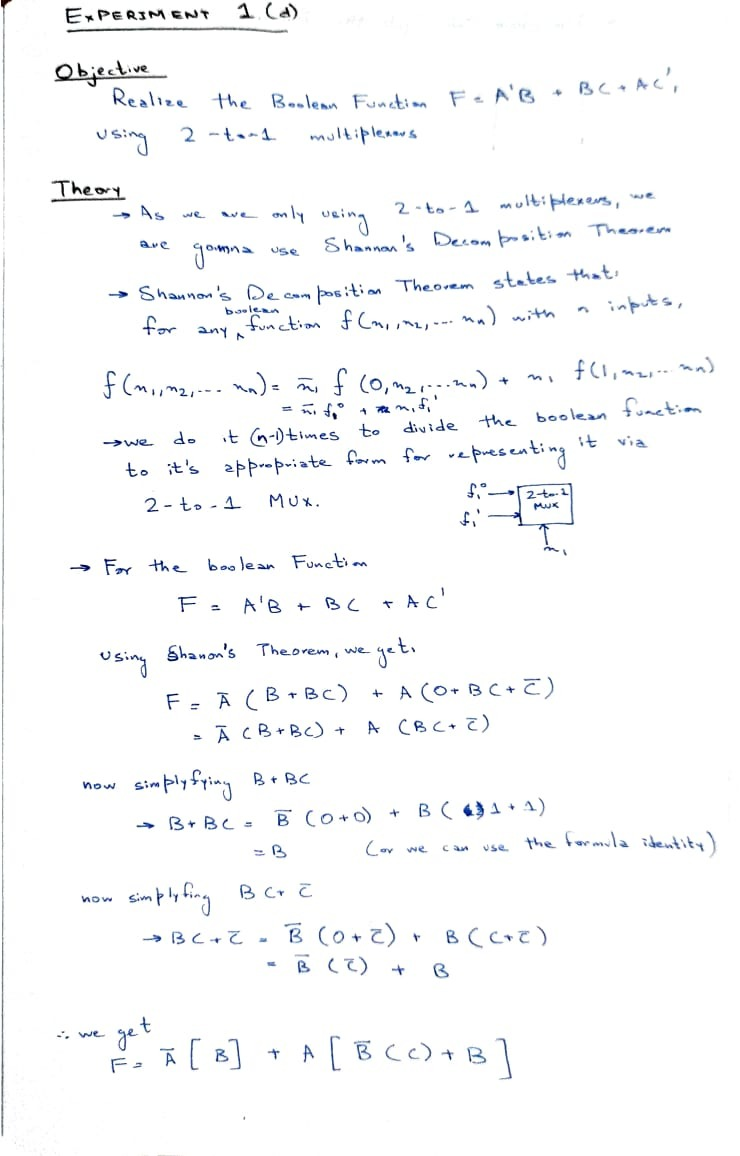


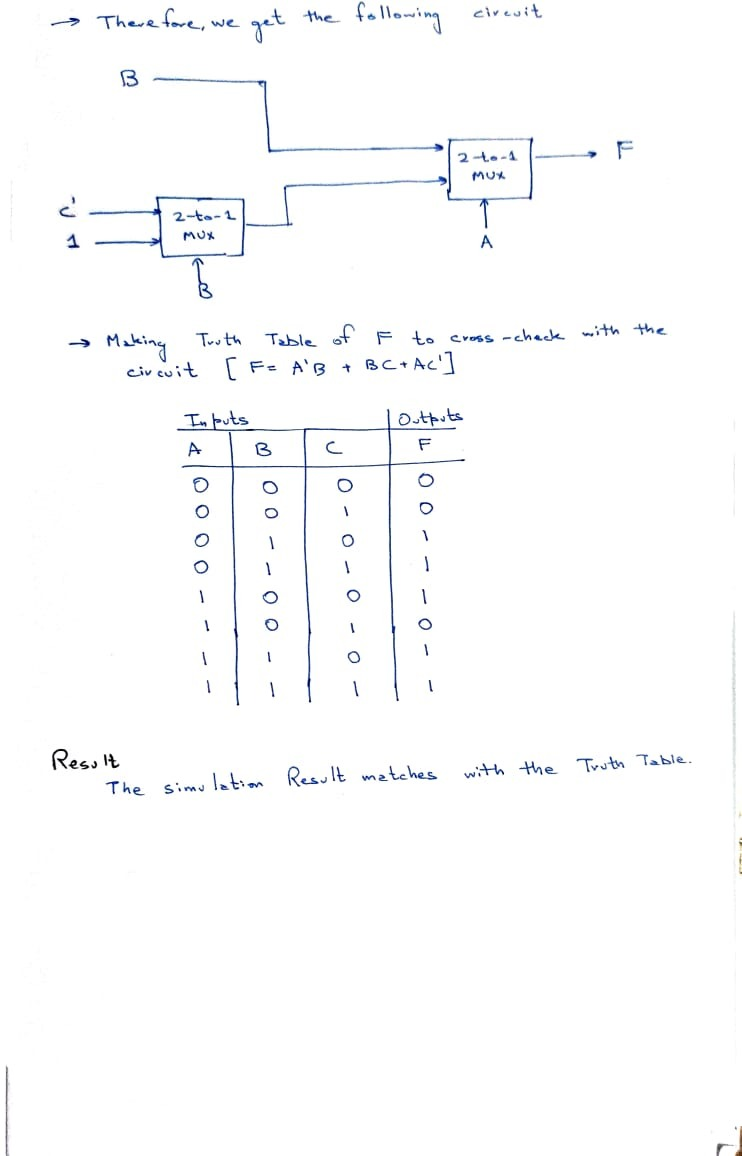
Figure 13: S2 = 1, S1 = 1, S0 = 0, I6 = 0; Y=0

Figure 14: S2 = 1, S1 = 1, S0 = 0, I6 = 1; Y=1

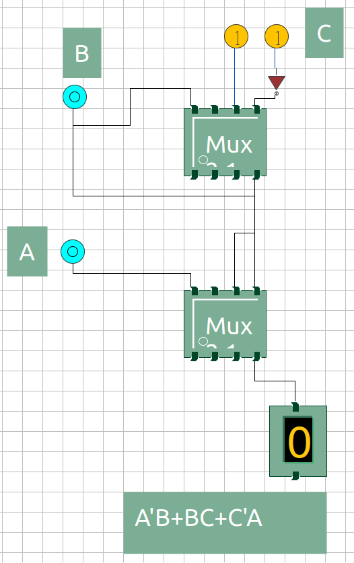
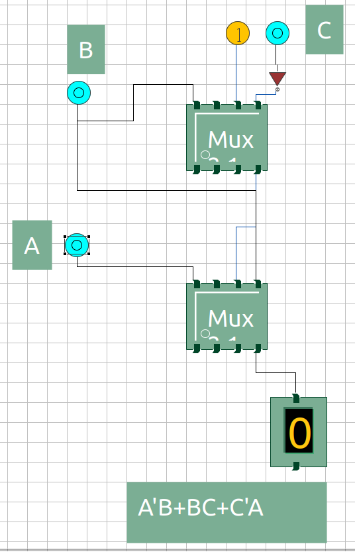
Figure 15: S2 = 1, S1 = 1, S0 = 1, I7 = 0; Y=0

Figure 16: S2 = 1, S1 = 1, S0 = 1, I7 = 1; Y=1





## Inputs / Outputs:



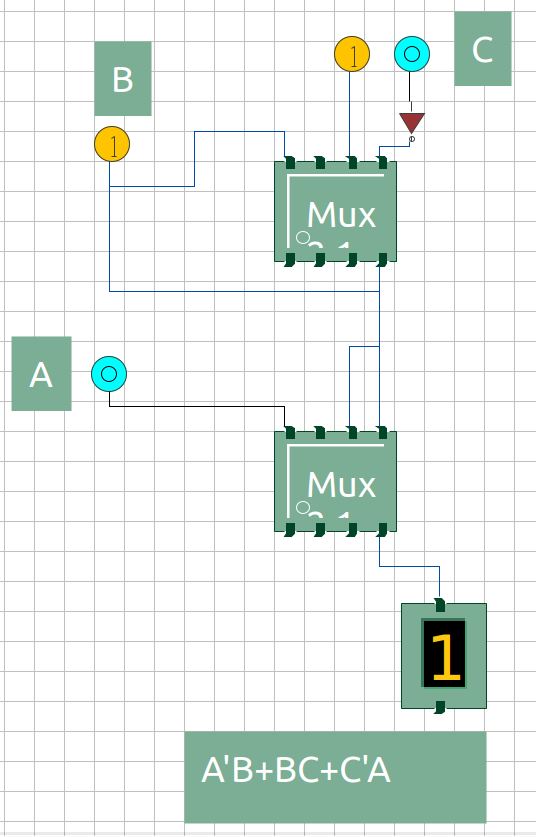
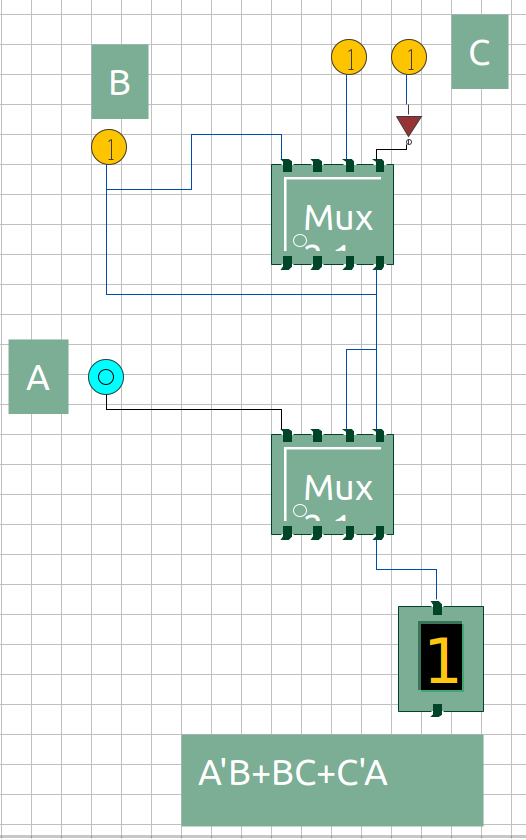


Figure 4: A = 0, B = 1, C = 1; Y=1

Figure 3: A = 0, B = 1, C = 0; Y=1

Figure 1: A = 0, B = 0, C = 0; Y=0

Figure 2: A = 0, B = 0, C = 1; Y=0

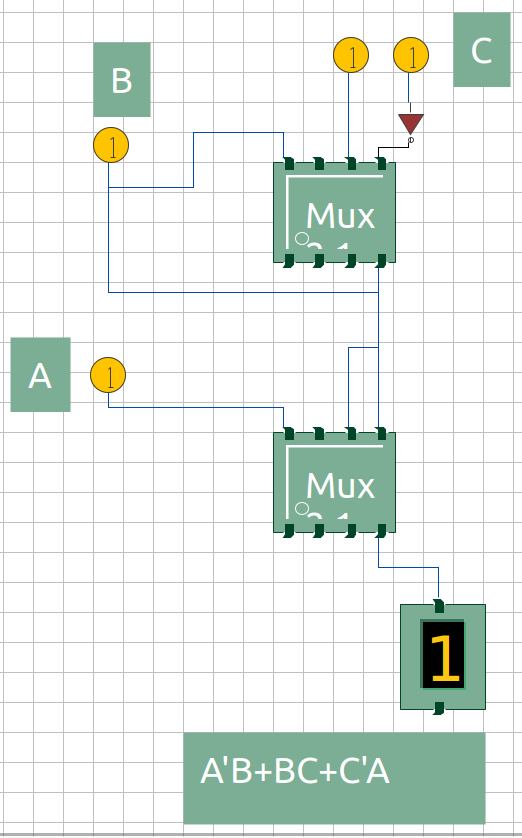
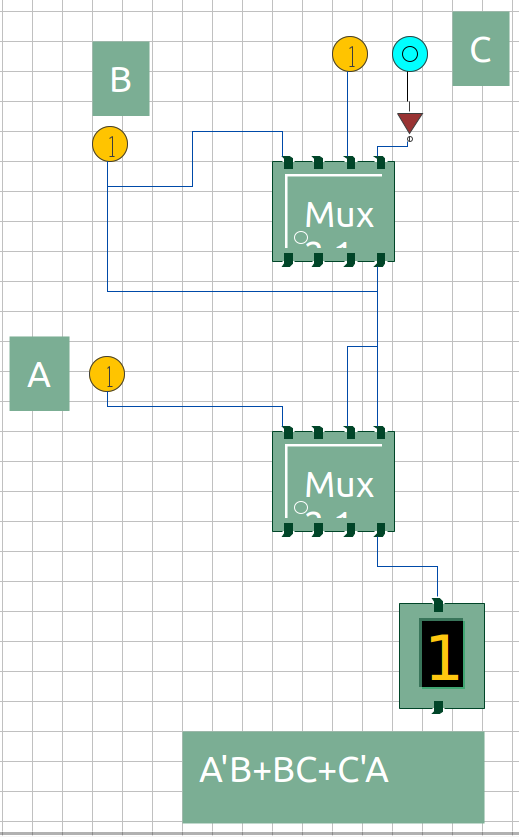
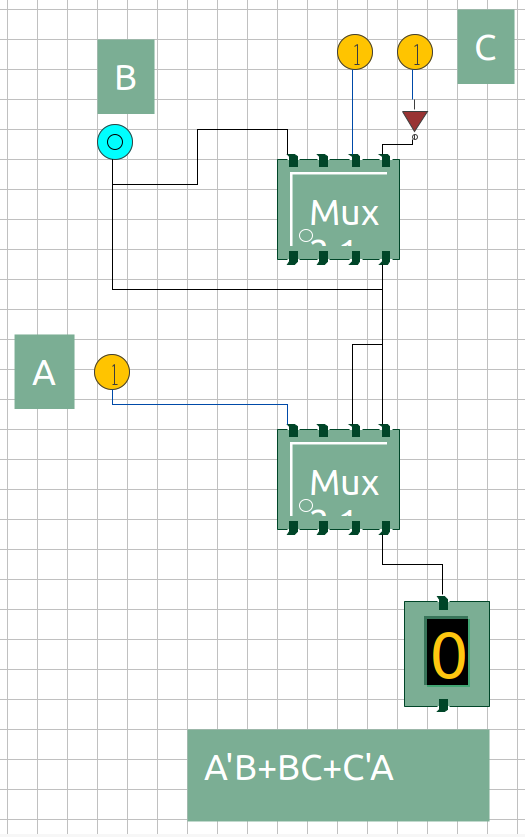
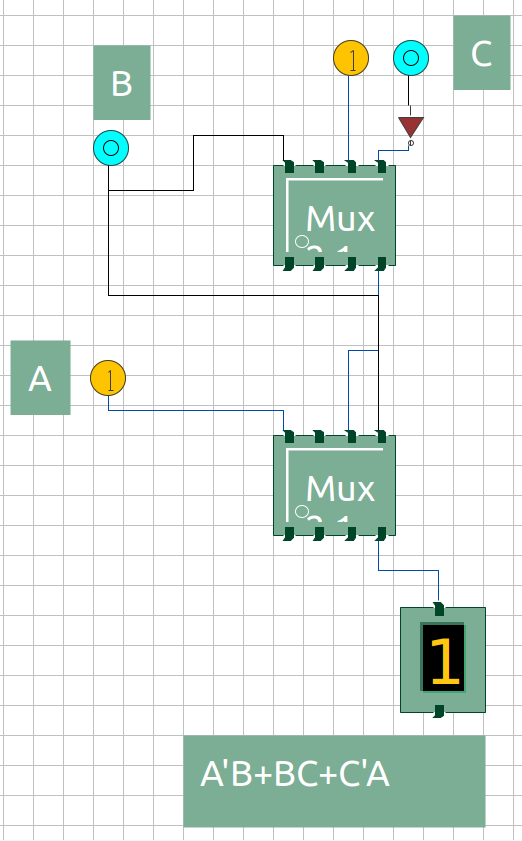


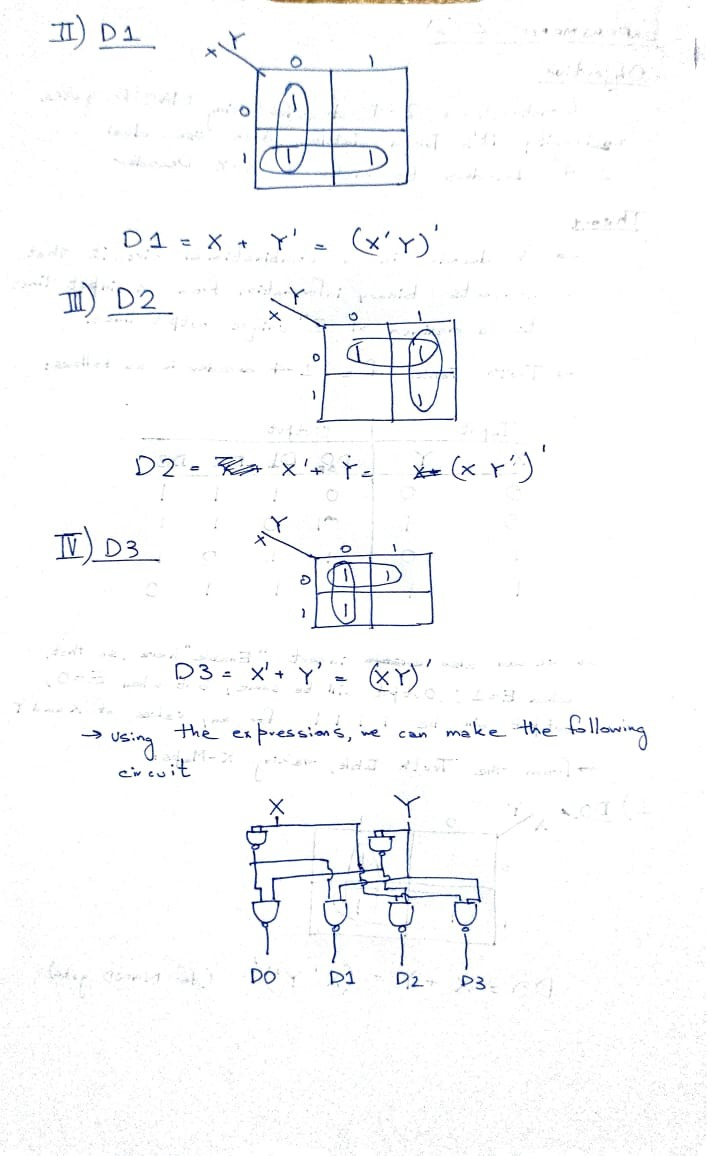
Figure 5: A = 1, B = 0, C = 0; Y=1

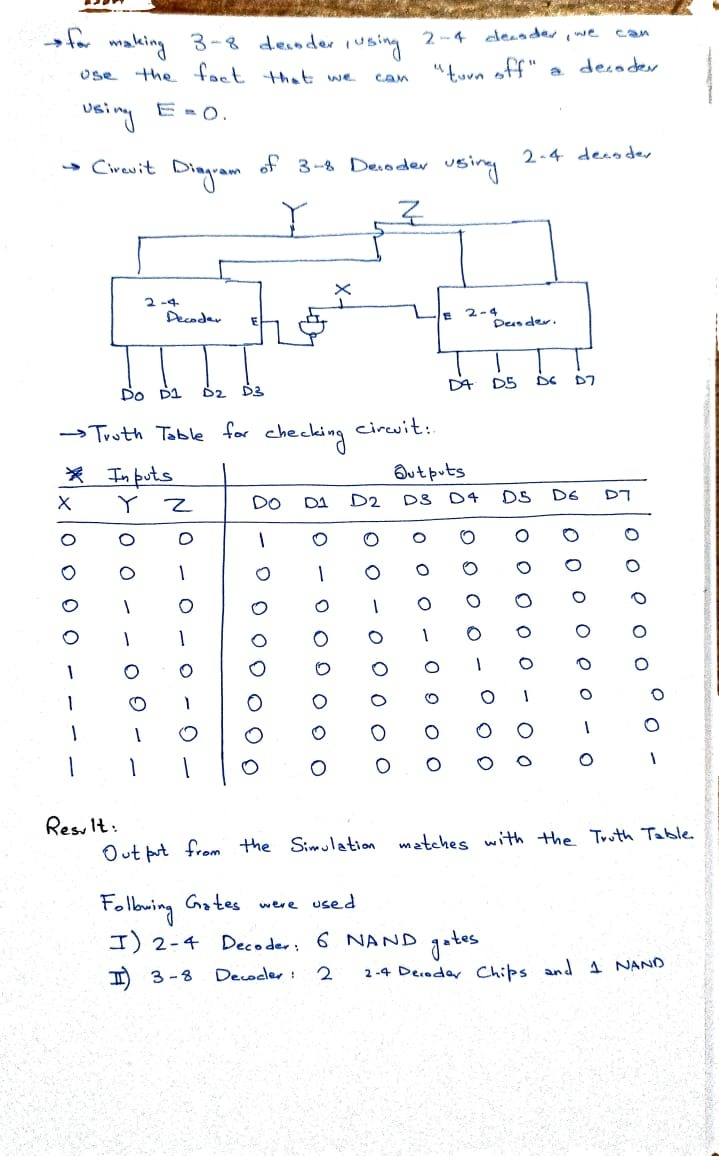
Figure 6: A = 1, B = 0, C = 1; Y=0

Figure 7: A = 1, B = 1, C = 0; Y=1

Figure 8: A = 1, B = 1, C = 1; Y=1







## Inputs / Outputs:

1. 2-4 Decoder

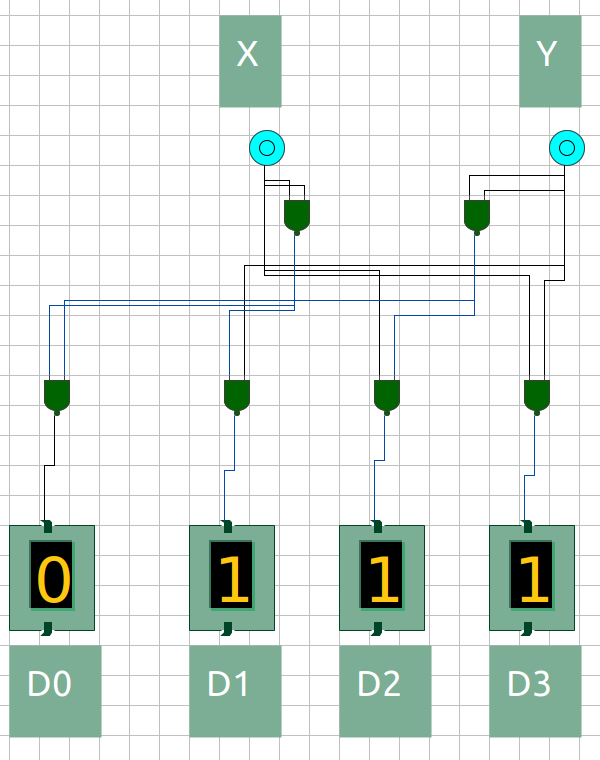
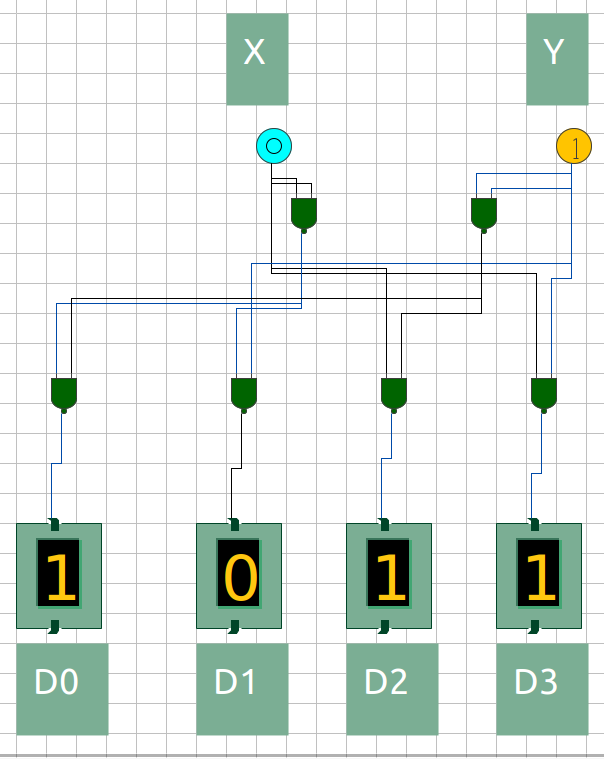
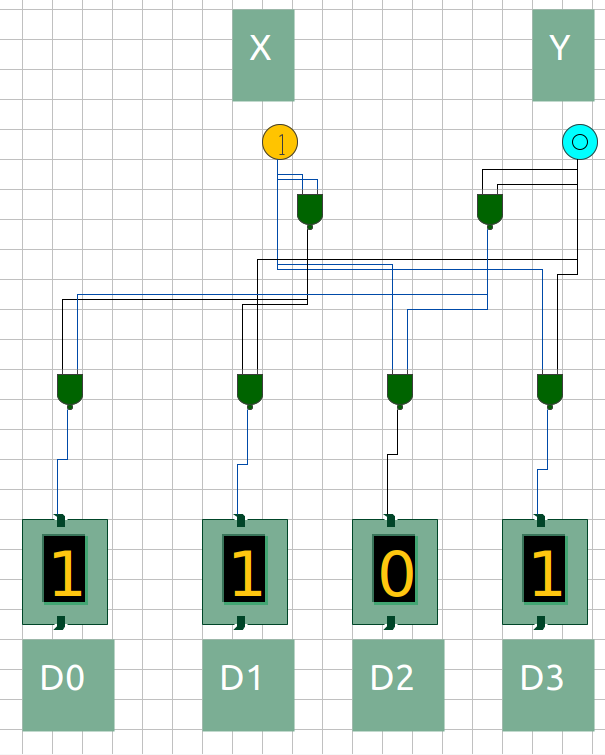
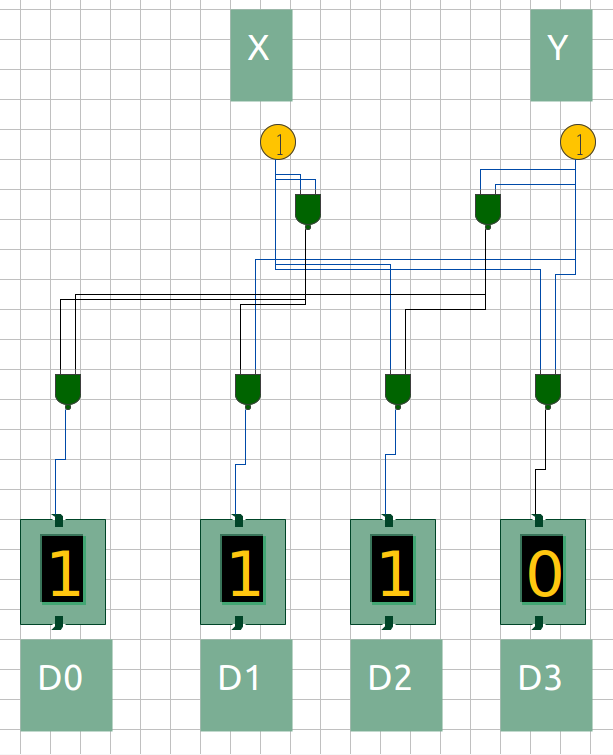


Figure 4: : X = 1, Y = 1; D0 = 1, D1 = 1, D2 = 1, D3 = 0

Figure 3: X = 1, Y = 0; D0 = 1, D1 = 1, D2 = 0, D3 = 1

Figure 2: X = 0, Y = 1; D0 = 1, D1 = 0, D2 = 1, D3 = 1

Figure 1: X = 0, Y = 0; D0 = 0, D1 = 1, D2 = 1, D3 = 1

1. 3-8 Decoder using Dual 2-4 Decoder

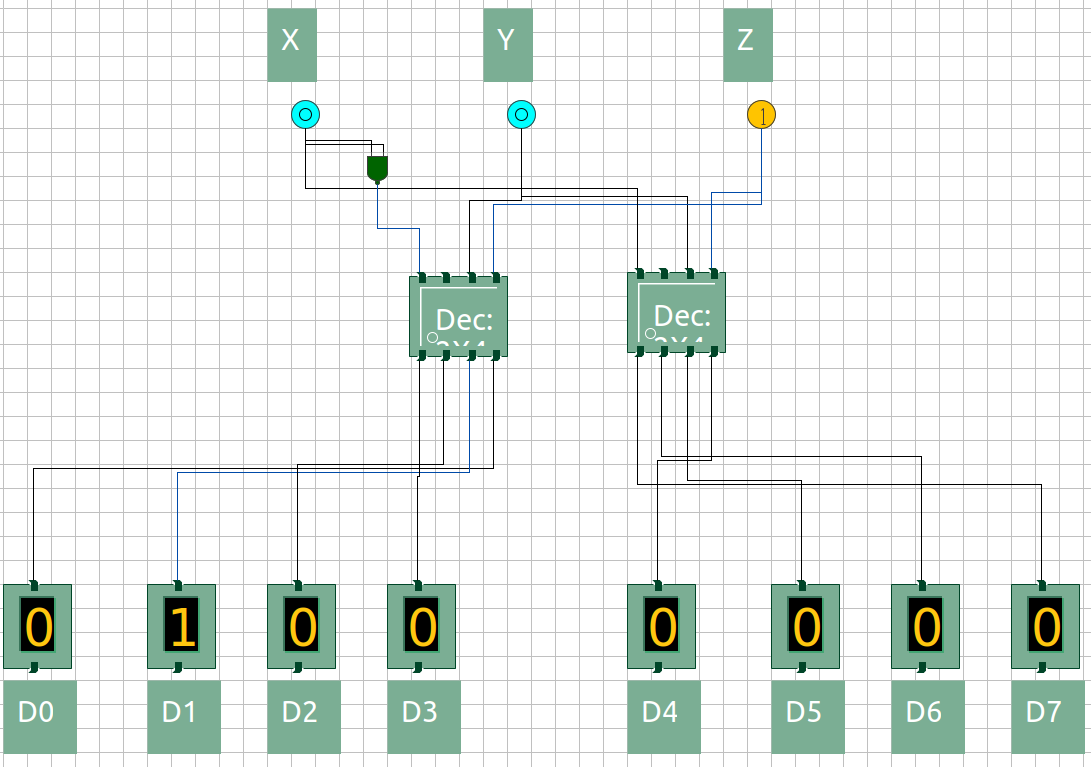
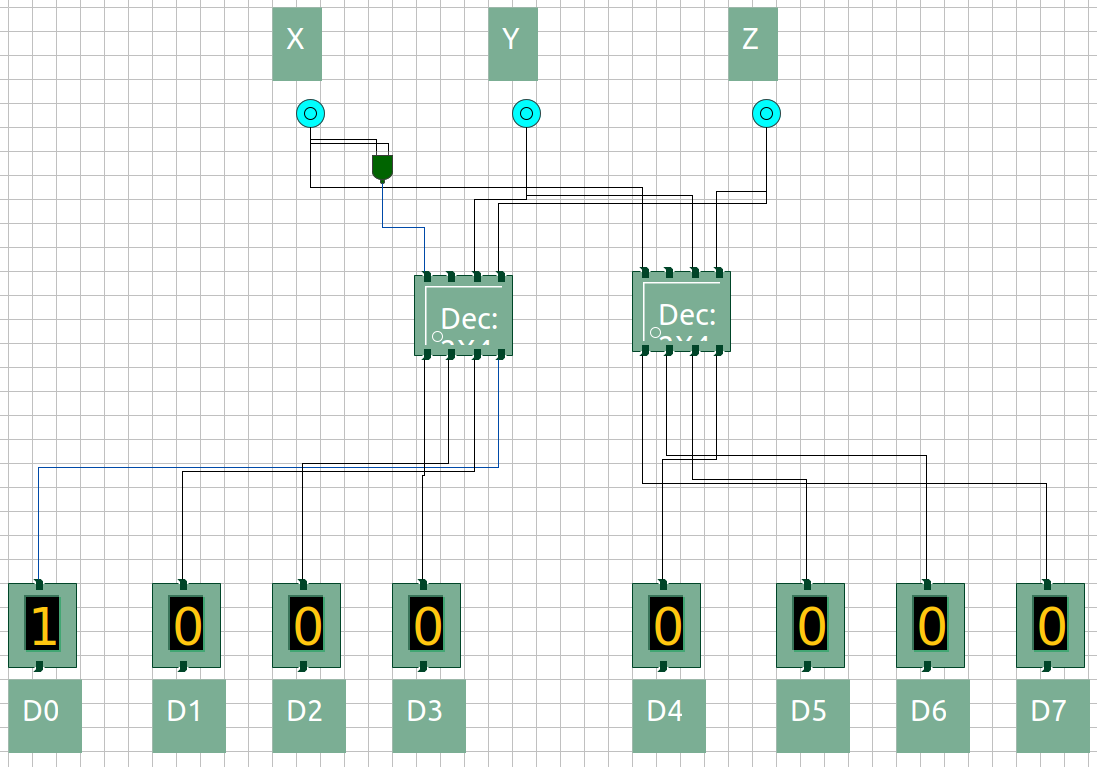


Figure 1: X = 0, Y = 0, Z = 0

Figure 2: X = 0, Y = 0, Z = 1

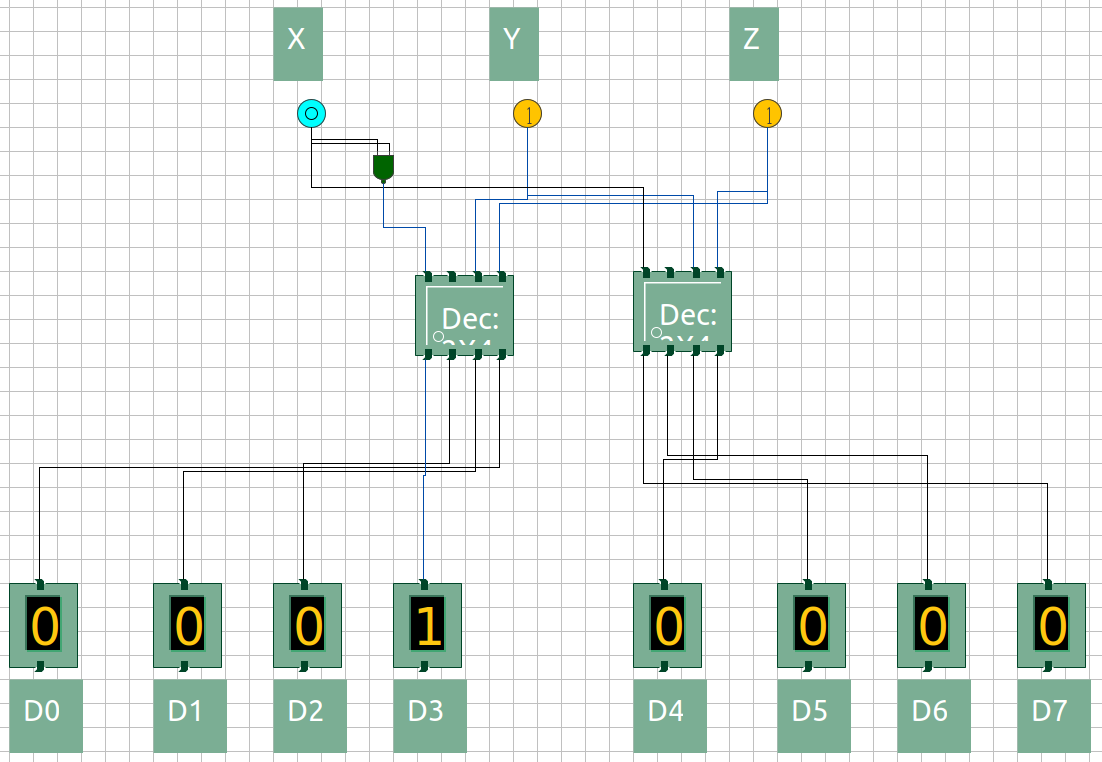
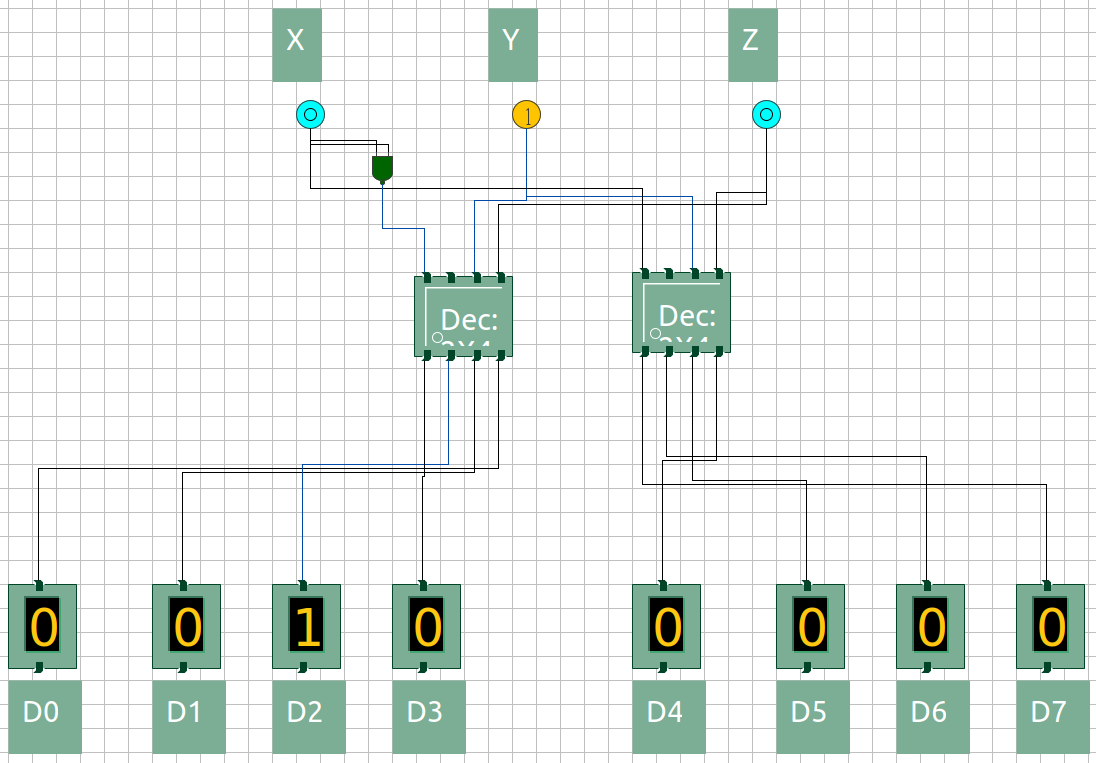


Figure 3: X = 0, Y = 1, Z = 0

Figure 4: X = 0, Y = 1, Z = 1

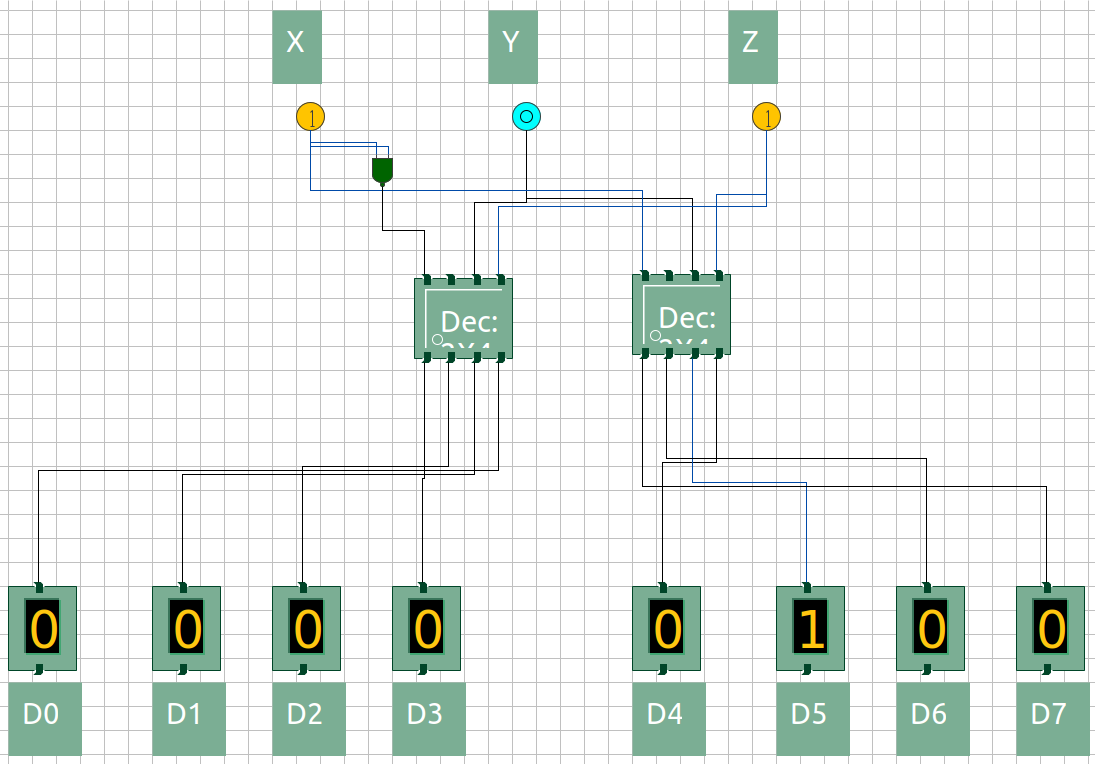
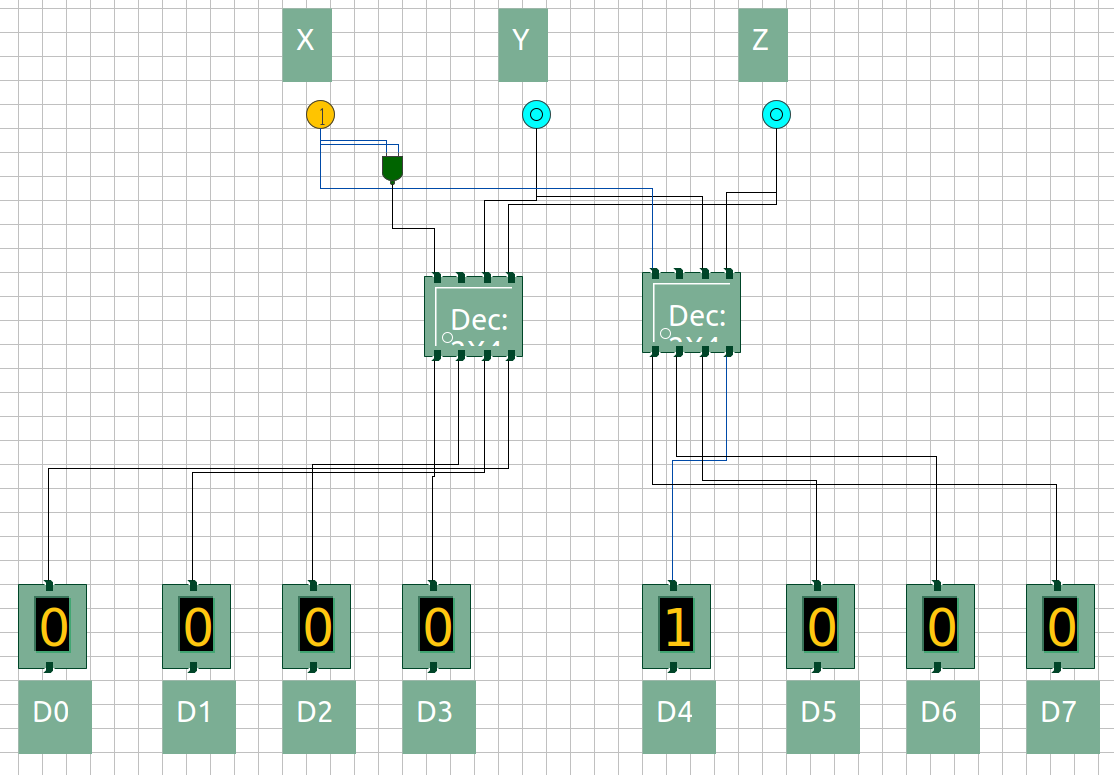


Figure 5: X = 1, Y = 0, Z = 0

Figure 6: X = 1, Y = 0, Z = 1

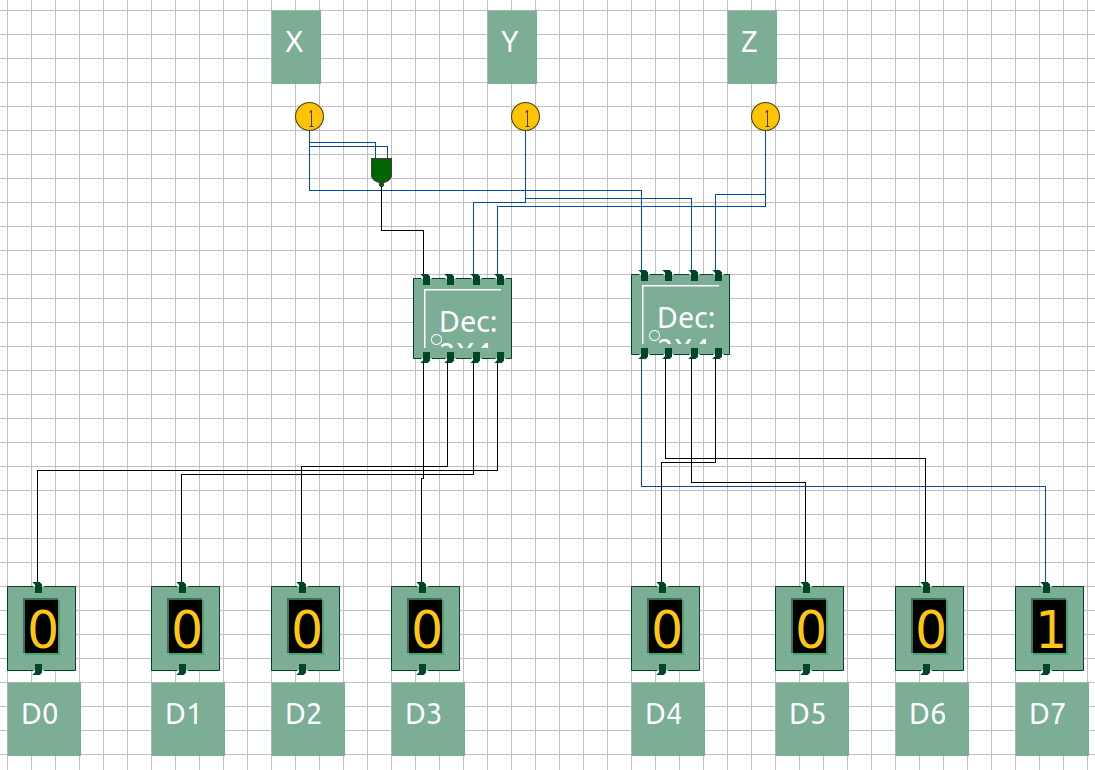
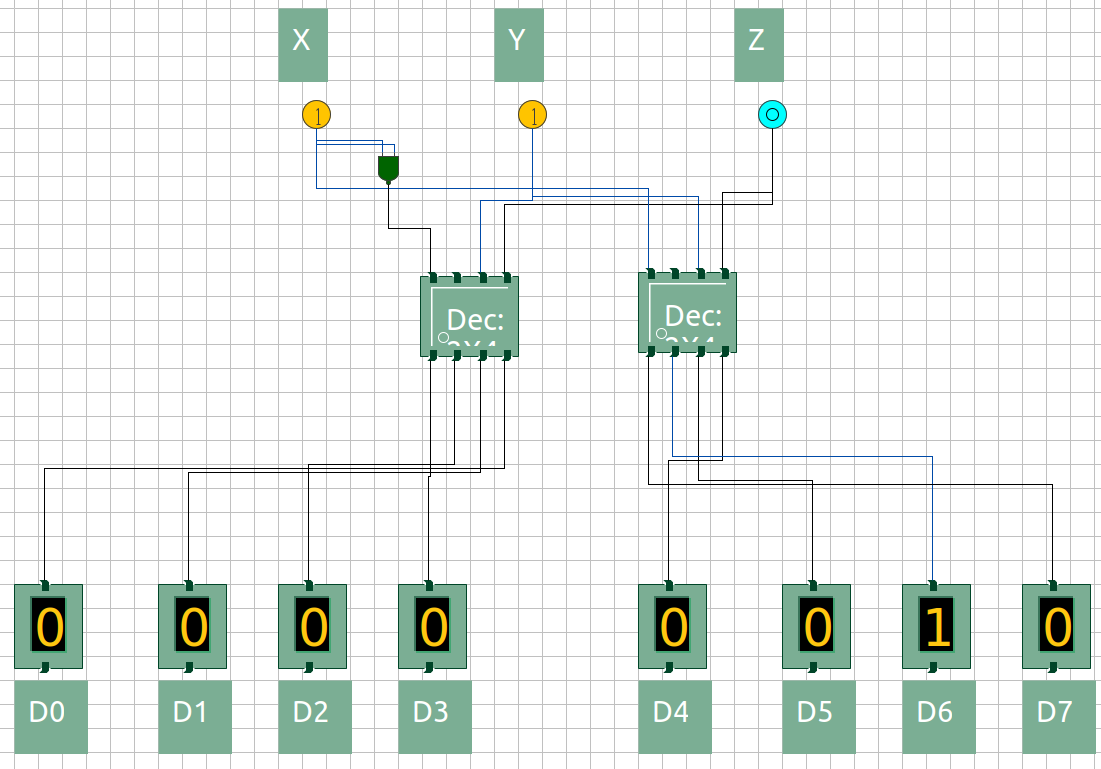
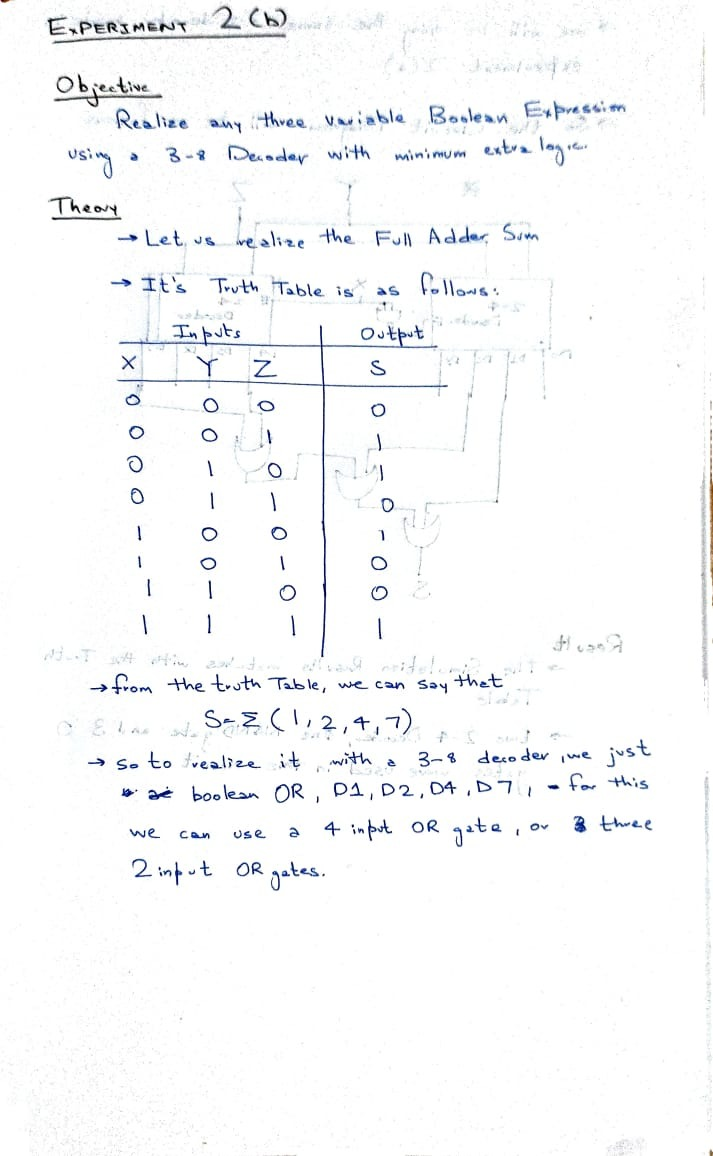
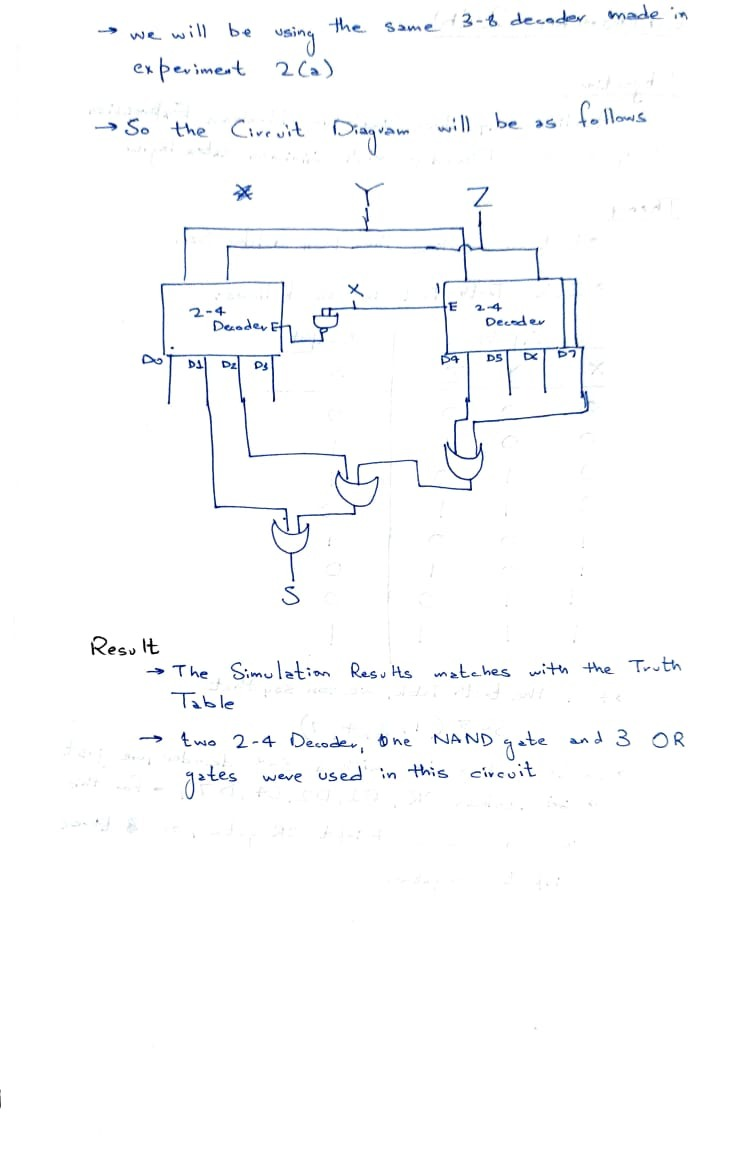


Figure 7: X = 1, Y = 1, Z = 0

Figure 8: X = 1, Y = 1, Z = 1





## Inputs / Outputs:

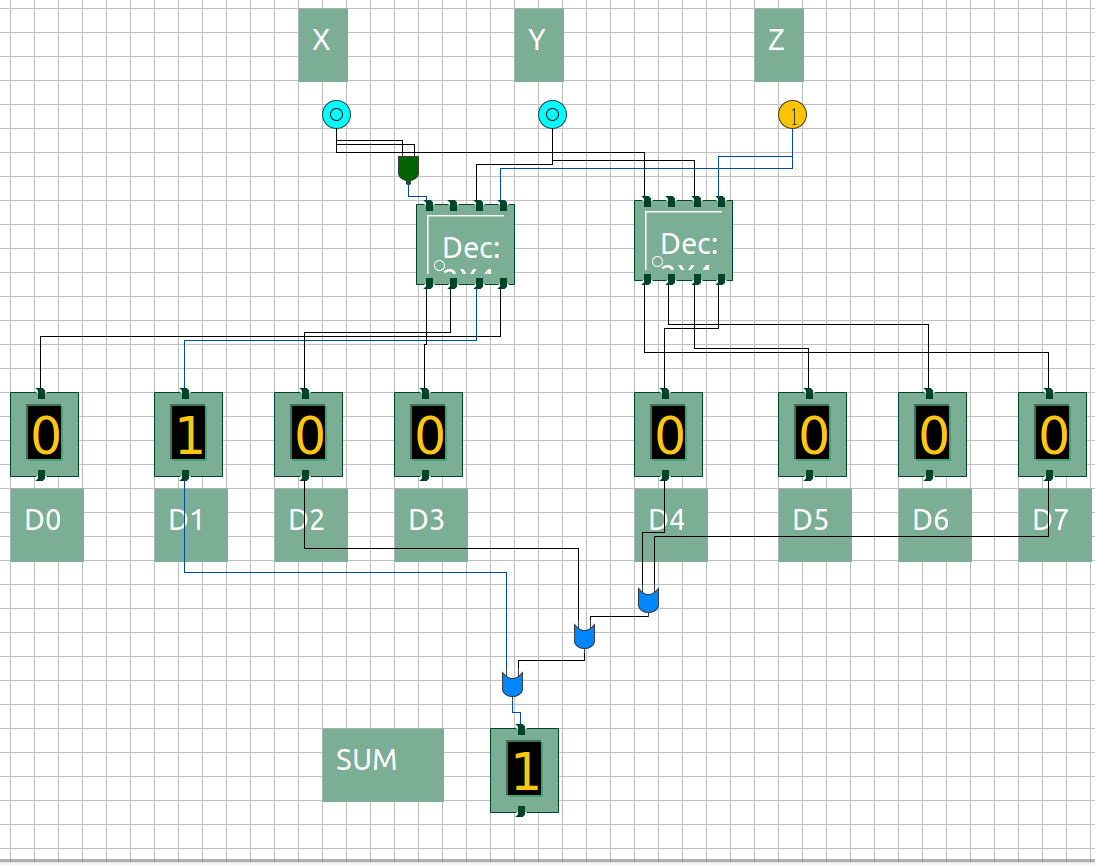
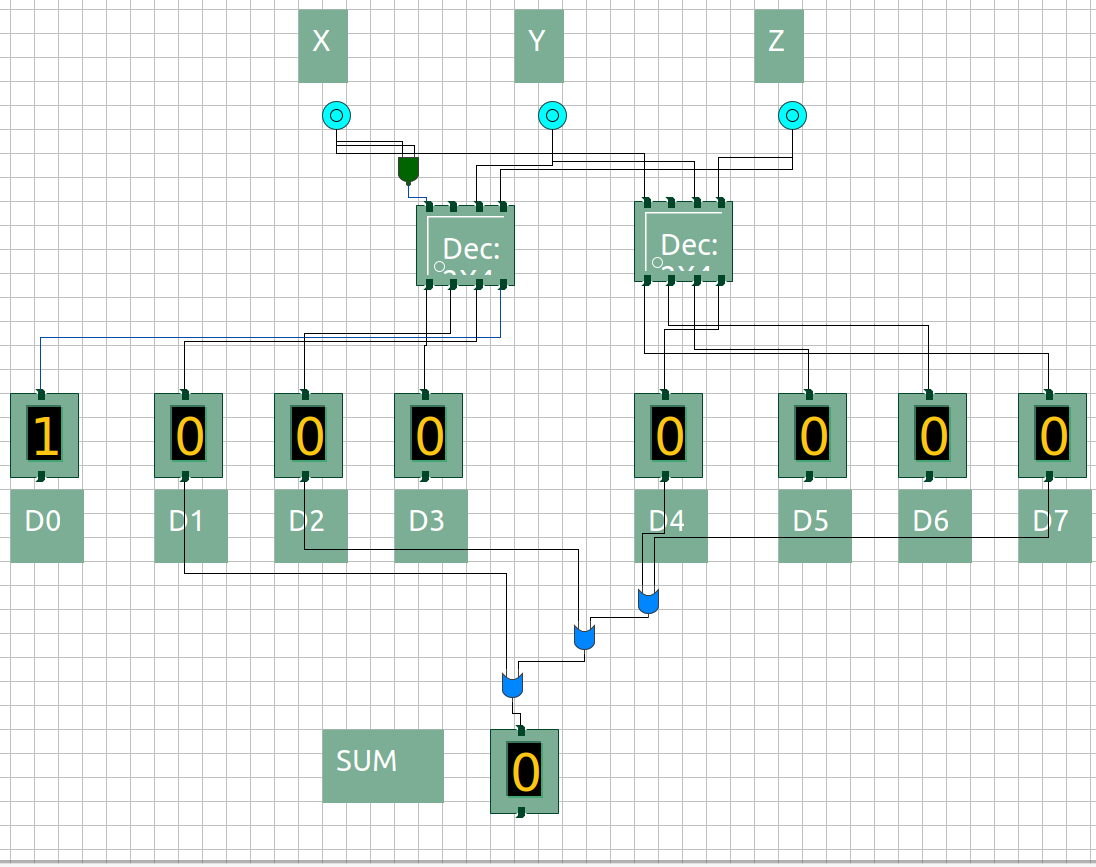
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Figure 1: X = 0, Y = 0, Z = 0; S = 0

Figure 2: X = 0, Y = 0, Z = 1; S = 1

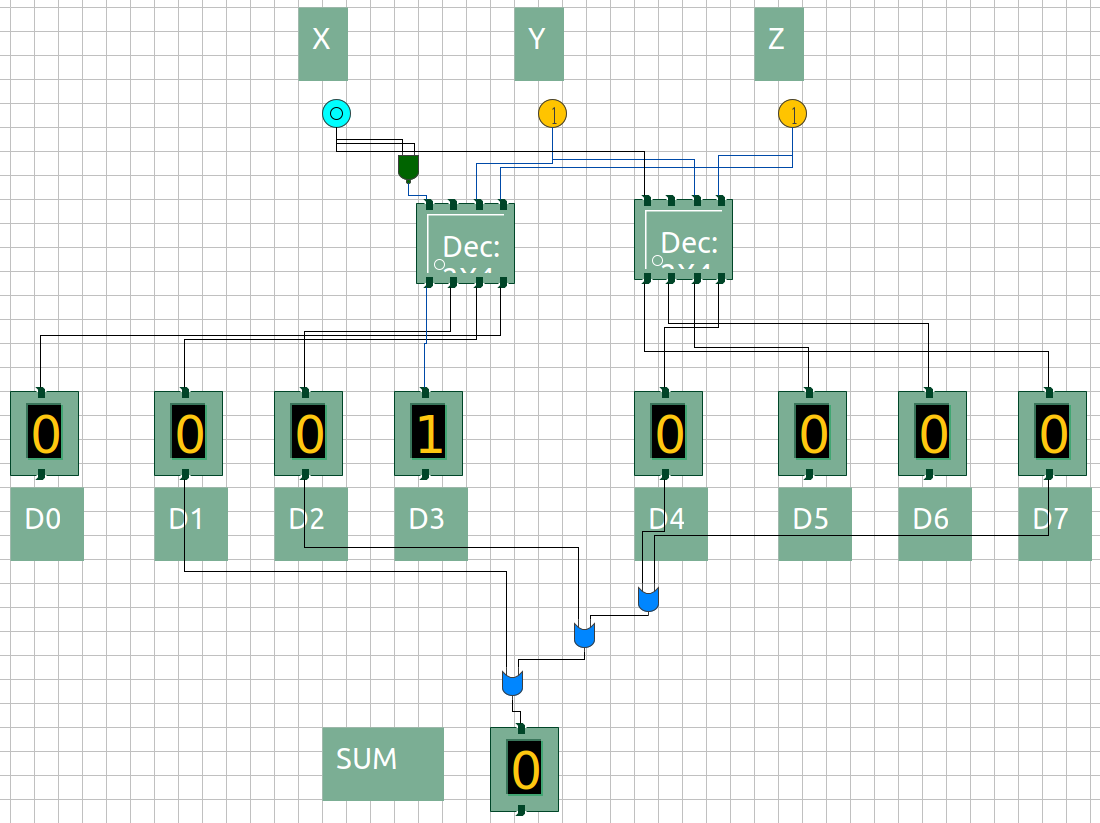
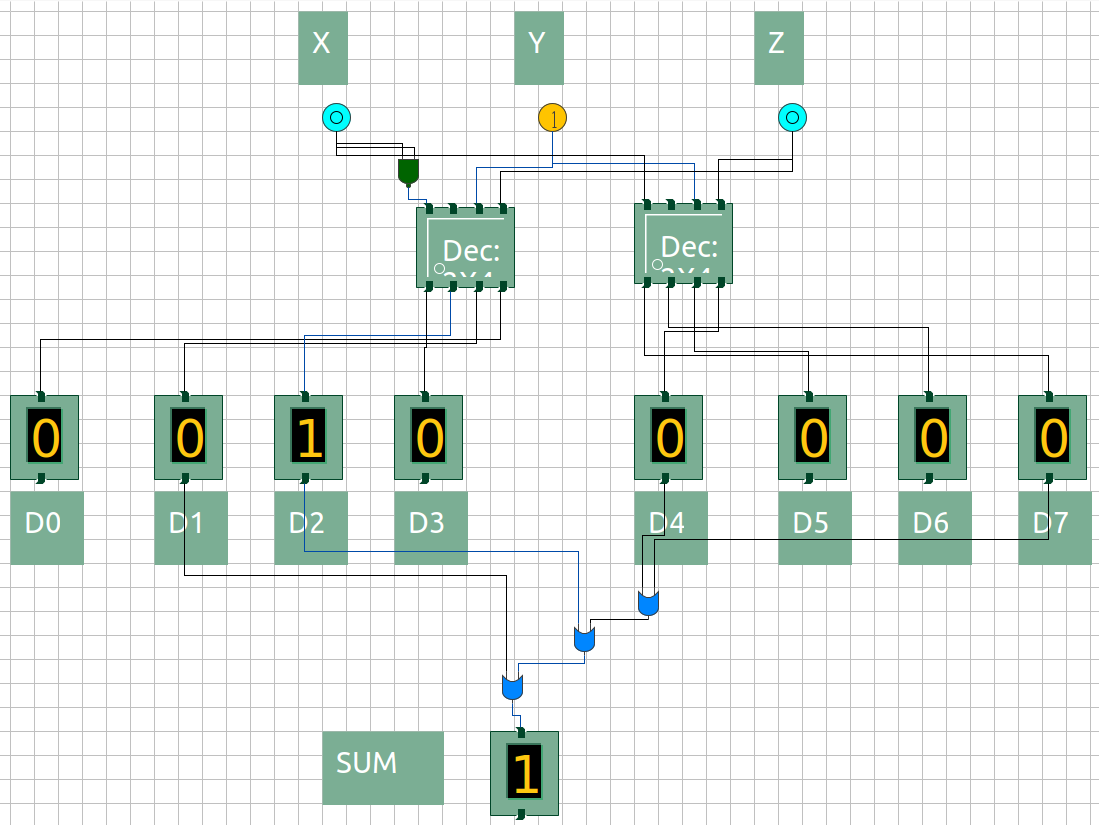
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Figure 3: X = 0, Y = 1, Z = 0; S = 1

Figure 4: X = 0, Y = 1, Z = 1; S = 0

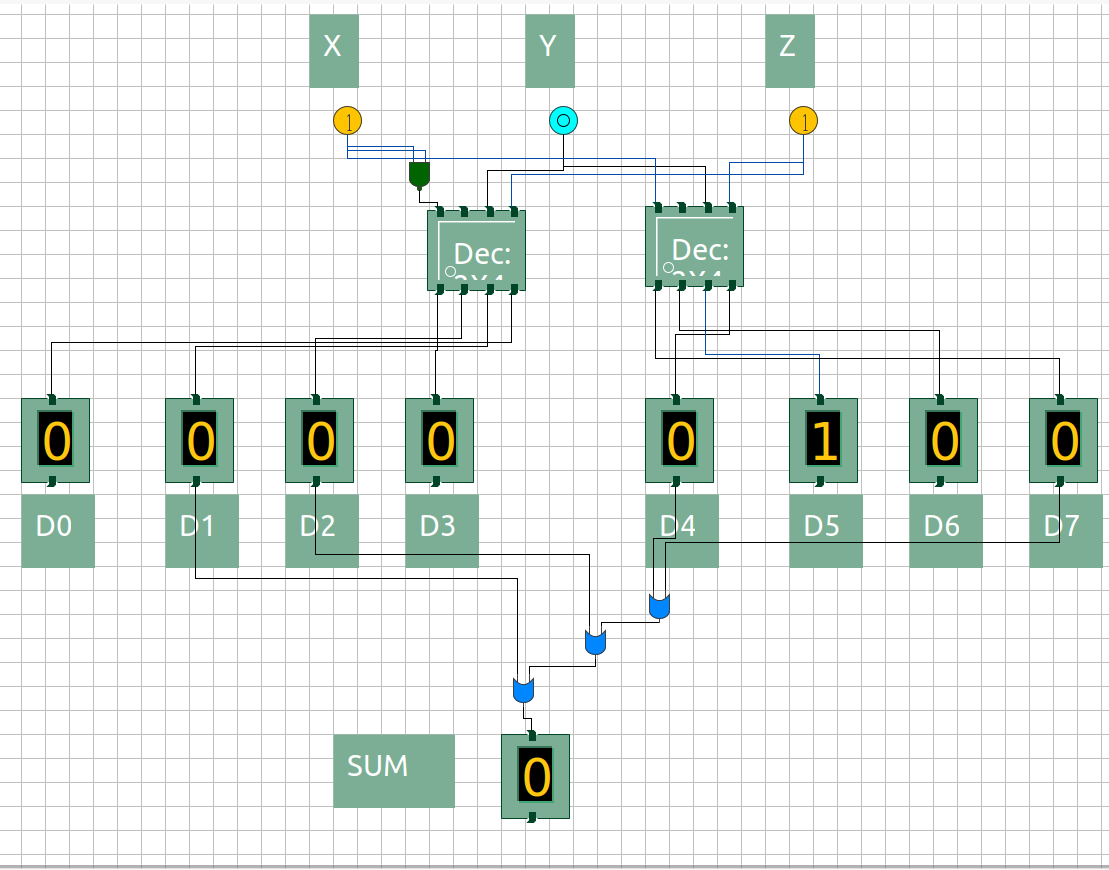
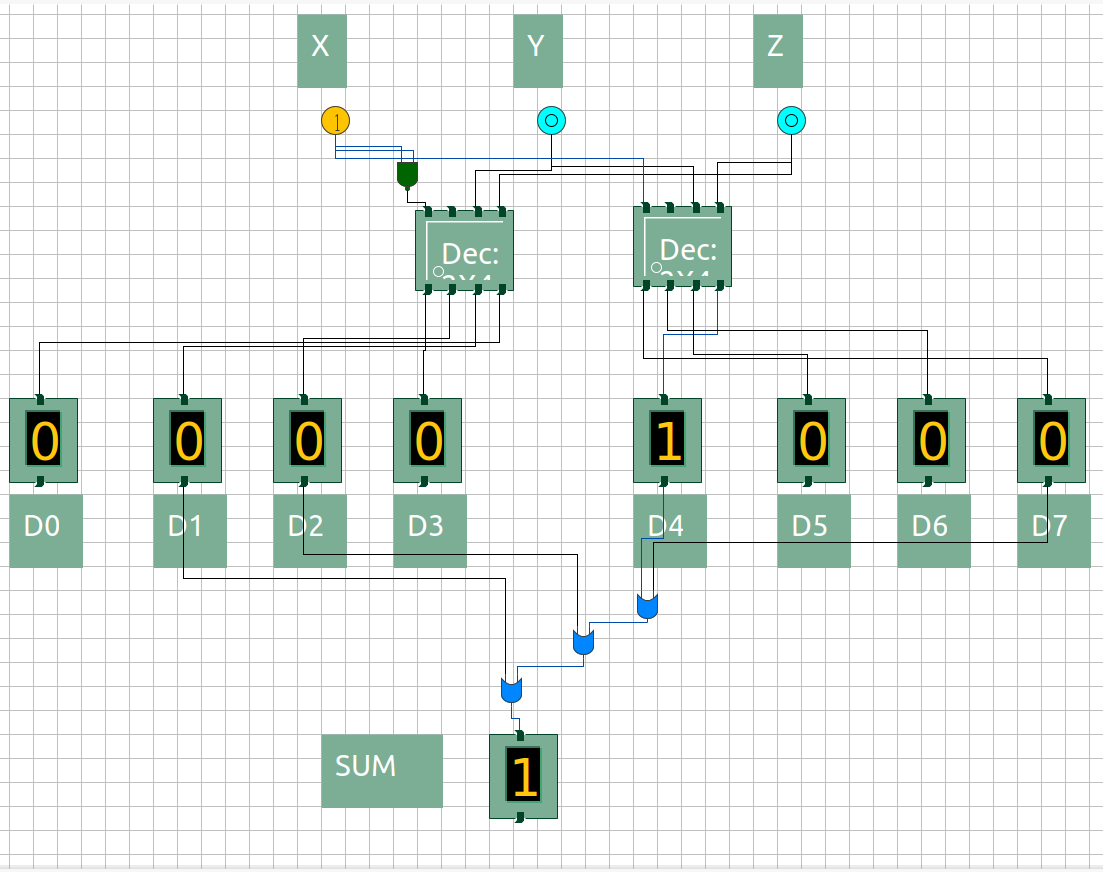
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Figure 5: X = 1, Y = 0, Z = 0; S = 1

Figure 6: X = 1, Y = 0, Z = 1; S = 0

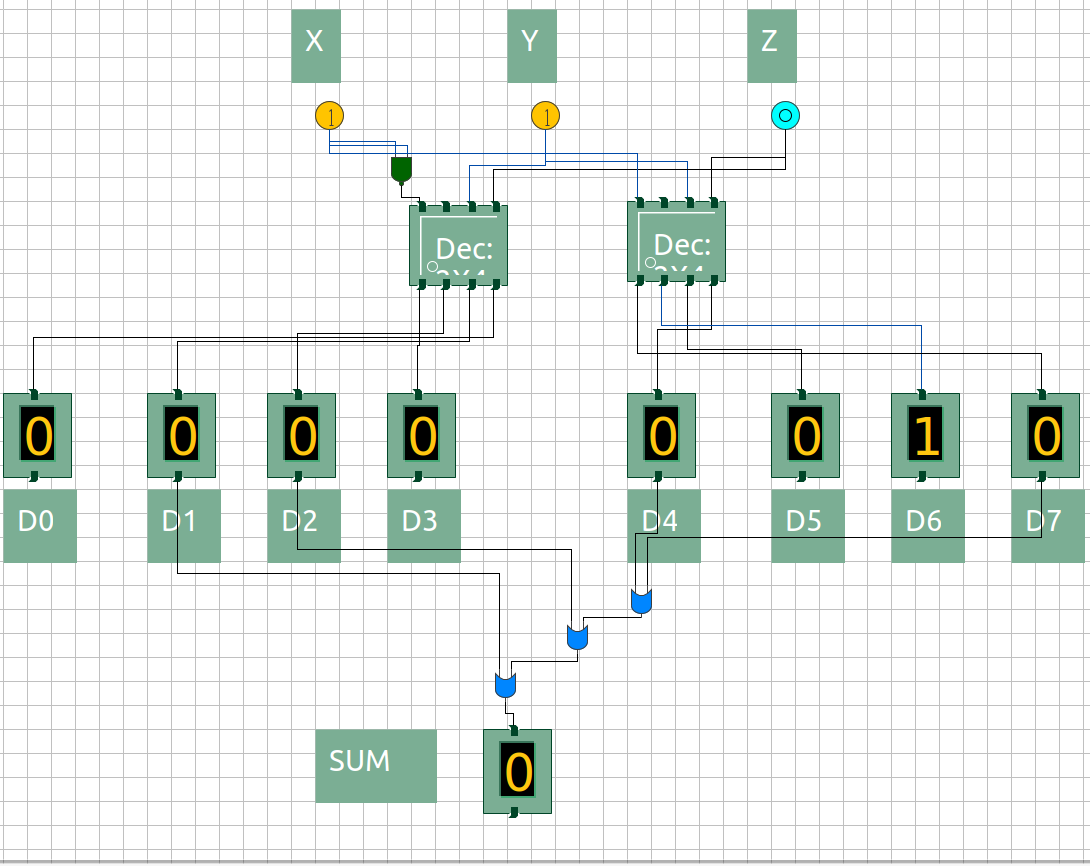
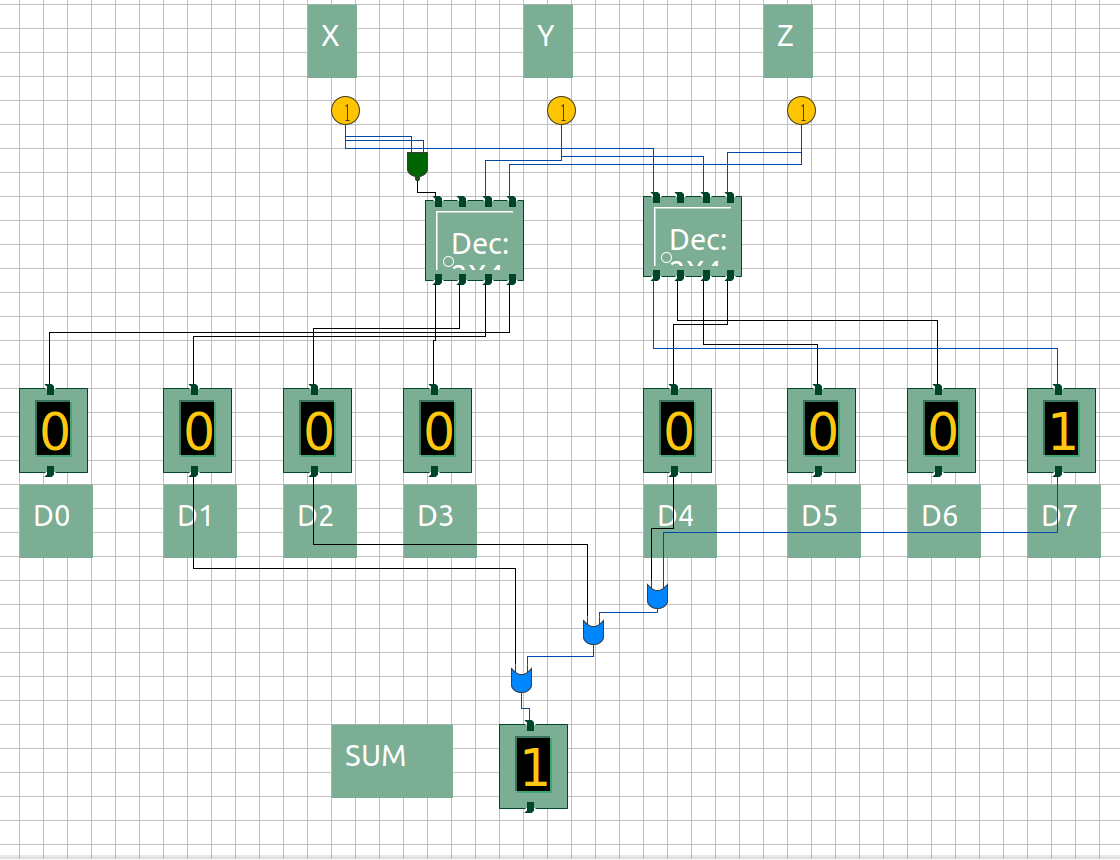
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Figure 7: X = 1, Y = 1, Z = 0; S = 0

Figure 8: X = 1, Y = 1, Z = 1; S = 1