Indian Institute of Engineering Science and Technology, Shibpur

BTech (CST) 4th Semester Examinations, 2021

Computer Architecture and Organization I (CS-2202)

Full marks: 50 Time: 1 hr 30 mins

Answer any *four*

1. Define *m*-addressed m/c. Write programs to compute Z = W + X - Y in 3-addressed, 2-addressed, 1-addressed and zero-addressed computers. Use temporary registers, if required, so that code should not overwrite operands. Compare the programs in terms of memory requirements to store the codes assuming 1-byte for opcode and 2-byte for an operand. 12.5

2. Define frequency dependent opcode selection scheme. Find Hoffman encoding for instructions of a hypothetical m/c with six type of instructions in its instruction set. The probable occurrence (frequencies) of instructions are - Data movement 25%, Logical 20%, Arithmetic 15%, Load/Store 18%, Branch 18% and Debug 4%. 12.5

3. Figure 1 describes the function (partial) of a processor control unit (CU). The i1, i2, … are the macro instructions and Cs represent control signals that correspond to micro-instructions. Duration of each control signal of Figure 1 is *t*. Show design of CU following sequence counter method. 12.5

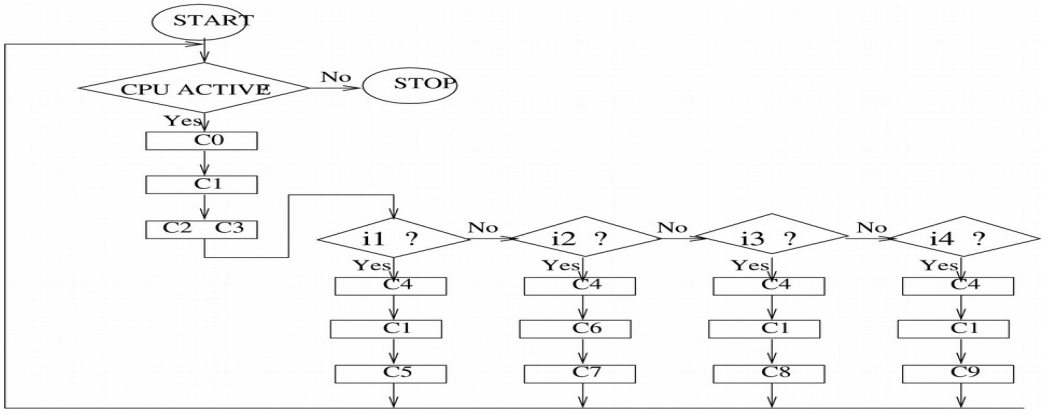

Figure 1

4a) Consider a dynamic RAM that must be given a refresh cycle 32 times per *ms*. Each refresh operation requires 100 *ns*; a memory cycle requires 200 *ns*. What percentage of the memory's total operating time must be given to refreshes? 6

b) Show the interfacing of one 4Kbyte ROM and one 8Kbyte RAM module, placed respectively at 0000_h $0FFF_h$ and at 8000_h to $9FFF_h$, with a processor having 16-bit address bus. Clearly mention the assumptions taken. 6.5

5. Consider a 4-way set-associative cache (initially empty) with total 16 cache blocks. The main memory consists of 256 blocks and a block consists of 4 words. The cache replacement policy implemented is LRU. The request for memory blocks is in the following order:

0, 255, 1, 4, 3, 1, 133, 216, 159, 129, 63, 48, 8, 32, 73, 92, 155.

(i) Show the format (tag, set/block and word fields) of the memory address.
(ii) Find the main memory blocks in the cache after service to each request. 12.5

6. Consider the reservation table of Figure 2 for a 4-stage (S1, S2, S3 and S4) pipeline. 12.5

(i) Identify the forbidden and non-forbidden latencies.
(ii) Find out collision vector of the pipeline architecture and draw the state diagram.
iii) Identify simple cycles, greedy cycles and compute MAL.
iv) Find lower bound of MAL.

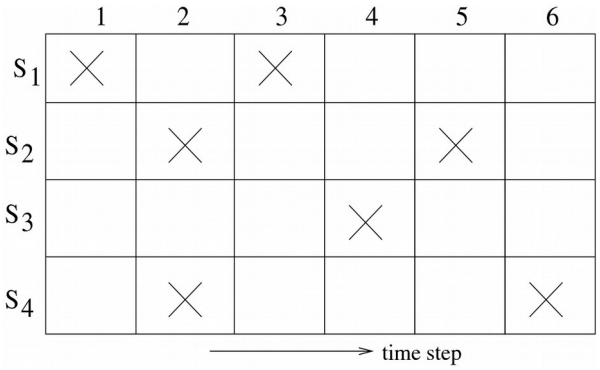

Figure 2