Computer Architecture and Organization Laboratory
Department of Computer Science and Technology, IIEST

Experiment No: 2 (Design of Carry-Look-Ahead adder)

Objective: To design

1. 4-bit carry lookahead adder (CLA) using half adders/full adders,
2. A 16-bit CLA using 4-bit CLAs.

The basic unit of a CLA is shown in Figure 1(a).

$p_i = x_i + y_i$ (or $x_i \oplus y_i$) is carry propagare and $g_i = x_i y_i$ is carry generate.

Figure 1(b) shows the n-bit CLA. The logic circuit for c_is are in CLA circuits.

For 4-bit CLA,

$$c_0 = g_0 + p_0 c_{in}$$
$$c_1 = g_1 + p_1 c_0 = g_1 + p_1 g_0 + p_1 p_0 c_{in}$$
$$c_2 = g_2 + p_2 c_1 = g_2 + p_2 g_1 + p_2 p_1 g_0 + p_2 p_1 p_0 c_{in}$$
$$c_3 = g_3 + p_3 c_2 = g_3 + p_3 g_2 + p_3 p_2 g_1 + p_3 p_2 p_1 g_0 + p_3 p_2 p_1 p_0 c_{in}$$

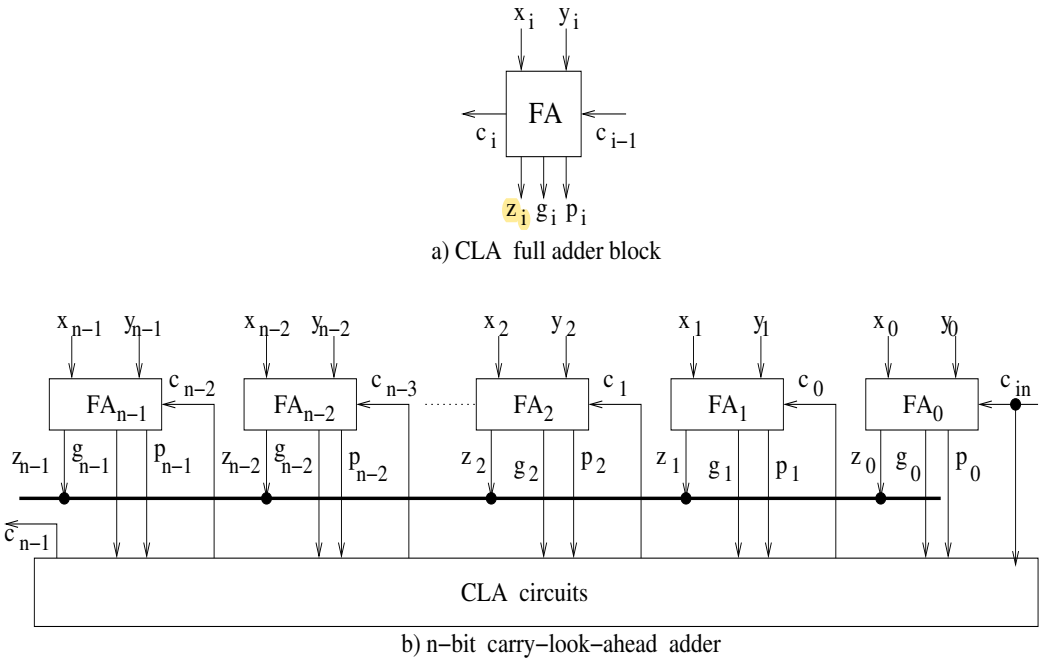

Figure 1: Carry look ahead adder

Task 1:

1. Contruct 4 modules as in Figure 1(a) (can use half adder).
2. Simplyfy the expressions for c_0, c_1, c_2 and c_3 assuming $c_{in} = 0$.
3. Design CLA circuits -that is, realize c_0, c_1, c_2 and c_3.
4. Design the CLA as in Figure 1(b) and verify a part of its truth table.

16-bit adder (Figure 2) can be implemented with cascade of 4-bit CLAs.

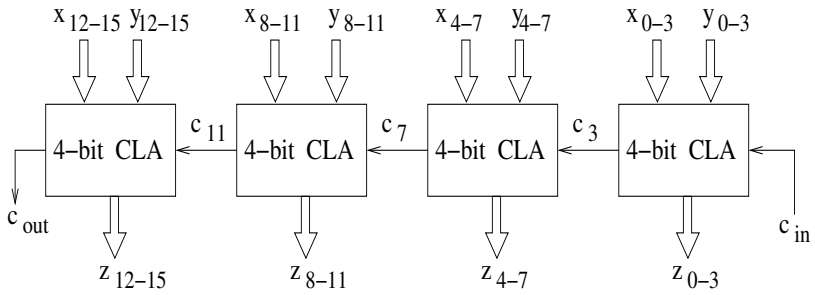

Figure 2: Cascaded carry look ahead adder

Task 2:
Report on the design of a 16-bit CLA as in Figure 2.