Indian Institute of Engineering Science & Technology, Shibpur

B.Tech (3^{rd} Semester CST) Final Examination, 2020

Digital Logic (CS 2102)

F.M. 50 Time: 1.5 hours

1. (a) Subtract decimal number 22 from 17 using 8 bit (representation) 2's complement method.

(b) A logic circuit has three inputs A, B, and C and output Y. Y is '1' for the following input combinations: (i) B and C are true (1), (ii) A and C are false (0), (iii) A, B, and C are true, and (iv) A, B, and C are false. Obtain the minimized expression for Y using algebraic manipulation.

(c) The shift register shown in the figure is initially loaded with the bit pattern 1010. Subsequently the shift register is clocked, and with each clock pulse the pattern gets shifted by one bit position to the right. With each shift, the bit at the serial input is pushed to left most position (MSB). After how many clock pulse will the content of the shift register become 1010 again? Justify your answer. [2 + 3 + 5]

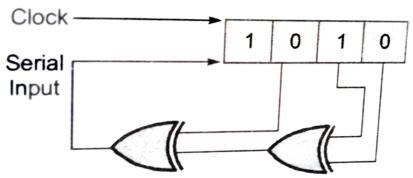

Figure 1: Shift Register

2. Design a combinational circuit whose input is a four-bit number and whose output is the 2's complement of the input number. Show that the circuit can be implemented using EX-OR and OR gates. [10]

3. Draw the state diagram and derive the state table for the following circuit.
A circuit accepts a serial bit stream 'X' as input and produces a serial bit stream 'Z' as output. When the bit pattern '1011' appears in the input stream, at that time, its output 'Z' = 1 and at all other times 'Z' = 0. The overlapping occurrence of patterns is also detected. [10]

4. A sequential circuit has one input and one output. The state diagram is shown in Figure 2. Design the sequential circuit with JK flip-flops. The circuit is to be designed by treating the unused states as don,t care conditions. [13]

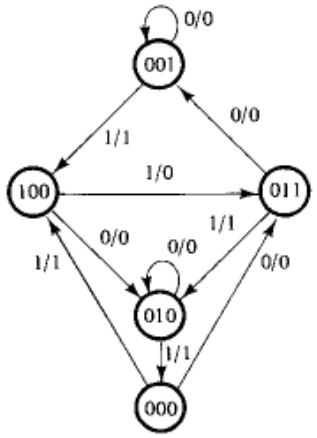

Figure 2: A Shift Register

5. (a) Which function is implemented using the circuit illustrated in Figure 3. Justify your answer.

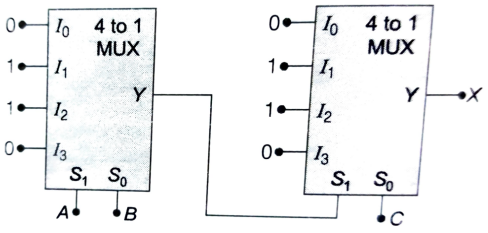

Figure 3: An application of Multiplexer.

(b) Implement the function $A + \overline{B}\ \overline{C}$ using 3×8 line decoder. [4 + 3]