Latch and Flip-Flop

October 5, 2020

Definition of Sequential Circuit:

- The outputs of a sequential circuit depend not only on the present inputs, but also the past history of the circuit. The circuit memorizes its present sate.
- Latches and flip-flops are the basic building block of storage devices.
- There are two types of sequential circuits, synchronous and asynchronous.
- Basic idea behind storing bit.

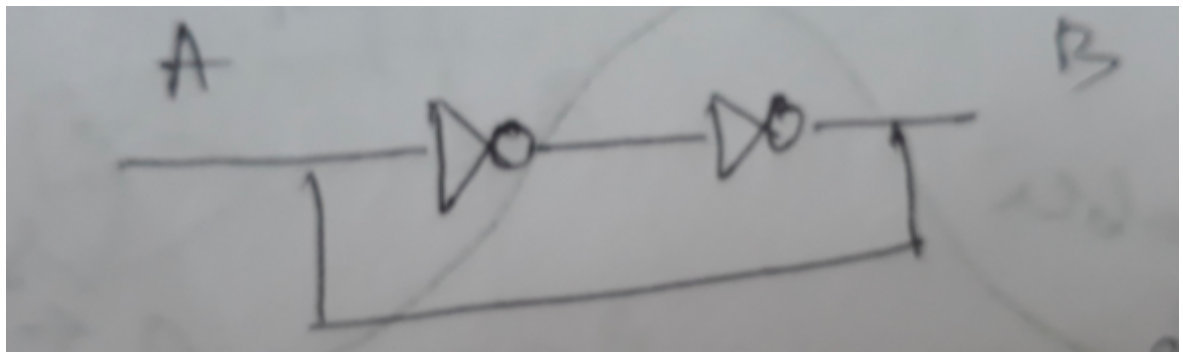


Figure: Cascaded Inverters with feedback.

Design of Latches

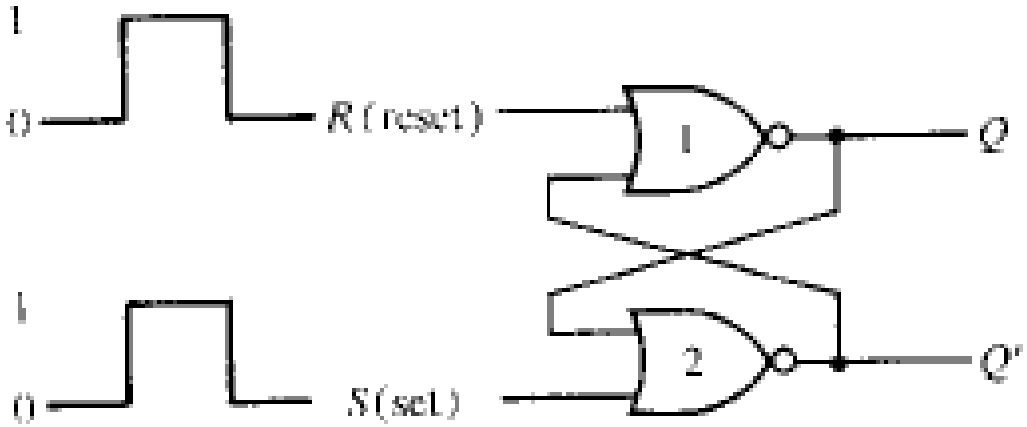
- A latch is a temporary storage device that has two stable states, 0 and 1.
- A flip-flop is a special kind of latch where a clock signal triggers the change in the stored value.
- Various types of Latches/flip-flops are:

  S-R (set-reset) type
  D (delay) type
  J-K type
  T (toggle) type

S-R Latch

1. It has a pair of cross-coupled NOR or NAND gates.
2. It has two inputs (S and R) and two outputs (Q and $\overline{Q}$).
3. The output can be set to 0 or 1 by applying suitable values on S and R inputs.

- The output of a NOR gate is 0 if any of the input is 1 and the output is 1 when only all the inputs are 0.



(a) Logic diagram

S	R	Q	Q'	
1	0	1	0	
0	0	1	0	(after S = 1, R = 0)
0	1	0	1	
0	0	0	1	(after S = 0, R = 1)
1	1	0	0	

(b) Truth table

Figure: S-R latch, (a) Logic diagram, (b) Truth table

S-R Latch

- Latch has two useful states. When $Q = 1$ and $\overline{Q} = 0 \Rightarrow$ set state. When $Q = 0$ and $\overline{Q} = 1 \Rightarrow$ clear state.
- When $S = 1$ and $R = 1$, $Q = 0$ and $\overline{Q} = 0$ which violates the definition of latch. Hence, $S = 1$ and $R = 1 \Rightarrow$ invalid state.
- $S = 0$ and $R = 0$ is a condition, which suppose to cause any change in the output of the S-R latch.
- First, we apply $S = 1$ and $R = 1$ then, $Q = 0$ and $\overline{Q} = 0$. Now apply $S = 0$ and $R = 0$ which makes the output to $Q = 1$ and $\overline{Q} = 1$. If the speed of the two gates are same then, output will oscillates.
- But in reality, two gates never have the same speed, one will be slightly slower than other. In that case we can not predict the output. The phenomenon is known as race condition.

S-R Latch

Race Condition

- A scenario where the final output depends on the relative speed of gates.
- If we apply $S = 1$ and $R = 1$, and then $S = 0$ and $R = 0$, the outputs will to either $Q = 0$, $\overline{Q} = 1$ or $Q = 1$, $\overline{Q} = 0$, depending upon the relative speeds of the two gates.

S-R Flip-flop

The S-R latch can be modified by providing an additional control input that determines when the state of the circuit is to be changed.

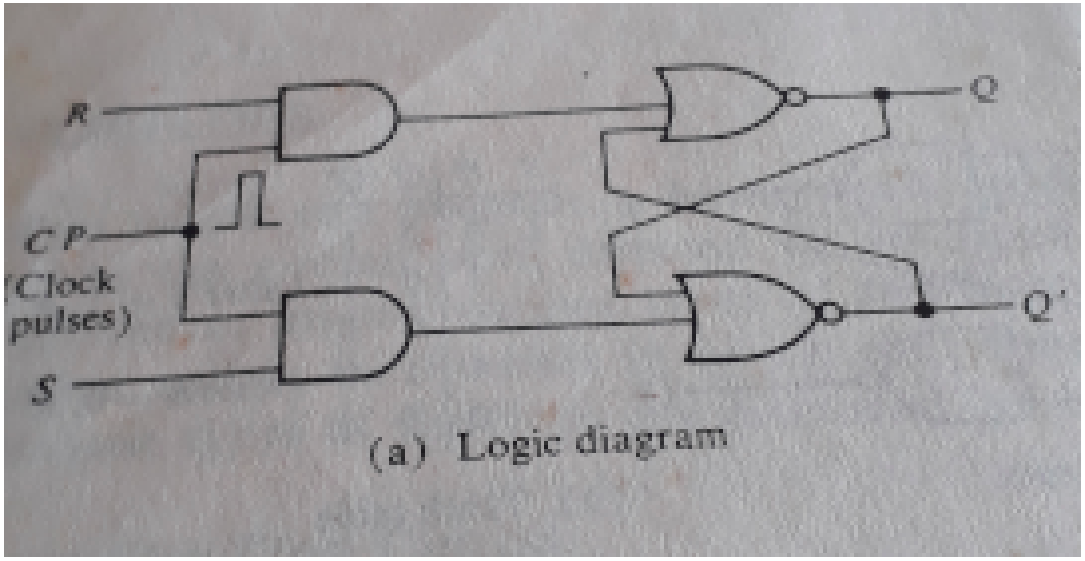


Figure: Logic diagram of S-R Flip-flop

- When the clock plus goes to 1, information from the S and R inputs is allowed to reach to the input of the basic latch.

S-R Flip-flop

The characteristic Table of the S-R flip-flop is given below:

Q(t)	S	R	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	indeterminate
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	indeterminate

- The set state is reached when $S = 1$, $R = 0$ and $CP = 1$.
- The attend the clear state, we have to apply $S = 0$, $R = 1$ and $CP = 1$.
- The characteristic equation of the S-R flip-flop is $Q(t+1) = S + \overline{R}Q(t)$

D Flip-Flop

- The logic diagram of D flip-flop is show below which is a modification of S-R flip-flop.

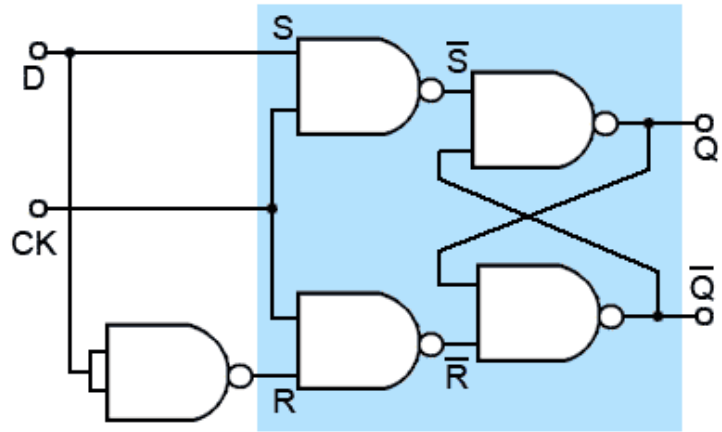


Figure: Logic diagram of D Flip-flop

- Right most two NAND gates form the basic S-R latch and next two NAND gates modify it into a clocked S-R flip-flop.
- The D input is applied directly to S input and its compliment is applied to the R input.

D Flip-Flop

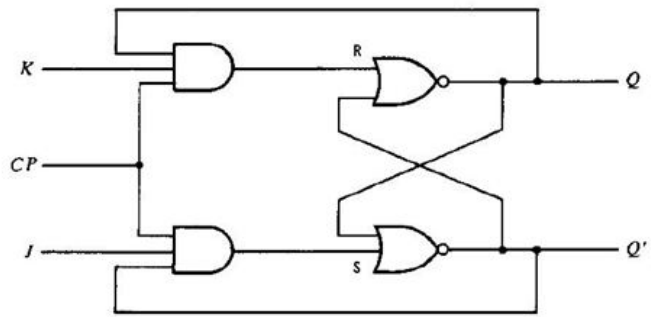
- As long as clock plus input is at 0, $\overline{S} = 0$ and $\overline{R} = 0$, regardless the value of the other inputs. This conforms that the two inputs of the basic S-R latch remain at 0 initially.
- The D input is sampled during the occurrence of a clock plus.
- When D = 1 and clock plus is also 1 then, $\overline{S} = 0$, $\overline{R} = 1$ and the flip-flop goes to set state.
- When D = 0 and clock plus is also 1 then, $\overline{S} = 1$, $\overline{R} = 0$ and the flip-flop goes to clear state.
- The characteristic table of D flip-flop is given below

Q(t)	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

- The Characteristic equation is $Q(t+1) = D$

J-K Flip-Flop

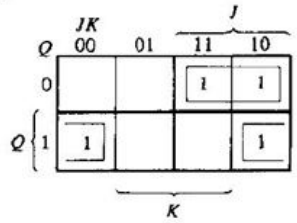
- J-K flip-flop is a refinement of the S-R flip-flop. The indeterminate state of the S-R flip-flop is defined in J-K flip-flop.
- When J = K = 1, the flip-flop switches to its complement state, that is if Q = 1, it goes to Q = 0, and vice versa.
- The Logic diagram and characteristic table of J-K flip-flop are shown below:



(a) Logic diagram

Q	J	K	Q(t + 1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

(b) Characteristic table



$Q(t+1) = JQ' + K'Q$

(c) Characteristic equation

J-K Flip-Flop

- Race in condition: Due to the feedback in J-K flip-flop, a CP signal which remains a 1 (while $J = K = 1$) after the outputs have been complement once will repeated and a continuous transition of the outputs.
- To avoid the undesirable operation, the clock pulse duration must be shorter than the propagation delay of J-K flip-flop.
- The restriction on clock pulse width can be eliminated with a master-slave or edge-triggered flip-flop.

T Flip-Flop

- The T flip-flop is a single-input version of J-K flip-flop. The T input is obtained from a JK type if both inputs are tied together.
- The T flip-flop goes its complement state when $T = 1$ and $CP = 1$.
- The logic diagram of the T flip-flop is shown below.

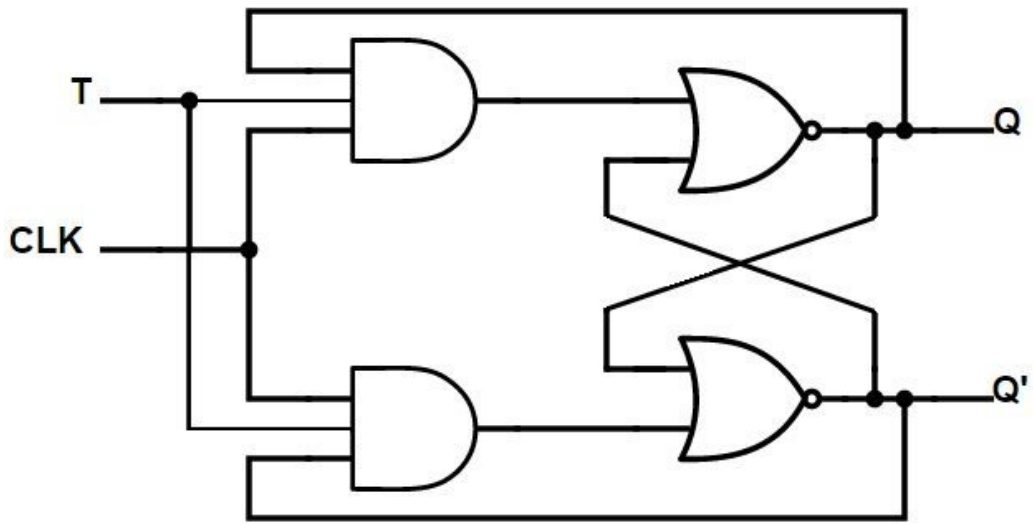


Figure: Logic diagram of T Flip-flop

Triggering of Flip-Flop

- The state of a flip-flop is changed by a momentary change in the input signal. This momentary change is called a trigger.
- Clocked flip-flops are triggered by pulses. A pulse starts from an initial value 0, goes to 1, and after a short time, returns to its initial 0 value.
- A flip-flop changes its state at rising edge of the clock pulse then, it is called positive edge trigger flip-flop. If the a flip-flop changes its state at falling edge of the clock pulse then, it is called negative edge trigger flip-flop.

Edge Trigger D Flip-Flop

- In this type of flip-flop, the output transitions occur at a specific level of the clock pulse. When the pulse input level exceeds this threshold level, the inputs are locked out and flip-flop is therefore unresponsive to further changes in inputs until the clock pulse returns to 0 and another pulse occurs.
- The logic diagram of a D-type positive edge-trigger is shown below.

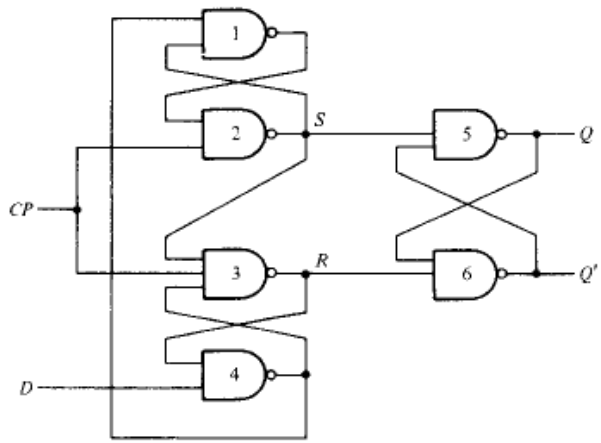


Figure: Logic diagram of D type positive-edge triggered Flip-flop

Edge Trigger D Flip-Flop

- The circuit consists of three basic latches. NAND gates 1 and 2 make up one basic latch and gates 3 and 4 form another latch. The third latch consisting of gates 5 and 6 provides the outputs of the circuit.
- The input S and R of the third latch must be maintained at logic -1 for the outputs to remain in their steady-state values.
- When S = 0 and R = 1, the output goes to set state with Q = 1.
- When S = 1 and R = 0, the output goes to clear state with Q = 0.
- The inputs S and R are determined from the states of the other two basic latches.

Edge Trigger D Flip-Flop

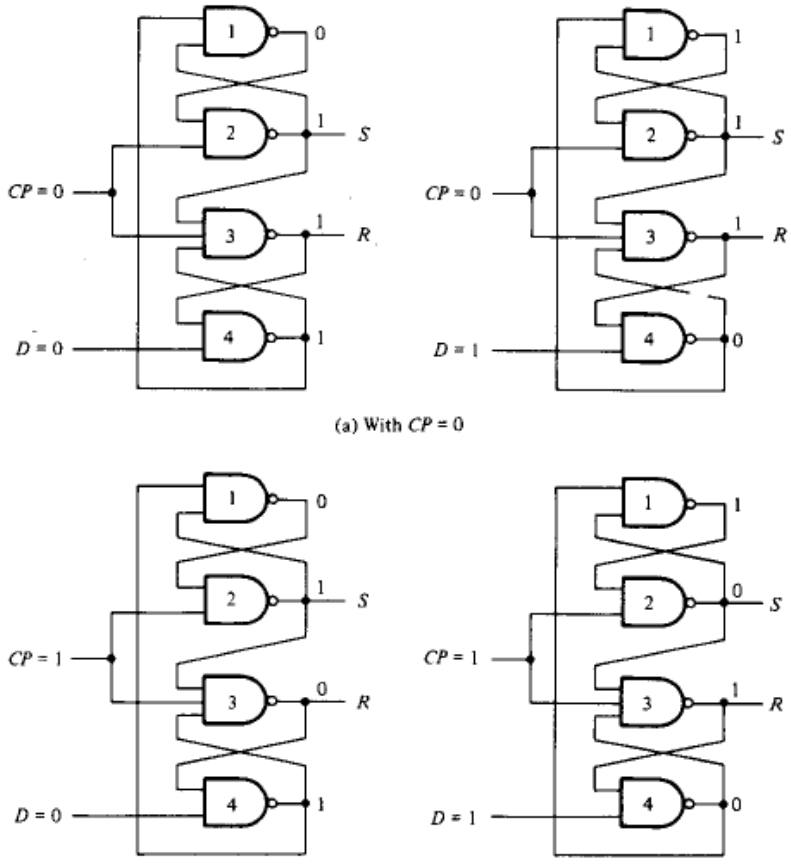


Figure: Operation of the D type positive-edge triggered Flip-flop

Edge Trigger D Flip-Flop

- When CP = 0 and D = 0 or D = 1, in either case outputs of gates 2 and 3 are equal to 1, thus making S = R = 1, which is the condition for a steady-state output.
- When D = 0, the output of gate 4 is at logic 1, which causes the output of gate 1 equal to 0.
- When D = 1, the output of gate 4 is at logic 0, which causes the output of gate 1 equal to 1.
- There is a definite time, called *setup time*, in which the D input must be maintained at a constant value prior to the application of the pulse.
- The *setup time* is equal to the propagation delay to through gates 4 and 1 since a change in D causes a change in the outputs of these two gates.

Edge Trigger D Flip-Flop

- Assume that D does not change during the *setup time* and CP becomes 1. If D = 0 and CP =1, then S remains in at 1 but R changes from 1 to 0. This causes output Q goes to 0.
- Now if while CP = 1, there is a change in the D input, the output of gate 4 will remain at 1 (even if D goes to 1).
- There is definite time, called the *hold time*, that the D input must not change after application of clock pulse. The *hold time* is equal to the propagation delay of gate 3, since it must ensure that R becomes 0 in order to maintain the output of gate 4 at 1, regardless the value of D.
- If D = 1 and CP = 1, then S = 0 and R = 1, which causes the output Q = 1.