Digital Logic Practical Lab Report

Latches and Flip Flops

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Course:

Digital Logic Laboratory (CS351)

Experiment 1 (a)

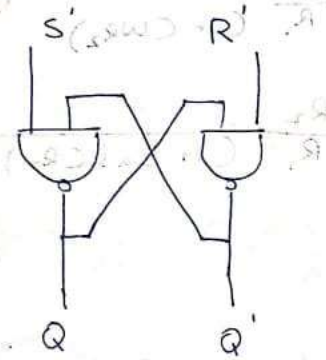
Objective

Design SR Latch using NAND gates to verify the state table of respective latches

Theory

An SR (Set/Reset) Latch ~~is~~ works independently of control signal (like clock) and only relies on the state of S and R inputs.

It can be made using two NAND gates as follows



where S' and R' ~~are~~ ~~rer~~ inverted inputs of S and R and Q and Q' are outputs.

a) when S = 1 (S' = 0), we see that Q = 1, regardless of any value of Q' as $\overline{0 \cdot Q'} = \overline{0} = 1$

b) when R = 1 (R' = 0), we see that Q' = 1, regardless of previous value of Q as $\overline{0 \cdot Q} = \overline{0} = 1$

c) when S = 0, R = 0 (S' = R' = 1), the ~~values~~ output will either remains same, or will give Q = Q' = 1 (which is not good, and hence we call it ~~"metastable"~~ "latched")

d) when S=1, R=1 (S'=R'=0), the output will be Q = Q' = 1, but this output, will again get feeded to latch, and will continue to do so, given sort of "infinite loop". This "metastable" is unstable condition, and should never be given as input,

→ From these observation, we get the following characteristic Table.

S'	R'	Q
0	0	Meta stable
0	1	1
1	0	0
1	1	Latched.

Result

→ Avoiding "Latched" and "Metastable" conditions, the output of the simulator made circuit matches with the Characteristic Table

→ Two NAND gates were used to make the SR latch

Inputs / Outputs:

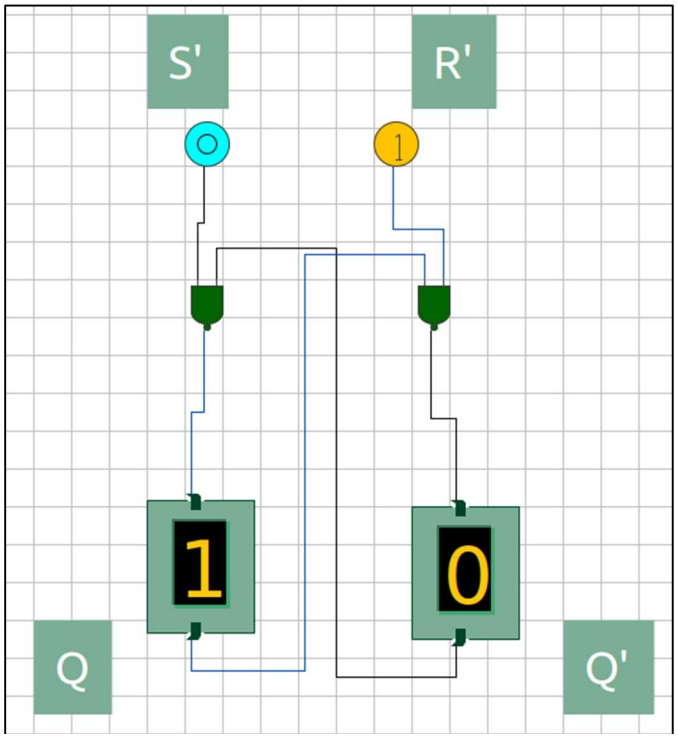


Figure 1: S’ = 0, R’ = 1; Q = 1, Q’ = 0

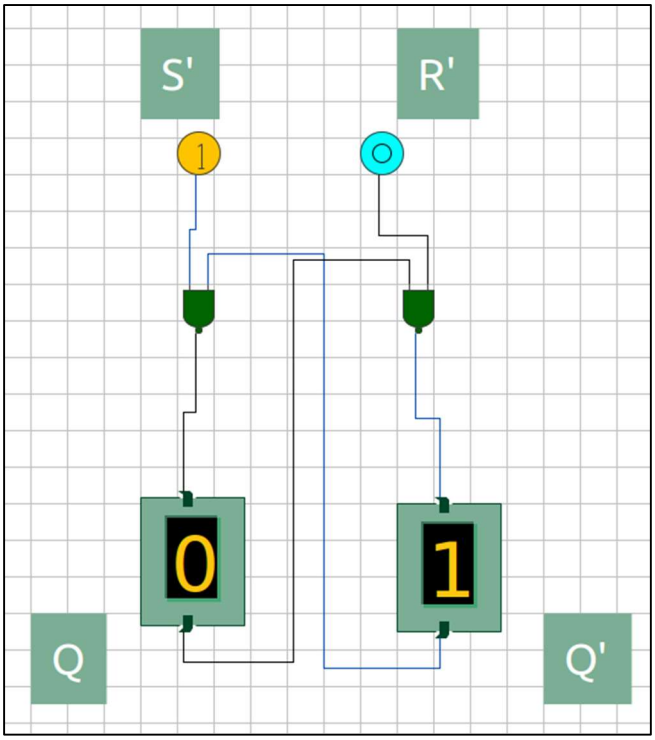


Figure 2: S’ = 1, R’ = 0; Q = 0, Q’ = 1

Experiment 1 (b)

Objective

Design D Latch using NAND gates to verify the state table of respective fourth Latch.

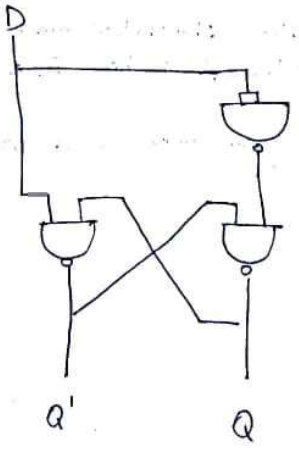
Theory

→ The D Latch is used to store, or capture the logic level which is present data line.

→ It's Characteristic Table is as follows.

D	Q	Q'
0	0	1
1	1	0

→ We can use three NAND gates to develop the D Latch.



Result

→ Three NAND gates were used to desing D Latch

→ The output from the simulator matches with the Characteristic Table.

Inputs / Outputs:

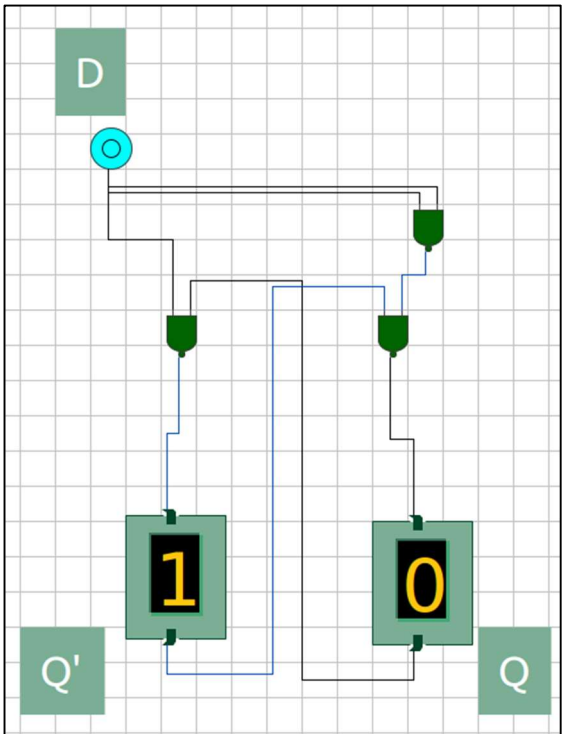


Figure 2: D = 0; Q = 1, Q’ = 0

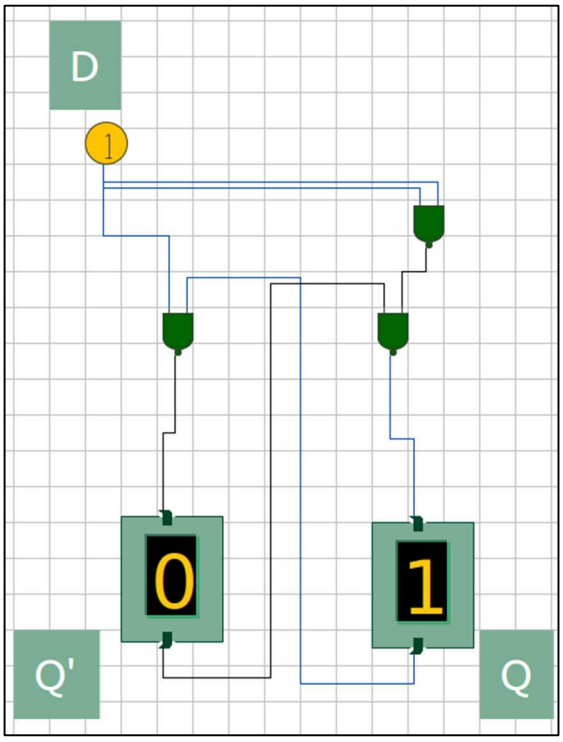


Figure 2: D = 1; Q = 0, Q’ = 1

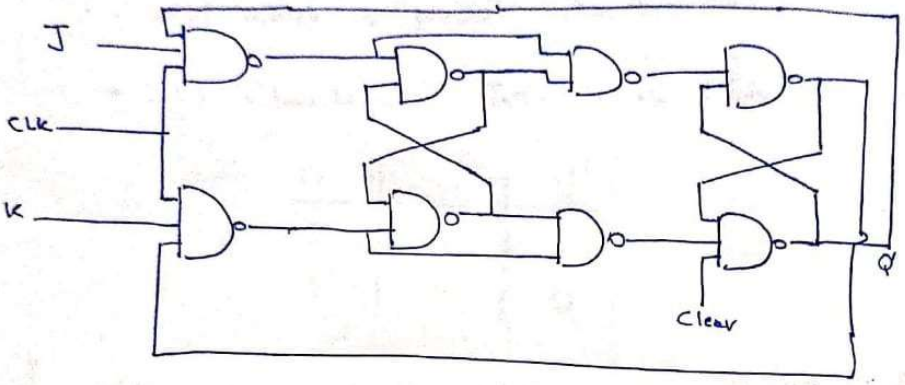
EXPERIMENT 2 (b)

Objective

Verify the Truth Table of a J-K Master Slave Flip-Flop.

Theory

Given Circuit is as follows:



It's Characteristic Table is as follows:

Q(t)	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

→ as it's not possible to display both previous Q(t) and present Q(t+1) simultaneously, ~~we will~~ we will only see the present Q(t+1) outputs.

→ also as we are using NAND gates, clear will be set to 1 always during operation as $\overline{1.x} = \overline{x}$

Result

→ The output of the simulator matches with the Characteristic Table

→ It is to be noted that as we are using Master Slave JK Flip Flop, we get output after two clock cycles, instead of one.

Inputs / Outputs:

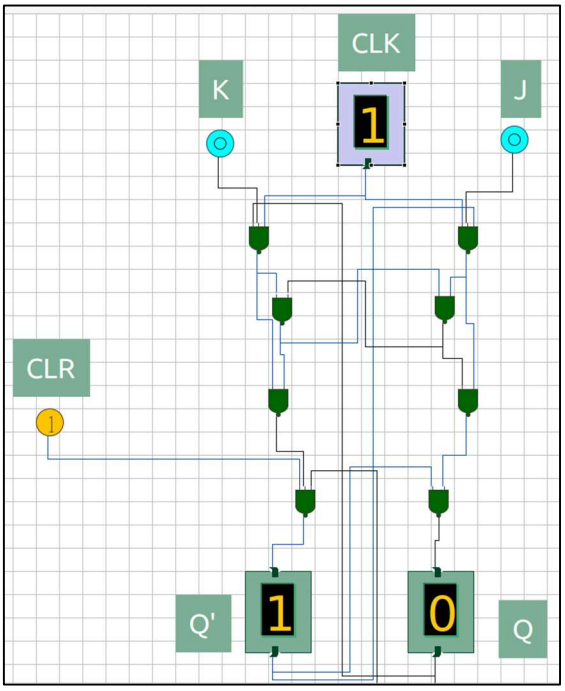


Figure 3: Q(t) = 0, J = 0, K = 0; Q(t+1) = 0

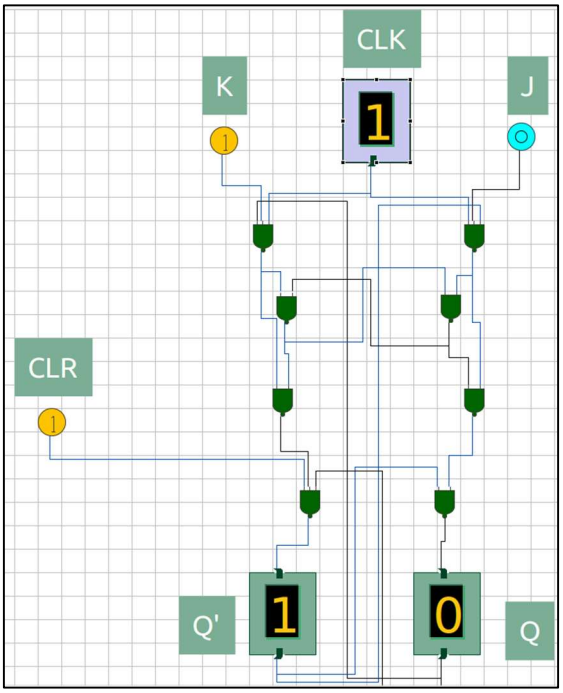


Figure 2: Q(t) = 0, J = 0, K = 1; Q(t+1) = 0

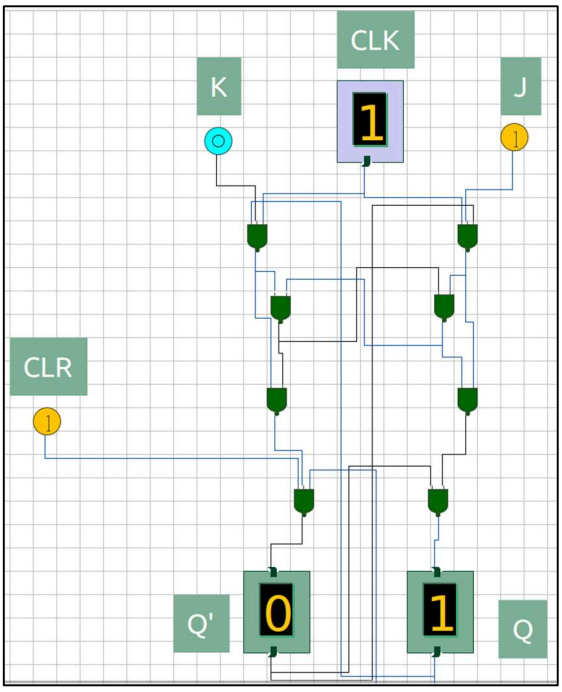


Figure 3: Q(t) = 0, J = 1, K = 0; Q(t+1) = 1

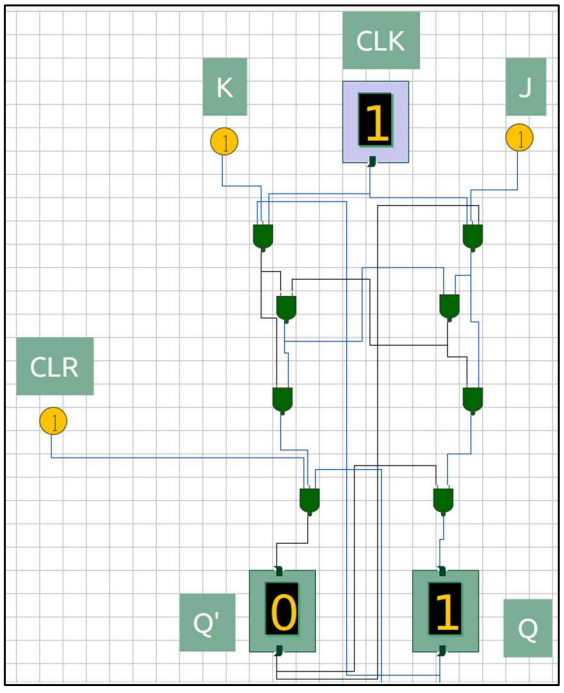


Figure 4: Q(t) = 0, J = 1, K = 1; Q(t+1) = 1

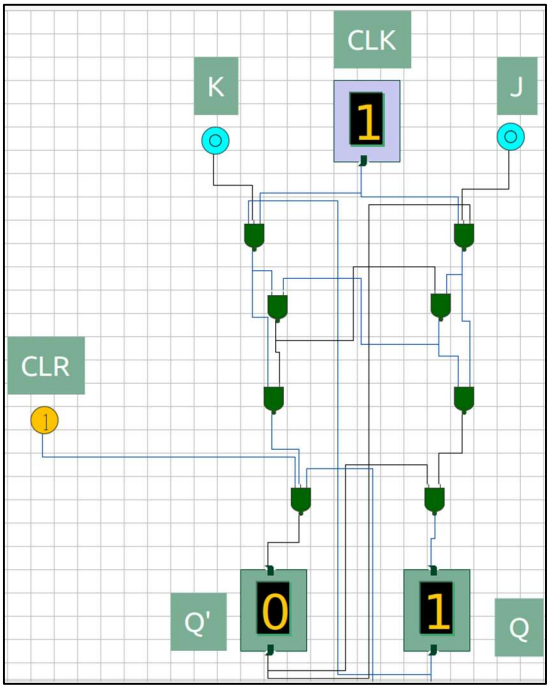


Figure 5: Q(t) = 1, J = 0, K = 0; Q(t+1) = 1

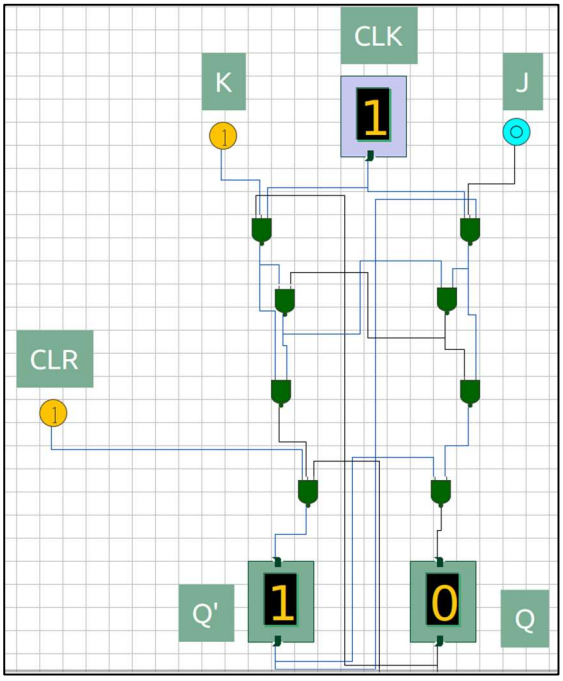


Figure 6: Q(t) = 1, J = 0, K = 1; Q(t+1) = 0

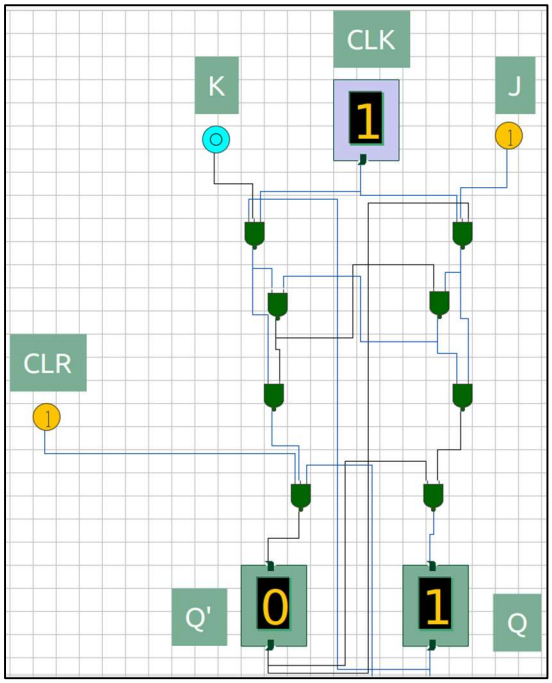


Figure 7: Q(t) = 1, J = 1, K = 0; Q(t+1) = 1

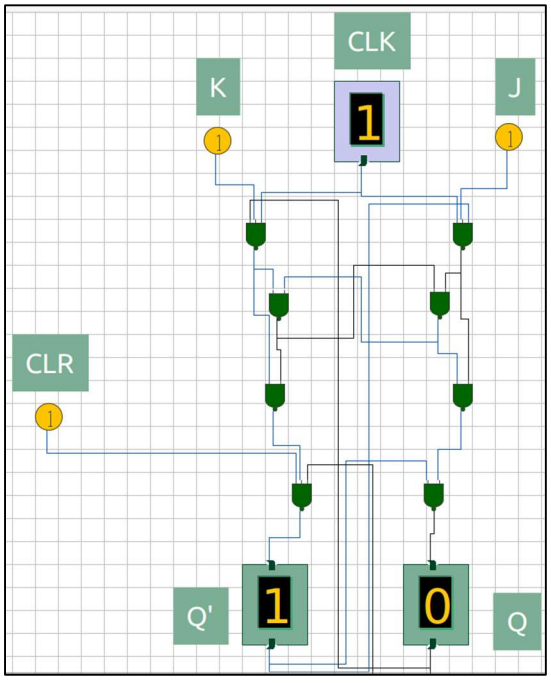


Figure 8: Q(t) = 1, J = 1, K = 1; Q(t+1) = 0

Experiment 2 (b)

Objective

Realise a D Flip Flop and verify the state table

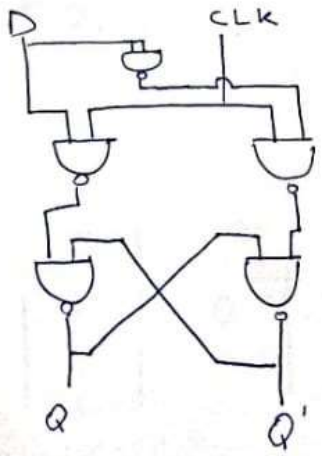
Theory

→ The D (Delay) Flip-Flop is a modified version of S-R Flip-Flop with addition of an inverter to prevent the S and R inputs from being at the same Logic Level

→ It's Characteristic Table is as follows:

Q(t)	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

→ We can realise following D Flip-Flop Circuit



Result

→ We have used five NAND gates to realise ~~D Flip-F~~ D Flip-Flop

→ The output of simulator matches with the characterist Table.

Inputs / Outputs:

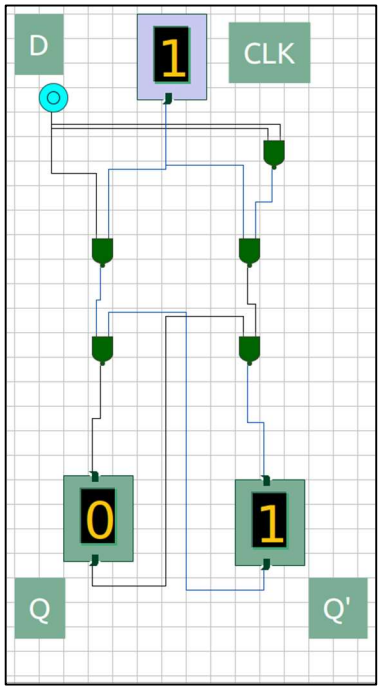


Figure 4: Q(t) = 0, D = 0; Q(t+1) = 0

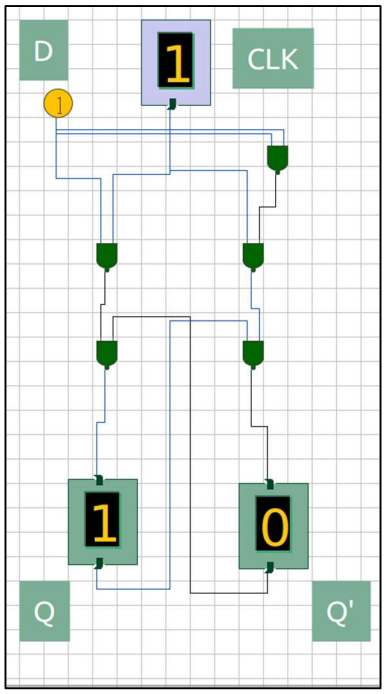


Figure 2: Q(t) = 0, D = 1; Q(t+1) = 1

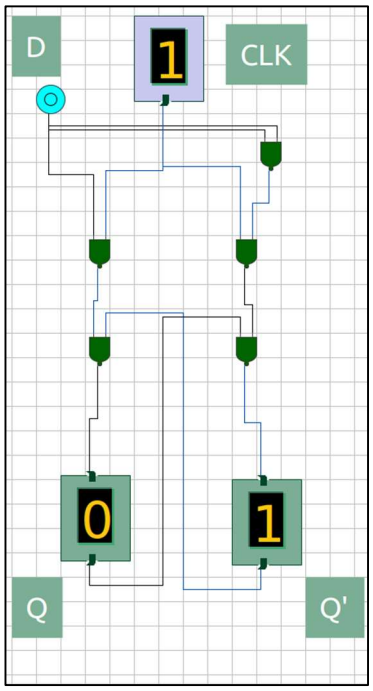


Figure 3: Q(t) = 1, D = 0; Q(t+1) = 0

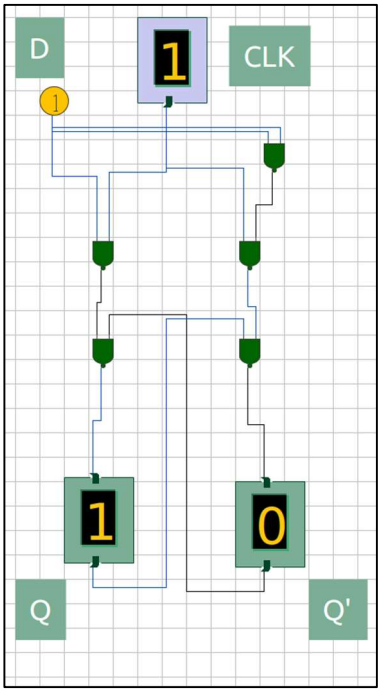


Figure 4: Q(t) = 1, D = 1; Q(t+1) = 1

Experiment 2 (c)

Objective

Design an Edge-Triggered D Flip-Flop and verify state Table

Theory

→ Edge-Trigger is a property of Flip-Flop which defines when output is displayed

→ a clock input in Sequential Looks like the fall

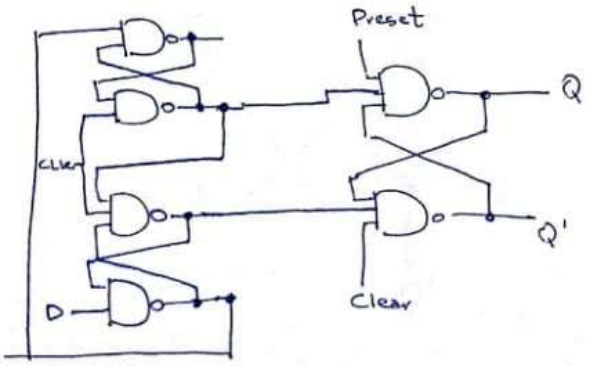
→ response to input can be displayed at two timings according to clock

i) when Clock goes from 0 to 1

ii) when clock goes from 1 to 0

→ These two trigger timing as described as positive edge-trigger and negative edge-trigger respectively.

→ Following circuit was given:



→ And the characteristic Table of D Flip Flop is as follows

Q(t)	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

→ As we are using NAND gates, Clear and preset should be kept 1 as $\overline{1.X} = \overline{X}$

→ As multiple Latches (depth = 2) are being used in the circuit, the output requires multiple clock pulses (2) to display as output.

Result

→ The outputs from the simulator is same as what we expected from the characteristic Table.

Inputs / Outputs:

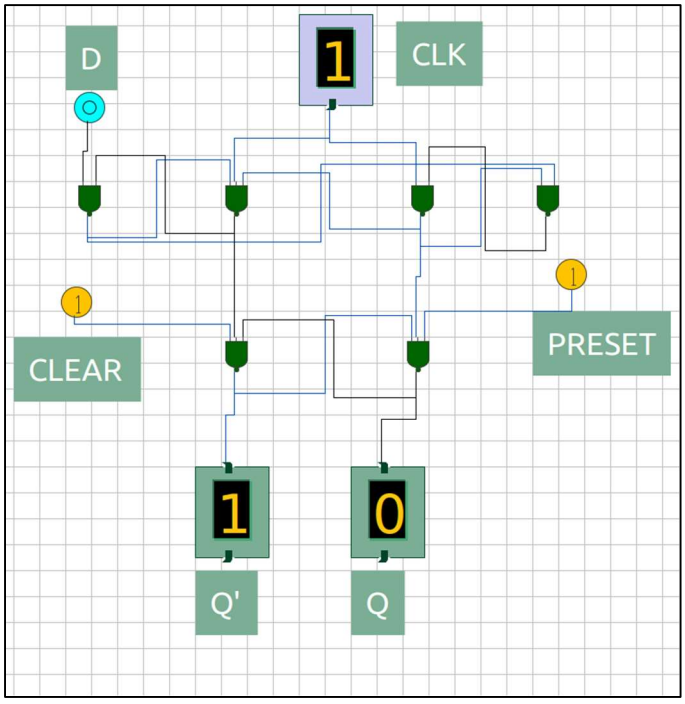


Figure 5: Q(t) = 0, D = 0; Q(t+1) = 0

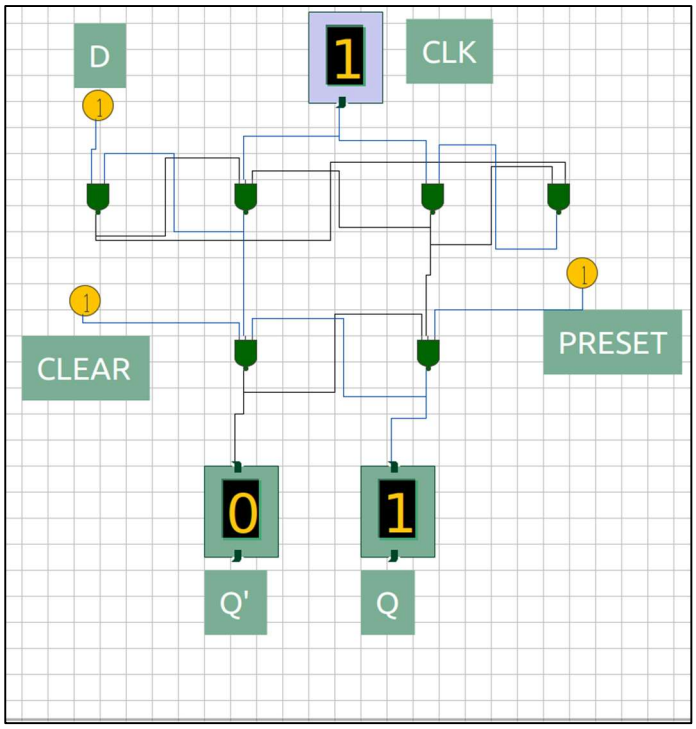


Figure 2: Q(t) = 0, D = 1; Q(t+1) = 1

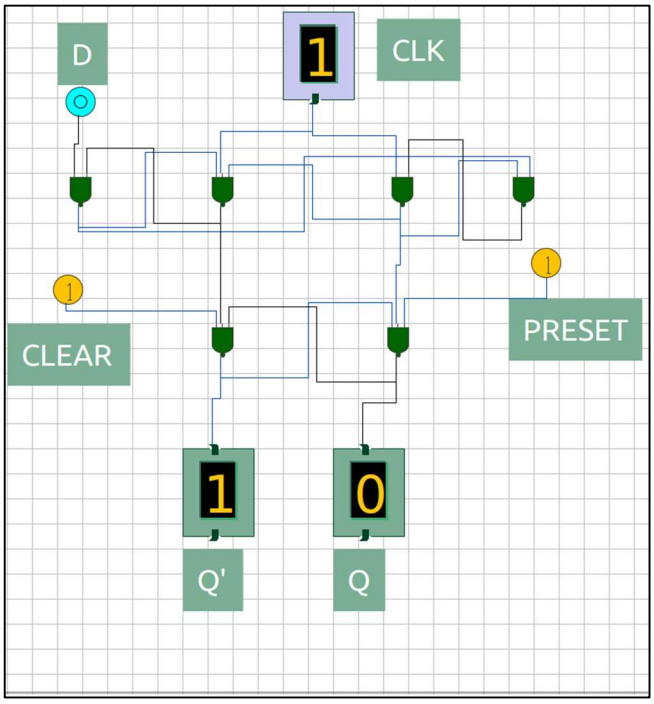


Figure 3: Q(t) = 1, D = 0; Q(t+1) = 0

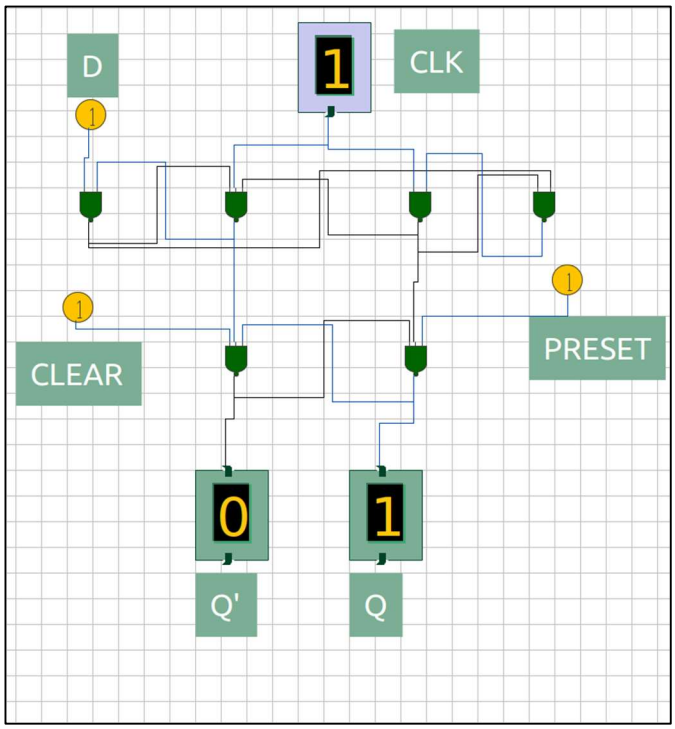


Figure 4: Q(t) = 1, D = 1; Q(t+1) = 1