10 Am 24/4/17

INDIAN INSTITUTE OF ENGINEERING SCIENCE AND TECHNOLOGY, SHIBPUR

B.E. 4th SEMESTER (CS) EXAMINATION, 2017

Computer Architecture and Organization – I (CS402)

FULL MARKS: 70 TIME: 3 Hrs

(Answer any five)

1. (a) What are the basic differences between bus master and bus slave? [2]
(b) How asynchronous data transfer differs from synchronous data transfer? [4]
(c) What is the advantage of using two way over one way type of asynchronous data transfer? [2]
(d) Why bus arbitration is required? Compare the performance of the three main bus arbitration schemes. [1+5]

2. (a) Define the following terms in the context of memory.
(i) Destructive read out (ii) Dynamic memory (iii) Cycle time (iv) Data transfer rate (v) Memory bus width [5]
(b) Compare the performance of direct mapped cache, fully associative cache and set associative cache. [6]
(c) What is the associativity of direct mapped cache? What is hit ratio? [3]

3. (a) What are the differences between the synchronous and asynchronous model of linear pipeline? [4]

(b) What is the speed up of a superscalar processor of degree 3 over the base scalar processor when the number of stages in the pipeline is 4 and the number of instructions to be executed is 9? [2]

(c) Define the following terms in the context of nonlinear pipeline:
(i) Latency cycle (ii) Forbidden latency (iii) Simple cycle (iv) Greedy cycle [8]

4. (a) What are the disadvantages of state table method in the context of hardwired control unit design? [2]
(b) What are the advantages and disadvantages of hardwired control unit? [3]
(c) What is control memory? How microcode compaction helps to minimize the size of control memory? [2+2]
(d) The microinstruction stored in the control memory of a processor have a width 26 bits. Each microinstruction is divided into three fields: a control field of size 13 bits, next address field of size X bits and MUX select field of size Y bits. There are 8 status bits in the input of MUX. How many bits are there in the X and Y fields? What is the size of control memory in number of words? [5]

5. (a) How many 256Kx4 bit memory is required to design 4Mx16 bit memory? [3]
(b) A computer has 256 Kbyte, 4-way set associative cache with block size 32 bytes. The size of address generated by the processor is 32 bits. Find the number of bits in the tag field of an address. [3]
(c) The access time of cache memory is 10 ns, hit ratio is 80%, average memory access time 24 ns. Find the access time of main memory? [2]
(d) An instruction is stored at location 300 with its address field at location 301. The address field value is 400. A processor register R contains the number 200. Evaluate the effective address for

direct, immediate, relative, index, register indirect addressing modes. What is the content of program counter? [5+1]

6. (a) A pipeline processor has 7 stages with latencies 2, 3, 4, 7, 3, 2 and 4 with 1 ns latency of latches. What is the minimum cycle time? [2]
(b) A non-pipelined system takes 50 ns to process a task. The same task can be processed using 6 segment pipeline with a clock cycle time 10 ns. Calculate the speed up for 100 number of tasks. [3]
(c) A magnetic disk has 1024 number of tracks, 512 number of sectors per track, 512 bytes per sector, 7200 rpm disk rotational speed and 9 msec seek time. Find data transfer rate. [3]
(d) Describe the followings
(i) Memory mapped IO vs. IO mapped IO (ii) Block transfer, cycle stealing and transparent DMA [2+4]

7. (a) Perform 5x-3 using Booth's algorithm. Consider 5 bit representation for each operand. [4]
(b) IEEE 754 representation of a number is given as 0 10000000 110 0000 0000 0000 0000 0000. What is the decimal value of the number if bias is 127? [2]
(c) Define the followings in the context of floating point number
(i) Normalization (ii) Overflow (iii) Underflow (iv) NaN [8]