Digital Logic Laboratory

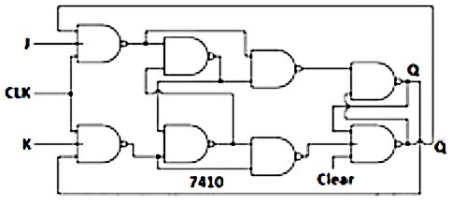
Assignment No. 4

Objective:

1. Design SR and D latches using NAND gates to verify the state table of respective latches.

2. Build flip-flops using NAND gates to:

a) verify the truth-table of a J-K Master Slave Flip-flop.



b) realise a D Flip-flop and verify the state table.

c) design an edge-triggered D Flip-flop and verify the state table.