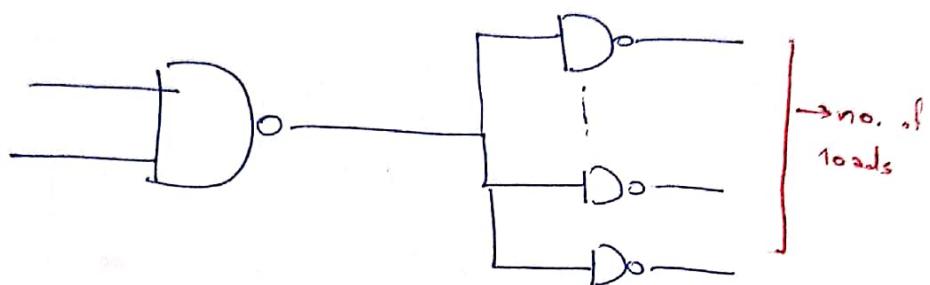


IC Digital Logic Families

Fan out

Specifies the number of standard loads that the output of the gate can drive without hampering its normal operation.

Eg



→ as signal gets divided, after a threshold no.,
the gates will receive very less power to actually work. That threshold is fan out.

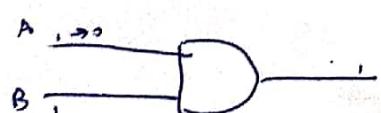
Power Dissipation

The power consumed by a gate

Propagation Delay

The average transition period for the signal to propagate from input to output, when the signal changes its value.

Eg



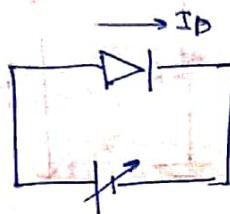
	A	B	Y
t_1	1	1	1
lrd	0	1	1
t_2	0	1	0

$$\text{propagation delay} = t_2 - t_1$$

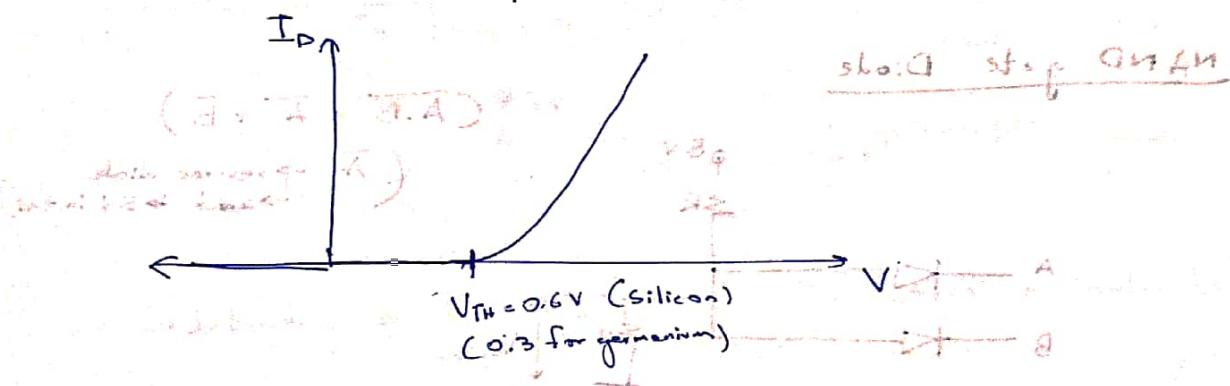
Noise Margin

The limit of a noise voltage which may be present without hampering the proper operation of the circuit.

Diode

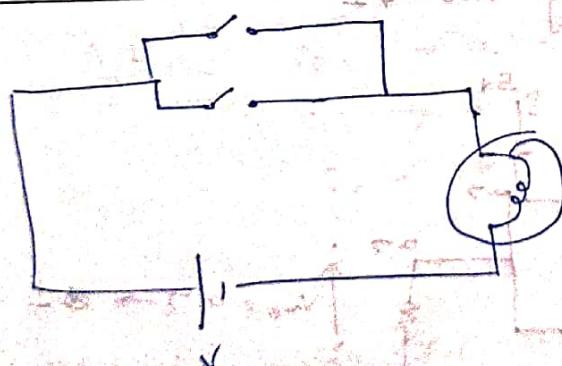


(assume silicon semiconductor)
(threshold $V = 0.6 \text{ V}$)
(for germanium, $V_{th} = 0.3 \text{ V}$)



∴ it can be used as switch.

A switch will function as (OR) logic function. As if if any switch closes bulb will glow.

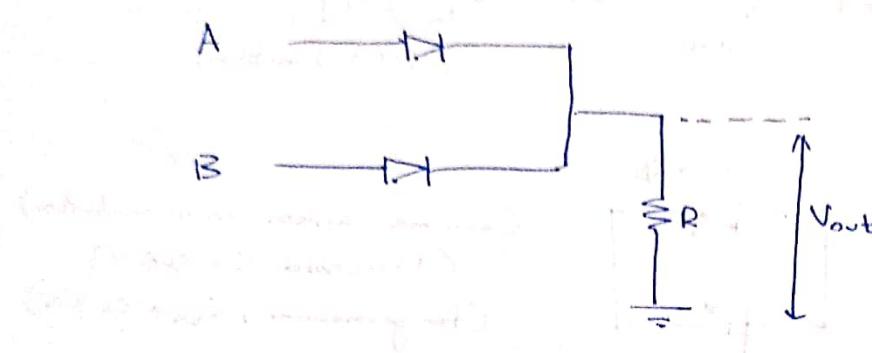


glow $\rightarrow 1$
off $\rightarrow 0$

OR gate Diode

0 V \rightarrow off \rightarrow 0 ($0 - 0.6$ V) (assuming S.)

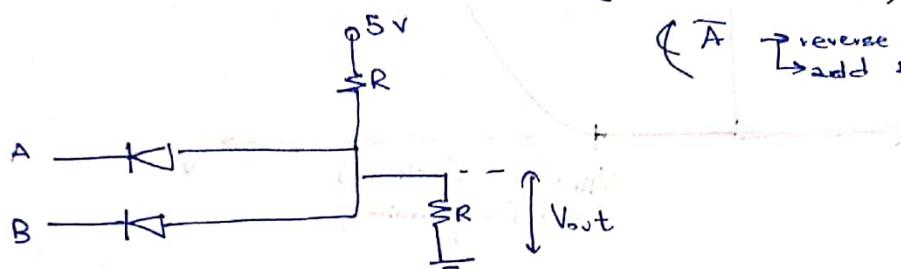
~~more than~~
5 V \rightarrow logic 1. (> 0.6)



NAND gate Diode

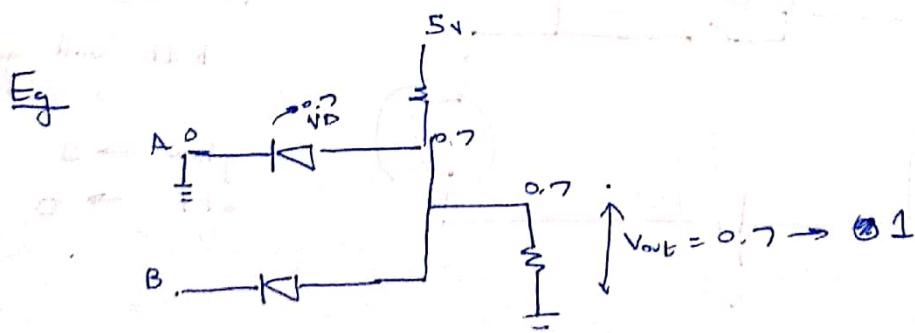
$$(\overline{A \cdot B} = \overline{A} + \overline{B})$$

(\overline{A} \rightarrow reverse diode
 \rightarrow add $\rightarrow 5V$ in end)



If A becomes ground ($A=0$), current flows through A.

(almost 0 res), making $V_{out} = 0.1$



→ if $A, B = 5V$, no current flow through diode,
 → making $V_{out} = \frac{5-0}{2R} = 2.5V \rightarrow 0$

Transistor

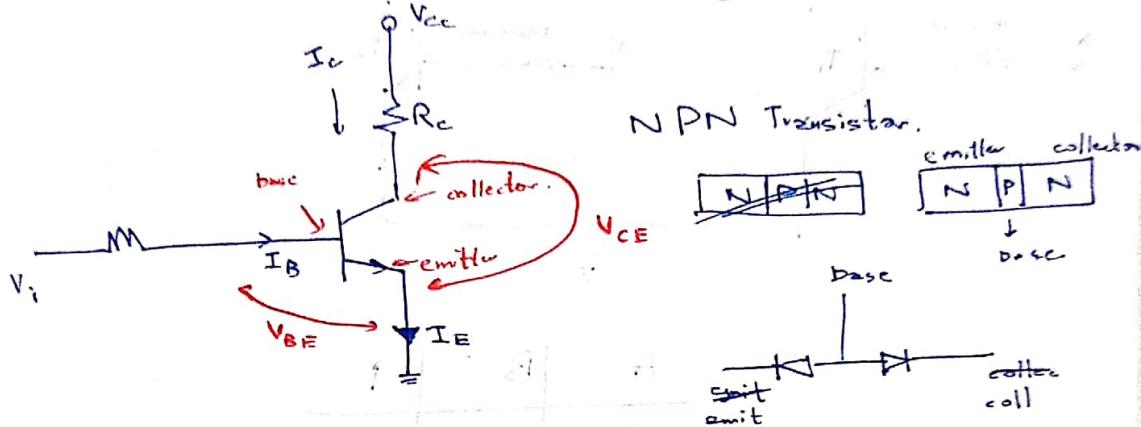
→ have 3 phase.

→ cutoff ($C \log_2 0$)

→ active ($C \log_2 1$) (not used, used as amp)

→ saturation ($C \log_2 2$)

(remember Top Today)



→ depending on I_B , transistor goes to cutoff or saturation

Cutoff: $V_{BE} < 0.6$

$V_{CE} \Rightarrow$ open (∞V)

$I_B = I_C = 0$

Active: $V_{BE} \rightarrow 0.6 - 0.7 V$

$$I_C = h_{FE} I_B$$

DC current gain. (Transistor parameter)

Saturation: $V_{BE} \approx (0.7 - 0.8)V$

$$V_{CE} = 0.2 V$$

$$I_B \approx \frac{I_C}{h_{FE}}$$

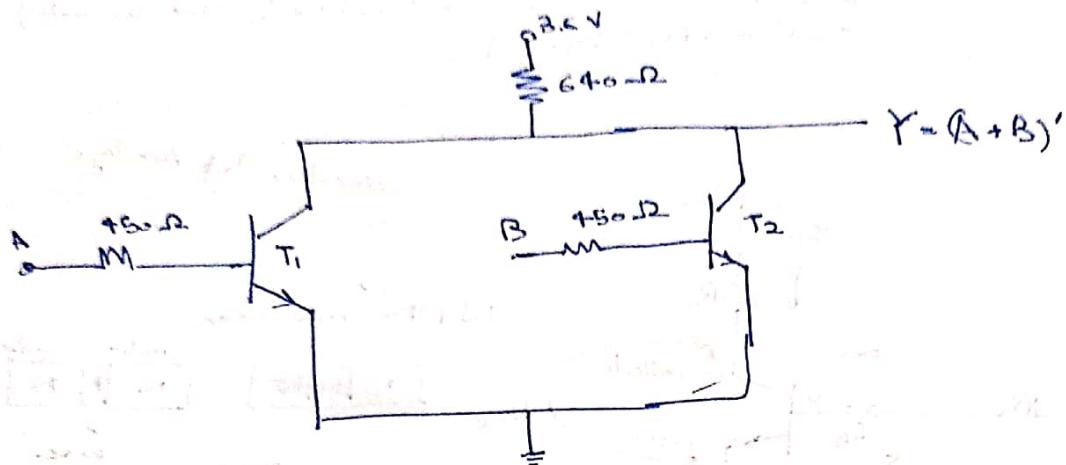
→ Transistor is called a current controlled device.
 (we control it by I_B)

Resistor Transistor Logic (RTL)

→ basic gate: NOR gate

→ Logic 0 : 0.2 V

→ Logic 1 : ~~1.2816 V~~ 1 - ~~2.28~~ 3.6 V



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

→ if $A = 3.6, B = 0$, $T_1 \rightarrow$ saturation $\rightarrow Y = 0$
 (T_{ap} open)

$A = 0, B = 3.6$, $T_2 \rightarrow$ saturation $\rightarrow Y = 0$

$A = 3.6, B = 3.6$, $T_1, T_2 \rightarrow$ saturation $\rightarrow Y = 0$

$\rightarrow A = 0, B = 0 \rightarrow T_1, T_2 \rightarrow$ cut off
 (T_{ap} off) $\rightarrow Y = 1$

→ if any of $A, B = 3.6$, $V_{CE} = 0.2$, making

$$Y = \frac{3.6 - 0.2}{640} \cdot 0.2 \rightarrow 0$$

\rightarrow if both $A, B = 0$, cut off $V_{CE} = \infty$

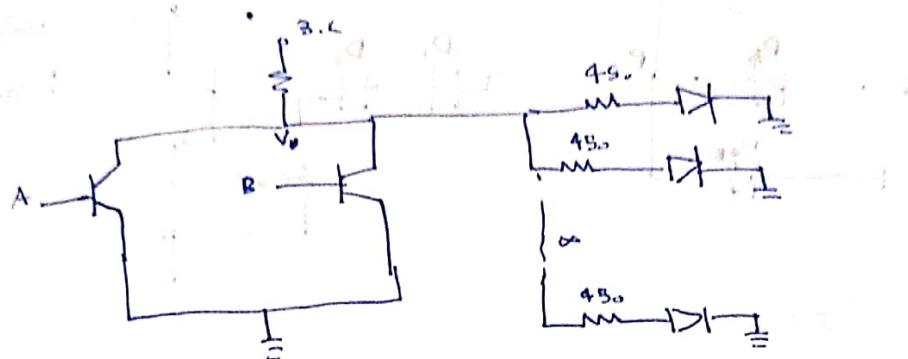
$$Y = 3.6 V \rightarrow 1$$

Fan out = 5

Power Dissipation: 12 mW

Propagation Delay: 25 ns

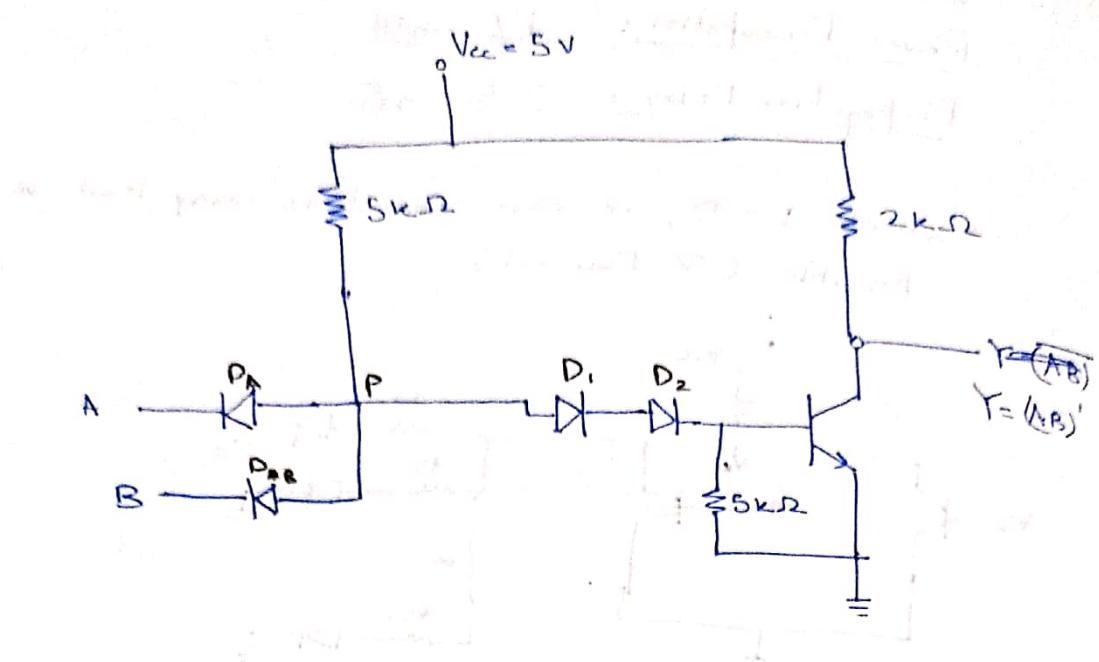
→ when $\gamma = 0$, we can connect as many load as possible (as Fan out)



→ when $\gamma = 1$, as we keep increasing load, Voltage for load decreases, when it become less than 0.2, it hampers the output, hence $\gamma=1$ is limiting factor for fan out.

(more load, more current, V decrease, after limit γ changes)

Diode Transistor Logic (DTL)



0 - 0.2V : Low level Logic

4-5V : High Level Logic

Basic Gate: NAND Gate

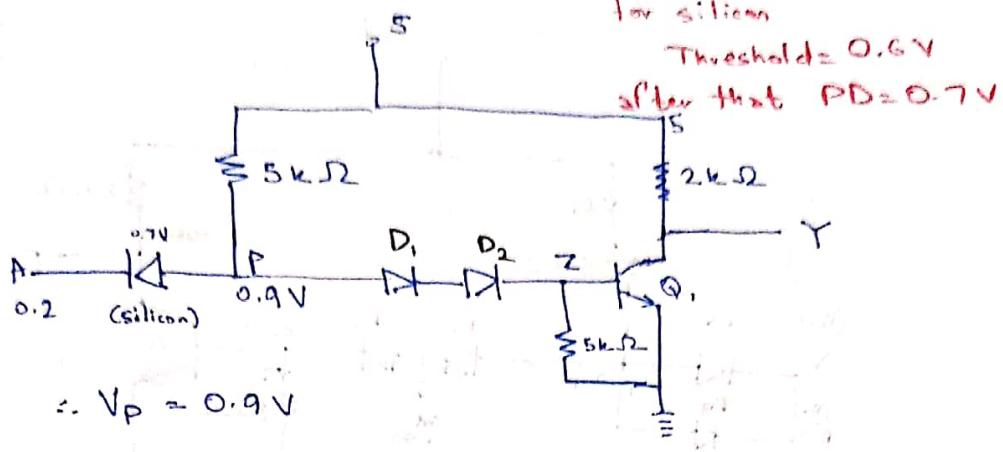
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

\rightarrow if $A = 0.2V, B = 5V$
~~V_P = 0.2V~~ $\therefore V_P = 0.2V$ $V_A = 0.2V$

\rightarrow ~~D_A~~ with conduct

hence

I) if $A = 0.2 \text{ V}$, $B = 5 \text{ V}$
 $\rightarrow D_A$ will conduct at $V_P = 0.2 \text{ V}$



~~$V_Z = 0.9V$~~

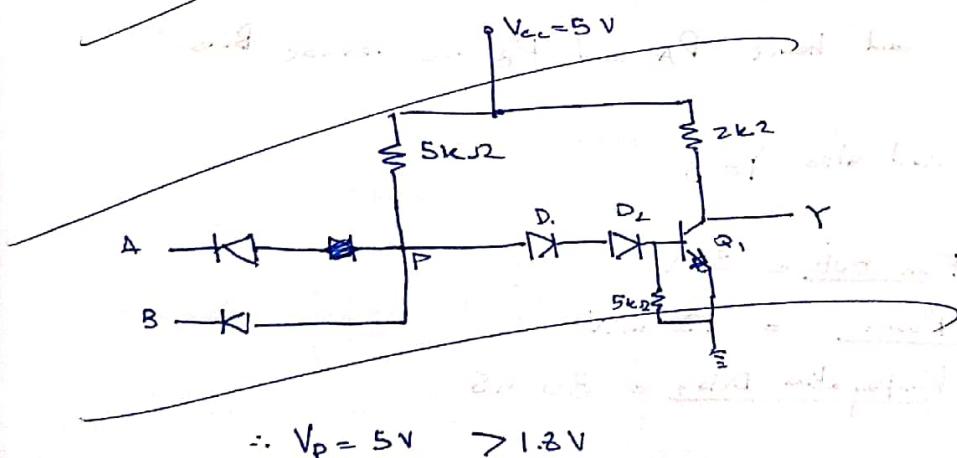
\rightarrow To run Q_1 , we need min. $V_p = 1.8V$

as we need $0.6 \times 2 = 1.2V$ for D_1 and D_2 and
more $0.6V$ for Q_1 to run.

\rightarrow but $V_p = 0.9V$, so Y will remain at logic 1

II) if $A = 5V$, $B = 5V$

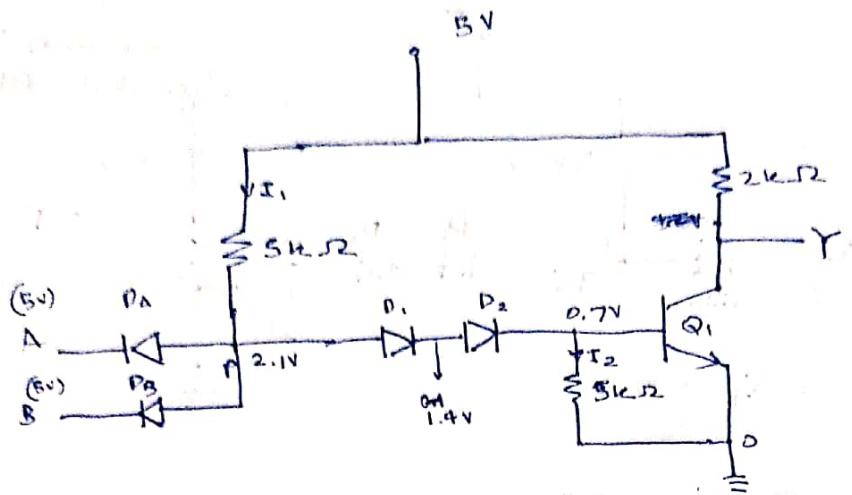
~~$\rightarrow D_A$ and D_B will not conduct~~



$\therefore Q_1$ will be active; $Y = 0$

II) if $A = B = 5V$

$\therefore D_A$ and D_B will not flow



$$\therefore I_B = I_1 - I_2 \quad (\text{Transistor saturation})$$

$$\therefore V_{CE} = 0.2V$$

$$\therefore V_{ES} - V_E = 0.2V$$

as both diodes D_1 and D_2 and Q_1 are flowing,

$$\text{Voltage Drop} = 0.7 \times 3 = 2.1V$$

$$\therefore V_{PE} = 2.1 + V_{CE} = 2.3V$$

$$V_{DA} = 2.1 - 5 = -2.9 = V_{DB}$$

and hence D_A and D_B are reverse biased

and also $Y = 0$

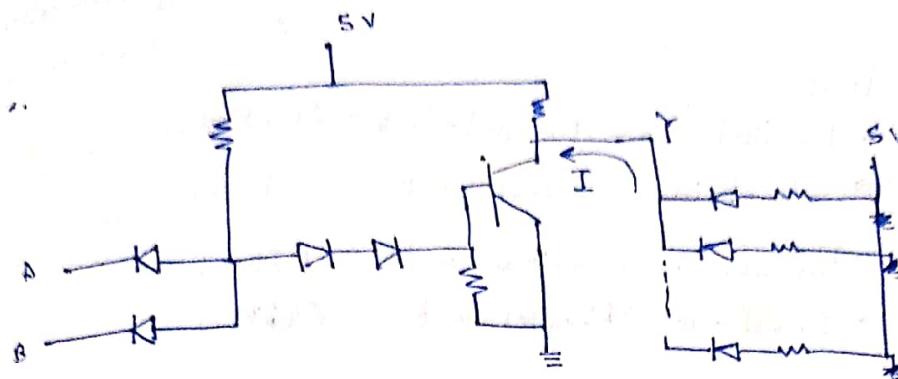
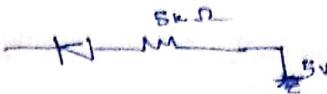
$$F_{out} = 8.4V$$

$$\text{Power} = 12mW$$

$$\text{Propagation Delay} = 30\text{ ns}$$

Limiting Fan out

Let Load be



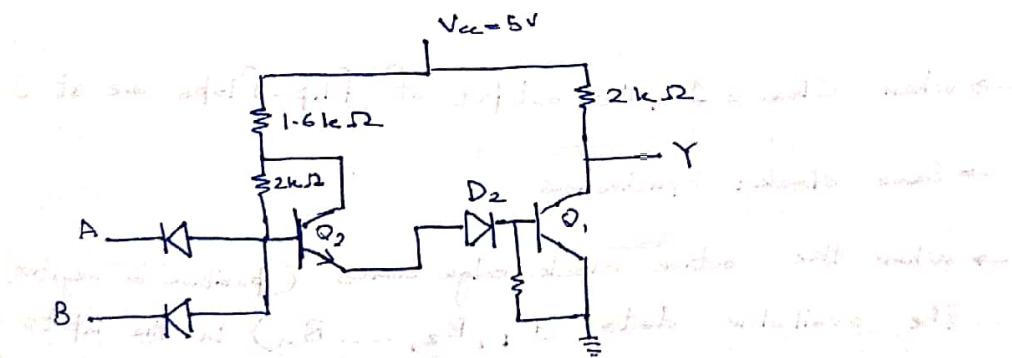
when $Y=1$, PD between load diode is ~~is~~ not flowing

when $Y=0$, current flowing to DTL, hence I_C will increase

as $I_B h_{FE} \geq I_C$ for saturation

as $I_C \uparrow$, after some load, transistor come out of saturation, hampering DTL

Alternative circuit to increase fan out



→ when Q_1 is saturated, Q_2 is active

$$Q_2 \text{ active } I_E = I_B + I_C$$

$$I_E = h_{FE_2} I_B ; I_B \text{ can be increased}$$

→ as hence I_E can be increased, which is I_B for Q_1

∴ for Q_1 : $I_B h_{FE_1} \geq I_C$

and Q_2 saturation can be maintained.

Using Q_2

can be increased will increase due to load

TTL

→ Transistor Transistor Logic

→ Types

→ Standard TTL

Standard TTL

Propagation Delay: 10 ns

Power Dissipation: 10 mW

Low Power TTL

Propagation Delay: 33 ns

Power Dissipation: 1 mW

High-Speed TTL

Propagation Delay: 6 ns

Power Dissipation: 22 mW

~~★ Schottky TTL~~

Propagation Delay: 3 ns very fast flip flop after

Power Dissipation: 19 mW with short switches

Low Power Schottky TTL

Propagation Delay: 9.5 ns

Power Dissipation: 2 mW p. & n channel diff.

→ all TTL family has three types of output configs:

→ Open-Collector TTL

→ Totem-Pole TTL

→ Tri-State TTL

V_{out} (open): V_{cc} = 9V

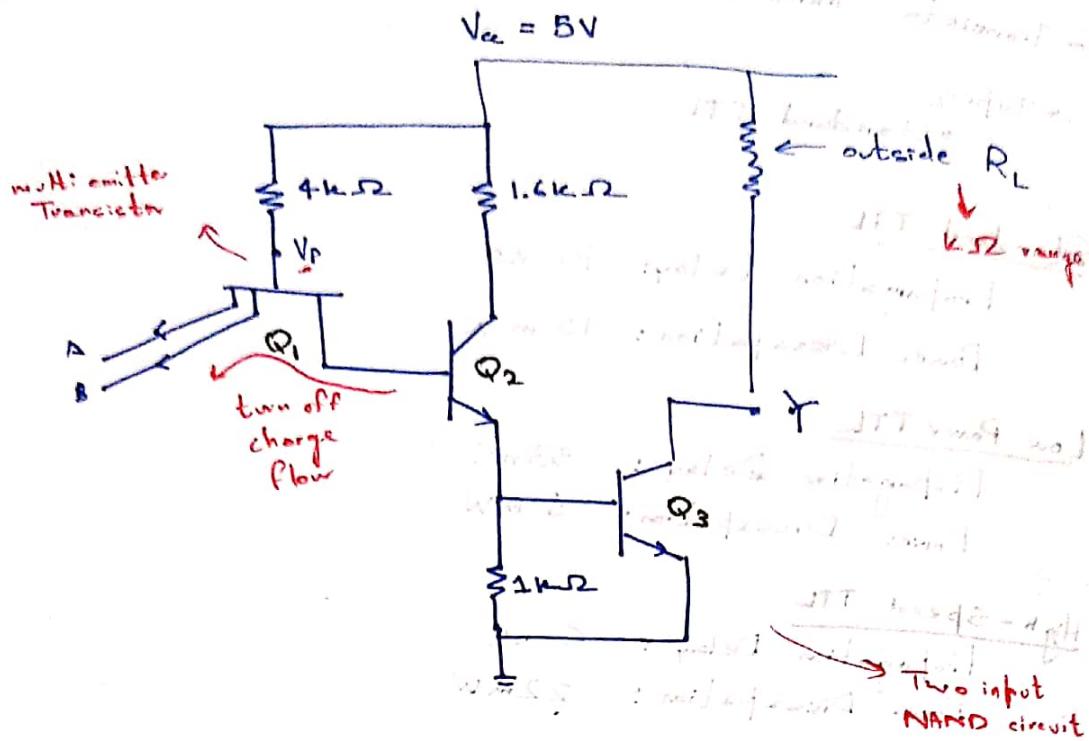
Output current of logic 0 is 0.01 A

Output current of logic 1 is 0.01 A

V_{th} (threshold)

V_{cc} = 9V

Open Collector TTL



→ To get output you have to externally connect resistor from V_{cc} to Y :

\rightarrow Low Level = 0.2 V

\rightarrow High Level = 2.4-5. V: voltage limit

→ Basic Circuit: NAND gate (part 1) ITT No. 1

\rightarrow if $A = 0.2V$, $B = 5V$ ($A = 0, B = 1$, Y should be 1)

$$V_P = 0.9 \text{ V} \quad (0.2 + 0.7) \text{ flowing V}$$

→ To get $V=0$, we need to cross the transistor
 $V_B = 0.6 + 1.2V$

$$\therefore \min V_p = 5 \times 0.8 = 1.8 \text{ V}$$

\downarrow
threshold V

$$\therefore V_p = 0.9 \text{ V}$$

$$\therefore Y = 1$$

→ if both $A = 0.2 \text{ V}$, $B = 0.2 \text{ V}$

$$V_P = 0.9 V$$

$$x = 0 \quad y = 1$$

→ if $A = S_V, B = S_V$

$$\rightarrow V_P = S_V$$

∴ $Y = 0$ [Q₁, Q₂, Q₃ saturation]

$$(V_Y = 0.2 \text{ V if } Q_3 \text{ saturates})$$

→ This is similar to DTL but propagation Delay in DTL is 30 ns, but here it is 10 ns, why?

→ consider initially A=S_V, B=S_V, Q₁, Q₂, Q₃ saturate.

→ why any of A or B (say A) becomes 0.2 V

Q₁ goes to active, base of Q₂ gives charge to Q₁, making turnoff faster.

→ Application of Open Collector.

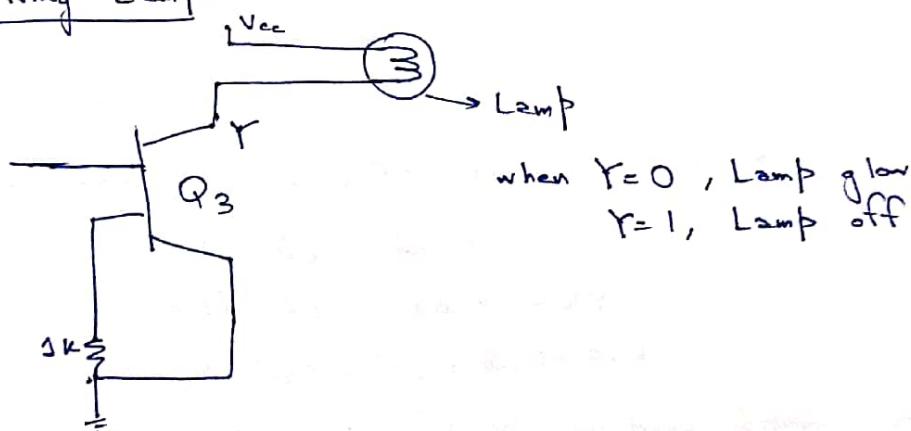
→ Driving Lamp or Relay or load etc.

→ Wired Logic for interconnection of logic

→ Construction of Common Bus System.

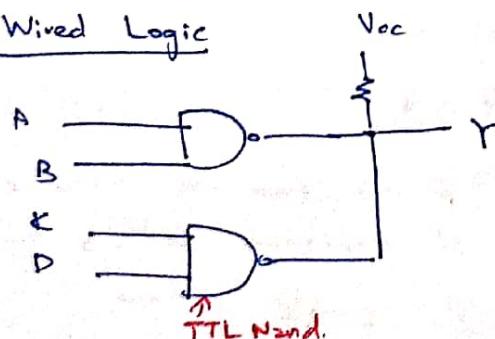
more details in notes about applications

Driving Lamp



when $Y=0$, Lamp glow
 $Y=1$, Lamp off

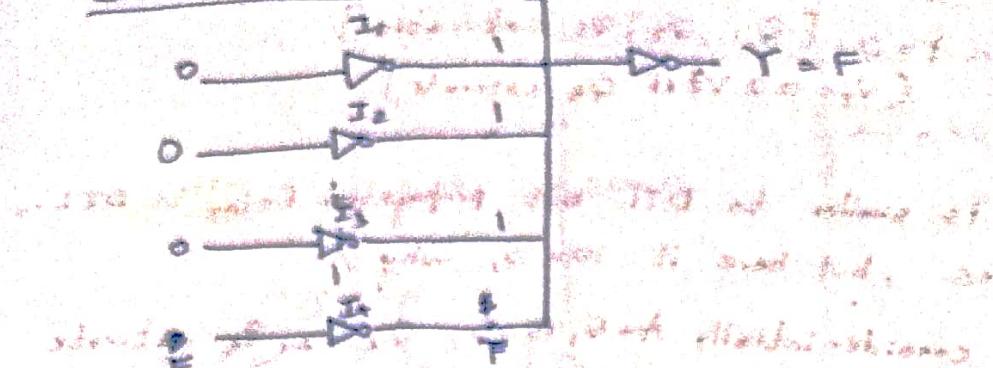
Wired Logic



→ output of TTL's can be connected

$$Y = (\overline{AB})' \cdot (\overline{CD})'$$
$$= (A+B) + (C+D)$$

Common Bus System

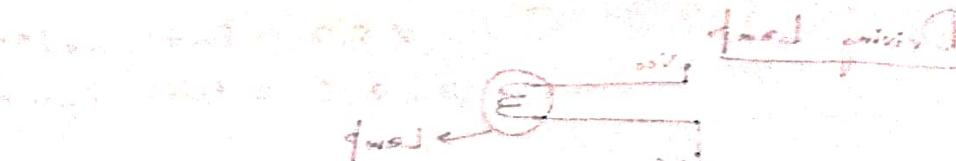


keep input for all $I_{in} \neq 0$
and to use I_{in} as signal

$\rightarrow Y = I_{in}$ input

~~inverted signal to make it a~~
 \rightarrow hence we can ~~also~~ connect lot of pulses of several
systems to one output ~~and having~~
~~inverted and non inverted signals~~
~~These not gate can be made by TTL~~

\rightarrow Systems can be made by TTL NAND GATE



Half quad, $Q = Y$ and
The quad, $Q = Y$



Half quad, $Q = Y$ for $I_{in} \neq 0$ and signal with
Inverters at $I_{in} = 0$ & TTL to logic 0



Output

inverters

Tafam - Pole TTL then went back to the stage area.

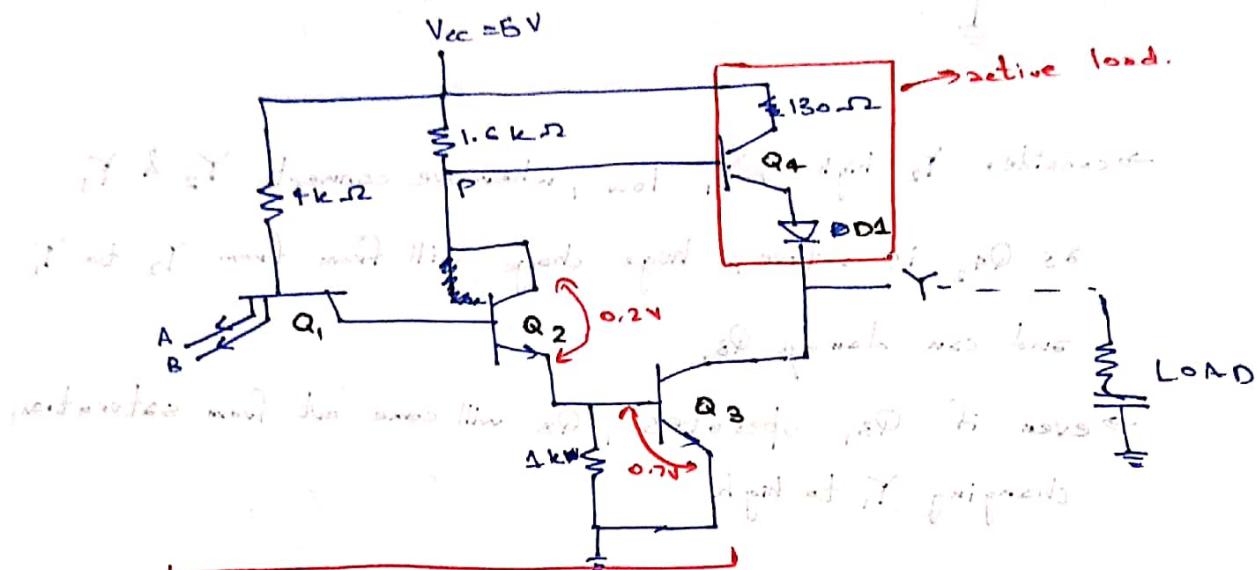
→ Why Totem-Pole.

→ In open circuit, propagation delay depends on output load (RL)

Beta i Load Resistance and Capacitance. (RC) P.D.

$\rightarrow R_{\text{in}}$ if we could reduce value of R , delay could decrease.

→ Tafey + Pote achieves this by changing passive P_2 to an active component.



Previous Circuit

Self as a component of the final 0 level signal

→ when $A = B$, Q_2, Q_3 for saturation ($X=0$)

$$\rightarrow f_{\text{av}} \text{ at } Q_3, V_{BE} = 0.7 \text{ V}$$

$$\rightarrow f_{ar} \text{ } Q_2, V_{CE} = 0.2V$$

$$\therefore V_p = 0.9V = (0.7 + 0.2)$$

→ To conduct through Y, we pass ~~I₁~~. Q₄ & D.

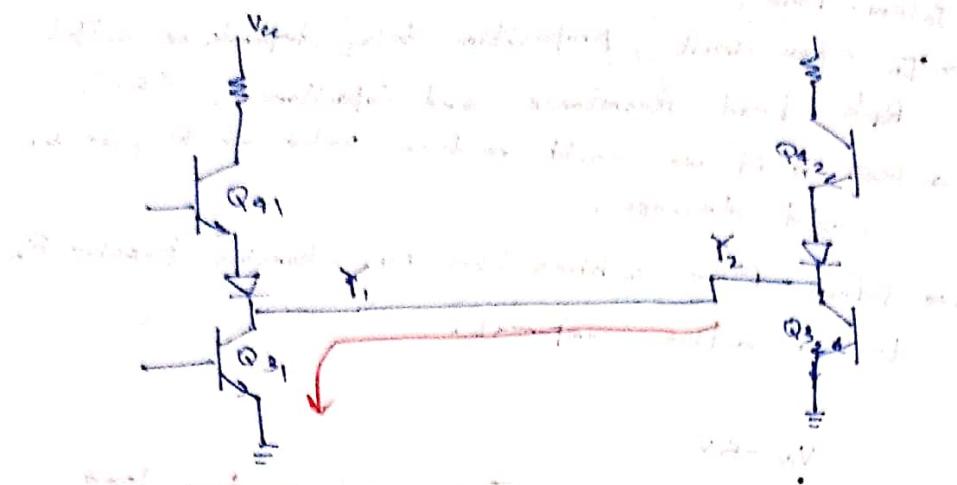
$$\therefore \min V_p = 0.6 \times 2$$

* ∴ R Resistance of active load high.

→ when ~~any~~ goes off. ($y=1$)

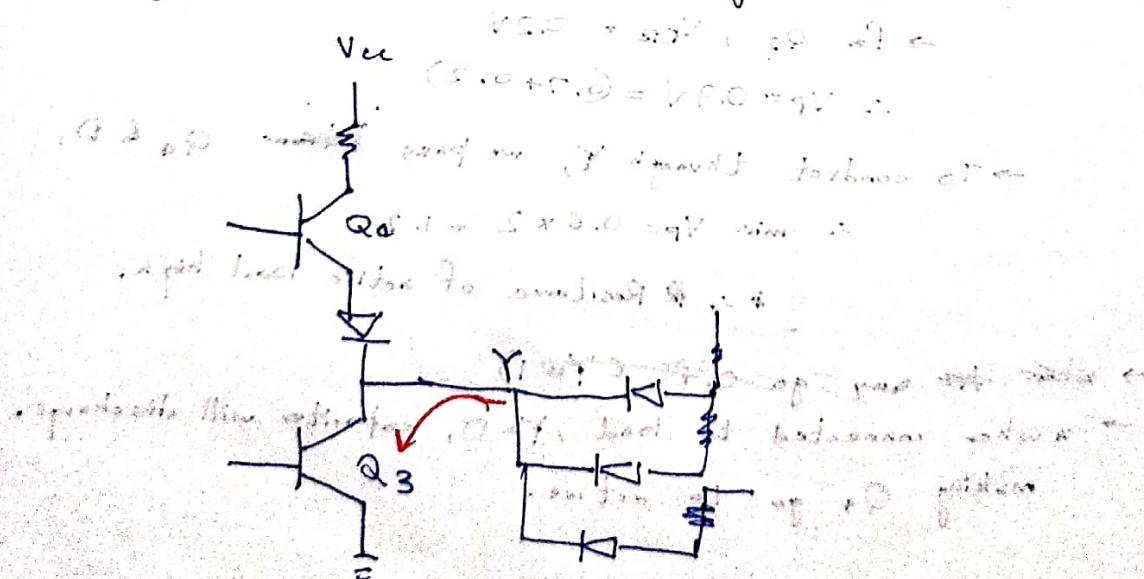
→ when connected to load, $\gamma = 0$, capacitor will discharge, making Q go to active.

→ we can't do wired Logic with Totem-pole.

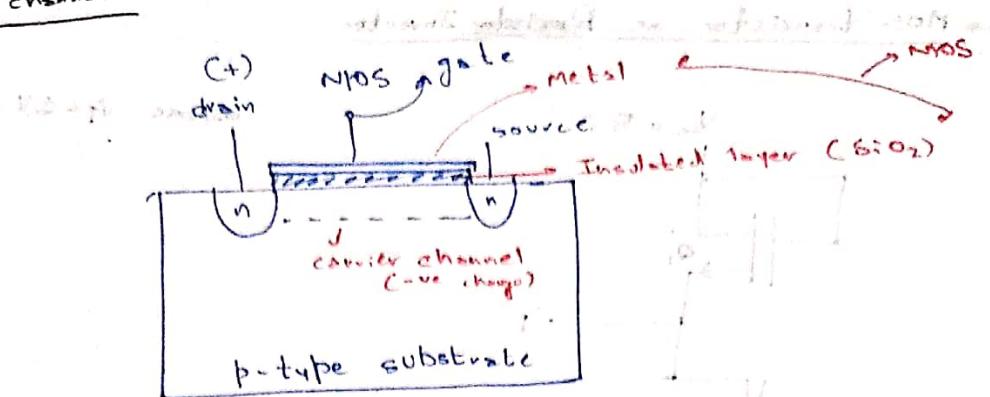


- consider Y_2 high, Y_1 low, when we connect Y_2 & Y_1 ,
as Q_{92} is active, huge charge will flow from Y_2 to Y_1 ,
and can damage Q_3 .
- even if Q_3 operates, Q_3 will come out from saturation,
changing Y_1 to high

→ Logic Level 0 limit fan out for totem-pole, as $Y=0$,
more load will inject current to Q_3 , after a limit, Q_3
goes out of saturation, changing output



n-type channel



→ When +ve voltage applied on drain, p-type substrate and Metal layer becomes like capacitor, forming a channel of carriers.

→ we can also make a p-type channel where all

- i) n-type becomes p-type due to +ve volt.
- ii) p becomes n
- iii) source is +ve due to -ve volt.
- iv) channel is of +ve charge.

Two types of MOS can operate

- i) Depletion mode
- ii) Enhancement mode

Depletion mode → Channel slightly doped with n-type, it decreases threshold

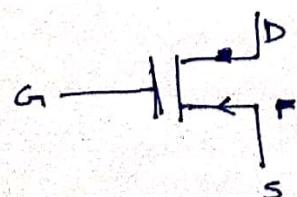
V_{DS} > 0 → The channel gets depleted as MOS becomes insulator from the +ve volt.

Enhancement mode

→ No channel initially

→ As we increase voltage, Channel gets made, enhancing channel region.

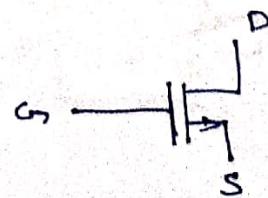
Symbol of p-channel MOS



$$V_{GS} = -ve > V_T$$

Eg conduct when $V_T = -1$ &
 $V_{GS} = -1.5$

n-channel

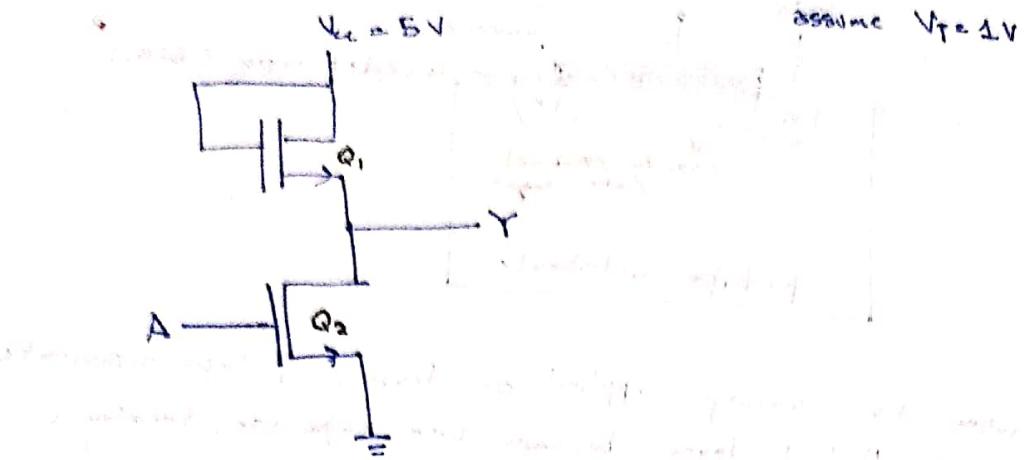


conduct when

$$V_{GS} = +ve > V_T$$

Threshold

MOS Transistor as Register Inverter

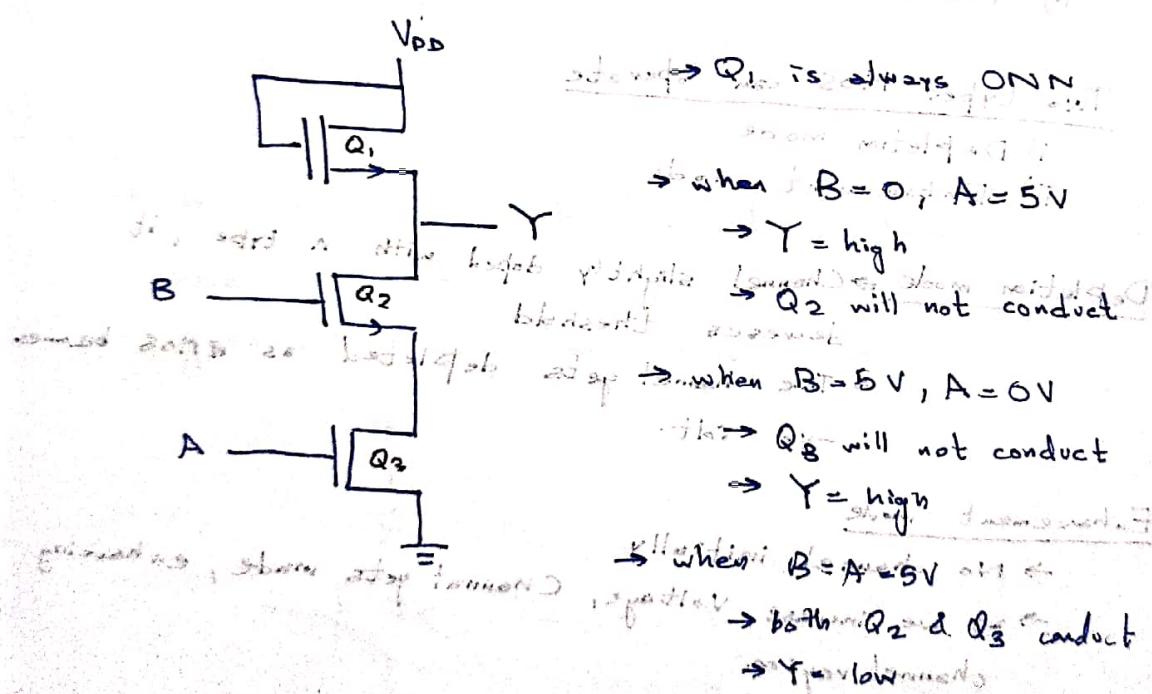


→ Q_1 is always on as Gate connected to V_{cc}

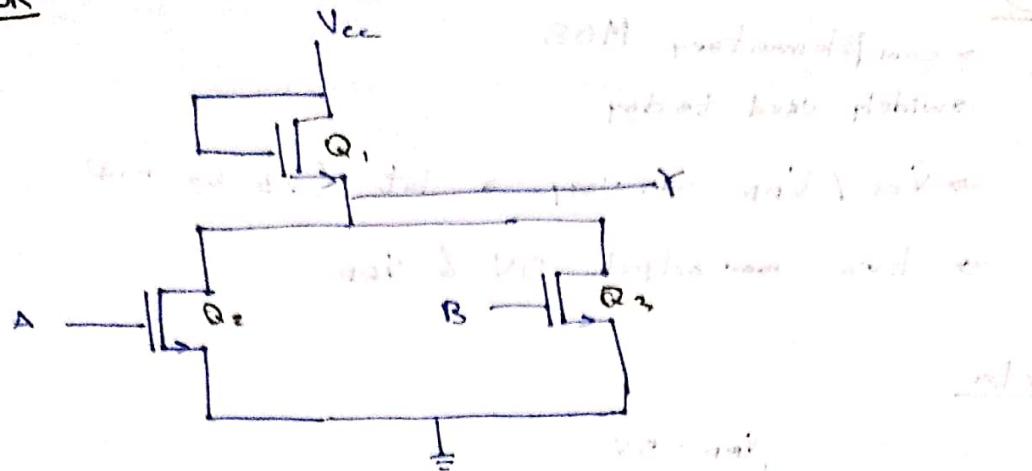
→ when $A = 0$, Q_2 will not conduct, $Y = 1$

→ when $A = 1$ (sat), Q_2 will conduct, $Y = 0$

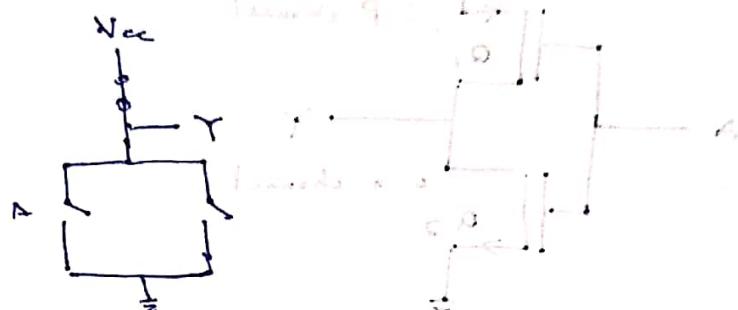
NAND



NOR



Simple diagram



→ Q_1 always conduct

→ when any A or B , $Q \rightarrow Y = \text{high}$

→ when none A and B , $Q \rightarrow Y = \text{low}$.

Because $Q_1 \in Q_2$, $Q = Q_1 + Q_2$ reduces

1st:

2nd:

3rd:

4th:

5th:

6th:

7th:

8th:

9th:

10th:

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CMOS

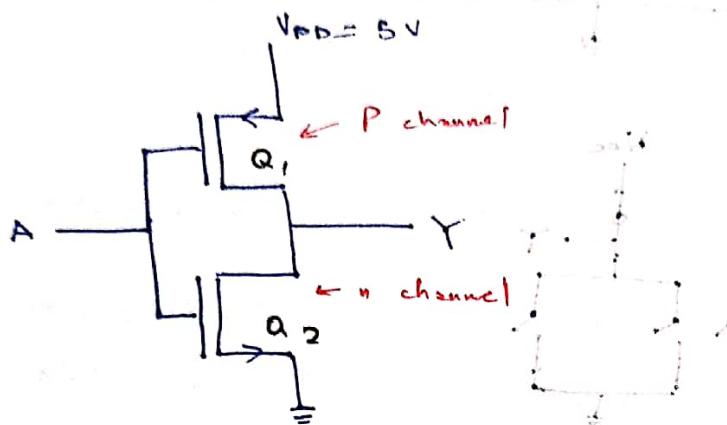
→ complementary MOS

→ widely used today

→ V_{DD} / V_{SS} can vary a lot ($+3$ to $+12$)

→ two main output, OV & V_{DD}

Inverter



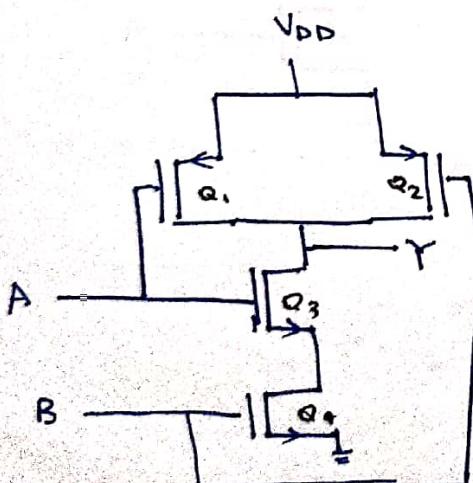
→ when $A = 0$

for $Q_1 \rightarrow V_{GS} = -5V \rightarrow$ not conduct

for $Q_2 \rightarrow V_{GS} = 0V \rightarrow$ not conduct

$$\therefore Y = 1$$

NAND



when $A = B = 0$, Q_3, Q_4 conduct

$$Y = 1$$

When $A = 5, B = 0$

Q_1 not conduct
 Q_2 not conduct

Q_3 conduct
 Q_4 not

$$\therefore Y = \text{high}$$

→ when $A = B = 5$

Q_1, Q_2 not
 Q_3, Q_4 conduct

$$\therefore Y = 0$$

Tri-State TTL

→ As Totem-Pole can't handle wired input, we use Tri-State.

→ There are three possible output.

$Y = 0, 1 \text{ or high impedance.}$

→ here Q_6, Q_7, Q_8 are open collector TTL and Q_1, Q_2, Q_3, Q_4, Q_5 are totem-pole TTL

→ When $C=0$ ($0V \approx 0.2V$)

→ Q_7 and Q_8 not flow, Q_6 flow

→ base voltage $Q_6 \rightarrow V_{BE} = \text{conducting}$

V_{BE}

voltage at the base of $Q_6 = 0.9V$
($0.2 + 0.7$)

↑
conducting
threshold

→ but for Q_2 to flow, we need at least 0.6×3
 $= 1.8V$, so Q_2 not flow (similar to open collector TTL)

→ hence for D1  (can be ignored)

→ now when $A = \text{high}$

$Q_2, Q_3 \rightarrow \text{on}$

$Q_4 \rightarrow \text{off}$ $Y = \text{low}$

→ now when $A = \text{low}$ ($0.2V$)

$Y = \text{high}$.

$C=0$, NOT gate

→ when $C=1$

→ Q_6 not flow, Q_7, Q_8 flow (saturation)

∴ D1 conducts

→ Q_1 conducts $\rightarrow Q_2$ off

→ Q_5 base voltage = $0.9V$, but we need $0.6+2V$

($C=1$, high impedance ∵ Q_4 not conduct)

∴ Y is basically open (high impedance)

Circuits

Infra-red sensor detected from short range at 10 cm
at 10 cm \rightarrow Vcc = 12V \rightarrow 12V

shorting diodes of 100 ohm connected to
shorted output of 12V \rightarrow T

and T releases logic and 8955 & 8956 remain
T222 triggered on 12V, 8955, 8956, 8957 turn

(8956) and makes
motor 8957 work for 8956 base 8957

protection against short connection \rightarrow

motor to work with the ~~short~~
(open)

motor driver based on motor with 8956
motor driver work for 8956 V 3.12
motor driver work for 8957 vehicles

(example no 3) \rightarrow K1000 L4 not sensed
motor driver work for 8956
motor driver work for 8957

motor driver work for 8956 (V 3.12) and L4 makes working
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motor driver work for 8957 (V 3.12) and L4 makes working

- This circuit can be used for wire logic
- for Bus, all but one should be in high impedance and one should give data.

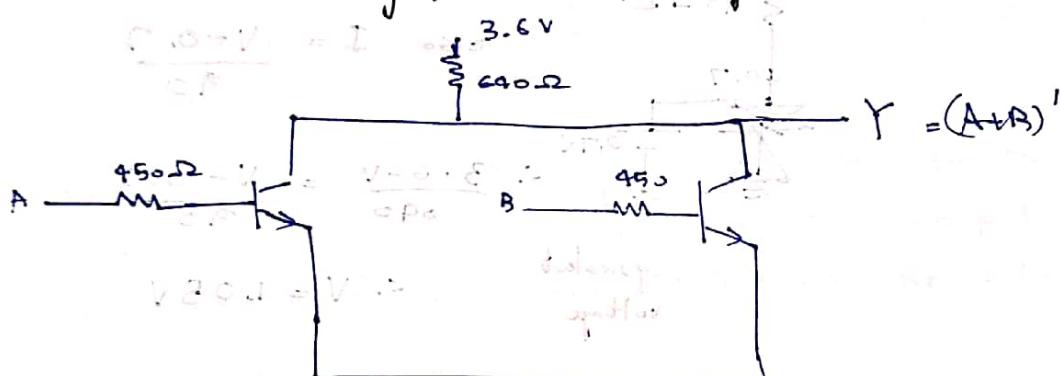
Q) DTL question

Q) a) Determine high-level output voltage of RTL for a fan-out of 5

b) Determine the min. input voltage required to drive an RTL

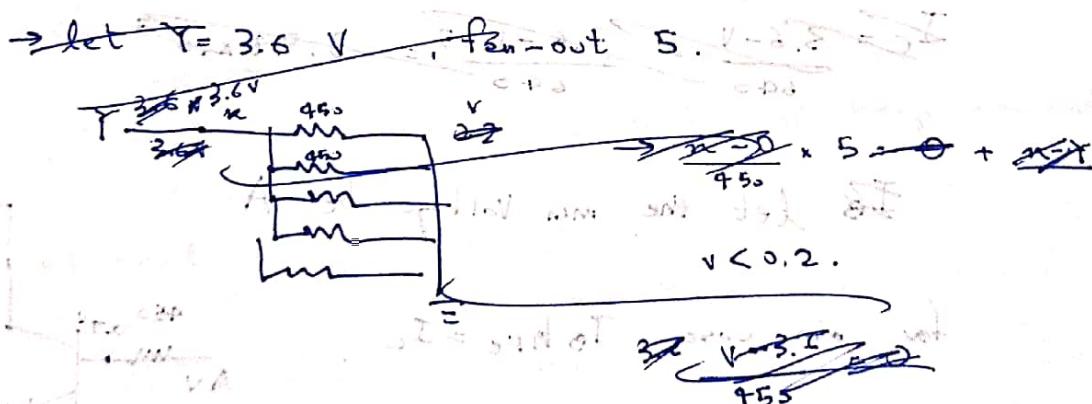
Transistor ~~base~~ to saturation when $h_{FE} = 20$.

c) find noise margin when input high, and fanout 5



$V_{BE(on)} = 0.7V$, $0.8V - 0.7V = 0.1V$ of noise is tolerated.

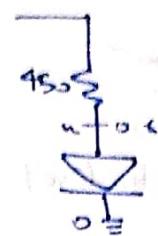
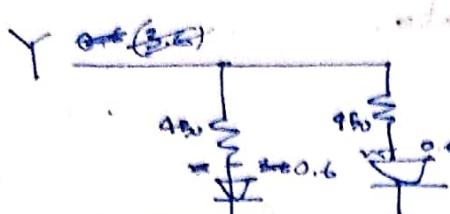
→ LOAD → similar inputs will be connected.



(5)

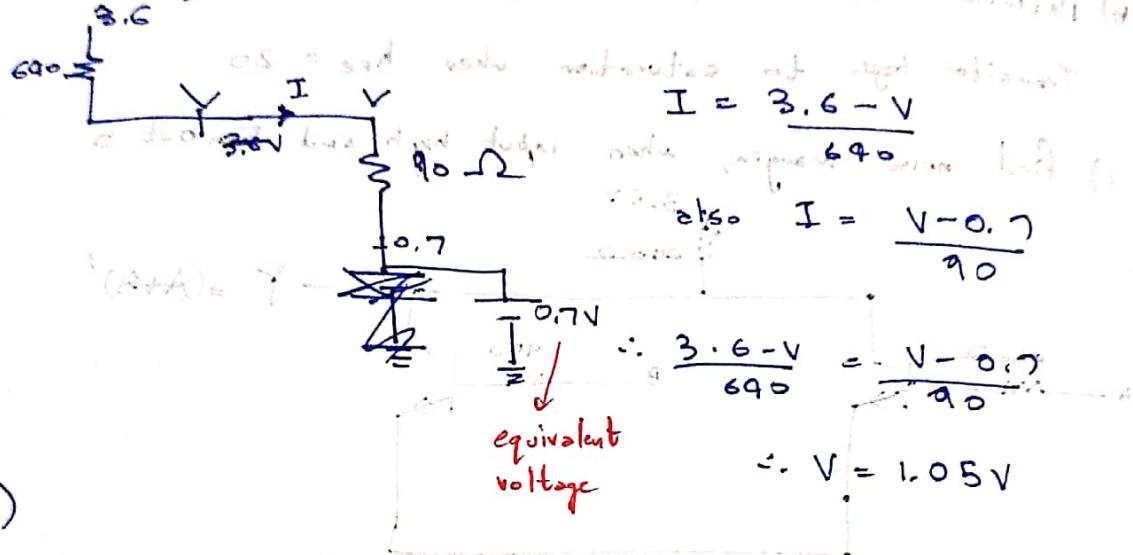
$$V_{BE(on)} + 0.2 = 0.7 + 0.5 + 0.2 = 1.4V$$

simplifying



3.7. March

QPS \rightarrow equivalent circuit after input voltage is applied (a)



b)

Saturation: $I_B \geq \frac{I_c}{h_{FE}}$, $h_{FE} = 20$, $V_{CE} = 0.2V$

and now we have to find minimum value of I_B

~~$I_C = \frac{3.6 - V}{690} = \frac{3.6 - 1.05}{690} = 3.93 \times 10^{-3} \text{ A}$~~

let the min. voltage be A

for min. case, $I_B h_{FE} = I_C$

$$\therefore I_C = \frac{3.6 - 0.2}{690} = 5.31 \times 10^{-3}$$

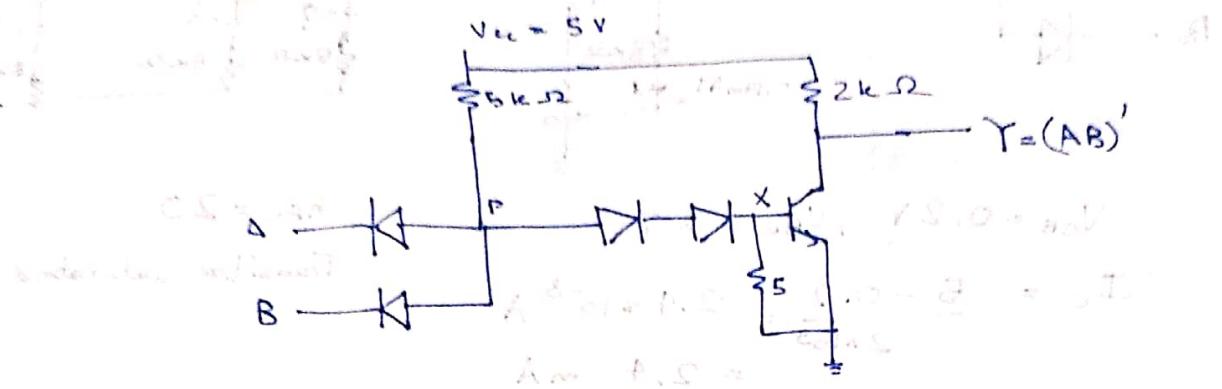
$$\therefore I_B \cdot \frac{I_C}{h_{FE}} = \frac{3.6}{690 \times 20} = 2.65625 \times 10^{-4} \text{ A}$$

$$\text{now } I_B = \frac{A - 0.7}{450} = \frac{3.4}{690 \times 20}$$

$$A = 0.7 + \frac{3.4 \times 450}{690 \times 20} = 0.819 \text{ V}$$

c) Noise Margin = $1.05V - 0.819V$
 $= 0.23V$

Q) Show that output transistor of DTL gate goes to saturation, when all inputs are high, if $h_{FE} = 20$.



when $A=B=5V$, $V_P = 8V$, $V_x = 5 - 1.4V = 3.6V$
 (done in Theory)

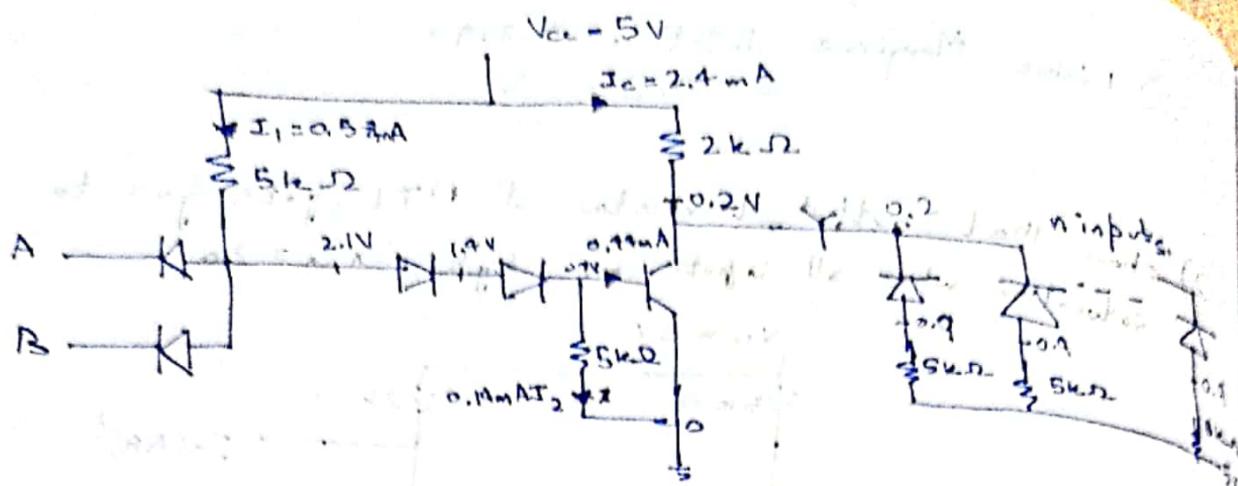
Q) Connect the output Y of the DTL gate to N inputs of other similar gate. Assume that the output transistor is saturated & base current = $0.49mA$. $h_{FE} = 20$

- a) calculate current in $2k\Omega$ resistor.
- b) calculate the current coming from each input connected to the gate

c) Calculate the total collector current in the output transistor as a function of N .

d) Find the value of N that will keep transistor in saturation at $I = 0.49mA$

e) what is Fan-out?



$$V_{CE} = 0.2V, V_{BE} = 0.7V$$

$$I_c = \frac{5 - 0.2}{2 \times 10^3} = 2.4 \times 10^{-3} A = 2.4 \text{ mA}$$

$$h_{FE} = 20$$

Transistor saturated

$$I_B = \frac{5 - 2.1}{5 \times 10^3} = 0.5 \text{ mA}$$

$$I_B = \frac{5 - 0.7}{5 \times 10^3} = 0.74 \text{ mA}$$

b) When $V_D = 0$, current coming from each gate is

$$\Rightarrow \frac{5 - 0.9}{5 k} = 0.8 \text{ mA}$$

c) for n gates, $I_{B\text{tot}} = 0.8 \times n \text{ mA}$

whereas if we want to keep I_B below limit

d) To keep I_B in saturation $I_B h_{FE} \geq I_{B\text{tot}}$

$$I_c = 2.4 \text{ mA} + n \times 0.8 \text{ mA}$$

$$\therefore I_B = 0.44 \text{ mA}, h_{FE} = 20$$

$$\text{limit} \rightarrow I_B h_{FE} \geq I_c$$

$$\therefore 0.44 \times 20 \geq 2.4 + n \times 0.8 / 2$$

$$n = 7.2 \leq 7.80$$

$\therefore n$ should be kept ≤ 7

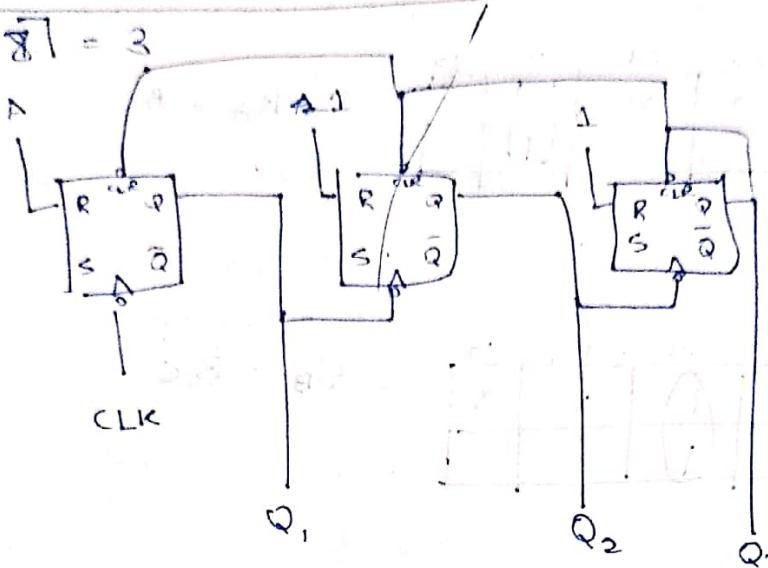
e) Fanout = 7

Q6) b) Design a counter with following binary sequence:

0, 1, 3, 2, 6, 4, 5, 7 and repeat.

Use RS Flip Flop in the design process.

$$\lceil \log_2 8 \rceil = 3$$



A	B	C	S ₀₀₀ A	R ₀₀₀ A	S ₀₀₁ B	R ₀₀₁ B	S ₀₁₀ C	R ₀₁₀ C
0	0	0	0	X	0	X	1	0
0	0	1	0	X	1	0	0	X
0	1	0	0	X	X	0	0	01
0	1	0	1	0	X	0	0	X
1	0	0	X	0	0	1	0	X
1	0	0	X	0	0	X	1	0
1	0	1	X	0	1	0	X	0
1	1	1	0	1	0	1	0	X1

Example: given function, find minterms & maxterms

S_A	A	B	C	R_A	R_B	R_C
0	00	01	11	10	00	01
1	X	X	X	X	11	10

$R_A = \bar{B}C$

S_A	A	B	C	R_A	R_B	R_C
0	00	01	11	10	00	01
1	X	X	X	X	11	10

$S_B = \bar{A}C$

S_B	A	B	C	R_A	R_B	R_C
0	00	01	11	10	00	01
1	0	X	X	X	11	10

$R_B = \bar{A}B$

S_B	A	B	C	R_A	R_B	R_C
0	00	01	11	10	00	01
1	X	0	X	X	11	10

$S_C = \bar{A}\bar{B}$

S_C	A	B	C	R_A	R_B	R_C
0	00	01	11	10	00	01
1	0	0	X	X	11	10

(Completed)

3 bit gray counter

11. Feb 2023

Q) calculate a) Fan-out b) Noise Margin of a DTL NAND gate. given

Diode + Voltage Across the conducting diode = 0.7V

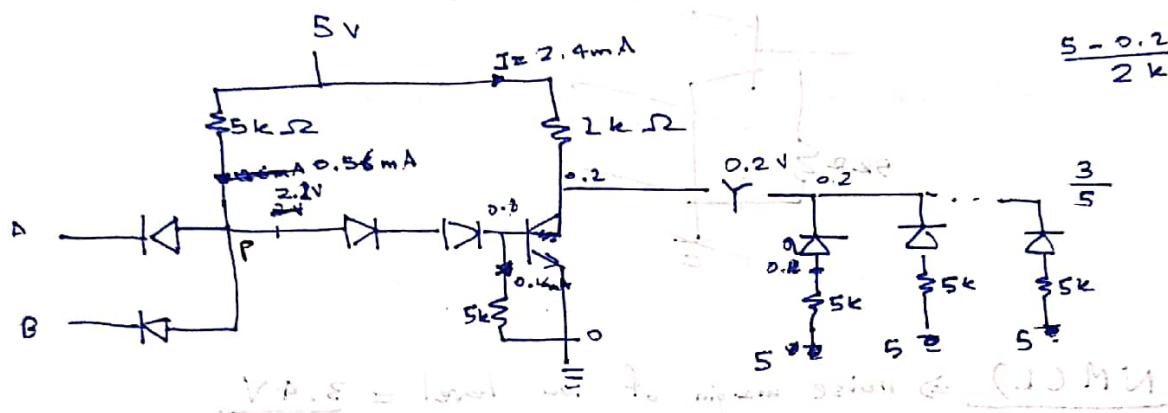
Cut-in Voltage = 0.6V

Transistor cut-in Voltage = 0.5V

$$V_{BE, sat} = 0.8V$$

$$V_{CE, sat} = 0.2V$$

$$hFE = 30$$



→ Transistor saturated at Y=0 ($V_{CE} = 0.2V$)

$$I_C = 0.4mA$$

$I_B = 0.56mA$ sh $h_{FE} = 30$ and consider 3. losses

assumed now $\therefore I_B h_{FE} \geq I_C$ and $I_C \leq 0.12mA$

$$\cancel{I_B h_{FE}}$$

and hence

$$I_C = 2.4mA + I_{\text{incoming}}$$

(0.8 + 0.8) current assumed at about not specified $\frac{0.8}{5k} = 0.16mA$

from one output, current incoming = $\frac{0.8}{5k} = 0.16mA$

for n output $\rightarrow I_{\text{incoming}} = 0.16n mA$

$$\therefore I_C = 2.4 + 0.16n \leq 0.12$$

$$\therefore 2.4 + 0.16n \leq 0.12$$

$$0.16n \leq 15.12$$

$$n \leq 97.5 \approx 11$$

for fan out 11

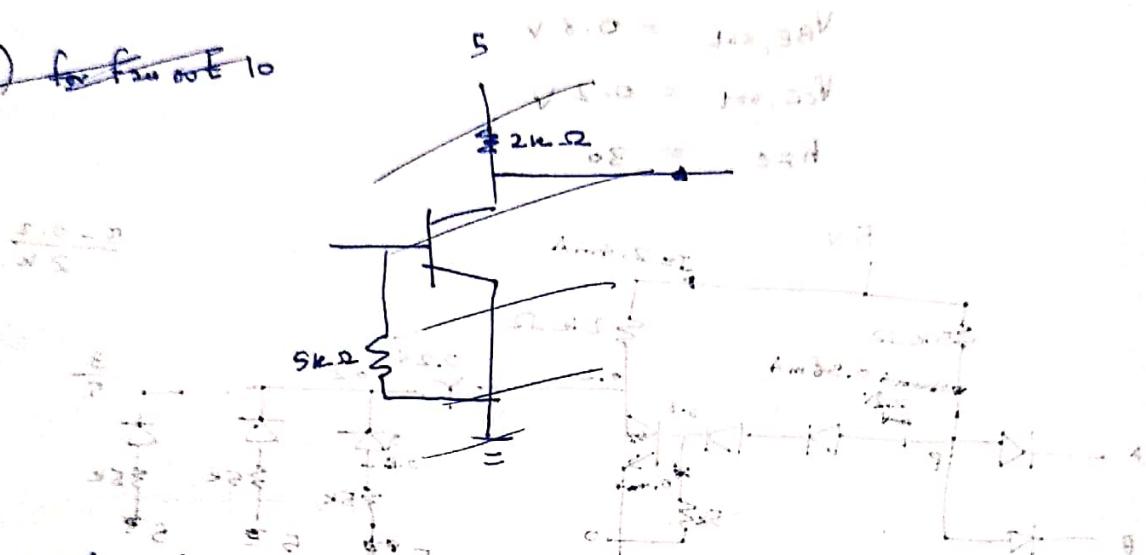
$$\Rightarrow I_{ao} = 2.4 + 0.82 \times 11 \\ = 11.42$$

and $11.42 < 12$ with enough margin so it's OK

$$\therefore \text{Noise Margin} = 12 - 11.42$$

$$= 0.58 \text{ mV}$$

b) for fan out 10



b) NM(L) \Rightarrow noise margin of low level = 3.4V

$V_p = 2.2 \text{ V}$ (from Q1) or the minimum voltage at output.

amount of reverse bias voltage is $AB - 2.2 \text{ V} = 2.3 \text{ V}$

\rightarrow if V_p decreases, the Diode at A or B can become forward bias.

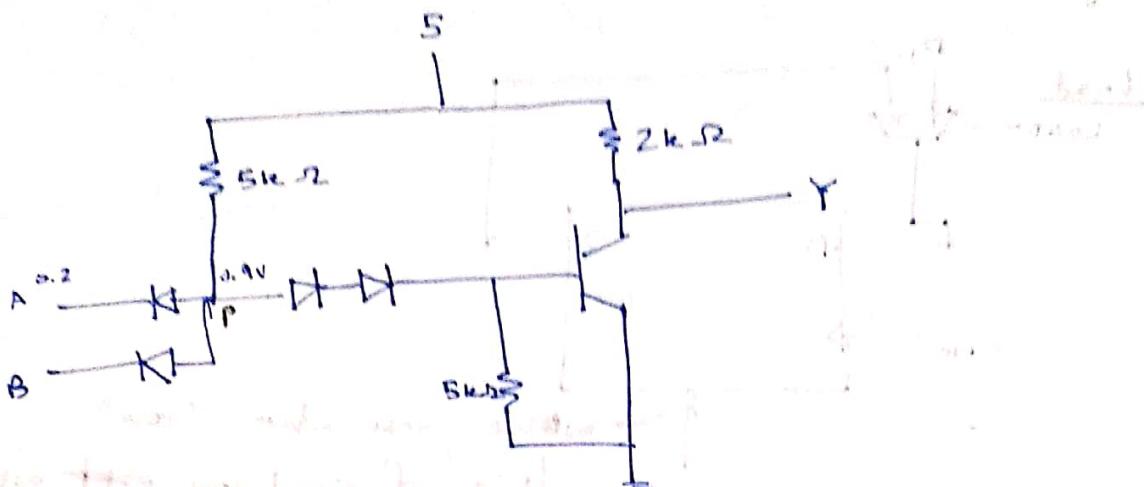
minimum I_o = $A \times I_s$ & $I_s = I_{ao}$

\therefore Voltage for Diode to become forward = $-(2.3 + 0.6)$

\therefore Noise Margin $\approx 3.4 \text{ V}$

\rightarrow if V_p increase ~~positively~~ no change in operation

NM (High), A or B = 0.2 V



we need $\frac{0.6 \times 2 + 0.5}{2} \text{ V}$ for Transistor to flow
current. So 1.7 V

∴ if V_P increases, it could happen that Transistor become saturated.

$$\therefore \text{Noise Margin} = 1.7 - 0.9 = 0.8 \text{ V}$$



and maximum voltage is limited to 2.15 V.

