Indian Institute of Engineering Science and Technology, Shibpur

B. Tech. (CST) 5^{th} Semester End-Term Examination, November, 2022

Microprocessor Based Systems (CS 3101)

Full Marks: 50 Time: 3 Hours

- Attempt any five (5) questions.
- Answers should be precise, to the point, and in your own words as far as practicable.
- If not explicitly mentioned, assume Intel 8085A as the base microprocessor.
- Make your own assumptions, if necessary, and state them at proper places.

1. (a) What are the addressing modes supported by Intel 8086 microprocessor?

   (b) Describe the advantages of the additional addressing modes that Intel 8086 microprocessor has over Intel 8085 microprocessor. [4+6]

2. In the context of Intel 8086 microprocessor based IBM PC running Microsoft DOS operating system, explain with suitable examples the interrelationship among hardware (CPU, Main Memory, IO Devices), BIOS (firmware), Operating System, and user programs. [10]

3. Say, in a hypothetical Intel 8085 based system 2 user programs need to be executed parallelly. That is, at a time 2 user programs, P_1 and P_2 say, would reside in the main memory and after execution of one instruction from P_1, the 8085 microprocessor would execute one instruction from P_2, after which the next instruction of P_1 would be executed and so on. Propose a suitable scheme to achieve this. Please note that your scheme should ensure that the result of such execution of 2 programs would be consistent in the sense that the result would be "same" as their normal independent executions. Make your own assumptions, if necessary. [10]

4. (a) Justify how a particular memory location (having a unique physical address) in an 8086 based system may be referred by multiple logical addresses (Segment Address:Offset). How many such logical addresses are possible for a memory location?

   (b) Write an Intel 8086 assembly language progam to find the largest element of an array of n integers (16bit). [3+7]

5. (a) Can a Memory device be interfaced in the IO space of a microprocessor? If yes, what will be the limitation(s) of such memory?

   (b) Write an interrupt service routine for a software interrupt instruction of Intel 8085 microprocessor (RST 5, say), that saves the contents held by **all** the registers (before the execution of the instruction starts) at stack. [4+6]

6. (a) Write an 8085 **Assembly Language Function** "*unsigned int mult(unsigned int m, unsigned int n)*" that takes two 8-bit numbers m and n as parameters and returns their product $m \times n$.

   (b) Write an 8085 **Assembly Language Program** that reads a 2-bit number from the Port A of an 8255 PPI chip (from its PA_0 and PA_1 pins) and computes its factorial. You may use the *mult*() function of the previous part in your program. [4+6]

7. Write short notes on the following.

   (a) NodeMcu

   (b) Intel 8051 Microcontroller [5+5]

Indian Institute of Engineering Science and Technology, Shibpur

B. Tech. 5th Semester End-Term Examination, November 2022

Subject: Database Management Systems (CS 3102)

Full marks: 50 **Time: 3 hours**

[Answer Question No. 1 and any four from the rest.]

1. Answer any five from the following questions:
   a) Define BCNF.
   b) Explain the generalized projection operation in relational algebra with an example.
   c) What are the advantages of views in relational database?
   d) Explain the ACID properties of a transaction?
   e) How can we prevent cascading rollback of transactions?
   f) What are the actions to be performed to take a check point in the system log?

2. a) Draw an ER diagram that represents a many to many relationship between two entity sets. Then convert it to its equivalent relational schema. [2×5]
   b) Explain the idea of recursive relationship with the help of an ER diagram. Also show its conversion to relational schema.
   c) Compare and contrast centralized and distributed databases.

3. a) What are the different kinds of anomalies that may occur in DBMS? [3+3+4]
   b) Given a relation R(P, Q, R, S, T, U, V, W, X, Y) and Functional Dependency set FD = { PQ → R, P → ST, Q → U, U → VW, and S → XY}, determine whether the given R is in 3NF? If not convert it into 3 NF.
   c) What advantage we achieve when a relation is in 4 NF?

4. Consider the following relational schema: [3+5+2]

   EMPLOYEE(NAME, SSN, SUPERSSN, SEX, ADDRESS, DNO, SALARY)
   DEPARTMENT(DNAME, DNUMBER, DLOC)

   Here SSN is the social security number of the employees. SUPERSSN is the SSN of the supervisors of the employees. DNO and DNUMBER imply department number. DLOC is the location of the departments.

   a) Write the following queries in relational algebra.
      i) Retrieve the social security number of all the employees who either works in department number 5 or directly supervise an employee who works in department number 5.
      ii) Retrieve the maximum salary of each department excluding those that are below 10000.
   b) Write the following queries in SQL.
      i) Retrieve the employee numbers and names of all employees along with their immediate supervisor's employee numbers and names. The result must include the employee number and name of the employees who do not have any supervisor.
      ii) List the employees who earn the lowest salary in their respective department.

[(2.5×2)+(2.5×2)]

5. a) Draw and explain the state transition diagram of a transaction.

b) Explain the following problems (with suitable examples) that can occur when concurrent transactions execute in an uncontrolled manner.

i) Lost update problem.

ii) Dirty read problem.

c) What is strict two-phase locking in transaction processing?

6. a) What do you mean by serializable schedule? [3+(2.5×2)+2]

b) Consider three transactions T_1, T_2 and T_3 that are performing read and write operations on three database items X, Y and Z in an interleaved manner as shown in the following schedule S.

S: $r_2(Z)$; $r_2(Y)$; $w_2(Y)$; $r_3(Y)$; $r_3(Z)$; $r_1(X)$; $w_1(X)$; $w_3(Y)$; $w_3(Z)$; $r_2(X)$; $r_1(Y)$; $w_1(Y)$; $w_2(X)$.

Here, $r_i(.)$ and $w_i(.)$ represents read and write operations performed by transaction T_i, respectively. Explain the rules of constructing precedence graph for a given schedule and draw the precedence graph for the schedule S to determine whether it is serializable or not.

c) Explain the deferred update technique of database recovery.

[2+5+3]

Indian Institute of Engineering Science and Technology, Shibpur

BTech (CST) 5th Semester Examinations, 2022

Computer Architecture and Organization -II (CS-3103)

Full marks: 50 Time: 3 hours

Answer any five

1. Define the 1-bit and 2-bit prediction schemes. The series of branch outcomes stored in an 1-bit prediction buffer is 11001101 (1 represents taken branch and 0 is for un-taken branch).
(i) Identify the predictions at each branch instruction execution.
(ii) Find out mis-predictions. Assume predictor is initialized as 0. Mention assumptions taken.
(iii) If the 2-bit prediction is considered and the predictor is initialized with 10, then find the number of mis-predictions for the same branch outcome 11001101. 10

2. Define `structural hazard' and `data hazard' in a pipeline system.
(i) Identify the cases of possible structural and data hazards in a 4-stage instruction pipeline shown in Figure 1.
(ii) Show how pipeline bubbles can effectively be used to avoid the structural hazard in the machine with only one memory port.
(iii) Show how data forwarding can be used to avoid data hazard in the machine. 10

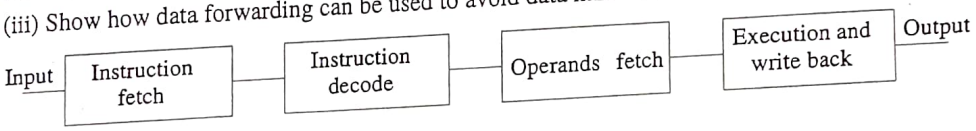


Figure 1

3a) A program consists of two nested loops, with only single branch instruction at the end of each loop. The outer loop is executed 100 times and the inner loop 200 times. Determine the accuracies of (i) Always predict taken, and (ii) Always predict not taken prediction strategies. 5

b) What do you mean by `exceptions'? Explain a case of out-of-order exceptions and the methodology for handling it in the instruction pipeline of Figure 1. 5

4a) Define compulsory cache miss. A program accesses each element of an 1024X1024 matrix 8 times in each course of its execution. If the data cache can accommodate 256 matrix elements and 16 matrix elements per block/page, then how many compulsory data cache misses are caused by this program's execution? 5

b) Show how loop interchange technique can reduce cache miss rate for the following nested loop

```
for (i = 1; i<101; i++)
    for (j = 1; j<4; j++)
        A[j][i] = B[i][1] * B[i+1][1];
```

Mention the assumptions taken. 5

5a) Describe in brief directory based protocol (with full directory) to ensure cache-coherence in a multi-processor system. Figure 2 shows a directory based cache system. Find out the number of bits in Directory A and B for- i) Full directory, ii) Limited directory, and iii) Chained directory. 5

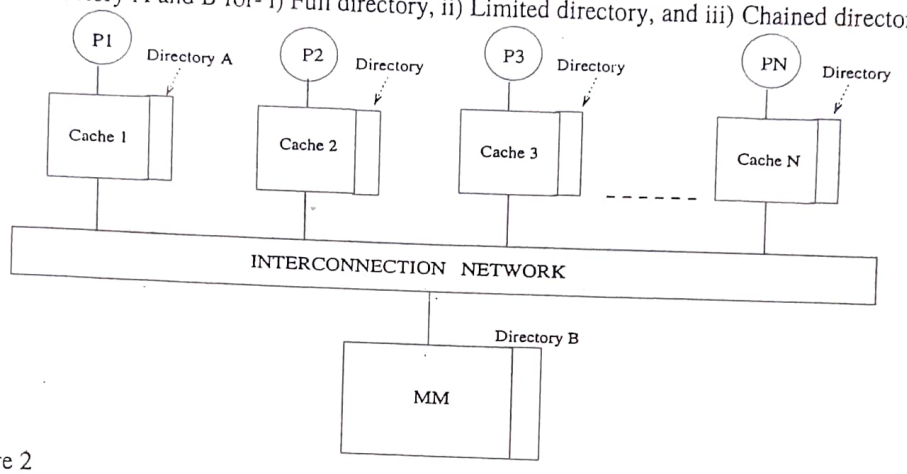


Figure 2

b) Describe the write-invalidate policy, implemented to enforce the cache coherence in a multiprocessor system. Evaluate performance of invalidation scheme in each of the following access patterns to variable V

i) Repeat a number of times: processor P1updates V and other 100 processors read the new value.

ii) Repeat a number of times: P1 updates V 100 times, then processor P5 only reads V. 5

6a) Define 1st and 2nd order predictor in context-based value predictor (CVP). Let sequence of values for a variable x is 1 1 1 2 2 3 4 3 1 1 1 2 2 3 1 1 1. Find the predicted value for x, in 1st and 2nd order predictor. 5

b) Define memory-wall in today's computation architectures. Introduce Near-memory Processing (NMP), Processing-in-Memory (PIM) and In-memory Computing (IMC) to address the issue of memory-wall. 5

7. Write short notes on the following

a) Uniform and Non-Uniform Memory Access system 3

b) Static and Dynamic Data Flow machine 3

c) CREW and ERCW Shared Memory SIMD m/c 4

Indian Institute of Engineering Science and Technology, Shibpur
B.Tech. - M.Tech. Dual Degree 5^{th} Semester (CST) Examination 2022
Graph Algorithms (CS 3104)

Full Marks: 50 Time: 3 Hours

Answer Question-1 and any four from the remaining.
Do all parts of a question together. Do not mix up answers to parts of different questions in the answer script.

1. (a) Prove that every component of the symmetric difference of two matchings of a graph is a path or even cycle.

   (b) Let $G = (\{V_1, V_2\}, E)$ be a bipartite graph with vertex partitions V_1 and V_2. Show that

$$\sum_{u \in V_1} deg(u) = \sum_{v \in V_2} deg(v)$$

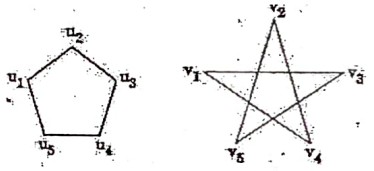
[3 + 3 = 6]

2. (a) Define vertex colouring of a graph G and show that every planar graph is 5-vertex colorable.

   (b) Given a directed graph $G = (V, E)$. Describe a fast algorithm to compute the connected components in a graph G.

[6 + 5 = 11]

3. (a) Define isomorphism. Determine whether the following pair of graphs are isomorphic. If yes, justify your answer.

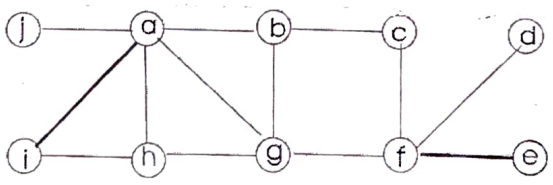


   (b) State and prove Handshaking Theorem.

[6 + 5 = 11]

4. (a) Prove that a graph is planar if and only if it contains no subdivision of K_5 or $K_{3,3}$.

   (b) Describe an algorithm that finds, as efficiently as possible, a matching of maximum cardinality in any graph. Consider the graph shown below with initial matching shown in bold, find augmenting paths iteratively to obtain a maximum matching for this graph.



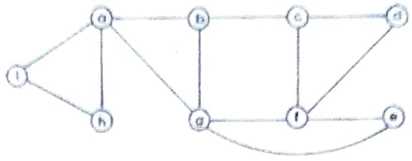
[5 + 6 = 11]

5. (a) Prove that in a connected planar graph with n vertices and e edges has $e - n + 2$ regions.

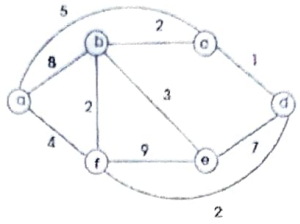
   (b) Define Chromatic Number of a graph. Prove that a graph with at least one edge is two chromatic if and only if it has no circuits of odd length.

[7 + 4 = 11]

6. (a) Find the clustering coefficient for each vertex in the graph shown below and also work out the average clustering coefficient.



(b) Compute the vertex betweenness values for each vertex for the graph as shown below. Find two influential nodes in this graph using this measures.



[5 + 6 = 11]

Indian Institute of Engineering Science and Technology Shibpur
Department of Computer Science and Technology
BTech (CST), 5th Semester, End Sem Examination, 2022
Computer Graphics (CS-3121)

Full marks: 50 **Time**: 3 Hours

Read the following instructions carefully

- *Answer any five questions.*
- *Answer parts of same question together.*
- *Use diagrams wherever appropriate.*
- *For plotting problem, draw grid on plain paper. Here no additional graph paper is needed. Before plotting show the steps of coordinate calculation.*

1. Write short note on

(a) Pseudocode of DDA algorithm for drawing straight line

(b) Derive the transformation matrix for rotation of a point about an origin

(c) Pseudocode of scanline polygon fill algorithm

(d) Applications of virtual reality

$[2\frac{1}{2}\times 4 = 10]$

2. (a) Discuss: i) World Coordinate ii) Device coordinate iii) Window iv) Viewport

(b) Show that window to viewport mapping obtained by 'normalization' and 'composite transformation' yields identical result. [5+5]

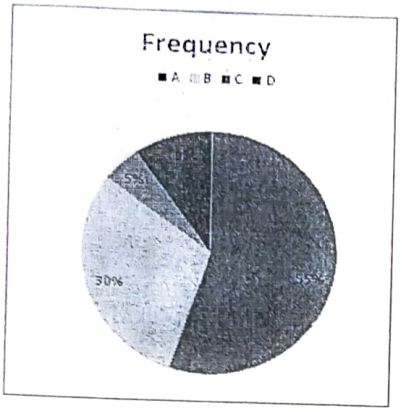
3. (a) Describe Floating horizon algorithm for hidden surface elimination.

(b) Discuss Sutherland- Cohen line clipping approach.

[5+5]

4. (a) Discuss Midpoint circle drawing algorithm.

(b) Discuss how the following pie chart can be drawn from the table.



Entity	Frequency
A	55
B	30
C	5
D	10

[5+5]

5. (a) Discuss properties of a Bezier curve?

(b) Plot the Bezier curve using the following equation with not more than 10 intervals (i.e. 'u' values) where (x_i, y_i) are control points.

$$x(u) = \sum_{i=0}^{3} {}^{3}C_i (1-u)^{3-i} u^i x_i \,, \quad y(u) = \sum_{i=0}^{3} {}^{3}C_i (1-u)^{3-i} u^i y_i \,, \quad 0 \le u \le 1$$

[5+5]

6. What are the factors to be taken into account while preparing illumination model of a scene? Derive the expression of illumination model of a scene. Mention each notation used in the expression. Update the expression considering the intensity attenuation and the transparency of the material.

[10]