Programmable Logic Devices

Programmable Logic Devices

- Flexible hardware that can be structured to fit the natural organization and data flow of a computation
- Two types: Fixed computing and Programmable computing
  - Fixed computing: Fixed logic devices are permanent
  - Programmable computing: Can be altered at any time to perform any number of functions

Why Programmable Logic Devices?

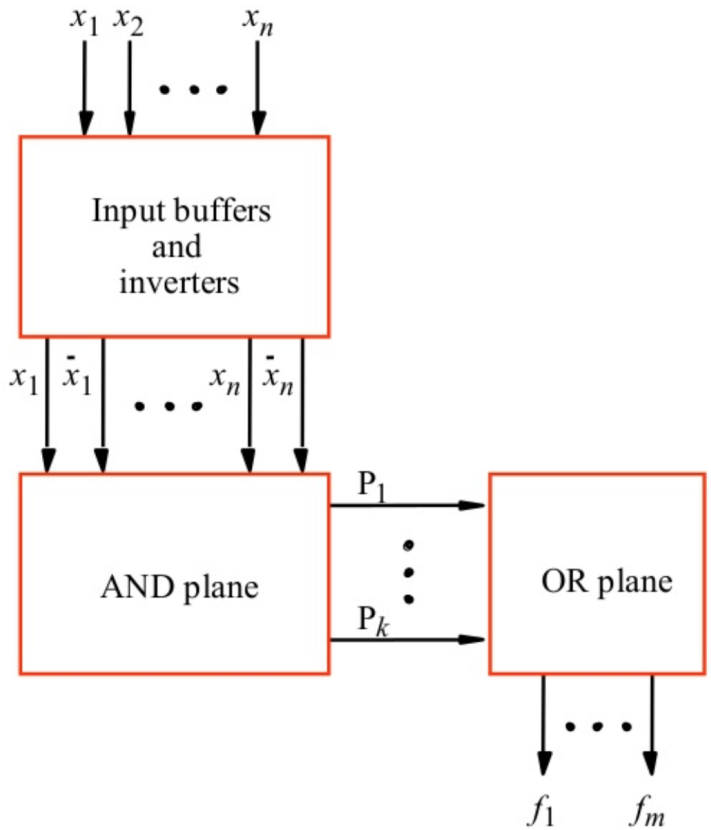
- With programmable devices, the same functionality can be obtained with one IC rather than using several individual logic chips
- Less board space
- Less power required
- Greater reliability
- Less inventory
- Overall lower cost in manufacturing

Programmable Logic Devices

- Advantages of Fixed logic devices:
  - Appropriate for large volume applications because they are economical for mass-production
  - Best choice for high performance applications
- Advantages of Programmable logic devices:
  - Provides flexibility during the design cycle
  - Do not require long lead times for prototypes or production parts
  - Do not require users to pay for large NRE costs
  - Can be reprogrammed even after a piece of equipment is shipped to a customer

Programmable Logic Devices

- Two logic planes
- Any combination of ANDs/ORs
- Sharing of AND terms across multiple ORs

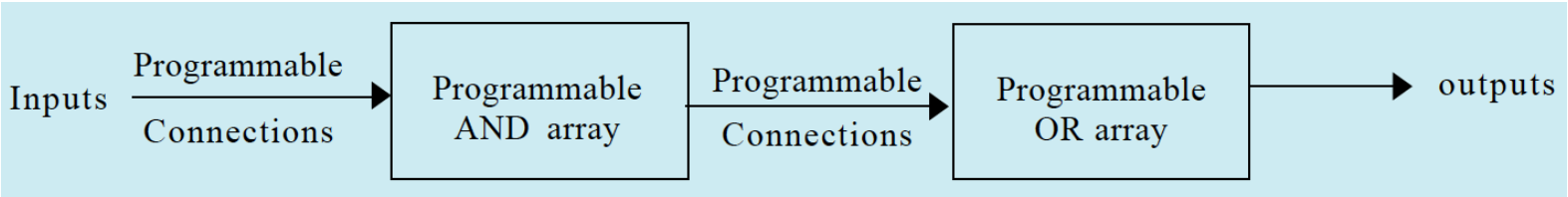


Programmable Logic Devices

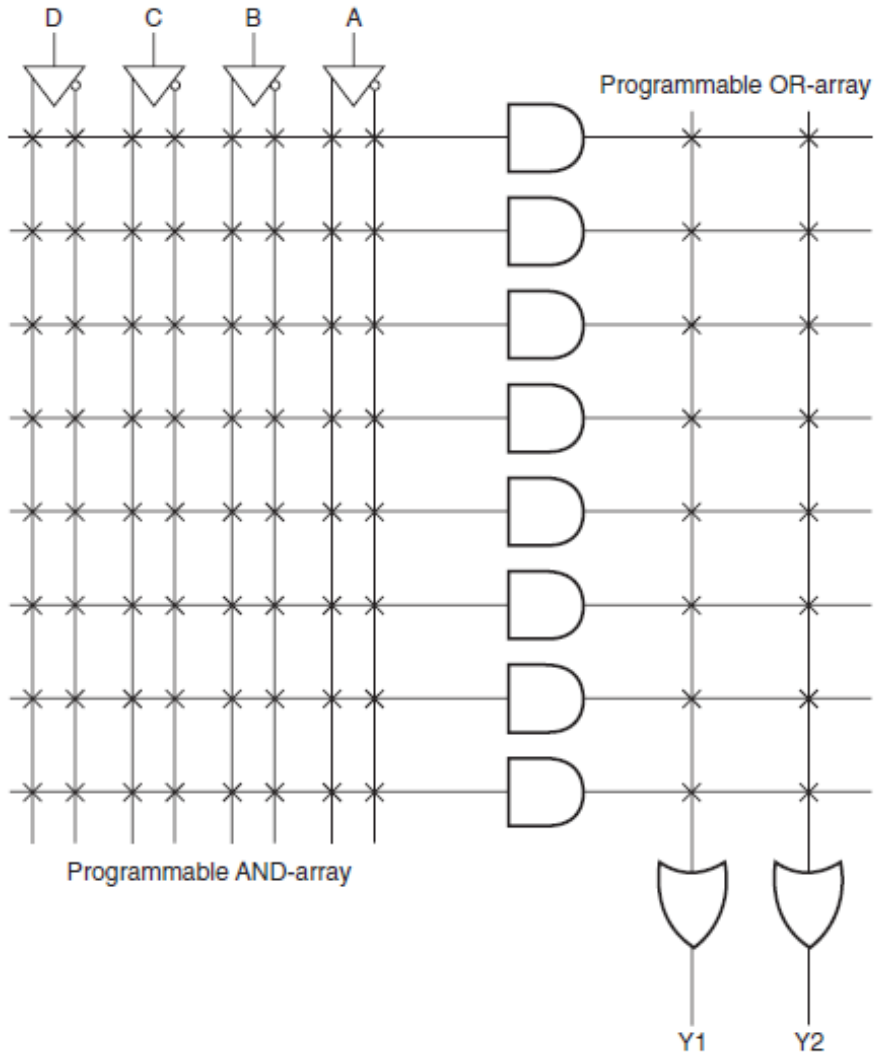
- Three categories:
  - **ROM-Based:** The input connection matrix is hardwired. The user can modify the output connection matrix.
  - **Programmable Logic Array (PLA):** The user can modify both the input connection matrix and the output connection matrix.
  - **Programmable Array Logic (PAL):** The output connection matrix is hardwired. The user can modify the input connection matrix.

Programmable Logic Devices: PLA

- Programmable Logic Array (PLA)
  - A programmable array of AND gates feeding a programmable array of OR gates
  - Two programmable ground planes
  - Any combination of ANDs/ORs
  - Sharing of AND terms across multiple ORs
  - Highest logic density available to user
  - High fuse count; slower than PALs



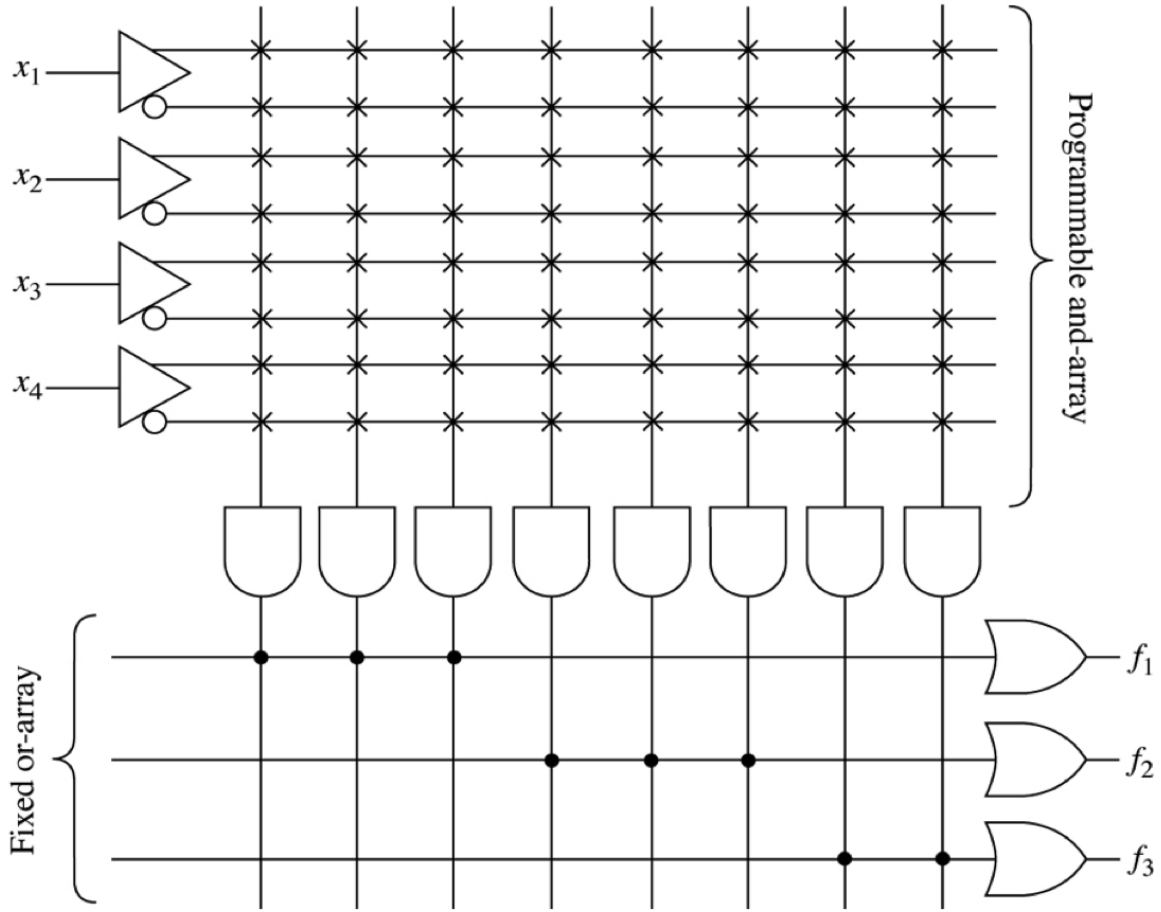
Programmable Logic Devices: PLA



Programmable Logic Devices: PAL

- Programmable Array Logic (PAL)
  - A programmable array of AND gates feeding a fixed array of OR gates
  - Benefit of faster propagation delay
  - Less complex software

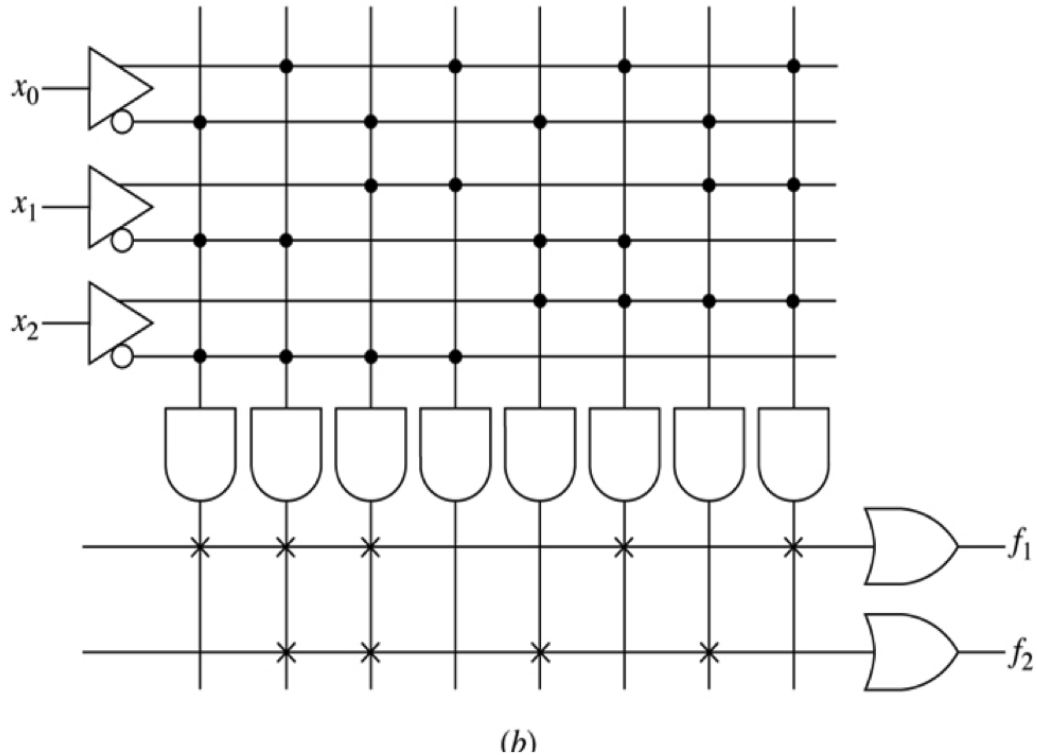
Programmable Logic Devices: PAL



Programmable Logic Devices: ROM-Based

x_2	x_1	x_0	f_1	f_2
0	0	0	1	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	0
1	0	0	0	1
1	0	1	1	0
1	1	0	0	1
1	1	1	1	0

(a)



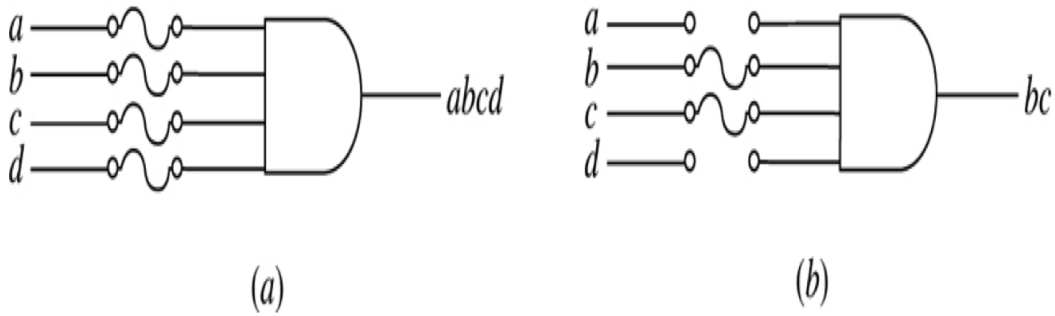
(b)

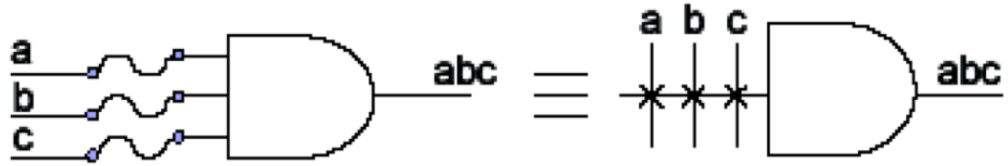
Programmable Logic Devices

Table: Programmability Comparison

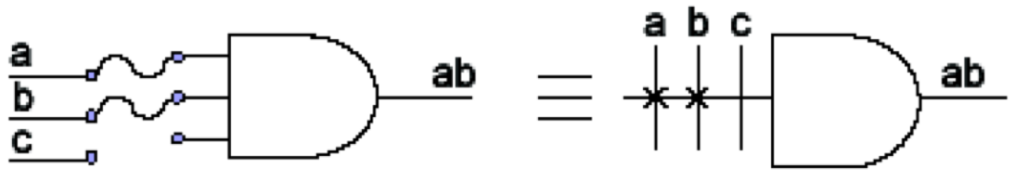
Device	**AND-Array**	**OR-Array**
ROM	Fixed	Programmable
PLA	Programmable	Programmable
PAL	Programmable	Fixed
GAL	Programmable	Fixed

Programming by blowing fuses



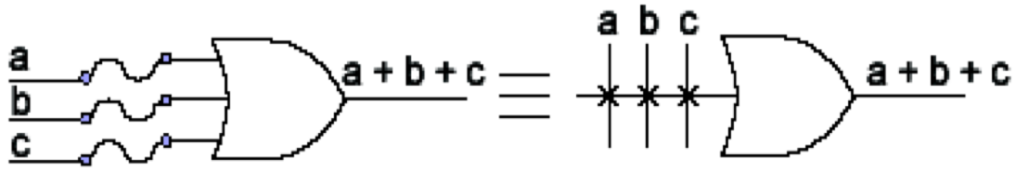


AND gate before programming

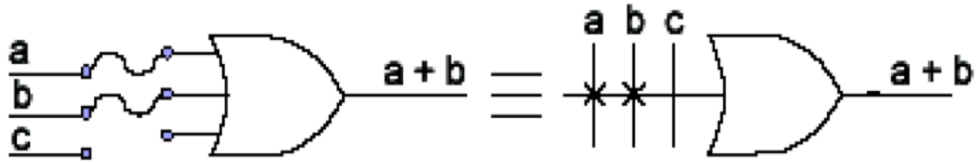


AND gate after programming

Programming by blowing fuses

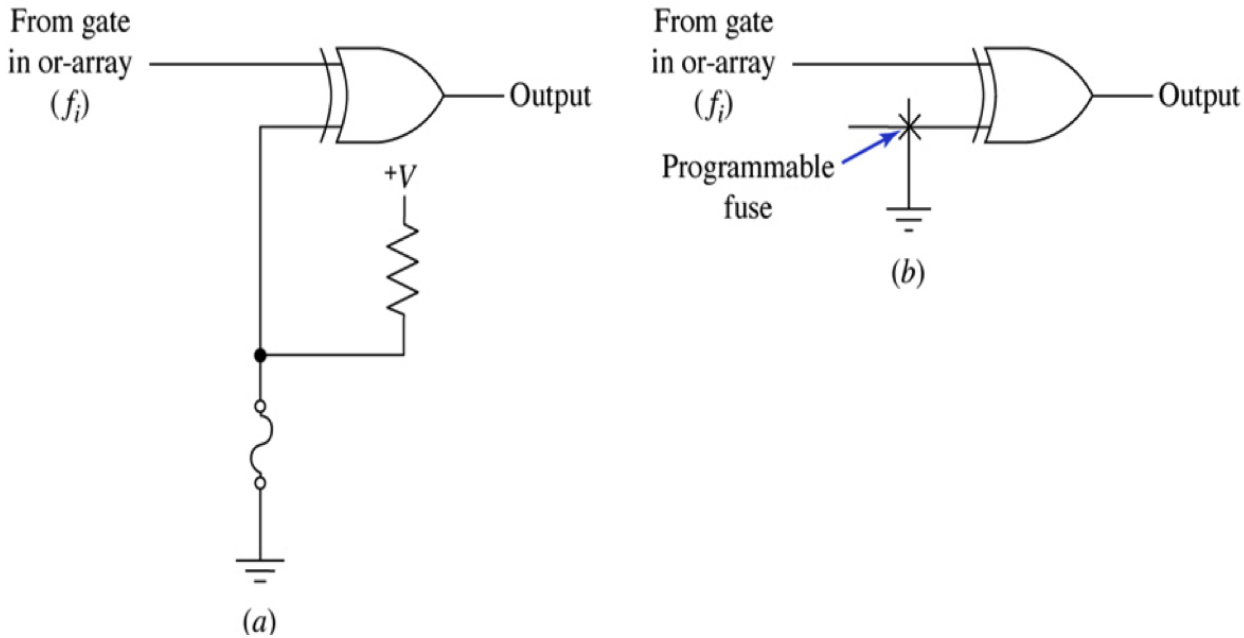


OR gate before programming



OR gate after programming

Programming by blowing fuses



Programming Methods

- Fuses or anti-fuses:
  - Programmed by passing a large current
  - One-time programmable (OTP) because user can't rewire them internally once the fuses are blown
- Pass transistors:
  - Opened or closed by storing a charge on their gate electrodes using a high-voltage pulse
  - Programmable device resembles an EPROM or EEPROM
  - User can erase it and then place it in a special programmer socket and reprogram it
- Static RAM or Flash bits:
  - To control the pass transistors for each interconnection
  - User can control whether the switch is closed or opened (i.e., two logic elements are connected or not) by loading 1 or 0.
  - PLDs built using RAM/Flash switches can be reprogrammed without removing them from the PCB
  - Often called in-circuit reconfigurable or programmable

Comparative study on some PLD technology

Technology	Typical data retention time	Typical erase / program cycles	Typical erase / program times
EPROM	Greater than 10-20 years	OTP-10,000 times	Some minutes UV-light / about 0.1 msec, per cell
EEPROM	Greater than 10-20-years	Greater than 1,000-10.000 times	Some milliseconds per cell / about 0.1 msec, per cell
Flash EPROM	Greater than 10-20 years	Greater than 50-10,000 times	About 1 sec. for whole chip / about 0.1 msec, per cell
SRAM	Only at stable power-on (volatile)	Unlimited	About some milliseconds / milliseconds.. minutes for whole chip (depends on ROM-interface)
Anti-Fuse	Unlimited	1 time (OTP)	Not erasable / some minutes for whole chip (depends on chip complexity)
Fuse	Unlimited	1 time (OTP)	Not erasable / some minutes for whole chip (depends on chip complexity)

PLD Architecture

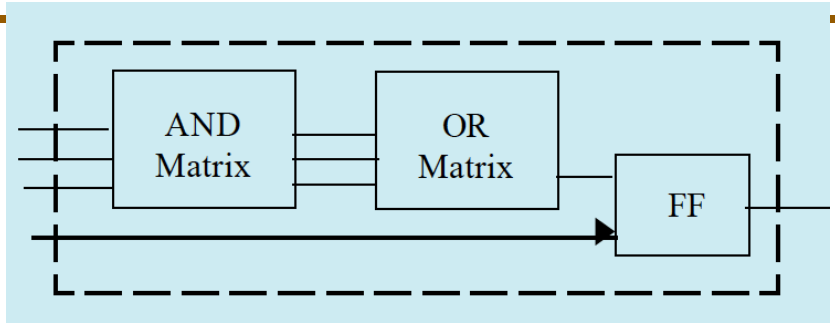
- Consists several logic gates and switches
- Three Types:
  - Simple Programmable Logic Devices (SPLDs)
  - Complex Programmable Logic Devices (CPLDs)
  - Field Programmable Gate Arrays (FPGAs)
- CLPDs and FPGAs are often referred to as high-capacity programmable logic devices (HCPLDs)

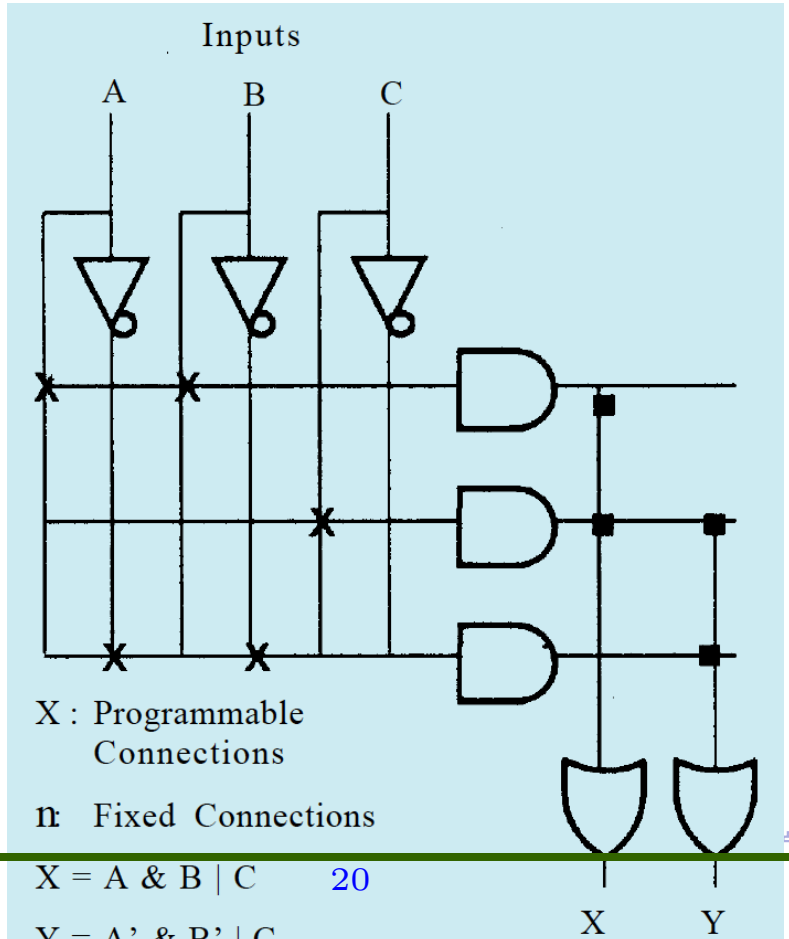
Simple Programmable Logic Devices (SPLDs)

- First real PLD was developed by Monolithic Memories Inc. (MMI) in 1978
- Kind of PAL architecture
- Predictable timing and easy to develop
- Inefficient resource utilization and only for simple logic functions
- Vendor-specific name of SPLD is Generic Array Logic (GAL)
  - GAL devices were created by Lattice Semiconductor Corporation in 1983
  - Offered sophisticated CMOS electrically erasable variations on PAL architecture

Simple Programmable Logic Devices (SPLDs)

SPLD Macrocell





Simple Programmable Logic Devices (SPLDs)

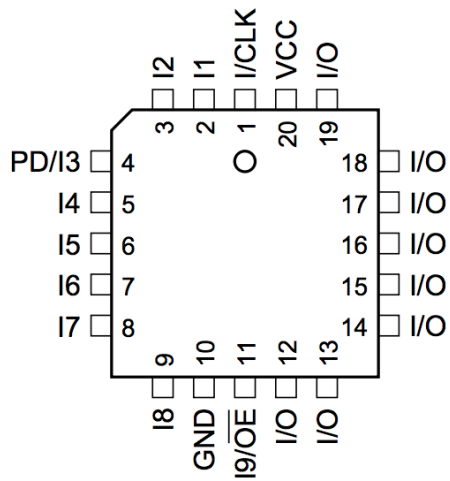
SPLD Manufacturers

Simple Programmable Logic Devices (SPLDs)

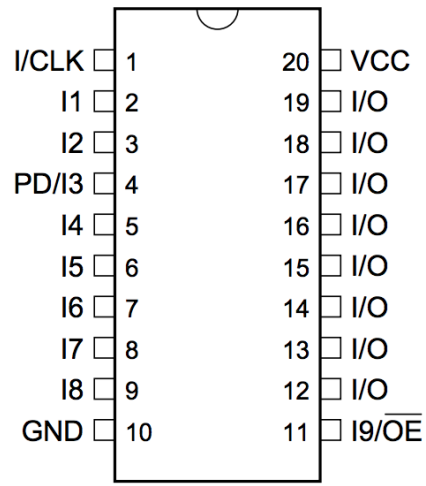
ATMEL High Performance SPLD: ATF16V8CZ

Pin	Function
CLK	Clock
I	Logic Inputs
I/O	Bidirectional Buffers
$\overline{OE}$	Output Enable
V_{CC}	+5V Supply
PD	Power-Down
GND	Ground

20-lead PLCC
(Top View)



20-lead PDIP
(Top View)



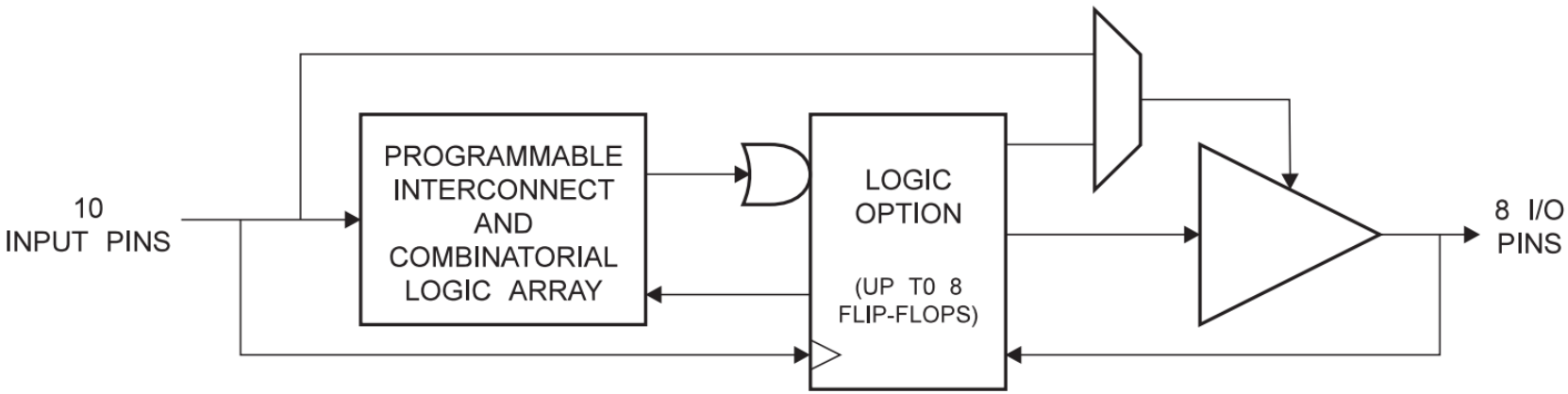
Simple Programmable Logic Devices (SPLDs)

Features of ATF16V8CZ:

- Industry Standard Architecture
  - Emulates Many 20-pin PALs
  - Low-cost, Easy to Use Software Tools
- High Speed EEPLD: 5-ns Maximum Pin-to-pin Delay
- Low Power, 100μA Pin Controlled Power-down Mode Option
- CMOS and TTL Compatible Inputs and Outputs
- Advanced Flash Technology: Reprogrammable
- High Reliability CMOS Process
  - 20 Year Data Retention and 100 Erase/Write Cycles
  - 2,000V ESD Protection and 200mA Latchup Immunity
- Commercial and Industrial Temperature Ranges
- Dual-in-line & Surface Mount Packages in standard pinouts
- PCI Compliant
- Green (ROHS Compliant) Package Options Available

Simple Programmable Logic Devices (SPLDs)

ATF16V8C: Block Diagram



Simple Programmable Logic Devices (SPLDs)

ATF16V8C: Macrocell Configuration

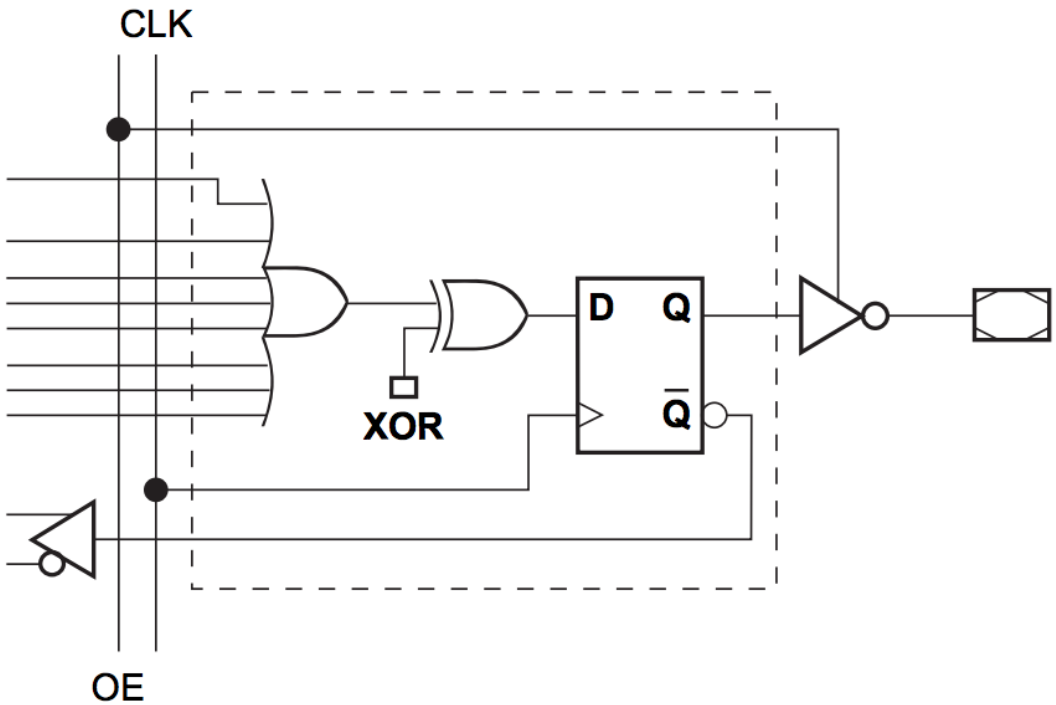
- Automatically select the device type, generally based on the register usage and output enable ($\overline{OE}$) usage
- Register usage on the device forces the software to choose the registered mode
- All combinatorial outputs with $\overline{OE}$ controlled by the product term will force the software to choose the complex mode
- Each macrocell can be configured as either a **registered or combinatorial** output or I/O, or as an input
- The software will choose the simple mode only when all outputs are dedicated combinatorial without $\overline{OE}$ control

ATF16V8C: Macrocell Configuration

- Registered Mode:
  - One or more registers are required
  - Eight product terms are allocated to the sum term
  - For a combinatorial output or I/O, the output enable is controlled by a product term, and seven product terms are allocated to the sum term
  - When the macrocell is configured as an input, the output enable is permanently disabled

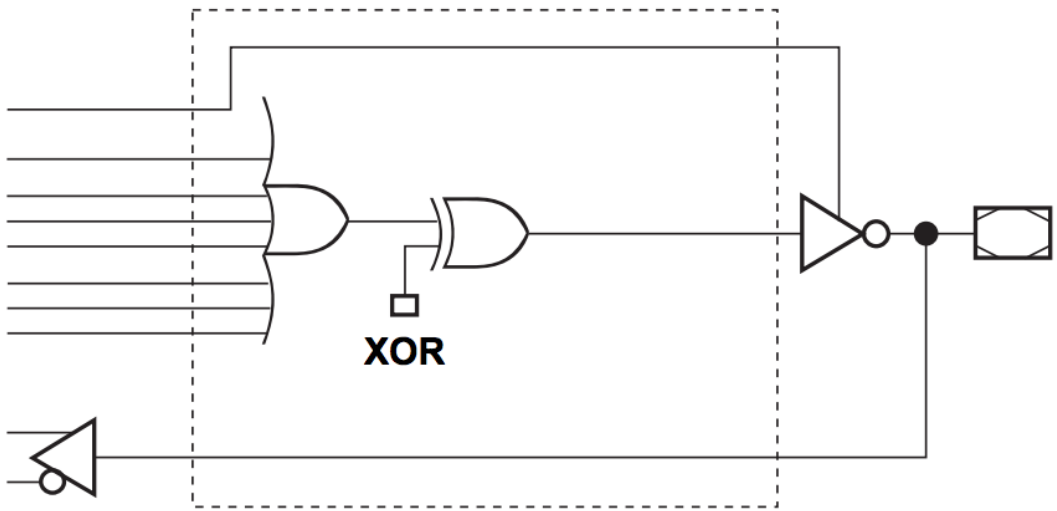
ATF16V8C: Macrocell Configuration

1) Registered Configuration for Registered Mode

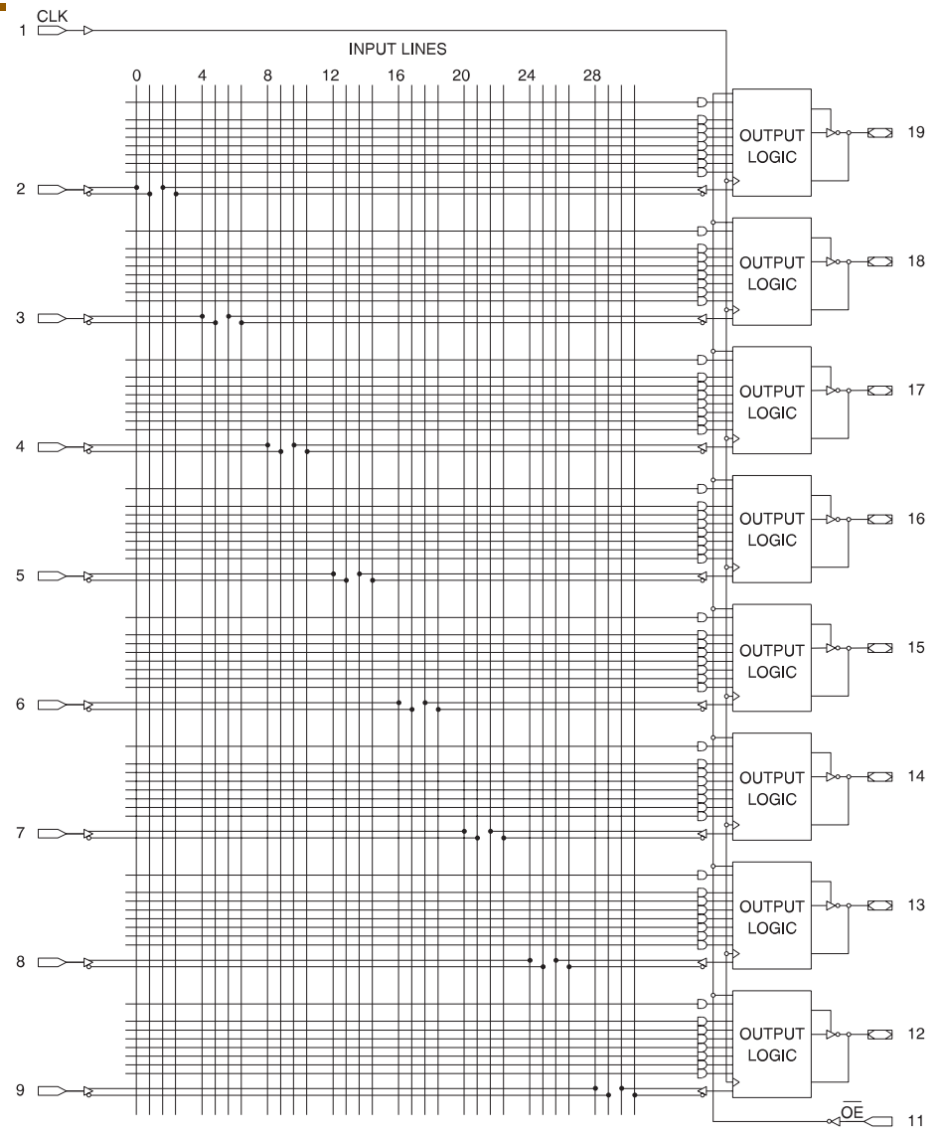


ATF16V8C: Macrocell Configuration

2) Combinatorial Configuration for Registered Mode



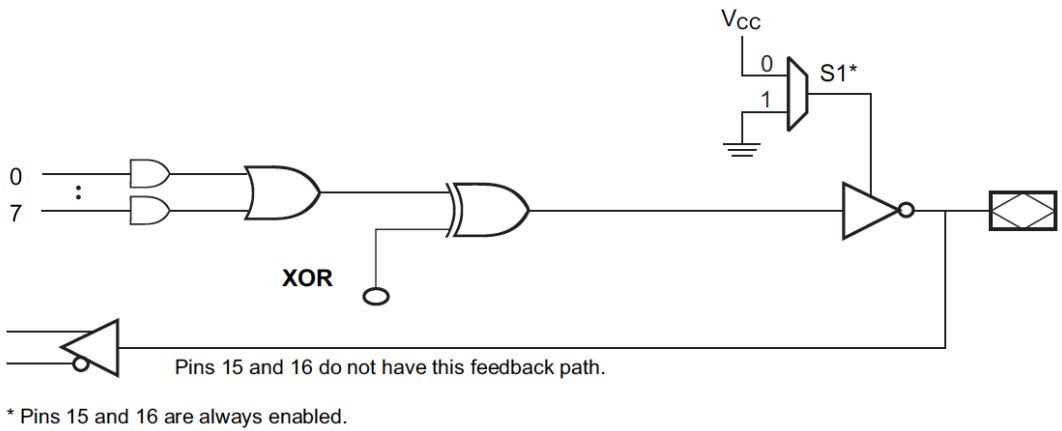
Simple Programmable Logic Devices (SPLDs)



Registered Mode Logic Diagram

ATF16V8C: Macrocell Configuration

- Simple Mode:
  - Eight product terms are allocated to the sum term
  - Pins 15 and 16 (center macrocells) are permanently configured as combinatorial outputs
  - Other macrocells can be either inputs or combinatorial outputs with pin feedback to the AND-array
  - The compiler selects this mode when all outputs are combinatorial without $\overline{OE}$ control



Simple Programmable Logic Devices (SPLDs)

ATF16V8C: Macrocell Configuration

- Complex Mode:
  - Combinatorial output and I/O functions are possible
  - Each macrocell has seven product terms going to the sum term and one product term enabling the output
  - Combinatorial applications with an $\overline{OE}$ requirement will make the compiler select this mode