Design of Counters

October 28, 2020

Design of Binary Counter of any Arbitrary Modulus

- Suppose we want to design a modulo M-counter for any arbitrary value of M.
- Counter will count from 0 to M-1, and back to 0.
- Assume that flip-flops have clear (CLR) inputs.

Basic Idea

- We first design a ripple counter with $\lceil log_2 M \rceil$ stages.
- Then, we will design a gating circuit which takes input from the outputs of the counter and generates a signal whenever the value reaches M.
- Connect the output of the gating circuit to CLR inputs of the flip-flops.

Modulo - 6 Ripple Counter

- The number of stages $= \lceil log_2 M \rceil = 3$
- The desired count sequences are as follows:
  000 001, 010, 011, 100, 101, 000,.....
- From the state 101, instead of going to the state 110, we have to bring back to 000.

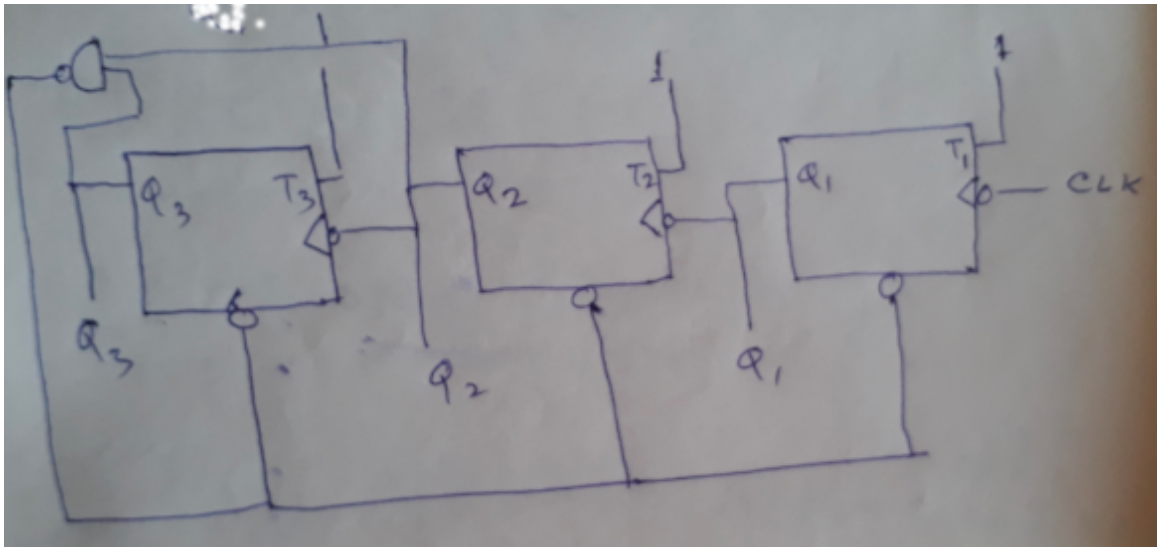
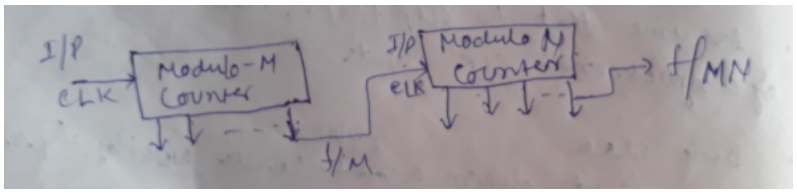


Figure: Circuit diagram of a Mod-6 Ripple Counter.

Cascading of Ripple counters

- If a mod-M counter and a mod-N counter are connected in cascade, the combination will count modulo-MN.



Lockout

- For a Mod-5 counter, logic states $Q_2 Q_1 Q_0 = 101$, 110, and 111 are not used. Suppose that, by chance, the counter happened at some point to find itself in any one of these unused states.
- Such a situation might develop as a result of external noise affecting the state of a flip-flop.
- we do not know the next state for a unused state. Hence, there is the further possibility that when a flip-flop is thrown into an unused state, the counter might cycle from unused state to unused state, never arriving at a used state.
- A counter whose unused states have this feature is said to suffer from *lockout*.

Example of synchronous Counter

- Design a Mod-5 synchronous counter such that if the unused states $Q_2Q_1Q_0 = 101$, 110, or 111 occur, the next clock pulse will reset the counter $Q_2Q_1Q_0 = 000$.

The excitation table of the circuit for the aforesaid problem is given below:

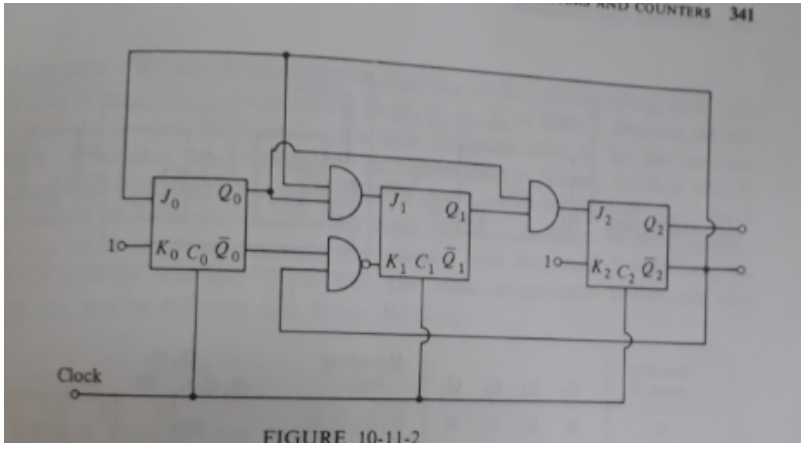
Counter state S	Q_2	Q_1	Q_0	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0	X	0	X	1	X
1	0	0	1	0	X	1	X	X	1
2	0	1	0	0	X	X	0	1	X
3	0	1	1	1	X	X	1	X	1
4	1	0	0	X	1	0	X	0	X
US	1	0	1	X	1	0	X	X	1
US	1	1	0	X	1	X	1	X	1
US	1	1	1	X	1	X	1	X	1

The Boolean functions for the flip-flop inputs are as follows:

$J_2 = Q_1Q_0$, $K_2 = 1$, $J_1 = \overline{Q_1}Q_0$, $K_1 = Q_2 + Q_0 = \overline{\overline{Q_2}\ \overline{Q_0}}$

$J_0 = \overline{Q_2}$, $K_0 = 1$

Mod-5 Counter



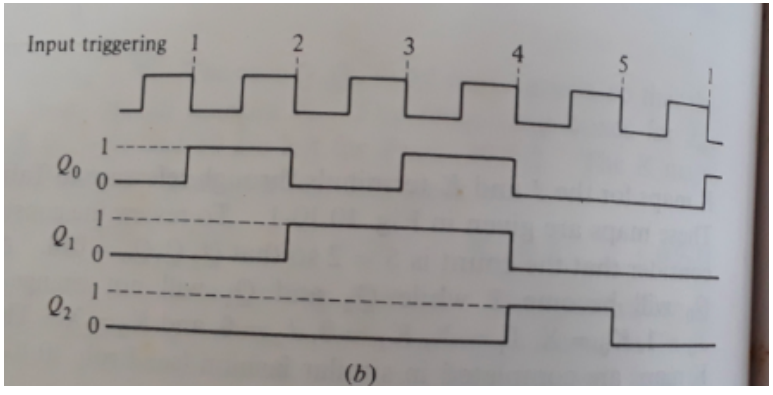


Figure: Timing Diagram