



**Bangladesh University of
Engineering and Technology**

Department Electrical and Electronic Engineering

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Section: C

Group No.: 13

Course name: EEE 310

Course Title: Communication Laboratory

Project Name:

TDM-PCM System Development in Proteus

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Project Objective:

In this sessional course project, we, group 13, tried to build a good TDM-PCM system.

We have simulated the circuit design in proteus.

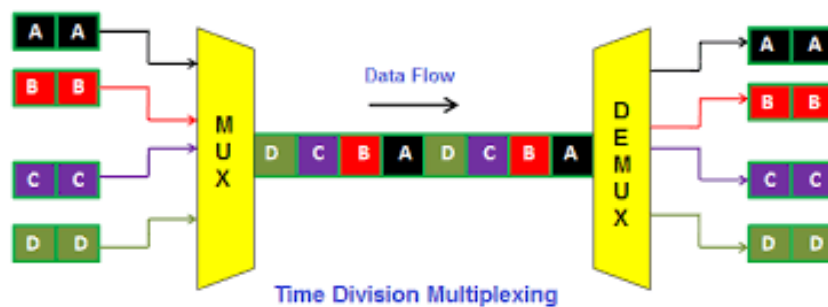
This project will be able to:

- ❖ Take multiple input signals
- ❖ Discretize them & Encode them and transmit through channel
- ❖ Decode the encoded signal to analog signal in receiver side
- ❖ Separate the analog signal into same number of channels of input side

Time division multiplexing

Time-division multiplexing (TDM) is a method of putting multiple data streams in a single signal by separating the signal into many segments, each having a very short duration. Each individual data stream is reassembled at the receiving end based on the timing. When we sample only one signal, there is a gap between two adjacent samples. This empty space can be used by another signal's sample.

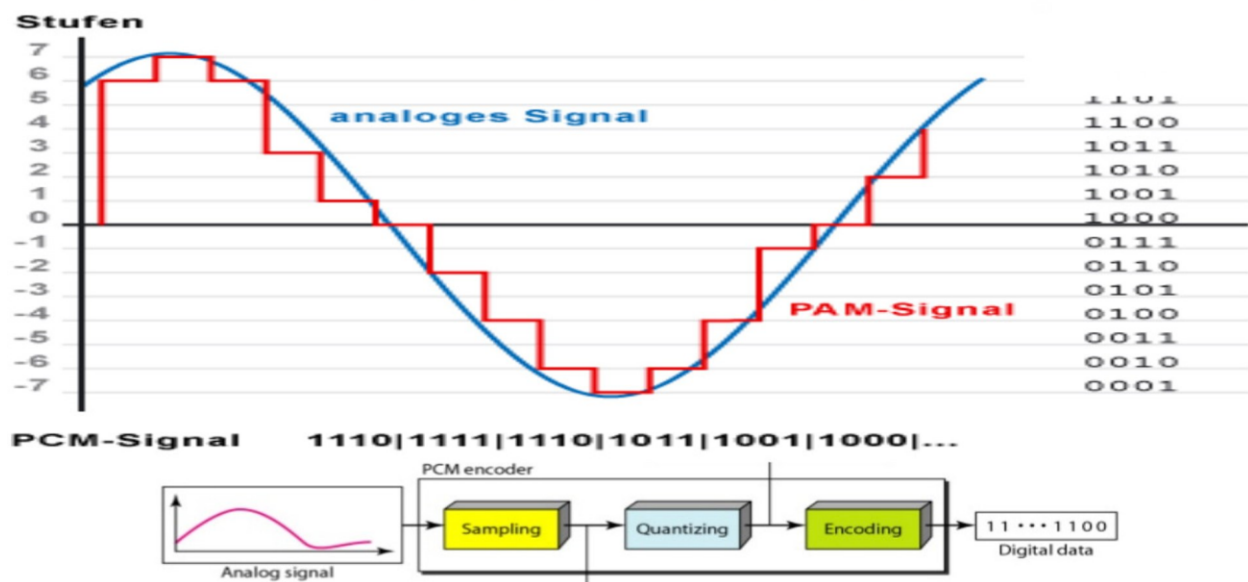
In the TDM system, other signal's samples are incorporated between two adjacent sample signals.



Pulse Code Modulation

Pulse-code modulation is a method used to digitally represent sampled analog signals. In PCM system, a message signal is represented by a sequence of code pulses, which is accomplished by representing the signal in discrete form in both time and amplitude. The basic operations performed in the transmitter of PCM system are sampling, quantization and encoding. In receiver side, the encoded signal is converted to decoded analog signal.

Pulse Code Modulation



TDM-PCM System:

In TDM-PCM system both feature of TDM and PCM are incorporated. We can do multiplexing of two or more signals, then we encoded the signals by PCM, after that this encoded a single signal is transmitted, in the receiver side, it become analog signal, finally all signals are separated from the analog signal. In the TDM-PCM system, TDM is done first and then PCM is done in transmitter side. But in receiver side, the reverse is happened that is, at first, decoding is done, finally demultiplexing is happened. For improvement of our output signal, we have also added the low pass filter. Thus, we can save Bandwidth, provide facilities to multiple users.

Block Diagram of TDM-PCM system:

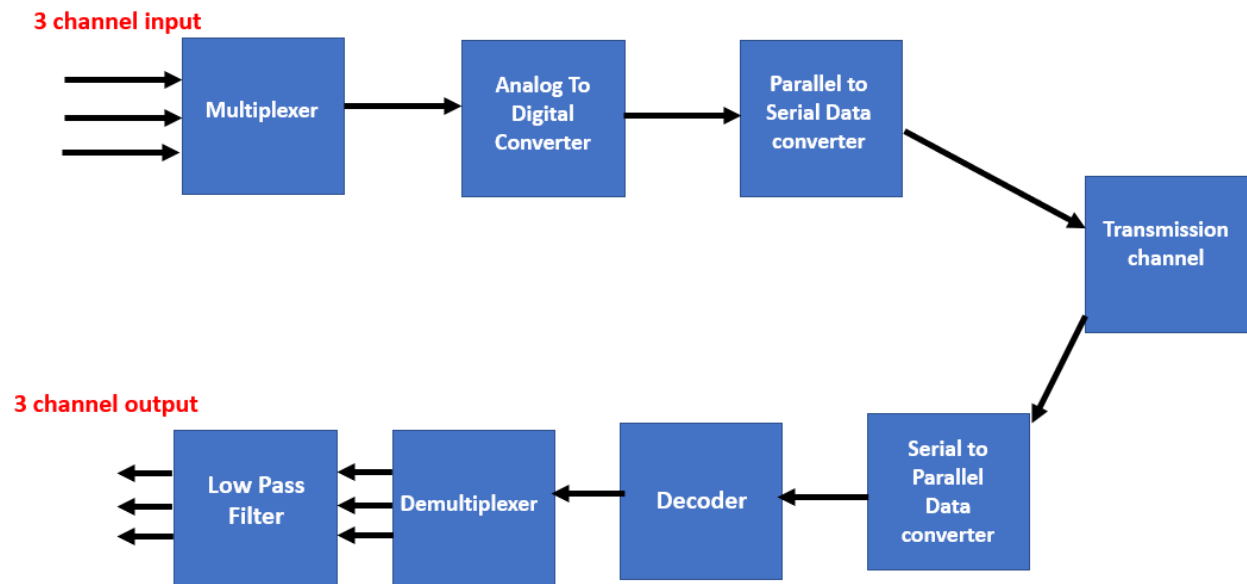
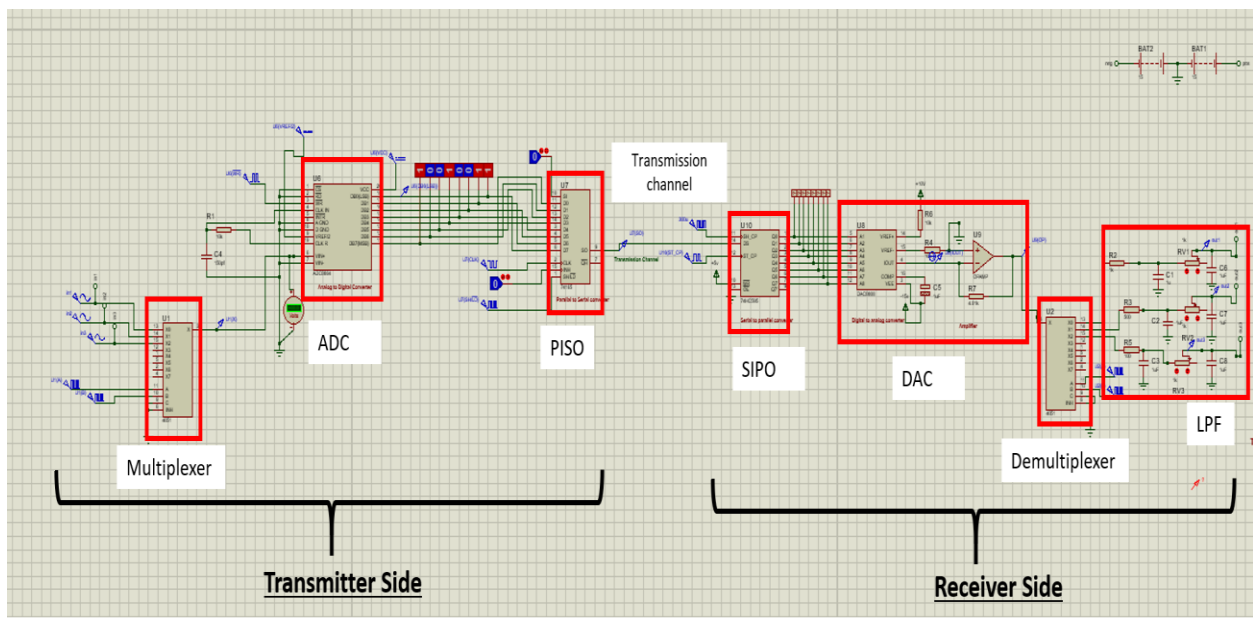


Figure 01: Block diagram of TDM-PCM system

Circuit Diagram at a glance:



Description of Blocks:

Time Division Multiplexer:

This block combines multiple communication signals to a single channel signal. For project purpose, we have taken only three channel input.

To implement this block, we have used cd4051 multiplexer, which takes three input signals, and turns into one signal. **We have selected sequentially X0, X1, X2 channel by controlling the clock A, B, C pin of multiplexer.**

Truth Table:

Data Select Inputs			Input Selected	Enable	Output (x)
C	B	A			
0	0	0	X0	LOW	X0
0	0	1	X1	LOW	X1
0	1	0	X2	LOW	X2
0	1	1	X3	LOW	X3
1	0	0	X4	LOW	X4
1	0	1	X5	LOW	X5
1	1	0	X6	LOW	X6
1	1	1	X7	LOW	X7

From truth table we can see the required clock to take input from specific channel. This clock signal combinations are similar for both multiplexing and demultiplexing.

Connections and Working Principle:

Three different frequency signals were taken as input for this block. But they have same amplitude peak to peak **0-10v unipolar** signals. Their frequencies were **respectively 10Hz at X0, 25Hz at X1 and 50Hz at X2 channel of multiplexer.**

Pin 'C' is grounded according to truth table. The clock signals are given at pin 'A' and 'B' by 'Dpattern' from generator mode of proteus. **Each clock's pulse width is 0.5ms.**

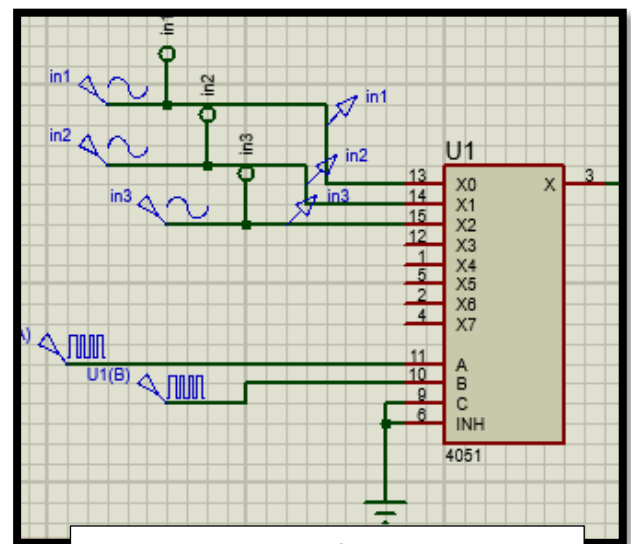


Fig 02: connection of multiplexer block

As ADC0804 (in later block) can't encode negative voltage, we have made our input signal from bipolar to unipolar at input of multiplexer. So, we have given 5V offset to each of input sources to make it unipolar.

How TDM is happening here?

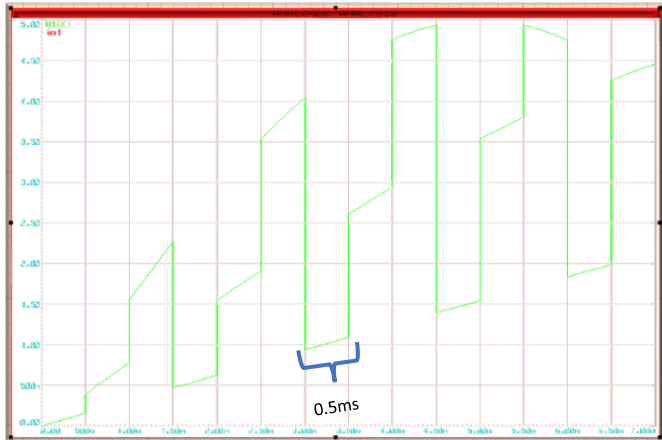


Fig.04: 1st signal(10Hz) follows the TDM signal

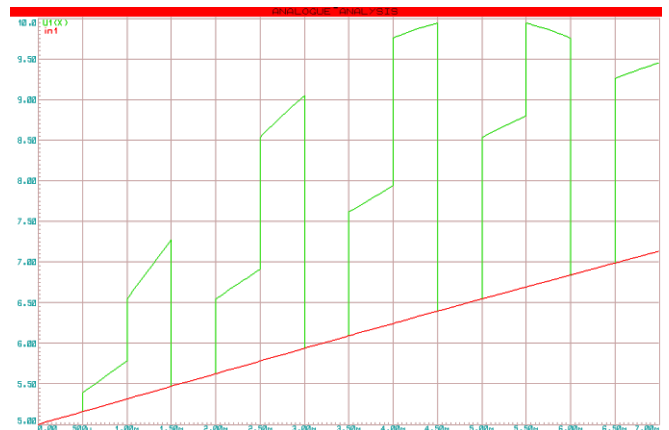


Fig 03: Time division multiplexing results for 7ms

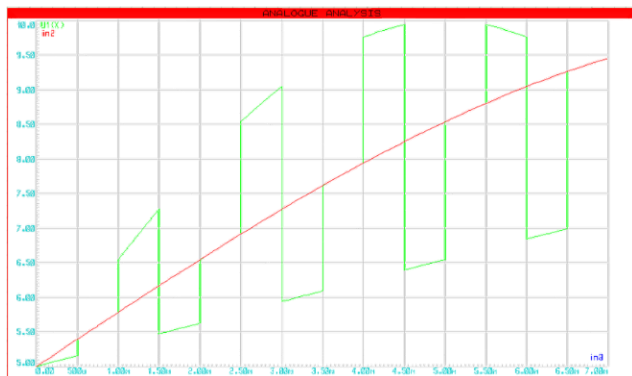


Fig-05: 2nd signal(25Hz) follows the TDM signal

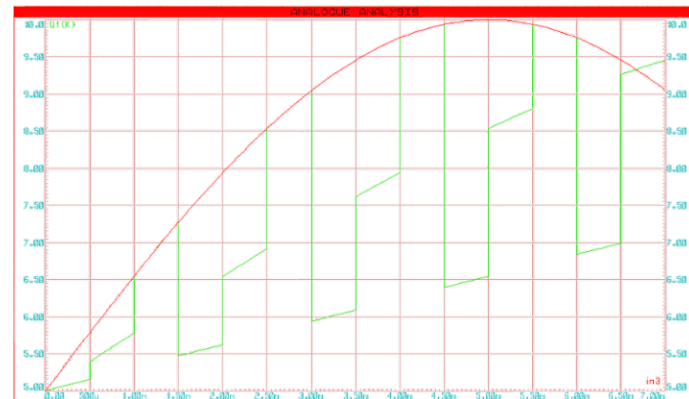


Fig-06: 3rd signal(50Hz) follows the TDM signal

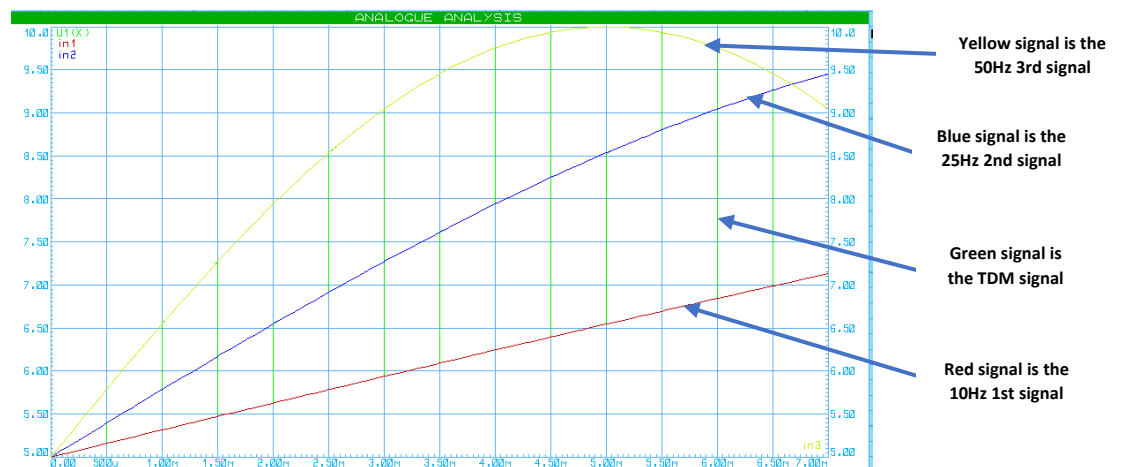


Fig-07: all three input signals (red, blue, yellow) are following the TDM signal(green)

From above five figures (plotted for 7ms), we can see that, the multiplexer taking data from each channel for the duration of 0.5ms. At first, it takes data from X0 channel for 0.5ms, then similarly for X1, X2. In the output signal of multiplexer, we get the combined signal, and TDM is happening in each channel

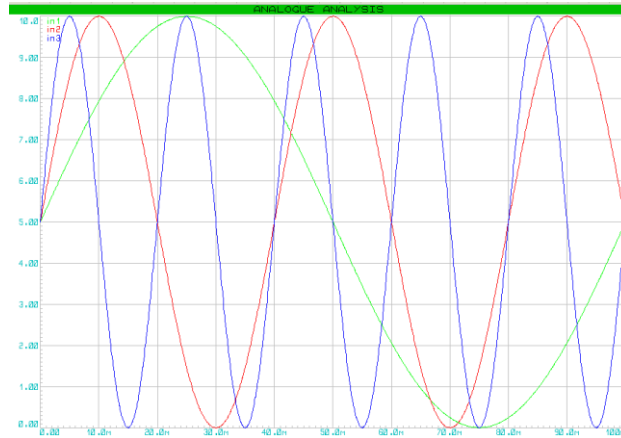


Fig. Three Input signals

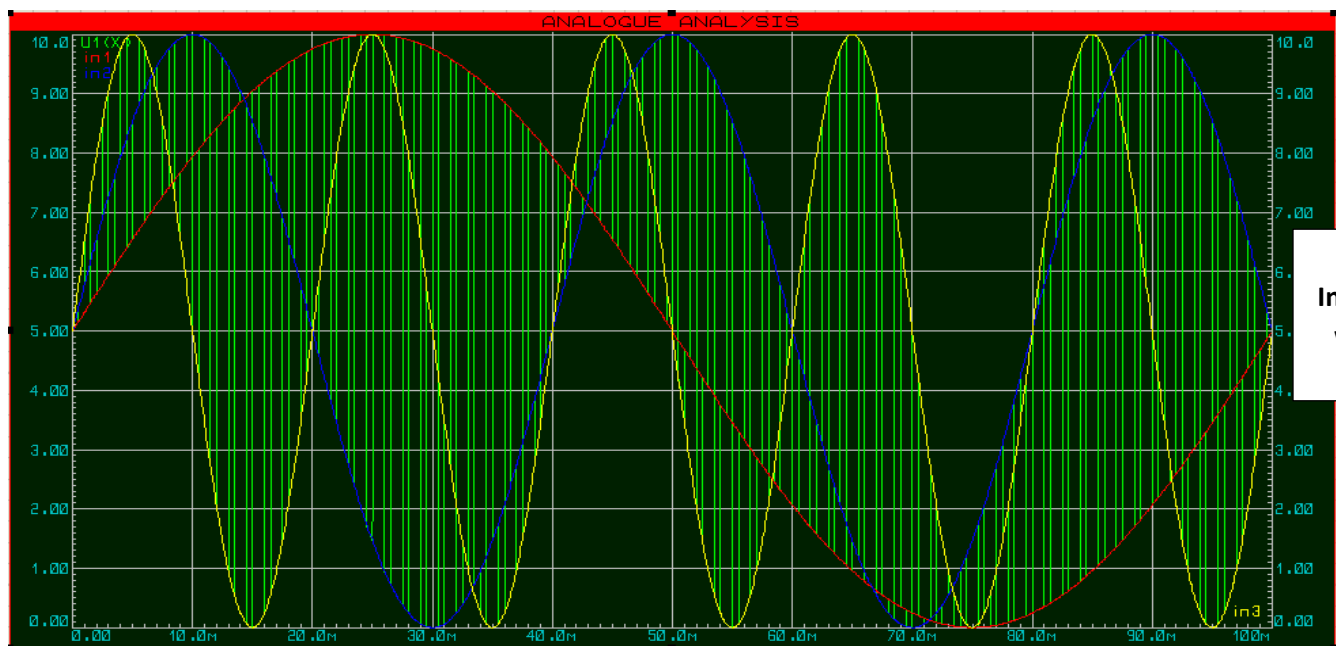


Fig. Three Input signals with TDM signal

From above figure we can see the time division multiplexed output for 0.1s duration. We had taken three signals as input to multiplexer, now we can see that all three signals are combined in the output of multiplexer

Here, the **green** signal is TDM output signal

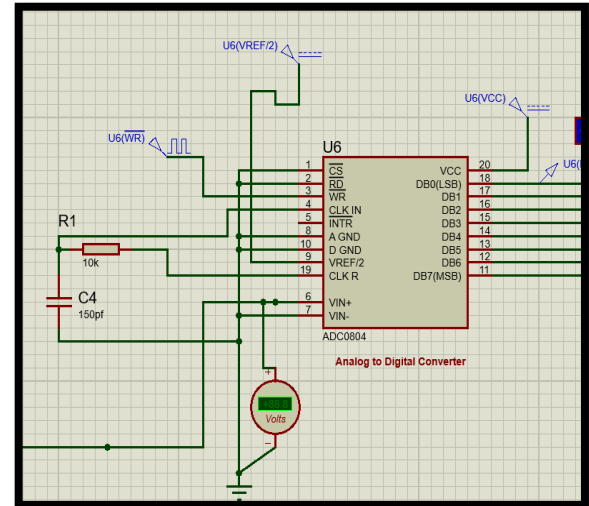
Red signal is 10Hz input signal

Blue signal is 25Hz input signal

Yellow signal is 50Hz input signal

Analog to Digital Converter

The PCM process is done here. This block samples, quantize and encoded. We have used 8-bit ADC0804, which convert the analog incoming TDM signal to encoded digital signal. The input is given at Vin+ pin. The output is collected through D0~D7 output line of ADC. 10v is given at VCC pin, and at Vref/2 is given 5 volts.



The clock signal **4k Hz** is given at WR pin. WR is active low input used to inform the ADC0804 to start the conversion process. If CS = 0 when WR makes a low-to-high transition, the ADC0804 starts converting the analog input into an 8-bit digital number. The amount of time it takes to convert varies depending on the CLK IN and CLK R values explained below.

Fig.-08: ADC0804

CLK IN is an input pin connected to an external clock source when an external clock is used for timing. However, the 804 has an internal clock generator. To use the internal clock generator (also called self-clocking) of the ADC0804, the CLK IN and CLK R pins are connected to a capacitor and a resistor, as shown in figure 08. In that case the clock frequency is determined by the equation:

$$f = \frac{1}{1.1 RC}$$

After conversion of analog to digital, **we get 8 bit stream output at D0~D7. Each bit(1 or 0) duration is 0.25ms.** (as WR pin changing in frequency of 4kHz)

Here, we have used 8 bit uniform quantization. So, it has total 256 different quantization levels. The quantized values are encoded between 0 to 255 to binary. The formula of corresponding analog to 0 to 255 quantization level is:

$$v_{\text{quantization_level}} = \frac{V_{in}}{V_{max}} \times 2^8$$

Here, v_{max} is 10 v, as our input signal is between 0-10v.

V_{in} is incoming analog signal value.

Say, $V_{in} = 4v$,

$$V_{\text{quantized}} = \frac{4}{10} \times 2^8 = 102.4 = 102$$

The binary value of 102 is “01100110”.

In below figure, we can see the binary output for corresponding analog value

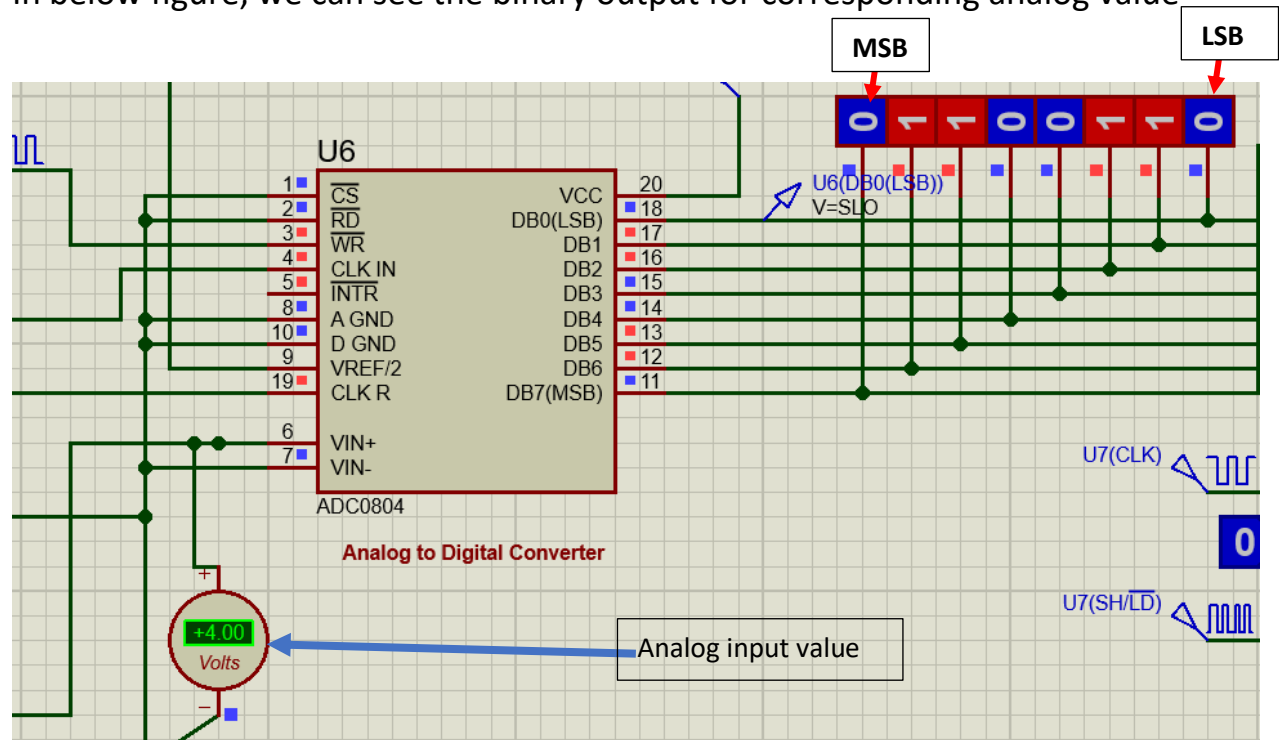


Fig.-09: Typical output value of ADC

Thus, we can map any input analog signal (0-10)v to (0-255) quantization level in binary value.

Parallel to Serial Converter

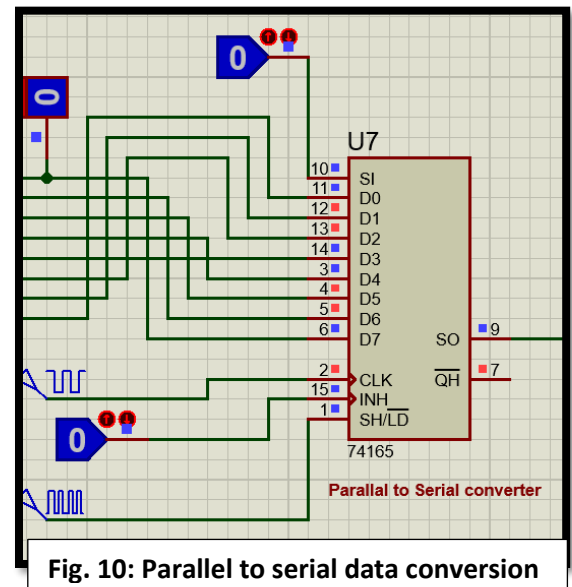
The parallel bit stream or word comes from ADC0804 block. But we have to make in serial data or line code. This operation is accomplished in this block. Here, parallel data comes, in goes out serially. So, we have **used 8 bit PISO(parallel In Serial Out) shift register IC, named 74165IC**. It takes 8 bit parallel data input and deliver serial data. **It produces the line code as NRZ-L.**

Connecection and Working Principle:

74165IC is can work both PISO and SISO mode. But we need only PISO mode, so pin SI(serial input) is given 0 or Low. The D0 to D7 pin of IC 74165 is connected with respectively from D7 to D0 of ADC0804. As **It shifts data from D0(LSB) to D7(MSB)**.

The clock frequency at pin CLK is 32k Hz . As clock of ADC is 4k Hz, so, we have used 8 times more frequency of ADC, as it is 8 bit data.

Parallel loading is inhibited as long as SH/LD pin is high. Data at the parallel inputs are loaded directly into the register while SH/LD pin is low.



In the left figure SH/LD pin is low for once, but high for remaining time in each 8-bit frame. When SH/LD pin is low, it loads parallel all data into IC. After that, in each clock pulse of CLK pin, it shifts one bit. And finally, it shifts all bit after 8 clock pulse.

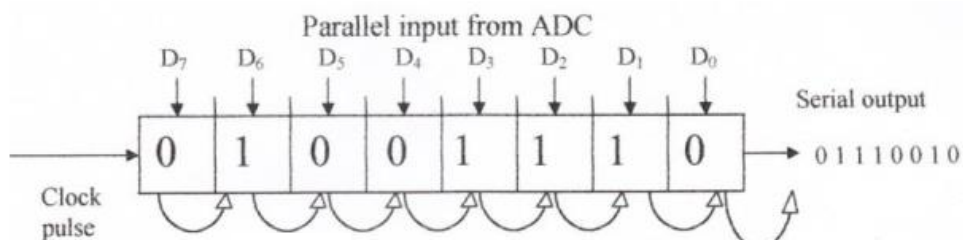


Fig-11 Example How to Shift 8-Bit of Data.

above figure, we can see, how parallel data is converting in to serial data by each clock pulse. At the output, we get line code like figure 12.

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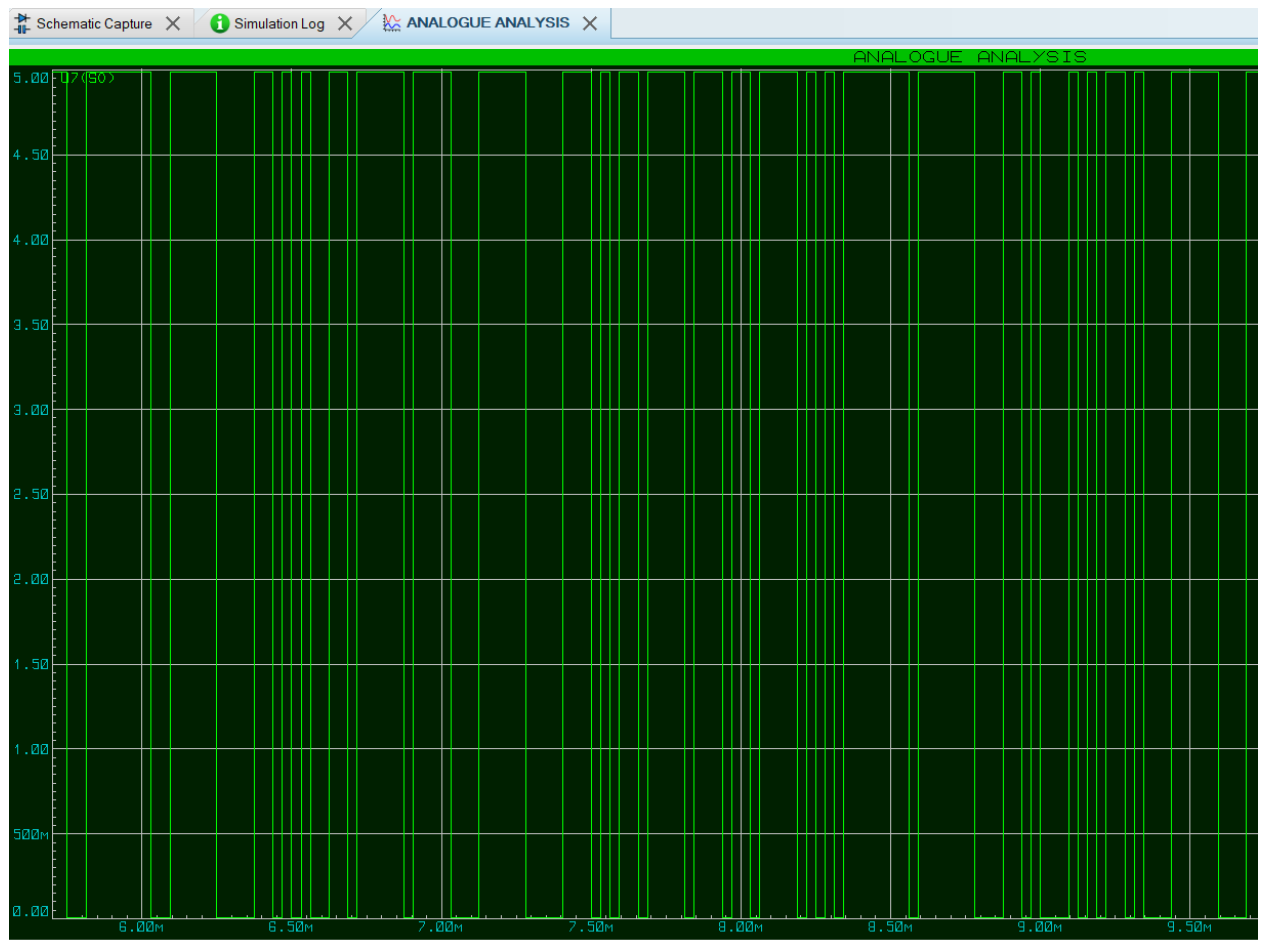


Fig. 12: Output of parallel to serial converter (NRZ line code)

The output of parallel to serial converter is transmitted to through transmission channel. The transmission channel is modeled as a wire in this project. The line codes go to receiver side via wire.

Serial to Parallel Converter

In receiver , the complementary operations of transmitter side is done . At first, we have to convert serial data or line code to parallel data.This parallel data or code word will be then converted analog voltage level.

Connections and Working Principle:

We have used **74HC595 IC** to perform serial to parallel conversion. 74HC595 is a shift register having an eight bit storage register and an eight bit shift register. The data is written first and then stored into the device. It is a high speed CMOS device. The data is usually entered in a serial format. Storage register is used to control the output lines of 74HC595.

The received serial data goes to DS pin of this IC. SH_CP pin stands for “shift Register clock input”, and ST_CP stands for “Storage register clock input”.

The clock pin needs to receive eight pulses. At the time of each pulse, if the data pin is high, then a 1 gets pushed into the shift register. Otherwise, it is a 0. When all eight pulses have been received, then enabling the 'Latch' pin copies those eight values to the latch register.

The ST_CP pin is used to update the data to the output pins.

The parallel bit is collected in Q0 to Q7 pin of 74HC595 IC. Then these pins are connected with digital to analog converter.

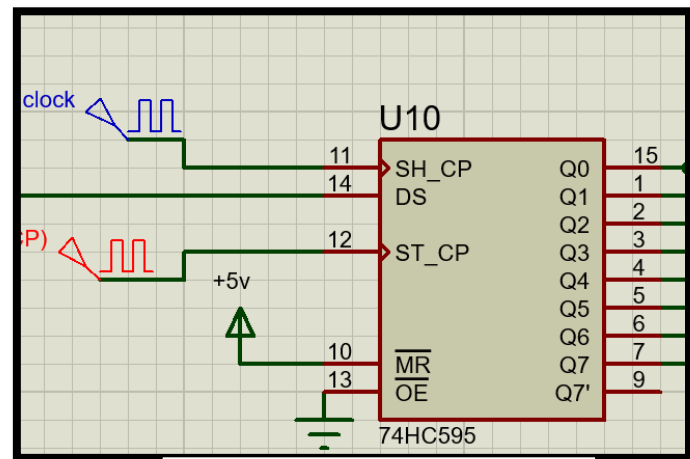


Fig.13: Connection of 74HC595

Digital to Analog Data Converter Block

After getting parallel code word in receiver side , now it is time to decode the signal into analog data or analog voltage level. To perform this operation successfully, we have used DAC0808 and OPAMP .

The DAC0808 turns the digital 8 bit input into current as output, and op-amp converts this current into voltage. Opamp correct the polarity of signal, to maintain similarity between transmitted and received signal. Op-amp is working as transimpedance amplifier here.

Connections of DAC:

The 8 outputs of SIPO shift register is connected with pin A1 to A8 of DAC0808 . The Vref+ & vref- work as respectively positive and negative reference voltage. Reference voltage defines the output voltage range of analog output signal from op-amp output. Iout pin is the output pin of DAC0808. In this pin, we get our output.

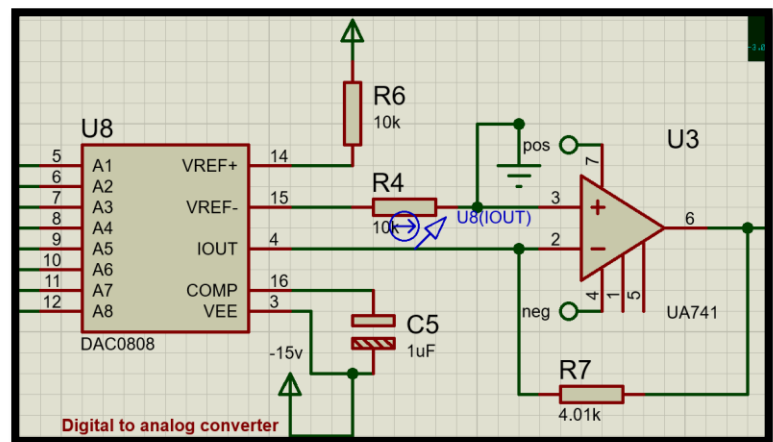


Fig 14 connection DAC and Op-Amp

The output signal magnitude is directly proportional to 8-bit input signal and reference voltage value.

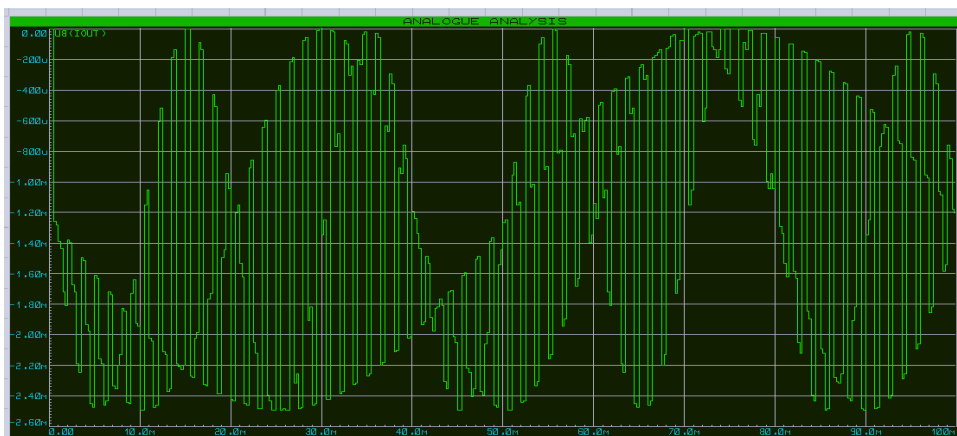


Fig 15: output of DAC0808

Here, op-amp is connected at inverting opamp. The output and input relation of this op-amp is defined as below....

$$I_{in} = \frac{V_1 - V_0}{R_f} = \frac{0 - V_0}{R_f} = \frac{-V_0}{R_f}$$

The output of op-amp is shown in below figure. This signal looks like the multiplexer output signal in transmitter side. That means we have correctly achieved our signal.

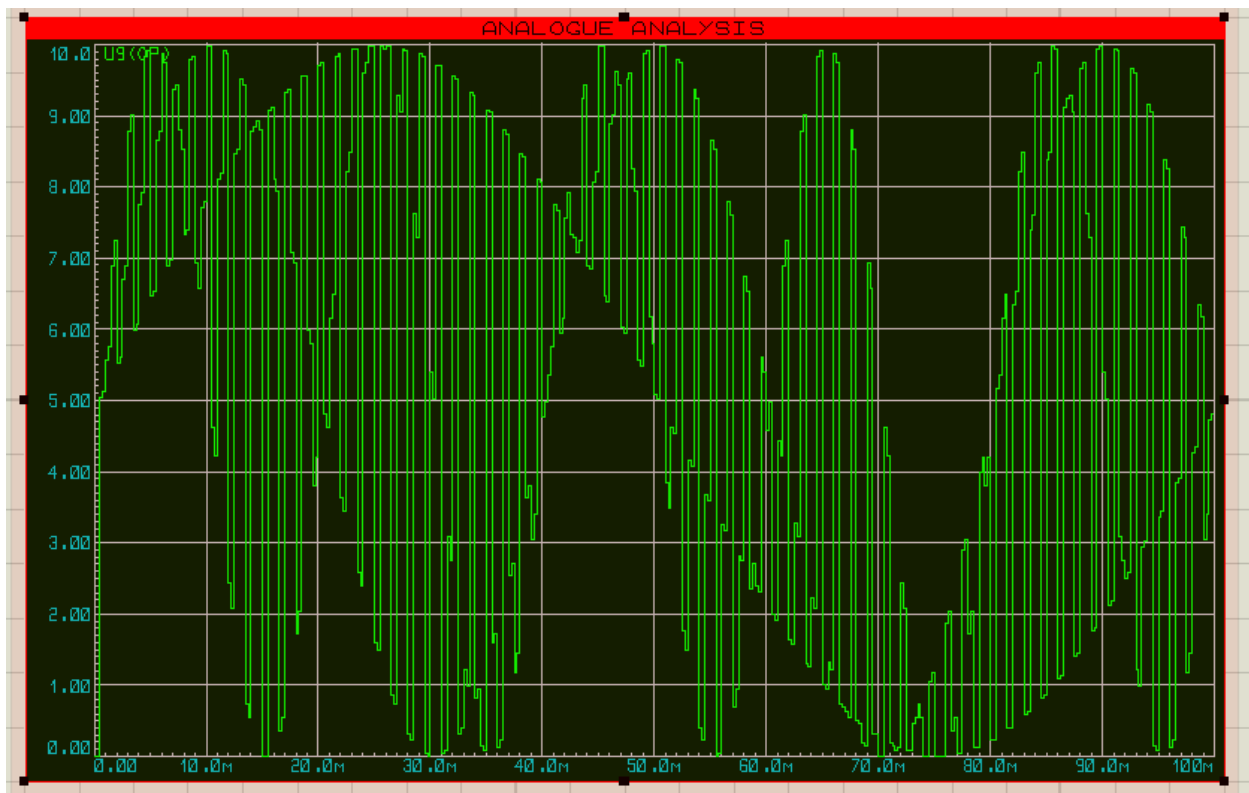


Fig. 16: Output of Op-amp

Time Division Demultiplexing

Now, we have to do the time division demultiplexing. Here, we will retrieve all three signals individually, which were transmitted as a combined or multiplexed signal. Here, we have same IC 4051, which was used in transmitter side.

Connections

Connections are similar to the multiplexer of transmitter portion. The input comes here through pin 3 (X). Pin 13 (X0), Pin 14 (X1), pin 15 (X2) are output pin. Pin A, B, C are selecting the channels of X0, X1, X2 sequentially. The input in pin A, B are “Dpattern” in proteus.

A->010

B->001

Pulse width is of each signal is A, B is 0.5ms.

Working Principle:

CD4051, as a demux, extracts all three channels signals. It distributes incoming data to X0, X1, X2 for a fixed duration.

There is some time lag between multiplexer input of transmitter side and demultiplexer output of receiver side. We had to incorporate this time lag in the demultiplexer's A, B, C pin to synchronize all three channel (X0, X1, X2) output.

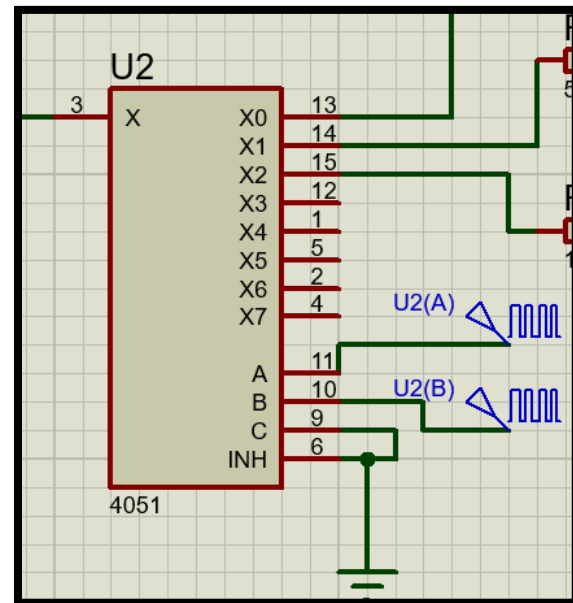


Fig. 17: Demultiplexer connections

Two Stage Low Pass Filtering

The output demultiplexer has some high frequency component, as it went through quantization. For smootheing the three signals, we have used simple RC low pass filtering.

The low pass filtering is occuring in each channel individually. In the first stage RC low pass filtering the cut off frequencies in X0,X1,X2 are respectively 150Hz, 318Hz, 1591Hz. In the next stage, we have used a pot, in the place of fixed resistor. So that, we can tune the filter , as per our requirement.

After filtering, we get our desired output. The output signals are very close to input signal. Although, there is some attenuation. Comparatively, greater attenuation has been occurred in the high frequency signal.

For remedy, we can do fast clocking in all block, or high frequency clock.

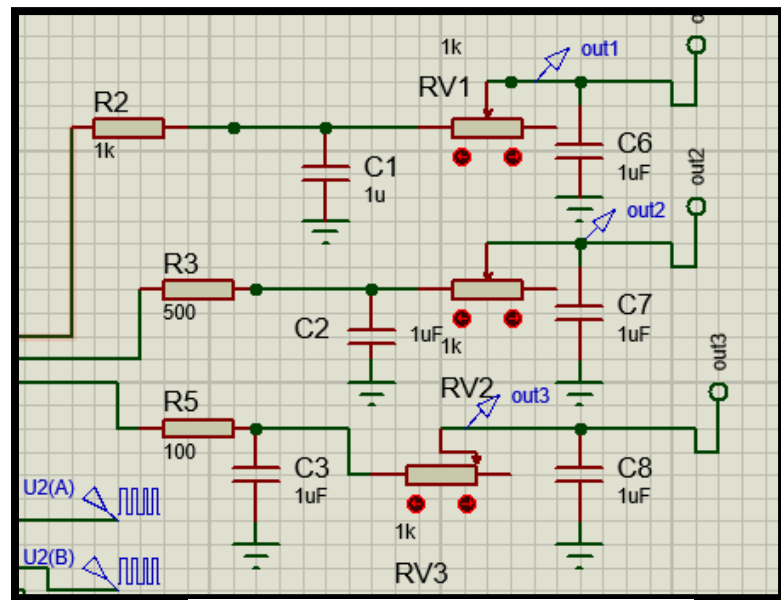


Fig. 18: Low pass filtering circuit

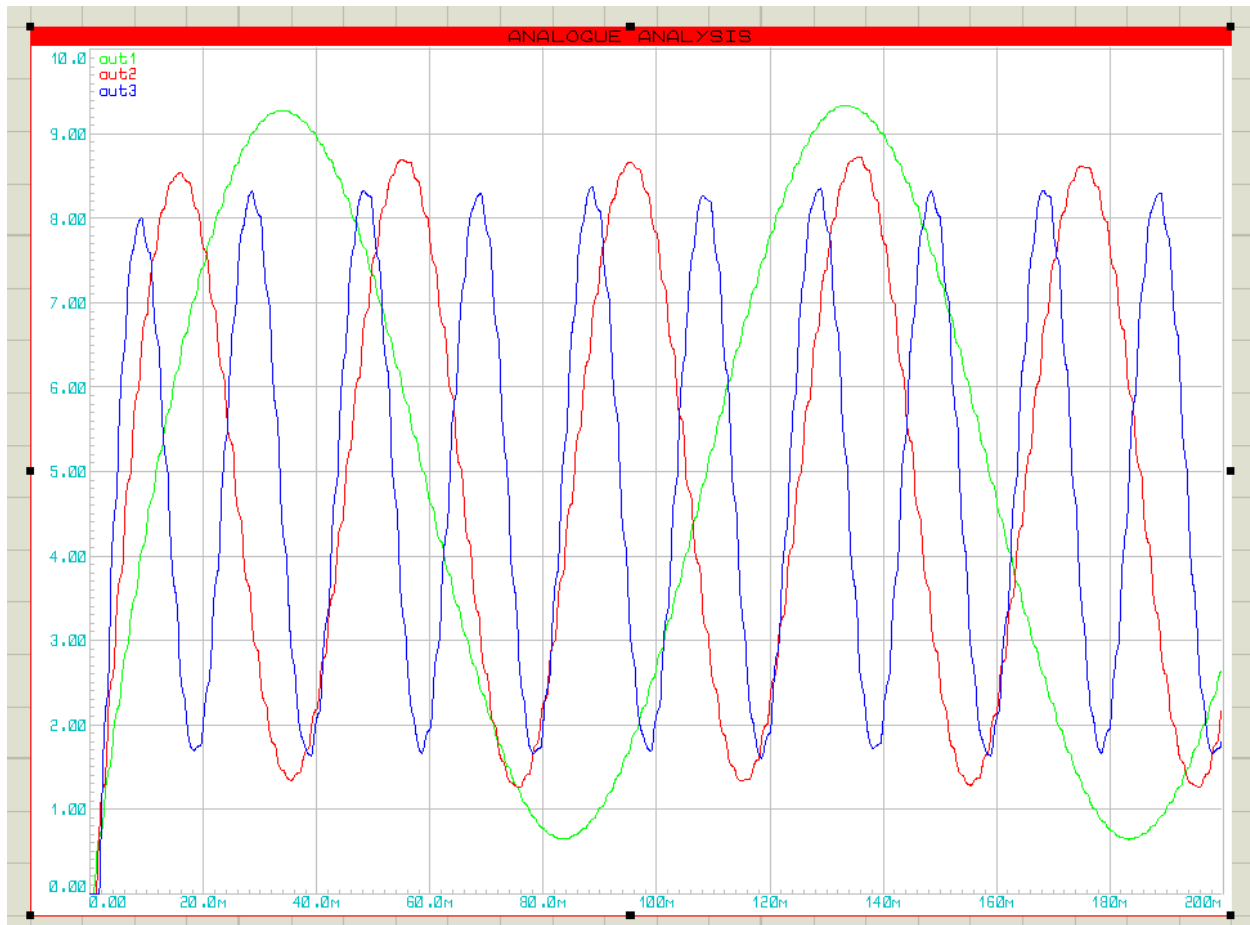
The amplitude of output signal is slightly reduced in each channel. By using proper amplifier , we can fix this issue.

The Final Output signals at a Glance:

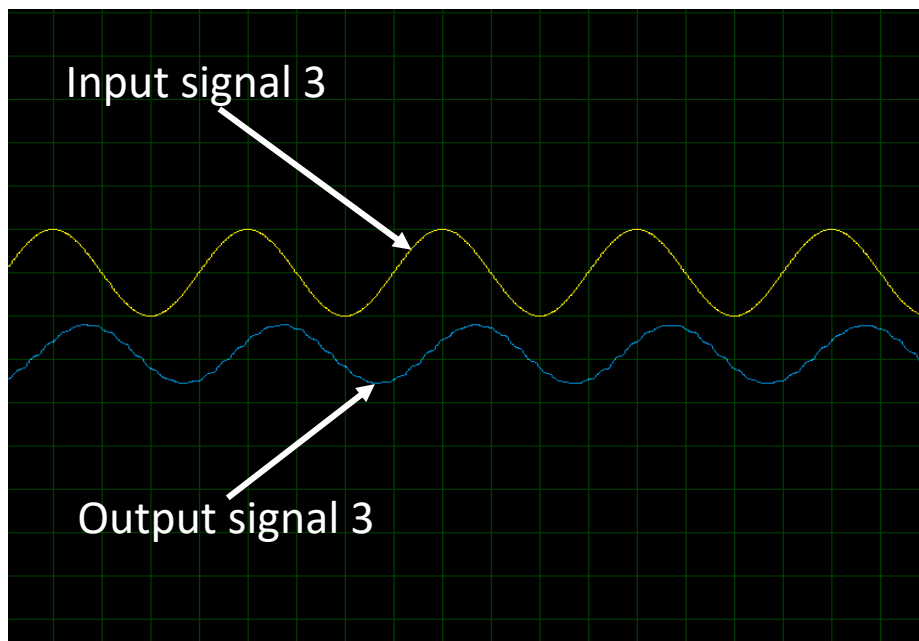
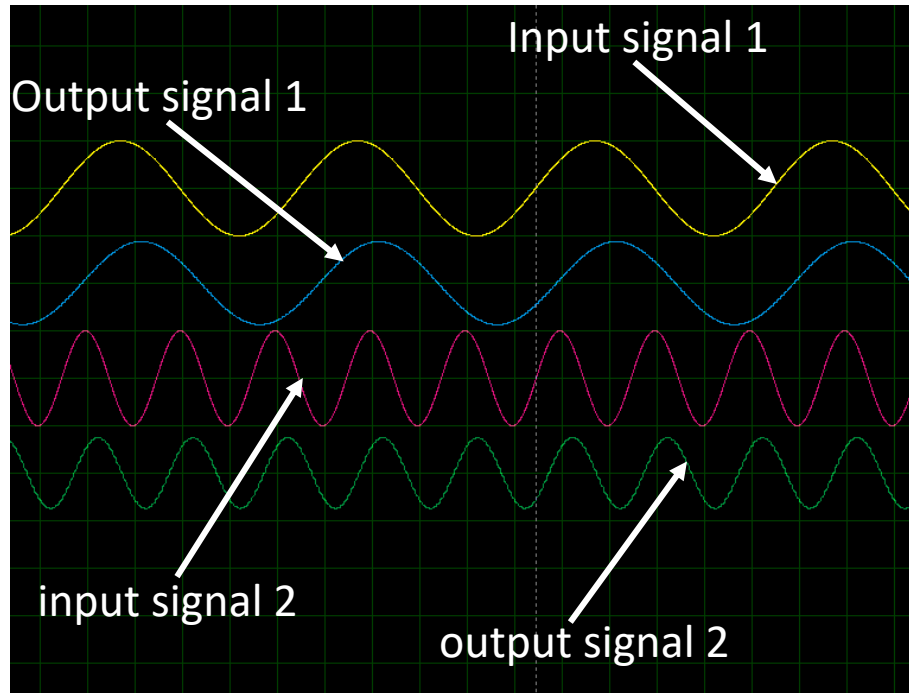
Here, **Green** signal is 10Hz output signal

RED signal is 25Hz output signal

Blue signal is 50Hz output signal



Output and Input signal Comparison



From the comparison, it is clear that, we can successfully retrieve our transmitted input signal in the receiver side. Although, there is light attenuation. After all, we think, we have completed our project objectives.

Conclusion:

In this project, we have tried to build a TDM-PCM system, which will be able to transmit multiple signal digitally, and finally retrieve the same input signals in receiver side.

To accomplish our project , we have used many IC to complete the whole project in the right time. If we used all analog devices, we think, it will be very tough for us to complete the project. After all, we have learnt every component, which are used in this project. Besides, we have also learn about the some basic priciples of digital communication system, which will be very helpful in the near future.

In this project, we have faced many difficulties to complete this project. But, it has helped us to learning a lot. In fututre, we will imporove the design to make it more sustainable and reliable.

***** **THE END** *****