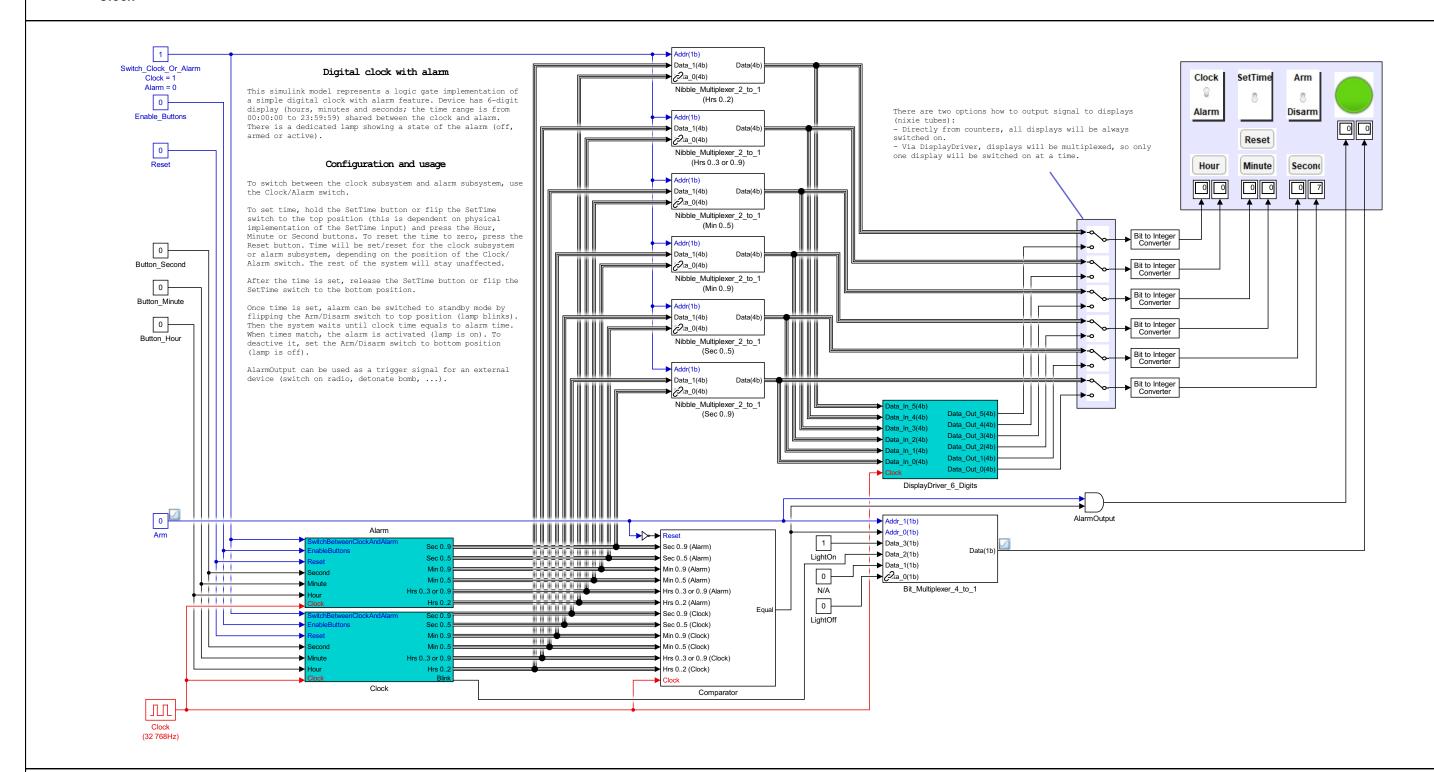
Clock

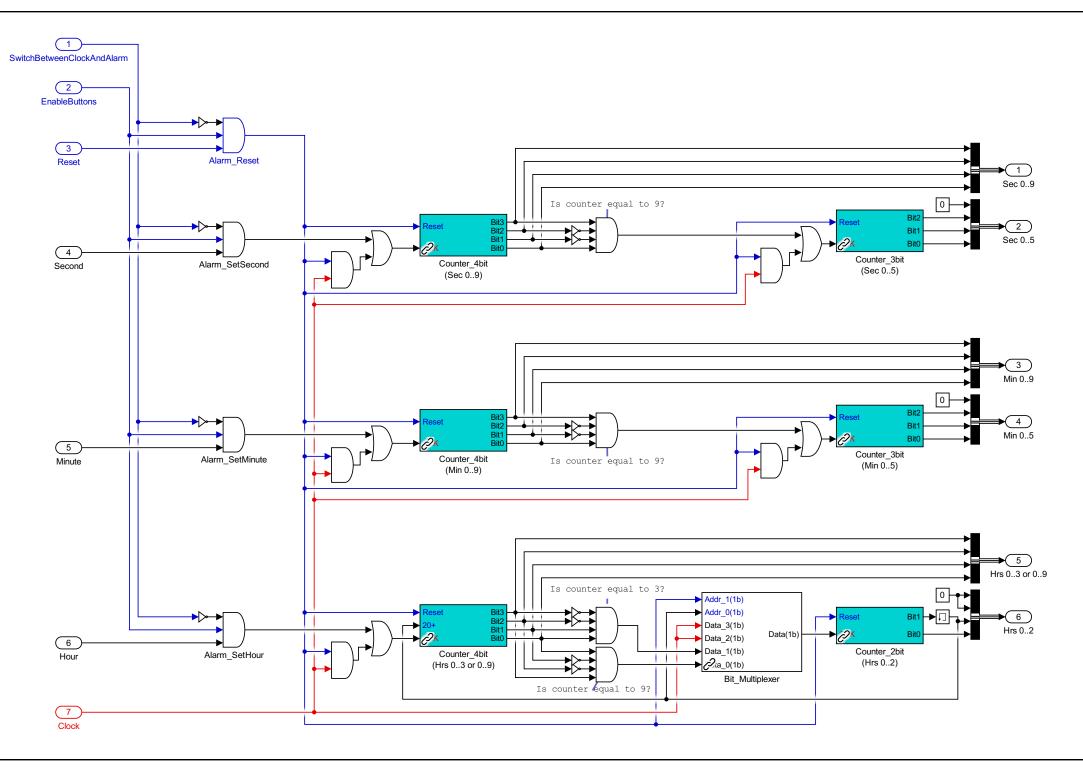


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Clock/Comparator 0 N/A 1 ResetVal 1 LatchVal 0 KeepVal F:\Workspace\05_Projekty\Projects_Simulink\Clock\Clock.slx printed 22-Apr-2024 17:39 page 2/14

Clock/DisplayDriver_6_Digits **1** Data_Out_5(4b) **2** Data_Out_4(4b) **→**(3) Data_Out_3(4b) **4** Data_Out_2(4b) **→** 5 Data_Out_1(4b) **→** 6 Data_Out_0(4b) Select_7(1b) Addr_2(1b) Select_6(1b) Select_5(1b) Select_4(1b) Addr_1(1b) Select_3(1b) Counter_3bit (0..5) Select_2(1b) Select_1(1b) Select_0(1b) Decoder_3_to_8 Addr_2(1b) Addr_1(1b) Addr_0(1b) 1)= Data_In_5(4b) ► Data_4(4b) ▶ Data_3(4b) 2 **▶** Data_2(4b) Data_In_4(4b) ■ Data_1(4b) (3)= **≥**2ia_0(4b) Data_In_3(4b) Nibble_Multiplexer_8_to_1 4 Data_In_2(4b) 5 Data_In_1(4b) 6 Data_In_0(4b) F:\Workspace\05_Projekty\Projects_Simulink\Clock\Clock.slx printed 22-Apr-2024 17:39 page 3/14

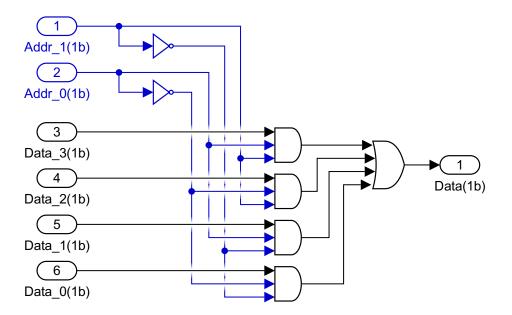
Clock/Alarm



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Clock F:\Workspace\05_Projekty\Projects_Simulink\Clock\Clock.slx printed 22-Apr-2024 17:39 page 5/14

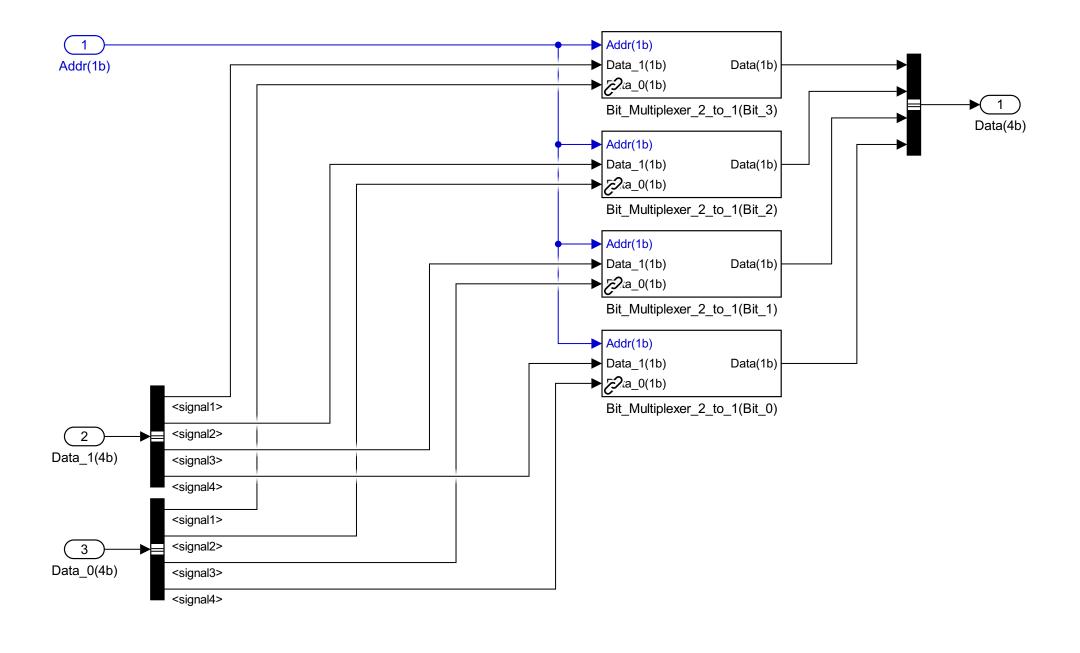
Bit_Multiplexers_Lib/Bit_Multiplexers_Lib/Bit_Multiplexer_4_to_1





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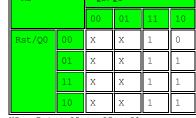
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3-bit counter with reset (0 -> 1 -> 2 -> 3 -> 4 -> 5 -> 0)

Pres	ent st	ate	Rst	:=0					Rs	:=1					Next State											
															Rs	:=0		Rst=1								
Q2	Q1	Q0	J2	K2	K2 J1 K		J0	K0	J2	K2	J1	K1	J0	K0	Q2	Q1	Q0	Q2	Q1	Q0						
0	0	0	0	X	0	Х	1	Х	0	X	0	Χ	0	Х	0	0	1	0	0	0						
0	0	1	0	X	1	Х	Х	1	0	Х	0	Χ	Х	1	0	1	0	0	0	0						
0	1	0	0	X	Χ	0	1	Х	0	X	Χ	1	0	Х	0	1	1	0	0	0						
0	1	1	1	X	Χ	1	Χ	1	0	Χ	Χ	1	Χ	1	1	0	0	0	0	0						
1	0	0	Χ	0	0	Х	1	Х	Χ	1	0	Х	0	Х	1	0	1	0	0	0						
1	0	1	Х	1	0	Х	Χ	1	Х	1	0	Χ	Χ	1	0	0	0	0	0	0						
1	1	0	Х	1	Χ	1	0	Χ	Х	1	Х	1	0	Χ	0	0	0	0	0	0						
1	1	1	Х	1	Χ	1	Χ	1	Χ	1	Χ	1	Х	1	0	0	0	0	0	0						

J2		Q2/	Q1		
		00	01	11	10
Rst/	00	0	0	Х	Х
Q0	01	0	1	Х	Х
	11	0	0	Х	Х
	10	0	0	Х	Х



 $J2 = \sim Rst.Q1.Q0$

 $K2 = Rst + Q0 + \sim Q2 + Q1$

J1		Q2/	Q2/Q1											
		00	01	11	10									
Rst/Q0	00	0	Х	Х	0									
	01	1	X	X	0									
	11	0	Х	Х	0									
	10	0	Х	Х	0									

1 Bit2

Bit1

J1 = ~Rst.~Q2.Q0

J0 Q2/Q1

00 01 11 10

Rst/Q0 00 1 1 0 1

01 X X X X

11 X X X X

10 0 0 0 0 0

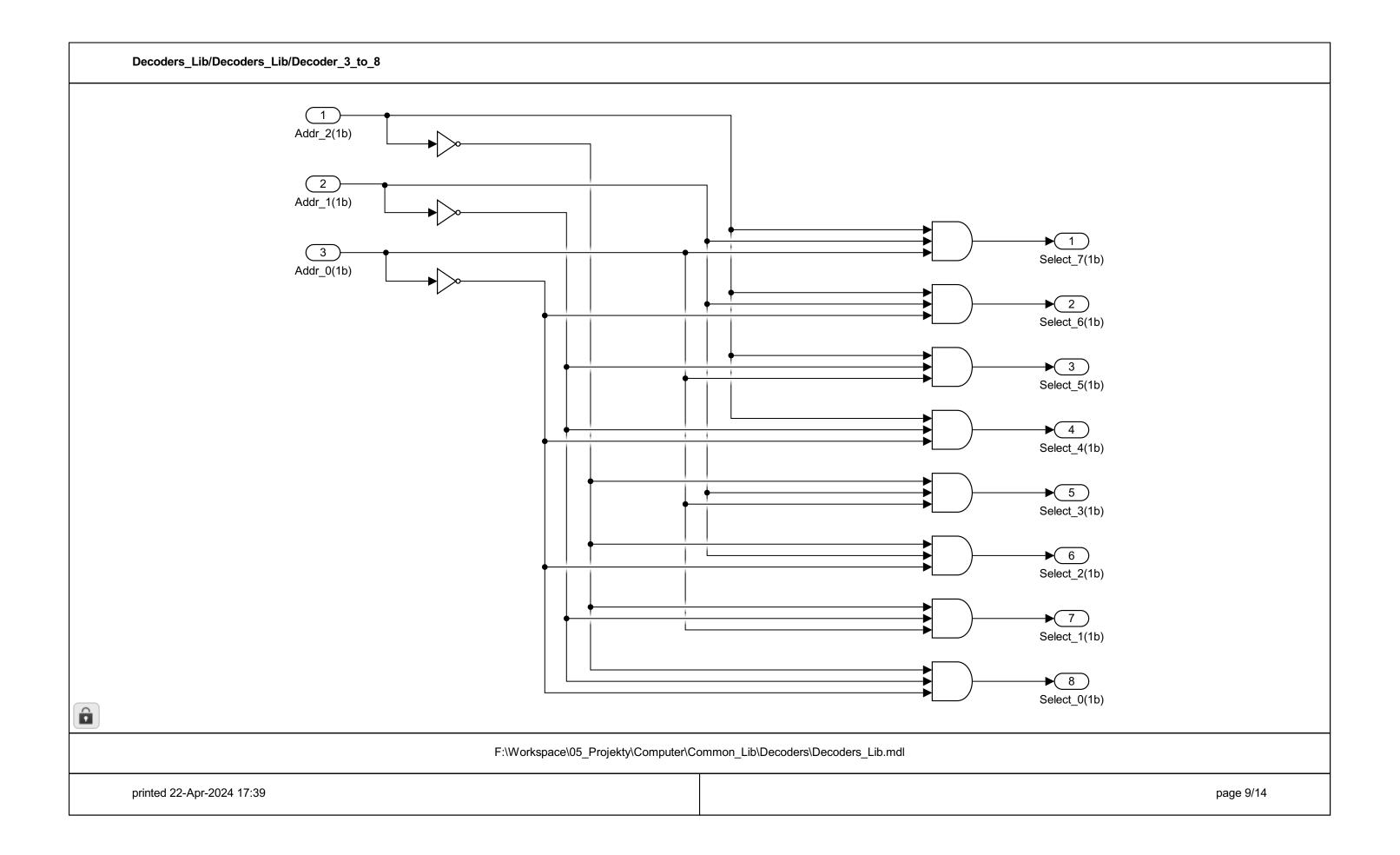
J0 = (~Q2 + ~Q1).(~Rst + Q0)

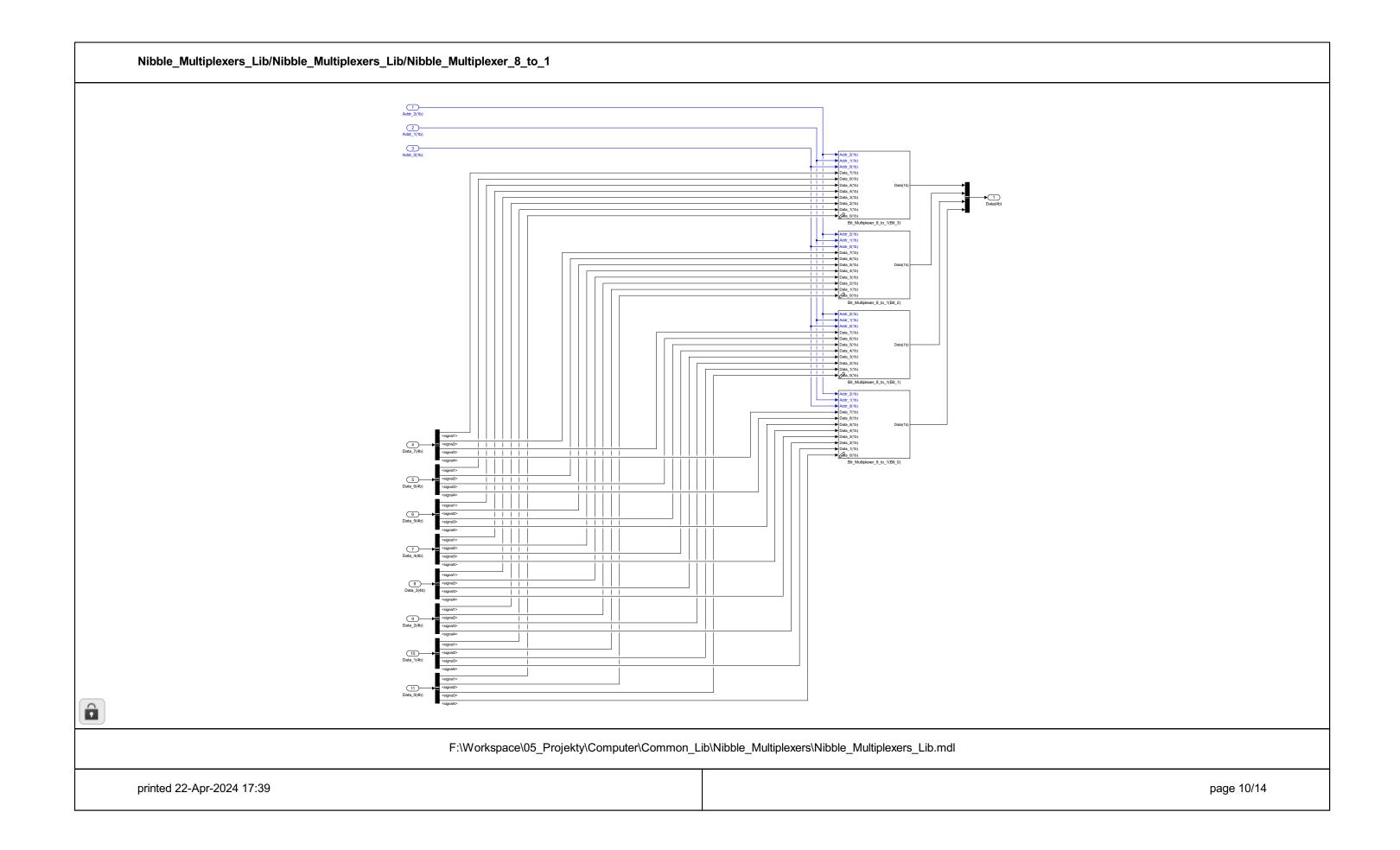
K0 = 1

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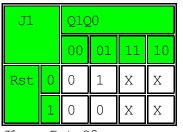
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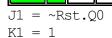


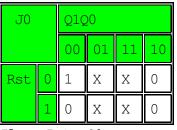


2-bit counter (0..2) with reset

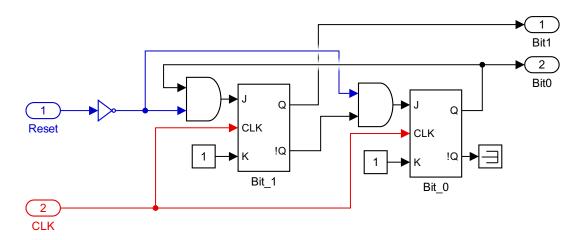
	sent ate	Rs	st=0			Rs	st=1			Next state									
Sto	ace									Rst:	=0	Rst	=1						
Q1	Q0	J1	J1 K1		K0	J1	K1	J0	K0	Q1	Q0	Q1	Q0						
0	0	0	0 X		Χ	0	Х	0	Χ	0	1	0	0						
0	1	1	Χ	Χ	1	0	Χ	Χ	1	1	0	0	0						
1	0	Х	1	0	Χ	X	1	0	Χ	0	0	0	0						
1	1	Х	X 1		1	Х	1	Χ	1	0	0	0	0						







 $J0 = \text{Rst.} \sim Q1$ K0 = 1



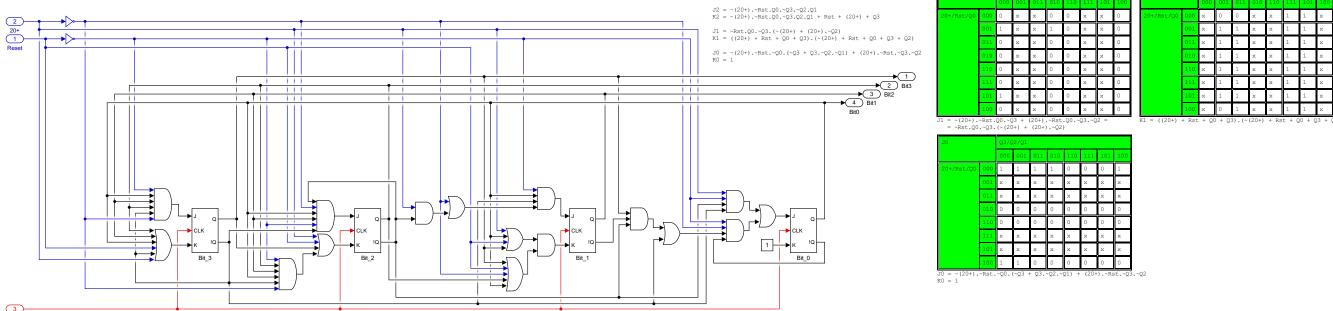
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4-bit counter with reset
If (Hours < 20) then
(0 -> 1 -> 2 -> 3 -> 4 -> 5 -> 6 -> 7 -> 8 -> 9 -> 0)

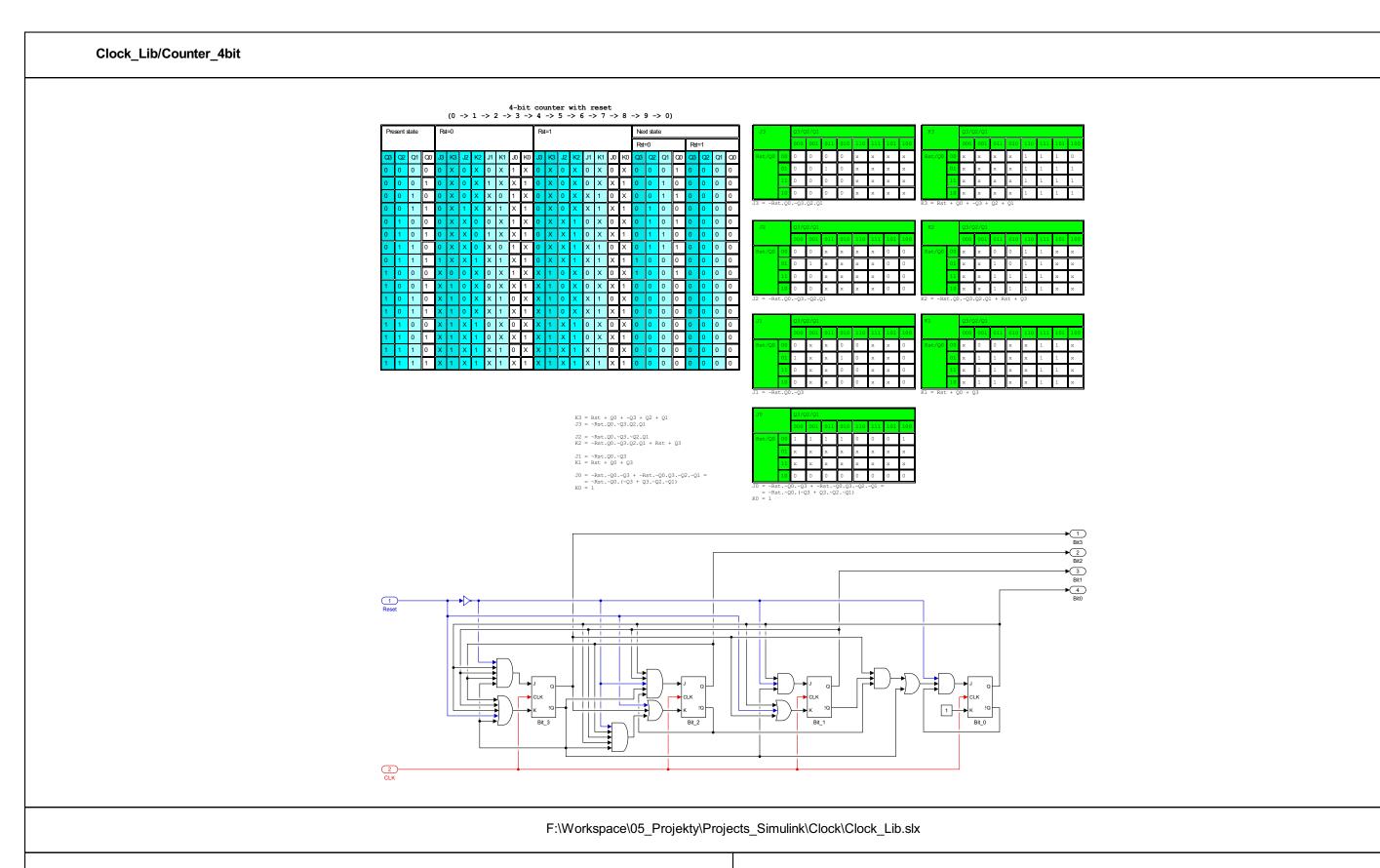
If (Hours >= 20) then

Presen	nt state	е																																				١	Next sta	ate						╝	J3			Q3/Q2	2/Q1							K3	3			
									ŀ	burs	< 20)												Hour	rs>=:	20									Hou	s<20)					Hours	s>= 20)						000	001	011	010	110	111	101	100					0
						Rst	= 0							Rst :	= 1						Rst	= 0						Rst	= 1				R	gt = 0	1	ĺ	Rst :	= 1		F	Rst = 0)		Rst	= 1		20+/Rs1	t/Q0	000	0	0	0	0	х	х	х	х	20+	/Rst/	Q0 0	00	x
Q2	Q1	Q0	J3	КЗ	J2	K2	J1	K1	J0	K0	J3	КЗ	J2	K2	J1	K1	JO K	(O J	3 K3	J2	K2	J1 k	(1 J) K0	J3	КЗ	J2	K2	J1	K1	JO K	(O)	3 Q2	2 Q1	1 Q0	Q3	Q2	Q1	Q0 C	Q3 Q	2 Q	1 Q0	Q3	Q2	Q1 C	00		ſ	001	0	0	1	0	х	х	х	х			0	01	х
0	0	0	0	Х	0	Χ	0	Х	1	Х	0	Х	0	Х	0	Х) >	(0	Х	0	Х	0 >	(1	Х	0	Х	0	Х	0	Х	0 X	0	0	0	1	0	0	0	0 0	0	0	1	0	0	0 0				011	0	0	0	0	х	х	х	х			C	11	х
0	0	1	0	Х	0	Χ	1	Х	Х	1	0	Х	0	Х	0	X	X 1	0	Х	0	Х	1 >	< X	1	0	Х	0	Х	0	X	X 1	0	0	1	0	0	0	0	0 0	0	1	0	0	0	0 0				010	0	0	0	0	х	х	х	х			0	10	х
0	1	0	0	Х	0	Х	Х	0	1	Х	0	Х	0	Х	Х	1) >	< 0	Х	0	Х	X C) 1	Х	0	Х	0	Х	Х	1	0 X	0	0	1	1	0	0	0	0 0	0	1	1	0	0	0 0				110	0	0	0	0	х	х	х	х			1	10	х
0	1	1	0	Х	1	Х	Х	1	х	1	0	Х	0	Х	х	1	X 1	0	Х	0	Х	X 1	Х	1	0	Х	0	Х	Х	1	X 1	0	1	0	0	0	0	0	0 0	0	0	0	0	0	0 0				111	0	0	0	0	х	х	х	х			1	11	x
1	0	0	0	Х	Х	0	0	Х	1	Х	0	Х	Х	1	0	Х) >	(0	Х	Х	1	0 >	(0	Х	0	Х	Х	1	0	х	0 X	0	1	0	1	0	0	0	0 0	0	0	0	0	0	0 0	1			101	0	0	0	0	х	х	х	х			1	01	х
1	0	1	0	Х	Х	0	1	Х	х	1	0	х	Х	1	0	X	X 1	0	Х	Х	1	0 >	(X	1	0	х	х	1	0	x	X 1	0	1	1	0	0	0	0	0 0	0	0	0	0	0	0 0	-			100	0	0	0	0	х	х	х	х			1	00	х
1	1	0	0	Υ	Υ	n	· Y	n	1	· Y	0	Υ	Υ	1	×	1))	(0	X	X	1	y 1		×	0	×	×	1	x	1	n x	0	1	1	1	0	0	0	0 0	0	٥	0	0	0	0 0	-	J3 = ~ (2	20+).~	-Rst.Ç	Q0.~Q	3.Q2.	.Q1						K3 =	(20+)) + F	st	+
1	1	1	1	^ Y	^ Y	1	Y	1	· ·	1	0	^ Y	^ V	1	^ v	1	y 1	, ,	Y	Y	1	Λ I	V	1	0	Y	^ V	1	^ Y	1	V 1	1				0	0	0	0 0	0	0	0	0	0	0 0	-	J2			Q3/Q2	2/Q1							K2				Ç
1	0	0	· ·	^	^	· ·	^	· ·	1	' '	· ·	^	^	' '	^	· ·	^ I	/	1	^	· ·	^ '	/ 0	· '	· ·	1	^	· ·	^	' '	^ I	/ 1	0	0	1	0	0	0	0 0	0	0	0	0	0	0 0	-				000	001	011	010	110	111	101	100	Ш				0
0	0	4	^	4	٥	^	٥	^	' V	^	^	1	0	^	0	^	<i>y</i> 1	` ^	1	0	^	0 /	()	^	^ ~	1	0	^	0	^	V 1		0	0	'	0	0	0	0 0	0	0	0	0	0	0 0	_	20+/Rst	t/Q0	000	0	0	×	х	х	х	0	0	20+	/Rst/	Q0 0	00	×
0	4	-	^	_	٥	۸	v	^	^	' '	^	1	0	^	U	^	<u>`</u>	· ·	<u>'</u>	0	^	0 /	` ^	· '	<u> </u>	÷	0	^	V	_	^	, O	0	0	0	0	0	0	0 0	0	0	0	0	0	0 0	-			001	0	1	х	х	х	х	0	0			0	01	×
0	1		Χ	1	0	X	Χ	1	U	Χ.	^	1	0	×	Χ	1	, ,	` ^	1	U	X	X 1	0	^		1	0	X	Χ	1	0 2	. 0	0	0	0	0	0	0	0 0	0	0	0	U	U	Ů	-		Ī	011	0	0	х	х	х	х	0	0			0	11	×
U	1	1	Х	1	0	Х	Х	1	Х	1	Х	1	0	Х	Х	1	X 1	×	. 1	0	Х	X 1	Х	. 1	X	1	0	Х	Х	1	X 1	0	0	0	0	U	U	0	0 0	0	0	0	U	U	0 0	-			010	0	0	×	х	х	х	0	0	1		C	10	×
1	0	0	Х	1	Х	1	0	Х	0	Х	Х	1	Х	1	0	Х))	(X	1	Х	1	0 >	(0	Х	×	1	Х	1	0	Х	0 X	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 0	-		Ì	110	0	0	×	х	х	х	0	0	1		1	10	×
1	0	1	Х	1	Х	1	0	Х	Х	1	Х	1	Х	1	0	X	X 1	X	1	Х	1	0 >	(X	1	Х	1	Х	1	0	Х	X 1	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 0				111	0	0	х	х	х	х	0	0			1	11	×
1	1	0	Х	1	Х	1	Х	1	0	Х	Х	1	Х	1	Х	1) >	(X	1	Х	1	X 1	0	Х	Х	1	Х	1	Х	1	0 X	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 0	4		Ì	101	0	0	×	х	х	х	0	0	1		1	01	×
1	1	1	Х	1	Х	1	Х	1	Х	1	Х	1	Х	1	Х	1	X 1	X	1	Х	1	X 1	Х	1	Х	1	Х	1	Х	1	X 1	0	0	0	0	0	0	0	0 0	0	0	0	0	0	0 0				100	0	0	×	х	х	х	0	0	1		1	00	×
																																															J2 = ~(2	20+).~	-Rst.Ç	Q0.~Q	.3.~Q2	2.Q1						K2 =	~ (20-	+).~F	ist	.QC
																																	J3	3 = ~	(20+)	.~Rst	.Q0.	-Q3.Q	2.Q1								J1			Q3/Q2	2/Q1							K1				(
																																					+ Q(Q1								ľ	000	001	011	010	110	111	101	100					Ī
																																	J2 K2	2 = ~	(20+)	.~Rst .~Rst	.00.	-Q3.~ -Q3.Q	Q2.Q1 2.Q1	+ Rst	: + (:	20+)	+ Q3				20+/Rst	t/Q0	000	0	х	×	0	0	х	х	0	20	+/Rst/	/Q0	000	,
					\perp								•		1				•													_	J1	L = ~	Rst.(0.~03	3. (~ (2	20+)	+ (20	+).~C	(2)							Ī	001	1	×	×	1	0	х	x	0			Ī	001	,
		1			H										-				+												+	٦l	K1	L = ((20+)	+ Rs	st + (20 +	Q3).(~ (20+	+) + :	Rst +	Q0 +	Q3 -	+ Q2)			Ì	011	0	х	×	0	0	х	х	0			Ī	011	
) = ~		.~Rst	.~Q0	. (~Q3	+ Q3	.~Q2.	~Q1)	+ (2)	0+).~	Rst.	~Q3.~Q2	2			010	0	х	×	0	0	х	х	0				01	0 3
																																Ш	r.U	, – 1															110	0	×	×	0	0	×	×	0					10 3



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Clock_Lib/Counter_15bit 1 1Hz F:\Workspace\05_Projekty\Projects_Simulink\Clock\Clock_Lib.slx page 14/14 printed 22-Apr-2024 17:39