Dedicated to

Work is dedicated to my Head of the Department, Project Co-ordinator as well as Project Faculty, for their encouragement and support of project

Rajiv Gandhi University of Knowledge and Technologies

Basar,Nirmal,Telangana,INDIA.

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE

This is to certify that the **Major Project report** entitled "***Current-based Data-retention-Characterization of GainCell embedded DRAMs across Design and Variations Space"*** being submitted to the Rajiv Gandhi University of Knowledge Technologies, Basar by **Mr. SAMA JAYAPRAKASH (ID: B151236** is work done by him and submitted during 2020 –2021 academic year, in partial fulfillment of the requirements for the award of the degree of BACHELOR OF TECHNOLOGY in ELECTRONICS AND COMMUNICATION ENGINEERING.

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CERTIFICATE OF EXAMINATION

This is to certify that I have examined the thesis entitled ***" Current-based Data-retention-Characterization of GainCell embedded DRAMs across Design and Variations Space***" submitted by **Mr. SAMA JAYAPRAKASH (ID: B151236)** and hereby accord my approval of it as a study carried out and presented in a manner required for its acceptance in partial fulfillment for the award of the graduate degree for which it has been submitted. This approval does not necessarily endorse or accept every statement made, opinion expressed or conclusion drawn as recorded in the thesis. It only signifies the acceptance of the thesis for the purpose for which it has been submitted.

External Examiner
Date: 05th April, 2021
Place: Basar

DECLARATION

I hereby declare that the work embodied in this thesis has been carried out by me under the supervision of Mr. Chintam Shravan in the department of Electronics and Communication Engineering, Rajiv Gandhi University of Knowledge Technologies, Basar and has not been submitted to any other University. Information derived from the published and unpublished work of others has been acknowledged and a list of references is given.

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ABSTRACT

Due to the technological advancements and research in memory cells, scientists are looking for low power, on chip memories with higher storage capacity and smaller size that can be fabricated on a single chip. The demand for this memory cells have been increasing day by day due to the advent of huge data generated by the digital world today. Everything can be seemed as a data. This data has to be stored, processed for getting relative information for the specific applications. Big data applications use memory a lot for storing data in the data centres where a huge hardware is required for storing them and their maintenace is another big challenge for tech companies. In this paper, GainCell embedded DRAM's data retention time is calculated. The present topic of memory cell is GCeDRAM because it provides high density, low leakage currents which is the requirement of today's world. But there is a limitation to this cell that it needs to be refreshed every time period called refresh period otherwise it may lost the data. The time upto which the DRAM cell can hold the data after a write operation is done until it is read is called as the Data retention time. The calculation of DRT is important because it can provide the details of when to refresh the cell inorder to avoid the data loss. The existing technologies are not efficient for calculating it accurately within the feasible times. Without using highly costliest software licenses, this current based data retention characterization methodology provides way for calculating DRT with 4% error rate within feasible run time.

ACKNOWLEDGMENTS

First we Would like to thank management of RGUKT-Basar for giving me the opportunity to do Major Project.

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and friends who helped me in successful completion of this internship.

CONTENTS

Abbreviations

Abbreviation	Description
eDRAM	Embedded dynamic random access memory
GC's	Gain Cells
LPV	Low Power Variations
GPV	Global Power Variations
MC	Monte-Carlo

Motivation and Objectives:

- The advent of the new technologies requires low power, small sized and high denser memory cells on the chips.
- The existing methodologies of data retention measurement have limitations of run time and accuracy and hence we require another method feasible for the above limitations.

Overview:

In the fulfilment with the objectives this report is divided into five parts, where each part requires knowledge from the preceding parts.

Part I :**DRAM and SRAM.** Presents a summary naive memory cells, working ,advantages and limitations.
Part II :GainCell eDRAM. Presents about the gain cell embedded DRAM and its working.
Part III : DRT Analysis Analysing importance of DRT measurement and discussion of the existing methodologies and their limitations.
Part IV :IDRT Methodology. Presents a discussion of the current based characterization for DRT measurement.
Part V :Gain Cell Macro Characterization. Presents a discussion of the extraction of key GCeDRAM characteristics and the effect of DRT on memory characteristics.

PART - I

Current based Data Retention Characterization methodology

1. **Introduction:** The use of data-intensive applications which used more power and silicon area are now dominated by embedded memories. The first memory cell we discuss here is SRAM.

1.1 SRAM:

SRAM is usually builtin CMOS Technology with six transistors. Two cross-coupled inverters are used to store the information like in a flip-flop. For the access control two further transistors are needed. If the Write Line is enabled then data can be read and set with the Bit-Lines.

States of an SRAM-Cell:

- **Standby:** Write Line is disabled, no reading and writing is possible

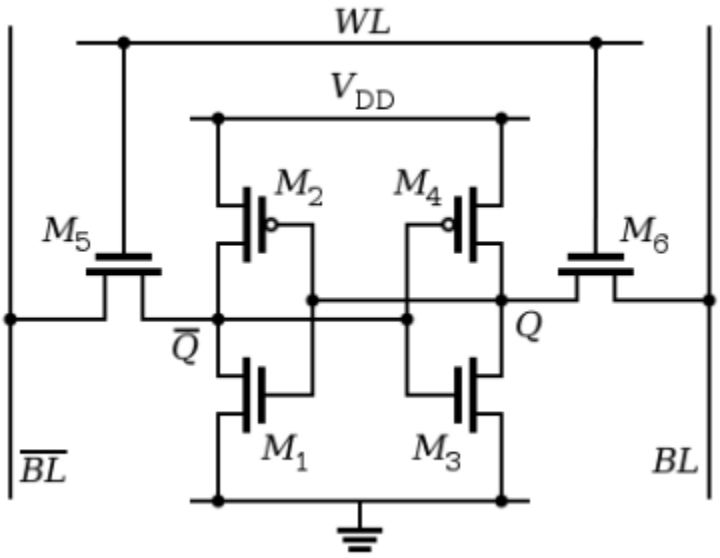
- **Reading:** Reading starts with preloading the Bit lines to 1. Now the Write line gets activated. If Q is 1 then BL gets pulled to one and *BL*bar towards zero. A sense amplifier senses which line has the higher voltage. If capacitor c2 is discharging, bitbar line will have a decreasing voltage and if the bit and bit bar lines voltages have given to the sense amplifier, it outputs 1 and vice versa.

- **Writing:** (Consider Q=0 and Qbar=1). Setting the Bit line to 1 (BL = 1) needs to pull down the bit bar line to ground. As it is pulled to ground, the transistor M1 will be off if the voltage of bit line bar becomes less than threshold voltage and M2 will be on which makes it to have 1 and vice versa.

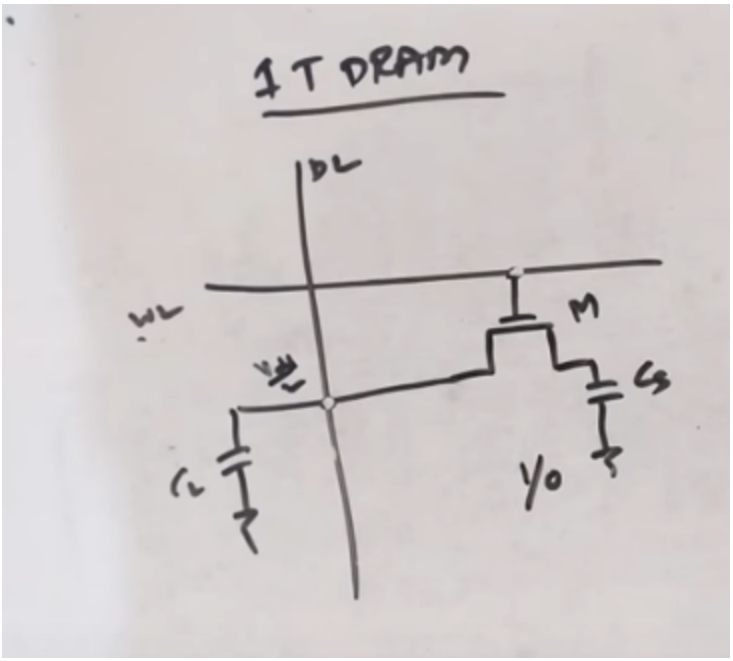
Advantages: Quick, easy to control, integrated in the chip -> fast because no bus is needed like in DRAM

Disadvantages: Many transistors are needed -> expensive, higher power consumption than DRAM.

In read operation, if the stored value is 0, the c1 capacitor discharges and if voltage is greater than threshold voltage of M3 then M3 is ON outputting the Qbar=0 and it is contradicting state because Q=0 already.



1.2 DRAM :



1) The level of charge on the memory cell capacitor determines whether that particular bit is a logical "1" or "0" - the presence of charge in the capacitor indicates a logic "1" and the absence of charge indicates a logical "0".
2) The basic dynamic RAM memory cell has the format that is shown below. It is very simple and as a result it can be densely packed on a silicon chip and this makes it very cheap.

3) Two lines are connected to each dynamic RAM cell - the Word Line (W/L) and the Bit Line (B/L) connect as shown so that the required cell within a matrix can have data read or written to it.

READ operation: The word line is asserted and it becomes the transistor to become ON and whatever the data present in the capacitor gets shared with the bit line. Lets say if capacitor is stored with logic 1, then the effective voltage becomes greater than than vdd and the sense amplifier outputs as 1. On the other hand, if the capacitor stores a logic 0 value, then capacitor voltage looses and if it sensed by sense amplifier , it outputs as a 0.

Write Operation : In write operation, the data/bit lines acts as inputs. The word line is asserted and transistor becomes ON and whatever data is present on the data line it is shared to capacitor.

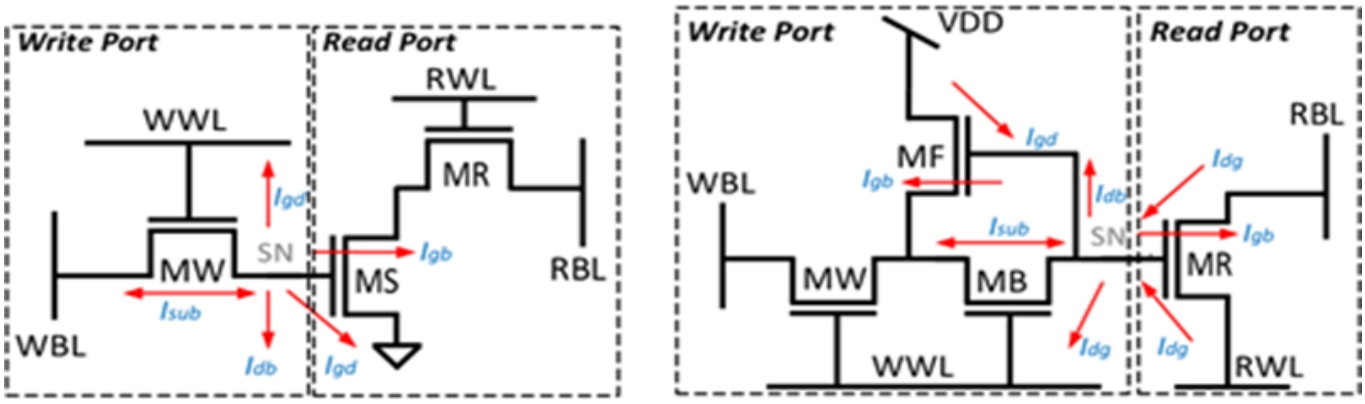
- ❏ This DRAM is not preferable because of its destructive read operation. It means for a read operation, the stored value gets lost after reading.
- ❏ We cannot fabricate capacitor on chip so it is not preferred in IC designs.
- ❏ 1 T-1C eDRAM requires dedicated process steps to fabricate the cell capacitor resulting in additional complexity and cost, and it suffers from a destructive read operation, which increases power consumption.

- ❏ GC-eDRAM offers higher density due to its lower transistor count, low-leakage, and inherent two-ported operation. Compared to 1 T-1C eDRAM, it is fully logic-compatible, thus it does not require additional process steps, and its read operation is nondestructive.

PART-II

2.0 GCeDRAM:

- ❏ GC-eDRAM offers higher density due to its lower transistor count, low-leakage, and inherent two-ported operation.
- ❏ Read operation is non-destructive. It has three main components.
- ❏ Storage Node(SN), Read port and Write port.
- ❏ In this paper, 3-transistor (3T) and 4T NMOS-only GCs, depicted.



(a) 3T all-NMOS gain cell. (b) 4T all-NMOS gain cell.

2.1 Working of GCeDRAM:

WRITE OPERATION:

When WWL line is activated, whatever the data present on WBL will get transferred to the SN.
When GC is not accessed, the data is dynamically stored on the parasitic capacitance of SN.

READ OPERATION:

RBL is precharged to Vdd.

Once the read word line (RWL) is driven to GND (4T) or V_{DD} (3T), allowing the read transistors (MR and MS) to conditionally discharge the RBL depending on value (charge) stored on the SN.

- ❏ As GC's store data dynamically, it needs to be refreshed frequently. The refresh period is determined by DRT.

2.2 Introduction to DRT :

- ❏ The DRT depends on various parameters, such as the stored data, the temperature and operating voltage, the amount of global process variations (GPVs) and local process variations (LPVs), and the operating frequency.
- ❏ The memory content is maintained only when the refresh period is set to a smaller value than the lowest DRT of the memory array and according to worst-case operating conditions, which maximize the leakage through the SN.
- ❏ With technology and voltage scaling, the increased leakage currents and process variations have been shown to reduce the DRT of GC-eDRAMs.
- ❏ The measurement of accurate DRT is needed because of the increased technology, the leakage currents also increasing which needs lower refresh rates to be measured.
- ❏ The conventional method of measuring the DRT is effective DRT measurement(EDRT).

2.3 EDRT :

- ❏ EDRT is a technique to measure DRT. In this method, a write operation is performed to GC's and a read operation is performed after an idle phase.

- ❏ This method is repeated for long idle phases. It is a trial and error method.

- ❏ The longest idle time that still ensures the correct data to be read is known as the DRT of the cell.

- This method although gives accurate DRT, it is not preferable for large memory cell arrays because calculation time for DRT becomes high.

- To reduce the DRT evaluation run-time and to avoid the need for high license costs, another method VDRT is introduced.

- This method produces accurate results but it cannot be used for measuring DRT of the large memory arrays as it takes a lot of time for trial and error experiments.
- It becomes impractical to evaluate the DRT of large memory arrays across LPVs, as many trial-and error transient simulations need to be repeated for each Monte Carlo (MC) run.
- In order to reduce the DRT evaluation run-time and to avoid the need for high license costs, a voltage-based DRT (VDRT) characterization methodology has been introduced.

2.4 VDRT:

- According to the VDRT methodology, the DRT is determined as the time interval after a write operation at which the voltage difference between stored '1' and '0' crosses a critical threshold at which its polarity can no longer be distinguished reliably using a read operation.
- Simulation time of the VDRT approach is shorter than the time required by the EDRT methodology as it does not require trial-and error read operations. Hence, it can be easily used for LPV analyses when executing a high number of MC runs.
- The consideration of the SN voltage only does not account for the DRT. Thus, the accuracy of the VDRT methodology is limited.

- ❑ To avoid the limitations of the above method and to determine the DRT, we present a new current-based DRT (IDRT) method.
- ❑ This method relies on current monitoring through the read port, which takes into account the LPV affecting both the SN voltage deterioration and the RBL driver.
- ❑ The IDRT method is compatible with MC runs as it does not compute time-consuming trial-and-error transient simulations of the read operation.
- ❑ It gives an accurate measure of the DRT across LPVs without the need for a large number of costly EDA software licenses.
- ❑ The IDRT method provides less than 3.7% DRT deviation from the reference EDRT approach, which is over 26 times lower than the average error of the VDRT method.

Contributions: The major contributions of this paper are summarized as follows:

1) The paper presents a Current-based DRT (IDRT) method, which provides an accurate DRT evaluation tool without relying on time-consuming trial-and-error transient simulations.

2) The IDRT method is compared with the EDRT and VDRT methods for different GC structures and across different process technologies (i.e., 28 nm FD-SOI and 28nm Bulk CMOS), demonstrating an average DRT error below 3.7 %.

3) The IDRT method is used to explore the design and variation space of 3T and 4T GCs in 28nm technology.

4)The DRT extracted from the IDRT methodology is used to evaluate key GC-eDRAM characteristics, such as retention power and memory availability for different memory.

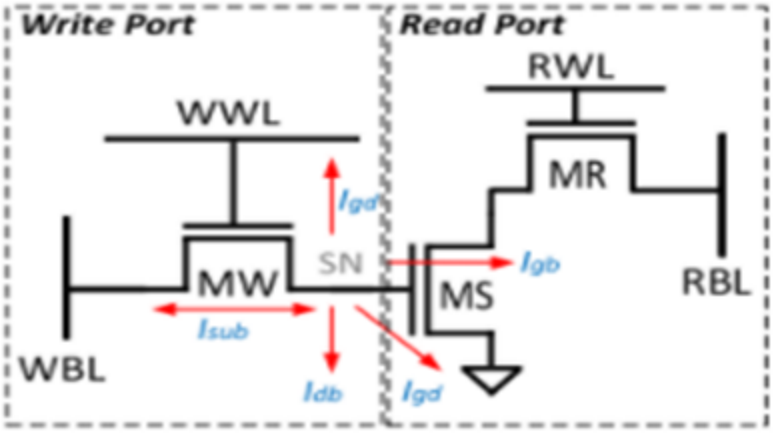
PART-III

3.0 DRT analysis :

- ❏ The DRT is primarily affected by the leakage currents, which deteriorate the SN voltage, and the read port variation, which affects the RBL access latency during read operations.

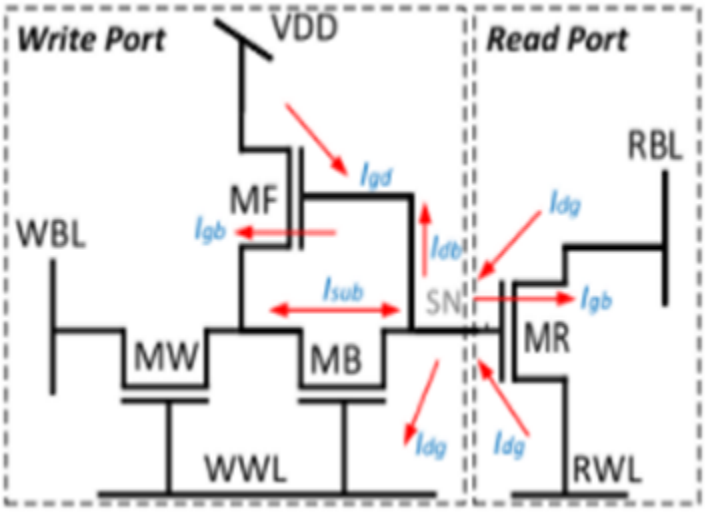
3.1 Storage Node Leakage :

- ❏ When the WBL holds an opposite value to the SN, a sub-threshold leakage (I_{sub}) path is created between the drain and source of MW.
- ❏ In addition, when the cell stores a '1', the SN deteriorates even further through gate leakage (I_{gate}) to WWL.
- ❏ There is bulk leakage (I_{bulk}) to the substrate of MW, resulting in a faster deterioration of '1' compared to '0'.



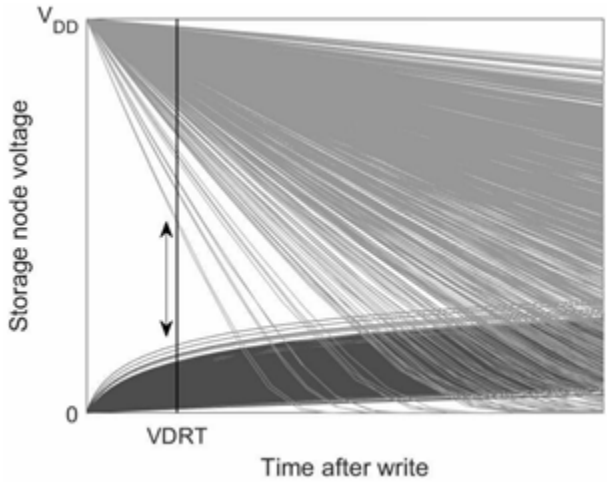
(a) 3T all-NMOS gain cell.

- The exponential dependence of I_{sub} on temperature and process variations, it remains the most significant leakage across corners which deteriorates the SN.
- To reduce the effect of I_{sub} on the SN degradation, a 4T GC with internal feedback was proposed.



- It introduces two additional transistors which form an internal feedback that helps to retain the

weaker (‘1’) voltage level by reducing the leakage from the WBL through MF.

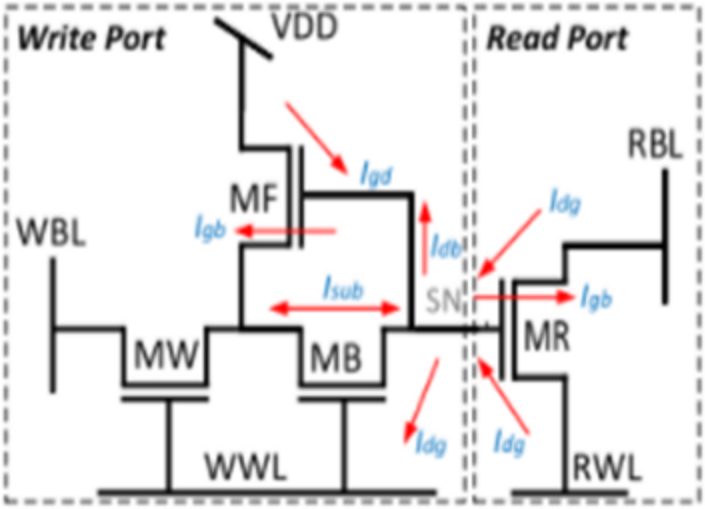


❑ Figure illustrating the SN voltage after write, as extracted from simulations of the 3T GC under worst-case biasing conditions.

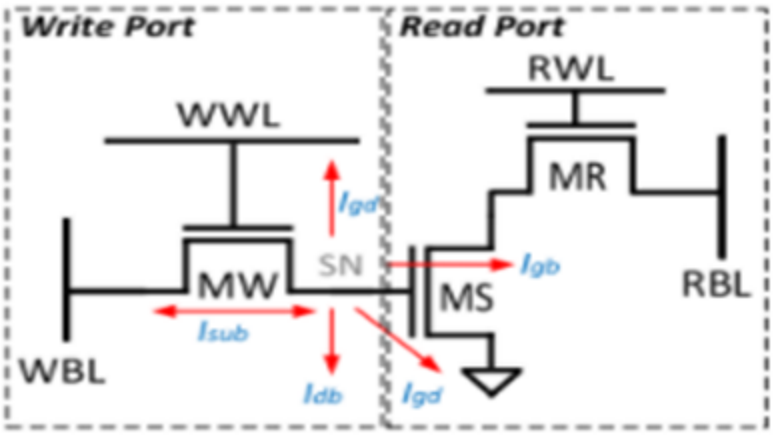
3.2 Read Port Variation :

❑ The read port has a strong impact on the DRT through the read access delay, which is determined by the on-current of the read transistors.

❑ A 1T read port, depicted in Figure below, contains a single transistor which is controlled by the SN.

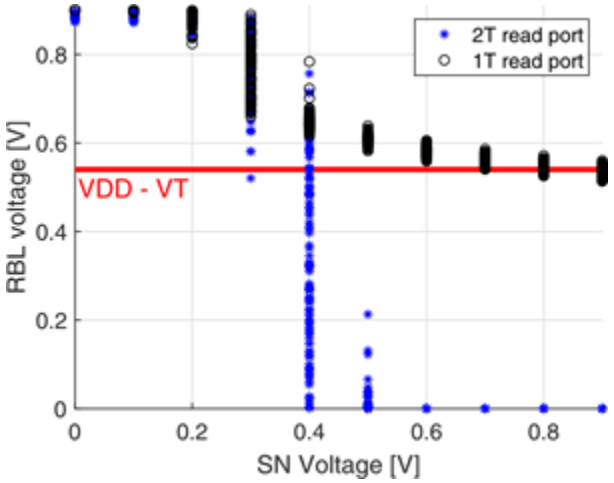


- It conditionally enables a current path between the RBL and the RWL to either discharge RBL when the cell holds a '1', or keep it charged at V_{DD} when it holds a '0'.
- The RBL evaluation delay is often the dominant portion of the total read latency of the GC array due to the large RBL capacitance and degraded SN voltage.
- 1T read port is affected by unselected transistors sharing the same column, which cause the RBL voltage to saturate at a level close to V_{DD}-V_T when other cells in the column store a '1'.
- In order to avoid RBL saturation, a 2T read port is incorporated in the 3T GC, as shown in Figure.



(a) 3T all-NMOS gain cell.

- The RWL is connected to the gate of MR, decoupling MS from the RBL when the cell is not selected.
- Figure below illustrates these phenomena by plotting the RBL voltage distributions as a function of the SN voltage across process variations following a read access from a 1T and 2T read ports.



- The RBL voltage of the 1T read port saturate at a level close to V_{DD}-V_T before completely discharging to GND.

- ❏ The RBL voltage of the 2T read port discharges close to GND when the SN voltage is high enough.

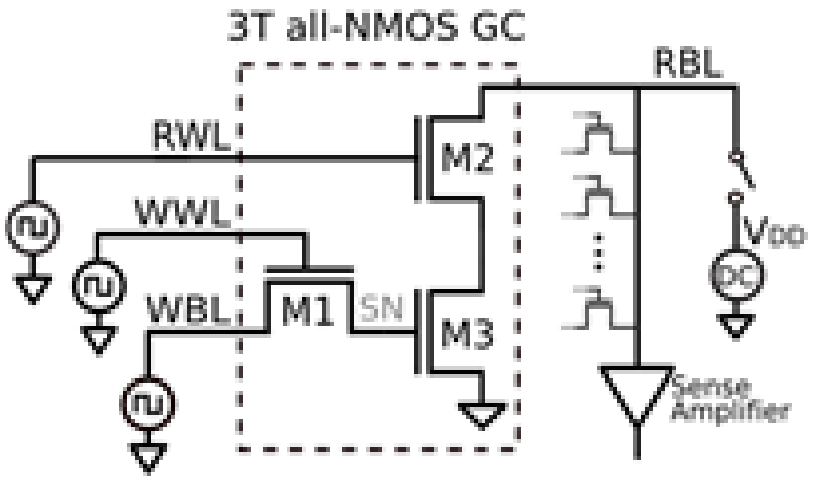
PART-IV

4.0 IDRT methodology:

- ❏ The DRT is determined according to the maximum time interval after a write operation until the moment when the current through the active read port crosses a critical threshold.
- ❏ It contains three phases. It is illustrated for 3T NMOS GC.

4.1 EDRT Measurement : The load of the GCs sharing the same column is added to the shared RBL and a sense amplifier is used to sense the RBL voltage.

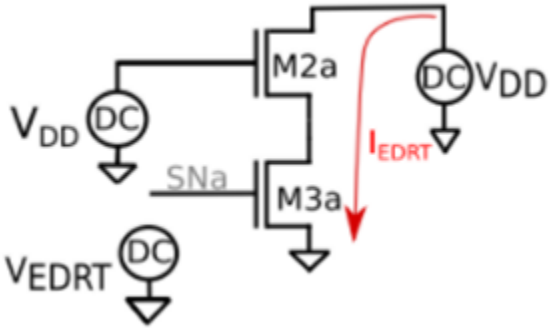
- ❏ During the idle phase, the WBL is forced to the opposite voltage of the written value in order to apply worst-case biasing conditions.
- ❏ Then, a trial read operation is performed following a determined idle phase and the output is compared with the written value.
- ❏ It is repeated for longer idle phases until the read operation is incorrect and the corresponding voltage of SN is noted.



(a) Effective DRT (EDRT) measurement.

4.2 Reference Current Acquisition : In this phase, we find critical current through the read port (I_{EDRT}) that still ensures a successful read operation.

- The value of I_{EDRT} is obtained using the test-bench shown in Figure.

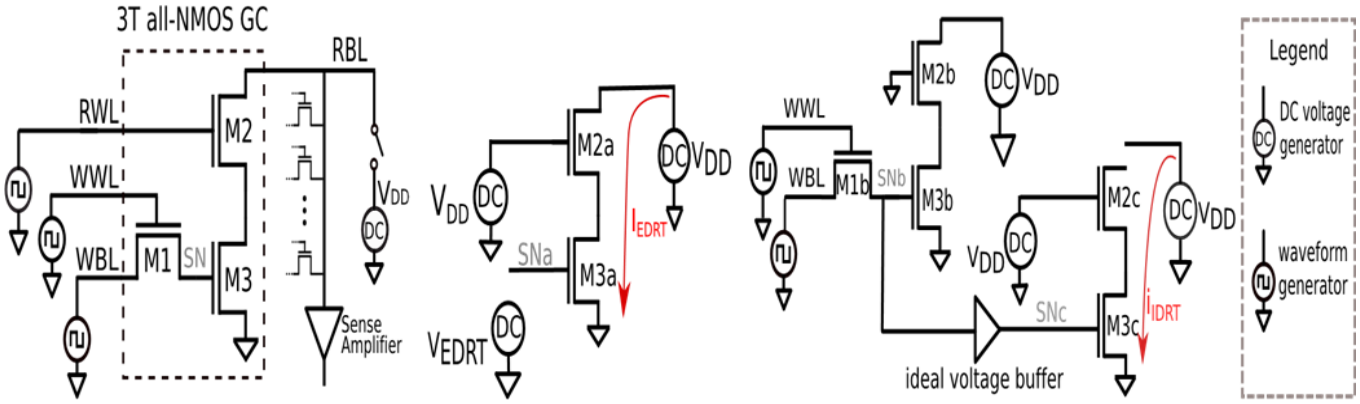


- The previously evaluated V_{EDRT} is applied to the storage node (SNa), followed by the assertion of the RWL and the pre-charge of the RBL (V_{DD} for an NMOS-only read port).
- The I_{EDRT} is evaluated as the DC current which dis-charges the RBL for the considered operating point.
- I_{EDRT} represents the minimum/maximum read-port current that is necessary for a correct read operation.

4.3 Evaluation Phase :

The evaluation phase is used to evaluate the DRT distribution under LPVs.

- This phase consists of a write operation to the GC (M1b–M3b), followed by an idle phase, during which the stored SNb voltage deteriorates over time as a result of the various leakage currents.
- The data deterioration is reproduced on the read port replica (M2c, M3c) using an ideal voltage buffer that applies the voltage of SNb to SNc.
- Using this setup, the read port replica is constantly enabled and its drive current (i_{IDRT}) is continuously monitored.
- The time interval following the write operation at which the i_{IDRT} crosses the critical I_{EDRT} threshold is taken as DRT.



(a) Effective DRT (EDRT) measurement. (b) Reference current acquisition. (c) Evaluation phase.

4.4 COMPARISON OF DRT CHARACTERIZATION METHODOLOGIES:

4.4.1 Accuracy of the methodology:

❑ A quantitative analysis of the accuracy achieved by the IDRT methodology is provided and compared to the other methodologies as simulated on a 3T and 4T all-NMOS GCs at 28nm FD-SOI and 28nm Bulk process technologies.

Technology	Bitcell	Temperature	EDRT	VDRT	VDRT Error	**IDRT**	**IDRT Error**
LP 28 nm FD-SOI	3T all-NMOS	0 °C	2.49 µs	3.15 µs	26.62 %	**2.49 µs**	**0.04 %**
LP 28 nm FD-SOI	3T all-NMOS	27 °C	673.60 ns	771.6 ns	14.55 %	**674.60 ns**	**0.15 %**
LP 28 nm FD-SOI	3T all-NMOS	85 °C	73.26 ns	70.2 ns	4.18 %	**75.23 ns**	**2.70 %**
LP 28 nm FD-SOI	4T all-NMOS	0 °C	788 µs	164 µs	79.19 %	**786.7 µs**	**0.17 %**
LP 28 nm FD-SOI	4T all-NMOS	27 °C	457 µs	112.2 µs	75.45 %	**459.1 µs**	**0.45 %**
LP 28 nm FD-SOI	4T all-NMOS	85 °C	81.6 µs	40.3 µs	50.62 %	**80.07 µs**	**1.88 %**
HP 28 nm Bulk	3T all-NMOS	0 °C	411.9 ns	451.9 ns	9.71 %	**416.0 ns**	**0.99 %**
HP 28 nm Bulk	3T all-NMOS	27 °C	128.4 ns	130.8 ns	1.91 %	**129.3 ns**	**0.66 %**
HP 28 nm Bulk	3T all-NMOS	85 °C	19.55 ns	18.13 ns	7.27 %	**20.27 ns**	**3.69 %**
HP 28 nm Bulk	4T all-NMOS	0 °C	44.42 µs	20.62 µs	53.59 %	**44.0 µs**	**0.94 %**
HP 28 nm Bulk	4T all-NMOS	27 °C	31.23 µs	10.53 µs	66.27 %	**30.78 µs**	**1.44 %**
HP 28 nm Bulk	4T all-NMOS	85 °C	18.34 µs	2.98 µs	83.76 %	**17.9 µs**	**2.39 %**

4.4.2 Comparison of Practical Aspects in DRT Characterization Methodologies :

- A qualitative comparison based on four relevant practical aspects is provided in Table II for the EDRT, VDRT, and IDRT methodologies.
- The considered metrics are the accuracy, the complexity of the measurement, the nominal measurement time (i.e., the required time to obtain the DRT under typical operating conditions), the MC measurement time, and the number of EDA software licences required to execute a large number of MC runs for LPV analysis.

	EDRT	VDRT	IDRT
Accuracy	Highest	Low	High
Complexity	Low	Lowest	Medium
Nominal Simulation Time	High	Low	Highest
MC Simulation Time	Highest	Low	Low
License Number for MC Runs	Highest	Low	Low

- Table below depicts the achieved run-times of the three DRT characterization methodologies for a nominal simulation and a varying number of Monte Carlo runs.

	EDRT	VDRT	IDRT
Nominal Reference Simulation	44 sec	2 sec	46 sec
1k Monte-Carlo Runs	1.25 hrs	125 sec	136 sec
10k Monte-Carlo Runs	~13 hrs	1588 sec	1647 sec
100k Monte-Carlo Runs	~5 days	~4.2 hrs	~4.4 hrs

4.5 DRT MEASUREMENT OF A 3T GC AND A 4T GC IN 28 nm FD-SOI :

- ❏ The DRTs of a 3T all-NMOS and a 4 T all-NMOS GCs designed in 28nm FD-SOI process technology are measured for different design choices as well as for global process and temperature variations using the EDRT methodology, while the impact of LPVs is evaluated with the IDRT approach.
- ❏ The following design and corner parameters are considered as a baseline:

  1)0.9V supply voltage

  2)1.3V boosting voltage to drive the WWL

  3) 0.7V reference voltage for the 4T GC-eDRAM sense amplifier

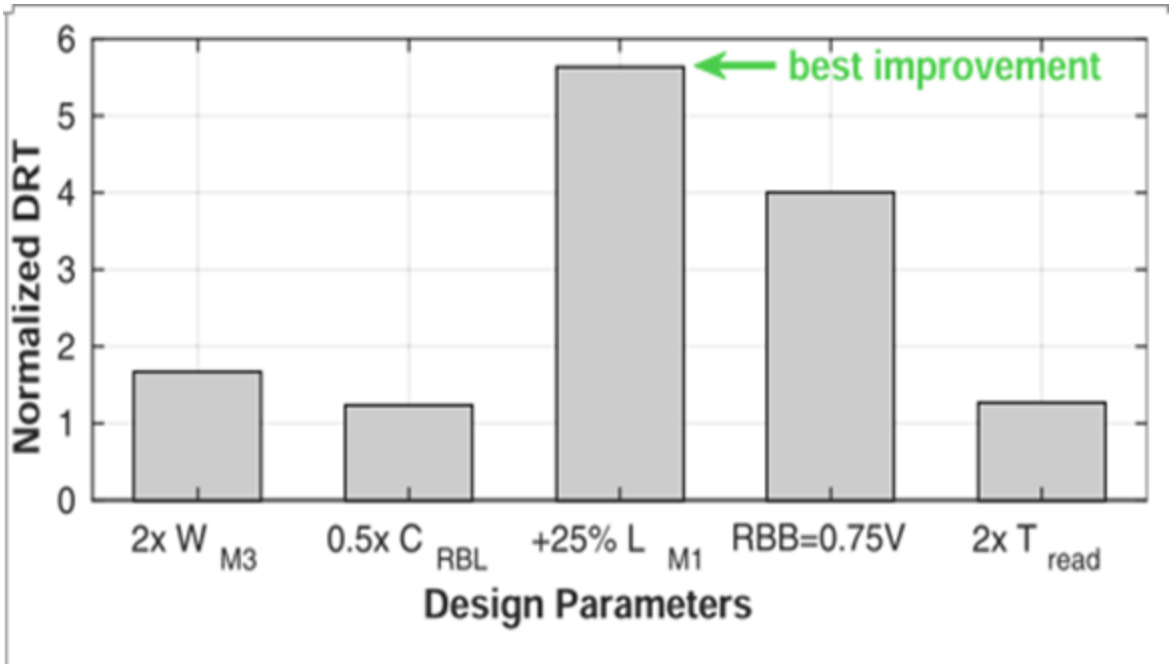
  4)minimum-sized transistors

  5)1ns period for single-cycle write and read operations

  6)Temperature at 27◦C, and typical (TT) process corner.
- ❏ The analyzed 3T and 4T GCs have nominal DRTs of **673ns** and **457μs.**

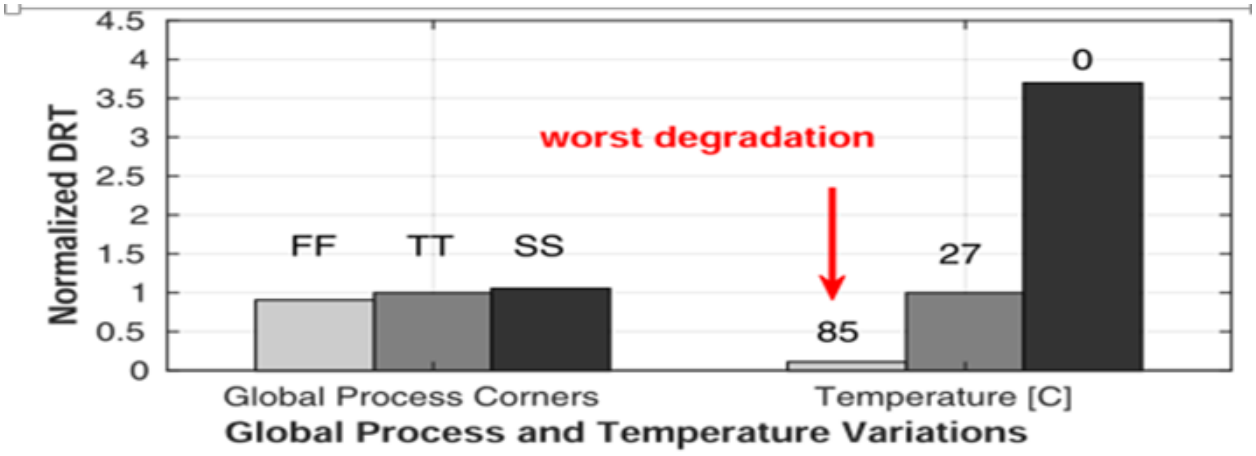
4.5.1. Exploration of the Design Space :

- In addition to the choice of the GC topology, several design choices can improve the DRT of a given GC and the impact of some of the most effective ones are evaluated in this subsection for the baseline 3T all-NMOS GC.

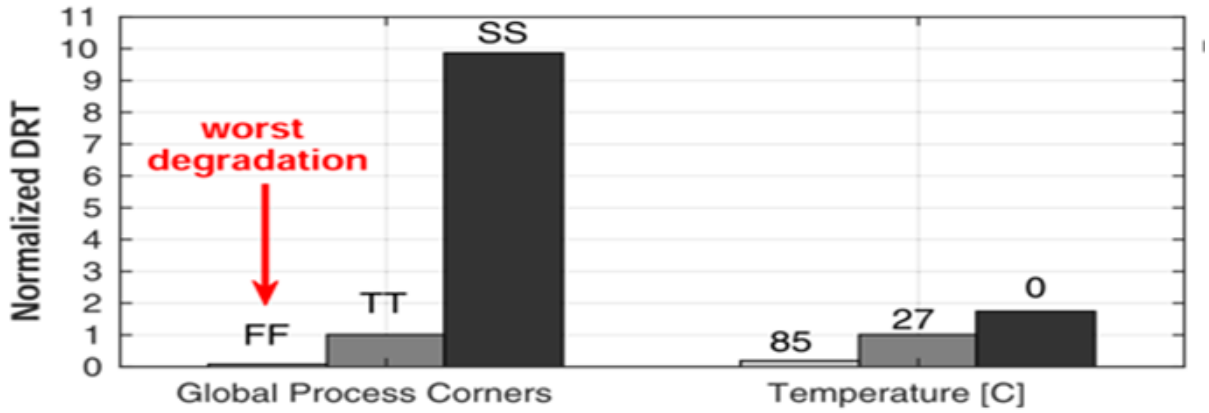


4.5.2 Global Process Variations:

- Both manufacturing and environmental variations can degrade the DRT.
- The impact of global process and temperature corners on the DRT is evaluated with the use of the EDRT method.
- In particular, the slow (SS), typical (TT), and fast (FF) process corners have been considered together with 0◦C, 27◦C, and 85◦C as temperature points.



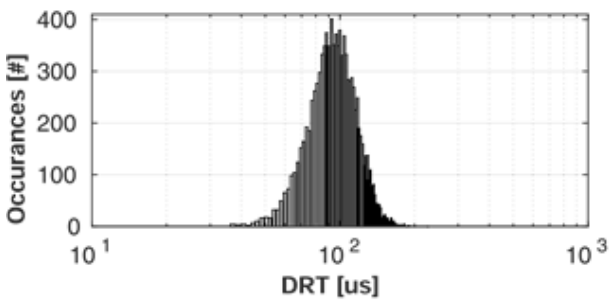
(a) 3T GC.



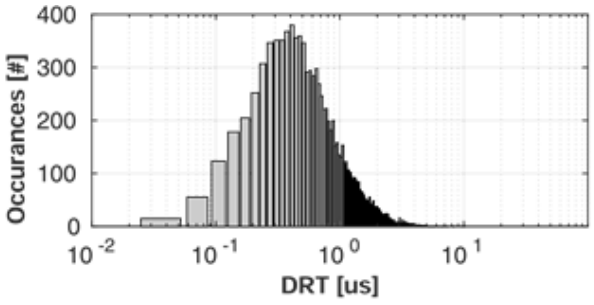
4.5.3 Local Process Variations :

- LPVs also affect the sub-threshold conduction and read current strength, and therefore, they significantly impact the DRT of GCs.
- The IDRT measurement is performed for the 3T and 4T GCs across LPVs with 10k MC runs including device mismatch around a typical (TT) corner at room temperature.
- The results of the LPV analysis are summarized in Figure below , where both a '0' and a '1' have been considered for the stored data.

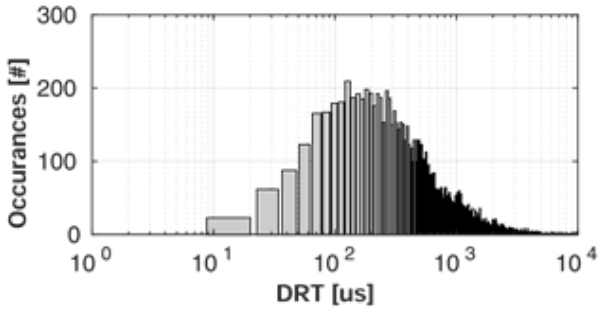
❑ the nominal DRT measurement. The average DRT was found to be 680ns, which deviates by 1%.



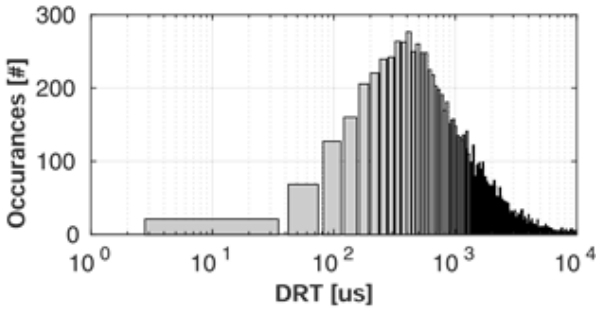
(a) 3T GC - Stored '0'.



(b) 3T GC - Stored '1'.



(c) 4T GC - Stored '0'.



(d) 4T GC - Stored '1'.

PART-V

5.0 GAIN-CELL MEMORY MACRO CHARACTERIZATION USING THE IDRT METHODOLOGY :

❑ The DRT has a significant impact on almost all GC-eDRAM characteristics, such as the refresh period, retention power, and memory availability.

5.1.DRT Affect on Memory Characteristics:

1) Retention Power: An important aspect of the need for a periodic refresh is the additional power component associated with the refresh operation.

- GC-eDRAMs consume another power component due to refresh. In order to provide a fair comparison to SRAM, the static power component of GC-eDRAM is redefined as retention power, which includes both the leakage and refresh power components, as follows:

$$\mathbf{P_{ret} = P_{leak} + P_{ref} = P_{leak} + (E_{write} + E_{read})/T_{ref}}$$

where P_{ret} is the retention power, P_{leak} is the leakage power of the GC array, P_{ref} is the average refresh power, E_{write} and E_{read} are the total write and read energies required to refresh the entire GC array, and T_{ref} is the refresh period.

2) Memory Availability: An additional consequence of the refresh requirement is the limited memory availability to external accesses, since whenever the memory is occupied with refresh it is unavailable for conventional write and read operations. The memory availability (α) is directly dependent on the refresh period set by the DRT and it is defined as follows:

$$\mathbf{\alpha(\%) = (1 - (N_{rows} \times T_{per})/T_{ref})) \times 100}$$

where N_{rows} is the number of rows in the GC array, and T_{per} is the clock period.

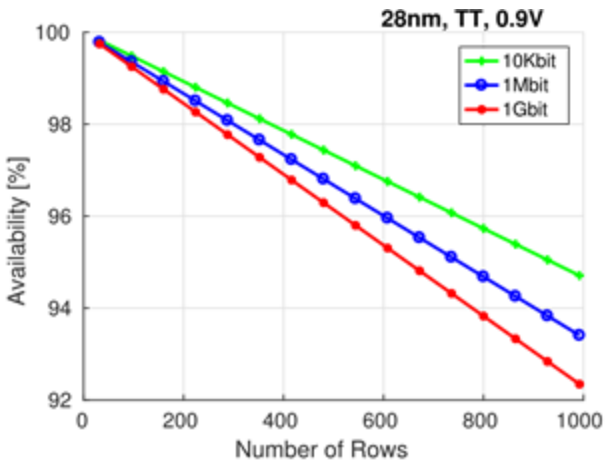


Fig. 11. Memory availability as a function of the number of GC array rows

5.2.Extraction of Key GC-eDRAM Characteristics :

- ❏ Figure below depicts the expected memory yield for 10kbit, 1Mbit, and 1Gbit 4T based GC-eDRAMs.
- ❏ The memory yield decreases as the memory size increases due to a higher probability for a DRT failure under a given refresh period.

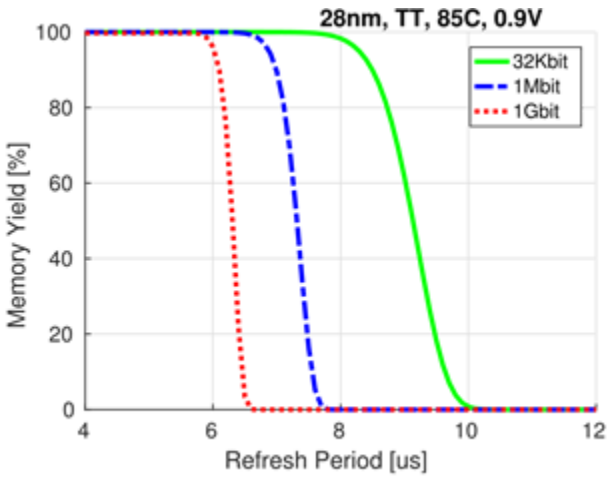


Fig. 9. Memory yield of 10 kbit, 1 Mbit, and 1 Gbit GC-eDRAMs based on

- ❏ Below figure depicts the refresh period distributions obtained for 10k TT chips containing 10kbit, 1Mbit, and 1 Gbit GC-eDRAMs under a 99% yield criterion.

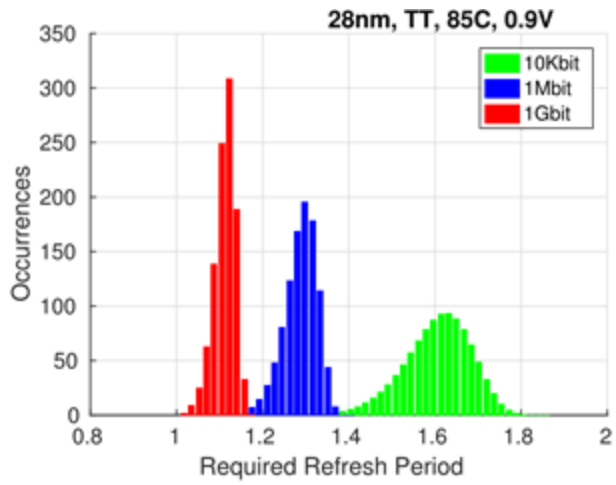


Fig. 10. Refresh period distributions for 10 kbit, 1 Mbit, and 1 Gbit

❑ Figure below illustrates the average memory availability evaluated for 10kbit, 1Mbit, and 1Gbit GC-eDRAMs with a varying ratio between rows and columns, assuming that all GC arrays are refreshed in parallel.

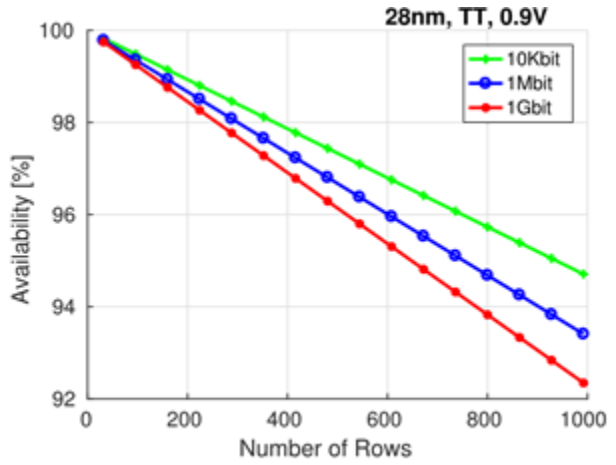


Fig. 11. Memory availability as a function of the number of GC array rows

6 FUTURE SCOPE:

There is a lot of scope in this research domain of memory cells as the technology is driving the world towards digitalization and there is much more data that is going to be generated in the future.

7 CONCLUSIONS:

- ❏ This paper presented a current-based data-retention time (IDRT) characterization methodology.
- ❏ The IDRT methodology shows an accuracy deviation of less than 3.7%.
- ❏ Together with the EDRT approach, the proposed methodology has been used to evaluate the DRT of GCs designed in 28nm FD-SOI and 28nm Bulk CMOS process technologies across a design and variations space.
- ❏ The IDRT methodology was used to extract the high-sigma DRT and evaluate key GC-eDRAM characteristics, including retention power, memory availability, and maximum frequency, for different memory sizes

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