A New Capacitorless 1T DRAM Cell: Surrounding Gate MOSFET With Vertical Channel (SGVC Cell)

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***Abstract*—We propose a surrounding gate MOSFET with vertical channel (SGVC cell) as a 1T DRAM cell. To confirm the memory operation of the SGVC cell, we simulated its memory effect and fabricated the highly scalable SGVC cell. According to simulation and measurement results, the SGVC cell can operate as a 1T DRAM having a sufficiently large sensing margin. Also, due to its vertical channel structure and common source architecture, it can readily be made into a $4F^2$ cell array.**

***Index Terms*—Memory effect, 1T DRAM cell, sensing margin, surrounding gate, vertical channel.**

I. Introduction

TO OVERCOME the scalability issues and process complexity of 1-transistor/1-capacitor DRAM cell, capacitorless 1-transistor (1T) DRAM cells have been recently proposed and investigated [1]. The mainstream 1T DRAM cell is a floating body transistor cell (FBC) which consists of a MOSFET with its body floating electrically. The FBC is realized by a MOSFET formed on partially depleted silicon-on-insulator (PD-SOI). When excess holes exist in the floating body, the cell state can be defined as "1" (decreased $V_{\rm th}$). On the other hand, when excess holes are swept out of the floating body through forward bias on the body–drain junction, the cell state can be defined as "0" (increased $V_{\rm th}$). By measuring the drain current difference between "1" and "0" states of the cell, we can sense whether the holes are accumulated in the floating body. Because the floating body is used as the storage node, the FBC has no complicated storage capacitor. Therefore, the FBC has a simple process and can have a cell area below $4F^2$. [2], [3]

In this work, we propose a surrounding gate MOSFET with vertical channel (SGVC cell) as a 1T DRAM cell. Unlike other 1T DRAM cells which are integrated on SOI substrates, the SGVC cell can be more cost effective since it can be fabricated on bulk Si substrates. Also, there is no need for the source contact and line due to the common source structure, which makes $4F^2$ structure possible and ultimately leads to superior scalability. The memory operation has been investigated by simulation. Also, we have successfully fabricated a highly scalable SGVC cell and the memory effect is measured for the first time.

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TABLE I
SGVC Cell Simulation Parameters

	Program (1/0) (Impact Ionization)	Read
Gate Voltage	**1 V**	**1 V**
Drain Voltage	**1 V (-1 V)**	**0.1 V**
Source Voltage	**0 V**	**0 V**

L(gate length)=0.1 um /t_{OX} (gate oxide)=50 Å

t_{Si} (Pillar Diameter)= 60 nm

$N_{S/D}$ (source/drain region doping)=10^{20} cm^{-3} (graded doping)

N_{body} (body doping) =10^{18} cm^{-3}

$t_{program}$ =10 ns

II. Simulation Results

Fig. 1 schematically shows the operation principle of an SGVC cell [4]. It can be noted that it has a floating body where holes are accumulated for memory effects. To verify memory cell operation, 2-D device simulation was performed. We used ATLAS as a simulator. Excess holes are generated by impact ionization in this simulation. Simulated parameters are listed in Table I. The difference in the body potential of each state and the $I_D - V_G$ characteristics were extracted first, in order to show the accumulation of holes in the body of the SGVC cell. Fig. 2 shows a comparison of the hole potential between "1" state and reference state ($V_{\rm gate} = 0$, $V_{\rm source} = 0$, $V_{\rm drain} = 0$). In the case of state "1," through impact ionization in the high field region near the drain, excess holes are injected into the body and then the body potential increases. Fig. 3 shows $I_d - V_g$ characteristics of the SGVC cell. The drain current of "1" state is larger than that of "0" state. This is due to the increase of the body potential when holes are accumulated into the body through writing operation, hence lowering the threshold voltage, which in turn increases the drain current. Subsequently, the drain current as a function of time was extracted to show