CHAPTER 5

Components, Part 2—Detectors and Other Circuits

In Chapter 4, we discussed dividers and oscillators. In this chapter we discuss detectors and other circuits that support PLLs. Detailed designs of phase detectors, lock detectors, and acquisition aids are studied.

Phase detectors are studied because understanding how phase detectors work is one of the major keys to understanding how PLLs work. Many systems use the lock detector to reset the system. This is a disastrous change to the operation of most systems. In a PLL, a reset can start the loop operating at a very low frequency (or with no output), which will then acquire lock at the normally much higher output operating frequency. Consequently, a small phase shift in the PLL that would marginally affect the system can cause a huge disruption in the operation of the system if a reset occurs. The key to lock detection is to alarm on behavior that shows that the PLL is broken. Quadrature phase detection, time-window edge comparison, tune-voltage window comparator, and cycle-slip detection are the lock-detection methods that are covered.

Open-loop sweep, closed-loop sweep, and discriminator-aided acquisitions are the methods that are covered. The phase/frequency detector uses discriminator-aided acquisition and is the most popular choice. Clock-recovery circuits cannot use phase/frequency detectors. Consequently, these circuits require an acquisition aid. Understanding the design details and trade-offs in these components is critical in designing monolithic PLLs.

A charge pump and operational amplifier provide a method to convert the differential up and down outputs of the phase/frequency detector to a single-ended positive and negative voltage source that charges and discharges capacitors in order to control the VCO in a PLL. These components also are used in synthesizing the loop compensation. For this function, the component that most closely models an ideal integrator is the best choice. Several different charge pump architectures are presented, and trade-offs between each are discussed. Then, operational amplifiers are presented. The evolution of operational amplifier architectures to the one that best fits a PLL is shown. Finally, trade-offs between charge pump and operational amplifier compensation designs are studied.

5.1 Phase Detectors

The phase detector in a PLL compares the reference-oscillator frequency with the VCO frequency and develops an error voltage for the loop to process. Consequently,

phase detector components have a critical impact on the performance of a PLL. Tracking range, acquisition range, loop gain, and transient response depend on the characteristics of the phase detector. The major characteristics of a phase detector include the input phase-difference range, the response to a frequency difference, the sensitivity to input amplitude, and duty cycle.

This section begins by presenting the linear phase detector equations and a figure of merit for comparing phase detectors. Then, a variety of analog and digital devices for phase detection are presented, and the variety of different characteristics are studied. Some have a simple topology, others operate at high frequency, and still others have a very low content of undesirable signals in their output. Mixers, exclusive-OR gates, RS latches, flip-flops, and phase/frequency detectors are presented. They represent the major types that are used to detect phase error in integrated circuit PLLs.

5.1.1 Linear Model

Developing a linear model will help our discussion of phase detectors by giving us a standard for comparing the different types of phase detectors. Equation (5.1) establishes a linear model with an offset for a phase detector:

$$V_d = K_d \theta_e + V_{do} \tag{5.1}$$

where

K_d = phase detector gain (V/rad);

θ_e = phase error of the VCO output relative to the input signal;

V_{do} = offset voltage, or "free-running voltage."

This linear model breaks down for large enough θ_e (phase error). The values of θ_e for which the linear model is valid define the range of the phase detector. Range, offset, and gain characteristics distinguish the differences between the detectors. A large offset with respect to the gain of the detector ruins the effectiveness of the detector. Consequently, a figure-of-merit ratio will help compare the effectiveness of each detector circuit.

5.1.2 Phase Detector Figure of Merit

Is an offset V_{do} = 193 mV too large for a phase detector to be effective? The amount of output voltage per radian, which is the gain of the phase detector K_d, determines the usefulness of the phase detector. Therefore, the ratio of output voltage gain to offset voltage, K_d/V_{do}, indicates the size of the offset. We will call this the figure of merit, M, of the phase detector as shown by (5.2):

$$M = K_d/V_{do} \tag{5.2}$$

For example, a phase detector with a gain of 5 V/rad and an offset of 193 mV produces a figure of merit M = (5 V/rad)/(193 mV) = 26. A phase detector should

reasonably be expected to have $M \geq 15$, and M as high as 500 is possible with careful matching.

Range, offset, and gain characteristics distinguish the differences between the detectors. However, they all share the same characteristics as a multiplier. A multiplier has the characteristics of a phase detector by the trigonometric identity in (5.3):

$$\sin(A)\cos(B) = 0.5\,\sin(A - B) + 0.5\,\sin(A + B) \tag{5.3}$$

We already studied this equation in Section 2.2, but we will review it here and adjust it for our linear model of a phase detector. Applying the trigonometric identity for products of a trigonometric function to the multiplication of two signals (at frequencies RF and LO) produces (5.4):

$$V_1(t)\,V_2(t) = V_{p1}\,V_{p2}\;0.5[\cos(\omega_{rf}t - \omega_{lo}t + \theta_e) + \cos(\omega_{rf}t + \omega_{lo}t + \theta_e)] \tag{5.4}$$

Eliminating the high-frequency product with a lowpass filter yields (5.5):

$$V_1(t)\,V_2(t) = V_{p1}\,V_{p2}\;0.5[\cos(\omega_{rf}t - \omega_{lo}t + \theta_e)] \tag{5.5}$$

$$= V_{pbeat}\cos(\omega_{beat}t + \theta_e) \tag{5.6}$$

where

$\omega_{beat} = \omega_{rf} - \omega_{lo}$ for $\omega_{rf} > \omega_{lo}$;

$V_{pbeat} = V_{p1}\,V_{p2} \times 0.5 \times$ mixer losses;

V_{pbeat} = resulting voltage level after mixing (V).

The derivative of (5.6) calculates the incremental phase slope. For the mixer operating with a 0 frequency difference ($\omega_{beat} = 0$, which is dc) and 90° phase shift, the derivative of (5.6) produces (5.7) and (5.8):

$$K_d(\phi) = \frac{d}{d\phi}[V_{pbeat}\cos(\phi)] \tag{5.7}$$

$$K_d(\theta_e) = V_{pbeat}\sin(\theta_e) \tag{5.8}$$

Equation (5.8) shows the origin of the phase detector gain and that it relates to the multiplication of two signals.

For θ_e equals $\pi/2$ rad (quadrature) in (5.8), K_d equals V_{pbeat} (V/rad). For θ_e equals 0 rad in (5.8), K_d equals 0 V/rad. This shows that maximum phase sensitivity occurs for a 90° phase difference between the input signals, while a minimum phase sensitivity of 0 occurs for a phase difference of 0°. With the linear model established, let's look at the various phase detectors.

5.1.3 Balanced Mixer

First, we will look at a balanced mixer, sometimes called a double-balanced mixer, because it is very close to a four-quadrant analog multiplier. Furthermore, we will begin by looking at diode ring mixers that are used in PCB design because their operation has been well established. Figure 5.1 shows a diode ring mixer. This circuit consists entirely of passive components (baluns and diodes). Baluns and diodes usually compose the major components in a ring mixer for PCB designs. These components allow operation at extremely high frequencies (>18 GHz) and across wide frequency range.

5.1.3.1 Diodes

Only devices that have nonlinear current-voltage relationships or that change as a function of time (are time-variant), or both, cause mixing products. Multiplication of the two input signals yields one of the mixing products. A switch toggling between either a short or an open as a function of time makes a time-variant circuit. Mixers require very fast switching (at the LO frequency). In PCB designs, obtaining low-noise figure and fast switching speed make Schotkey-barrier diodes the usual choice in ring mixers. The nonlinear properties of diodes cause mixing products, so the time-variant and nonlinear properties of diodes help produce mixing products.

Simultaneously applying two or more signals across a nonlinear diode causes mixing to occur. This action produces single- and multiple-tone intermodulation products. Two voltages applied in series across a diode cause the current through it to contain the IF and higher-order intermodulation products of the two voltage inputs. A lowpass filter after the mixer must significantly reject these products to have a good phase detector.

5.1.3.2 Baluns

Baluns are the other major components in a ring mixer. Inductive transformers or a microwave coupling structure are used for baluns. The balun balances the diodes and interfaces them with the unbalanced system. In addition, the balun current, I,

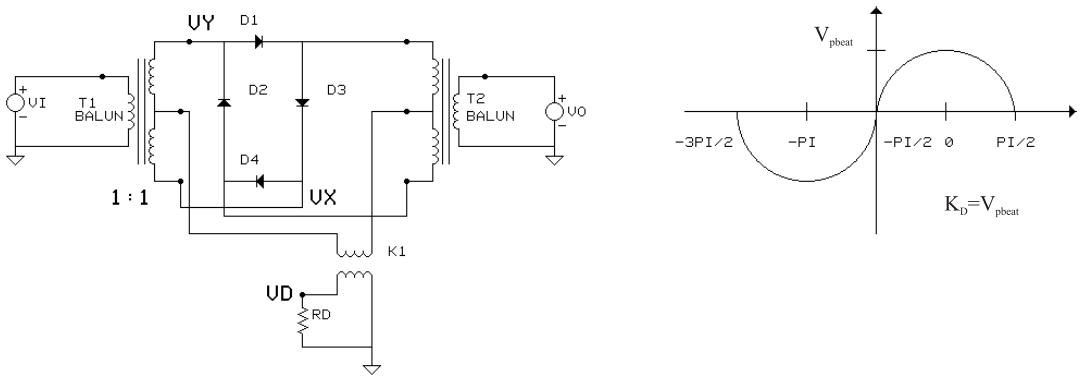


Figure 5.1 Diode ring mixer and transfer function of output voltage versus phase error.

matches system and diode impedance and provides interport isolation. The balun at the LO port provides the IF current return path to ground. Currents in the two balanced leads of a balun are 180° apart in phase and ±90° out of phase with respect to ground [1]. The amplitude and duty cycle of the input affect the phase detector gain. Consequently, these circuits should be used with large input signals.

The mixer circuit in Figure 5.1 operates with any waveform; however, using a square wave, like the V_o in Figure 5.2, eases understanding of the circuit's operation. The switching voltage V_o "turns on" either the bottom two diodes (D3, D4) or the top two diodes (D_1, D_2) depending on the polarity of V_o. A positive V_o makes the bottom two diodes (D_3, D_4) conduct. V_x equals the voltage at the midpoint of the secondary winding of transformer T_2, which is ground. Then, $V_y = V_i$, and $V_{davg} = 0.5V_y = 0.5\ V_i$. Similarly, a negative V_o makes the top two diodes (D_1, D_2) conduct. V_y becomes effectively ground. Then, $V_{davg} = -0.5V_i$. The bottom waveform in Figure 5.2 shows the resulting waveform of V_{davg}.

To determine the transfer function for the mixer, several SPICE runs must be done for several phase errors that cover the range of the detector (π). Figure 5.3 shows the average output voltage versus phase error for a mixer phase detector. Each curve is a SPICE run with a different phase-error difference input to the mixer. A lowpass filter is adjusted to filter out the harmonics of the 5-MHz input frequencies and not cause long simulation times. In this case, the simulation was adjusted so that the waveforms settle out in 2 μs with a 50-mV ripple. The remaining ripple can be minimized by averaging the waveform over the time period from 4 to 6 μs.

Figure 5.4 shows the transfer function plotted for mixer phase detector from the data shown in Figure 5.3. This figure shows the average detected voltage V_{davg} versus sweeping phase error. As θ_e increases with time, the average component V_{davg} varies sinusoidally. The maximum of the characteristic equals the phase detector gain:

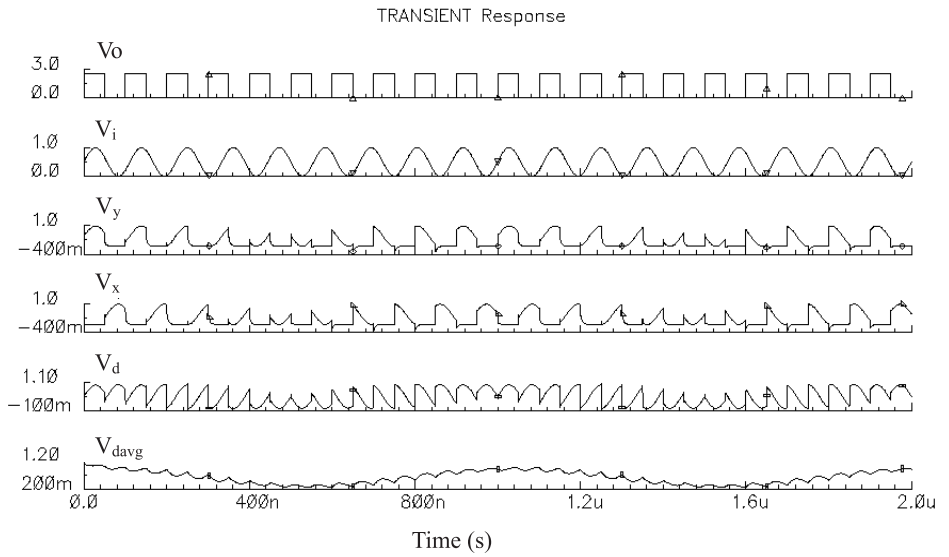


Figure 5.2 The switching waveforms in a diode ring mixer phase detector.

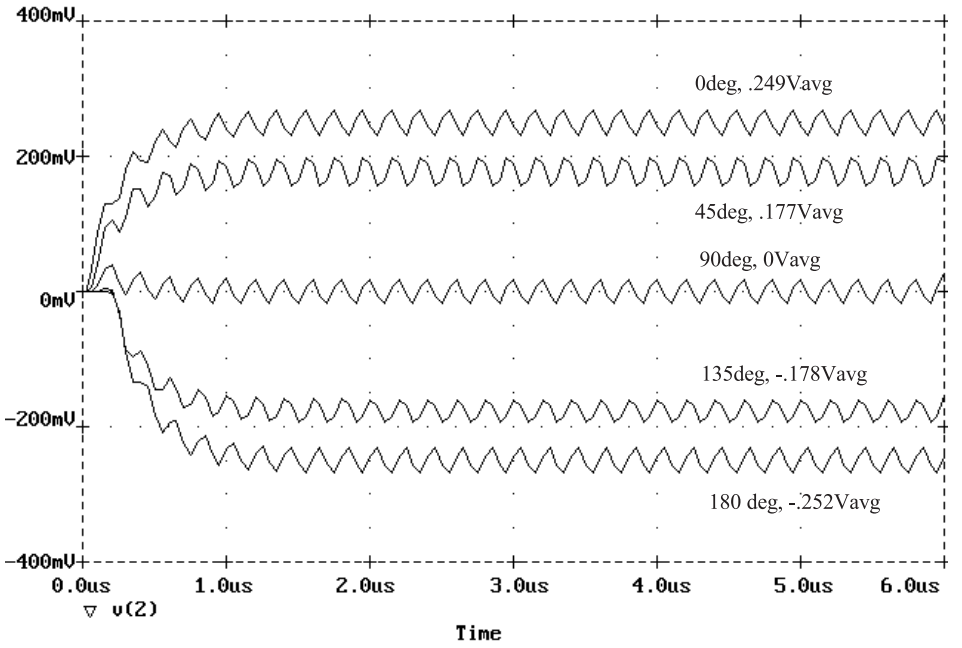


Figure 5.3 Average output voltage (lowpass filtered) versus phase error for a mixer phase detector.

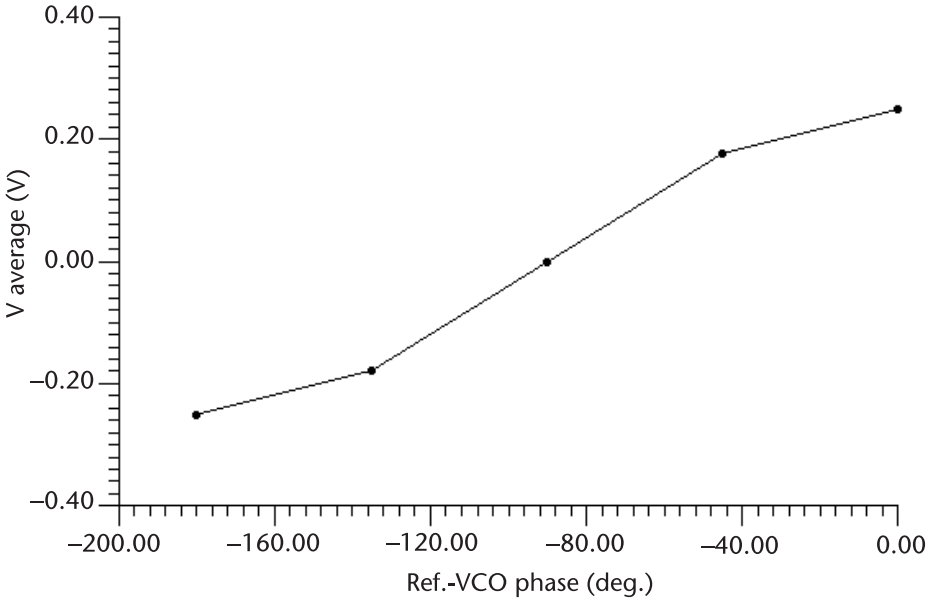


Figure 5.4 Transfer function for a mixer phase detector (average voltage versus phase-error difference in degrees).

$$V_{dm} = K_d = V_i / \pi \tag{5.9}$$

This assumes that both transformers have primary turns equal to secondary turns. A high signal amplitude V_i keeps V_{dm} high and gives the best figure of merit. For the operation as described above, the signal level of V_i should not cause a diode pair to conduct. This corresponds to $V_i \leq 1.2$V for equal transformer ratio. The fastest slope is at –90° phase shift, and the slope is reduced for shifts approaching –180° or 0°. For the peak-to-peak voltage of 0.5V, we can calculate the slope at –90°. From (5.8) this computes to 0.25 V/rad because V peak equals V peak to peak divided by 2 (0.5/2).

A figure of merit $M \geq 400$ can be achieved with well-matched diodes in an integrated circuit that produce a V_{do} of less than 1 mV. If low offset voltage of the phase detector is achieved, then the active loop filter usually becomes a significant contributor. The active loop filter can have an offset voltage of 5 mV; however, high-performance opamps can be used that have an offset as low as 0.1 mV.

In Figure 5.5, two signals with different frequencies (5 MHz and 5.5 MHz) are connected into a mixer phase detector, followed by a lowpass filter. This connection produces a sinusoidal output waveform that shows the sinusoidal shape of the phase detector transfer function. This characteristic waveform will also be seen in other phase detectors and will explain some of the behavior that can occur. Figure 5.6 shows the CMOS transistor ring mixer that is equivalent to the diode ring-based mixer. This connection can easily be integrated while the diode ring cannot.

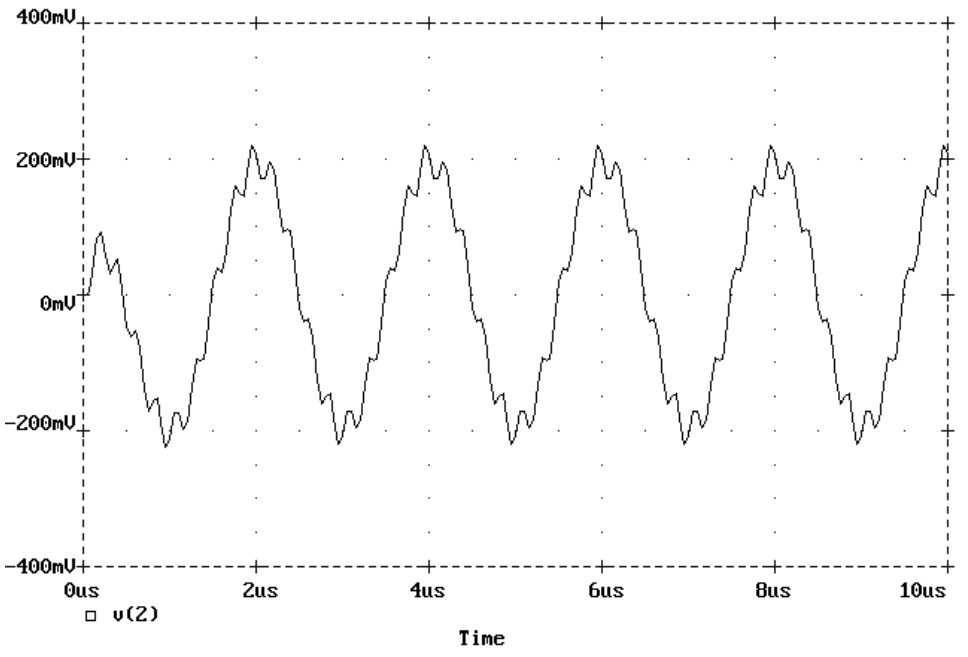


Figure 5.5 Waveform that results from two input frequencies into the mixer, showing the shape of the transfer function.

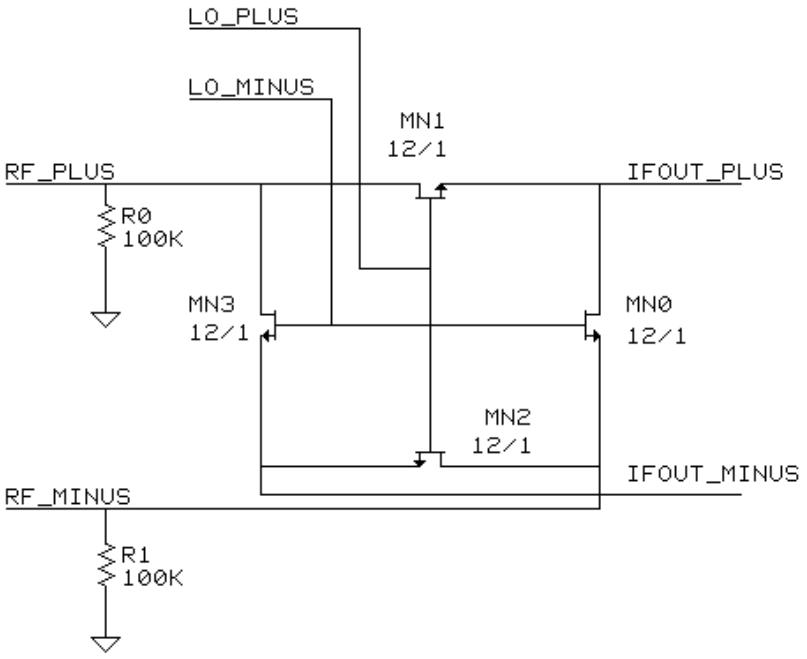


Figure 5.6 Schematic of CMOS ring mixer that can be used for a phase detector.

5.1.4 Gilbert Multiplier

The Gilbert multiplier circuit shown in Figure 5.7 also implements a four-quadrant multiplier. This circuit does not have a balun and can be more easily integrated into a monolithic circuit.

Figures 5.7 and 5.8 help describe the operation of the circuit. First, V_o splits the current I to the left as i_1 or to the right as i_2, according to the characteristic shown in Figure 5.8. V_i splits the current i_1 into currents i_3 and i_4, according to the characteristic shown in Figure 5.8. A similar characteristic holds for i_2. Similarly, V_i splits the current i_2 into currents i_5 and i_6. Combining the four currents produces (5.10):

$$\begin{aligned} V_{davg} &= (i_4 + i_6)R_1 - (i_3 + i_5)R_2 \\ &= (i_4 + i_6 - i_3 - i_5)R \end{aligned} \tag{5.10}$$

where

$$R_1 = R_2 = R.$$

In practical applications, R_1 and R_2 have different values, which causes a dc offset; we will discuss this effect later in (5.14) through (5.17).

Now let's study an equation for the average detected output voltage and its associated multiplier gain constant. Keeping V_i and V_o in the linear region of the characteristics in Figure 5.8 (amplitude less than 52 mV) produces (5.11) for the average detected output voltage V_d.

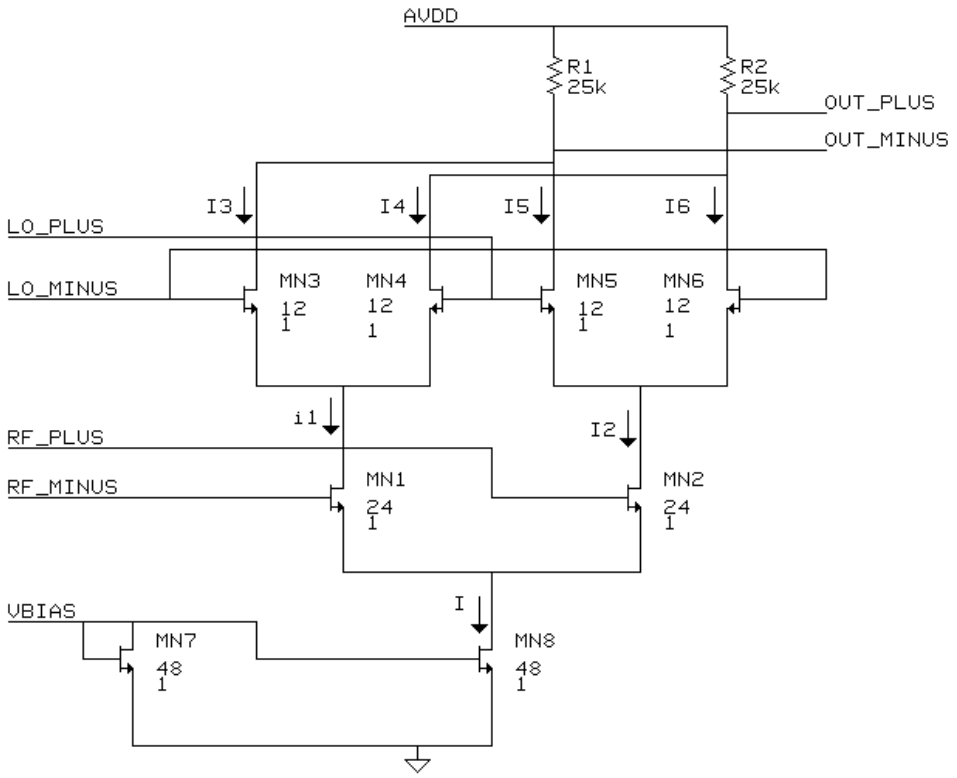


Figure 5.7 Schematic of CMOS Gilbert cell mixer.

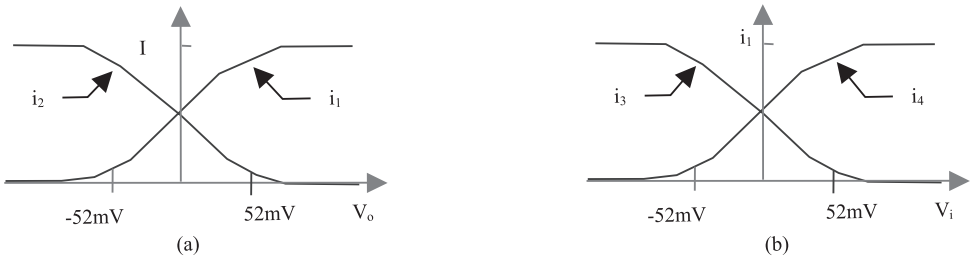


Figure 5.8 (a) Transfer function for the bottom difference amplifier and (b) the left-hand-side difference amplifier in Figure 5.7.

$$V_{davg} = K_m V_i V_o \tag{5.11}$$

K_m is a constant in volts^{-1} associated with the multiplier. Studying Figure 5.8 gives us the calculation for the multiplier gain constant. If we assume all the tail current I goes to i_1 and none goes to i_2, i_5, and i_6, then from the transfer function on the left-hand side of Figure 5.8 ($i_1 = V_o I/52$ mV). Again, if we assume that all the current goes into i_4 and none goes into i_3, then from the transfer function on the right-hand side of Figure 5.8, $i_4 = V_i i_1/52$ mV. Substituting the previous

equation into the last gives $i_4 = V_i V_o I/(52\text{ mV})^2$. Multiplying by R and comparing the equation to (5.11) gives (5.12) for computing the multiplier gain constant:

$$K_m = RI/(52\text{ mV})^2 \tag{5.12}$$

Equation (5.13) computes the maximum voltage out of the phase detector, which gives us the phase detector gain for sinusoidal inputs:

$$K_d = K_m V_i V_o \tag{5.13}$$

From (5.8) V_{dmax} equals K_d. Now, with the detector gain computed, let's look at the offset voltages that occur in the Gilbert mixer.

The mismatch of the transistors and of the resistors is the source of offset voltages. A mismatch in the transistors causes input offsets V_{io} of a few millivolts that add to the inputs V_i and V_o. Similarly, a mismatch between R_1 and R_2 causes the other offset to be added to the output. Equation (5.13) computes the effects of the mismatch:

$$V_{oo} = (R_1 - R_2)I/2 \tag{5.14}$$

Next, let's compute the average voltage at the output of the detector. Equation (5.15) computes the total expression for the output:

$$\begin{aligned} V_{davg} &= K_m(V_i + V_{io})(V_o + V_{io}) + V_{oo} \\ &= K_m V_i V_o + K_m\left(V_{io}V_i + V_{io}V_o + V_{io}^2\right) + V_{oo} \end{aligned} \tag{5.15}$$

Taking the time average, as we did in going from (5.3) to (5.6), gives (5.16):

$$V_d = V_{dm}\sin(\theta_e) + K_m(V_{io})^2 + V_{oo} \tag{5.16}$$

The dc terms in (5.16) can be combined as an effective offset voltage at the phase detector output to give (5.17):

$$V_{do} = K_m(V_{io})^2 + V_{oo} \tag{5.17}$$

Figure 5.9 uses signal flow graphs to summarize these relationships for calculating dc offset voltage.

Example 5.1

The Gilbert multiplier circuit in Figure 5.7 has a current $I = 2$ mA and resistance $R = 5$ kΩ. R_1 and R_2 differ by 2%, and $V_{io} = 5$ mV. Find the dc offset V_{do}, the gain of the phase detector K_d, and the figure of merit.

From (5.12) and (5.13), $K_m = (10\text{V})/(52\text{ mV})^2 = 3{,}698$, and $K_d = V_i V_o(3{,}698)$. K_d depends not just on the circuit but on the input levels. The maximum K_d

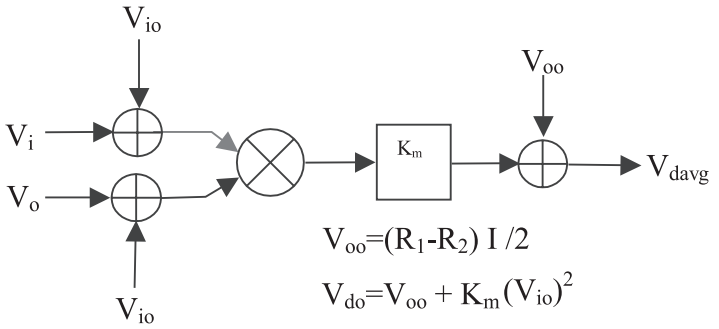


Figure 5.9 Signal flow graph of calculations for dc offset in Gilbert mixer. (*From:* [2]. © 1991 Prentice-Hall. Reprinted with permission.)

corresponds to $V_i = V_o = 52$ mV, which is the largest signal that (5.8) holds. Then, $K_d = (52 \text{ mV})^2$ 3,698 = 10.0 V/rad.

From (5.14), $V_{oo} = (0.02R)I/2 = (100\Omega)$ 2 mA/2 = 100 mV. Also, $K_m(V_{io})^2 = (5 \text{ mV})^2$ (3,698) = 93 mV. Then, by (5.16), the total offset is V_{do} = 92 mV + 100 mV = 193 mV. Then, from (5.2), the figure of merit for the multiplier is M = 10/0.193 = 51.8.

5.1.5 Exclusive-OR Phase Detector

An exclusive-OR logic circuit has essentially the same characteristics as an overdriven multiplier circuit. Overdriving the multiplier saturates the output at either a positive value, corresponding to a logic "high," or a negative value, corresponding to a logic "low."

A voltage at V_i in Figure 5.1 causes current to flow through either the left or right leg of the diode bridge, depending on the polarity of V_i. As the signal at V_i changes polarity, the conducting leg switches to the other side. This switching action inverts the polarity of a smaller signal at V_o as it appears at the output V_d. A negative or positive V_i and V_o input makes the output V_d positive. One positive input, with the other input being negative, makes the output V_d negative. The truth table for a multiplier is shown in Table 5.1.

Comparing this logic with a truth table as shown in Table 5.2 shows the multiplier logically functions as an exclusive-NOR gate. Consequently, an overdriven multiplier is an exclusive-NOR, with "+" corresponding to a logic high (1) and "–" corresponding to a logic low (0).

Then, an exclusive-NOR gate can be used for phase detection. The transfer function will have a triangular shape. In addition, an exclusive-OR gate can be

Table 5.1 Multiplier Truth Table

V_i	V_o	V_{davg}
–	–	+
–	+	–
+	–	–
+	+	+

Table 5.2 Exclusive-NOR Gate Truth Table

Input A	*Input B*	*Output OUT*
0	0	1
0	1	0
1	0	0
1	1	1

used. This gate just inverts the output logic. Consequently, a balanced output that is both positive and negative, where $V_{davg} = V_{bavg} - V_{aavg}$, uses an exclusive-OR output for V_{aavg} and its complement (exclusive-NOR) for V_{bavg}. Figure 5.10 shows a schematic of an exclusive-OR gate. This figure shows that it takes an inverter and four transistors to make an exclusive-OR gate. This is a minimum of transistor connections a (total of six transistors).

Figure 5.11 shows two square-wave inputs (A and B) to the exclusive-OR gate and the resulting output waveform at OUT. To determine the transfer function for the exclusive-OR phase detector, several SPICE runs must be done for several phase errors that cover the range of the detector (π). Figure 5.12 shows these multiple SPICE runs for 5-MHz reference and VCO frequency inputs. The figure contains lowpass-filtered output voltages versus phase error for an exclusive-OR phase detector. Each curve is a SPICE run with a different phase-error-difference input to the mixer. A lowpass filter is adjusted to filter out the harmonics and keep simulation times down. For this case, the output waveforms are settled at 2.5 μs. The remaining ripple can be minimized by averaging the waveform over the time period from 2.5 to 4 μs.

Figure 5.13 shows a plot of the average value of the output as a function of the phase difference between inputs. The phase error is plotted as the ratio of phase-error edge difference divided by the input source time period. This average value, which results from lowpass-filtering the gate output, detects phase error

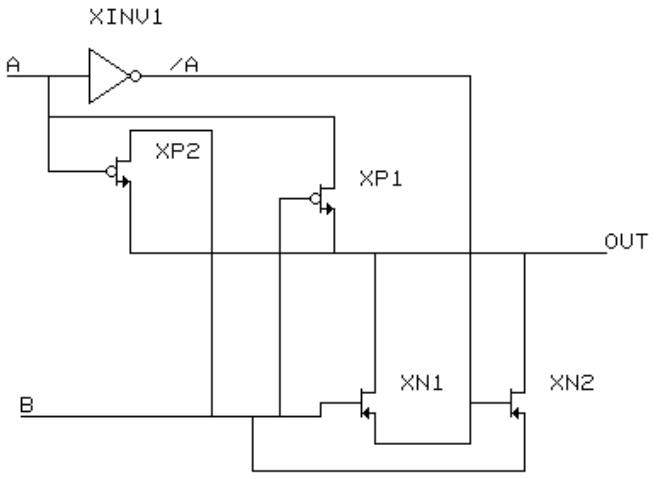


Figure 5.10 Schematic of an exclusive-OR gate.

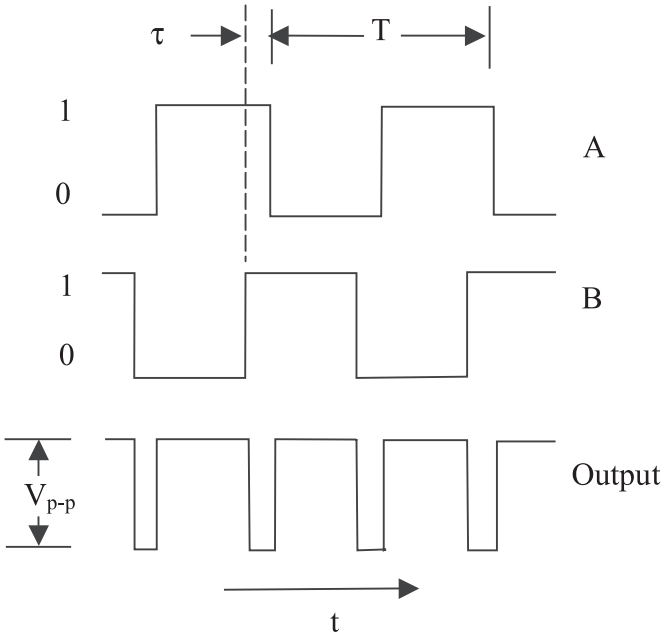


Figure 5.11 Input and output waveforms of an exclusive-OR gate that is used as a phase detector.

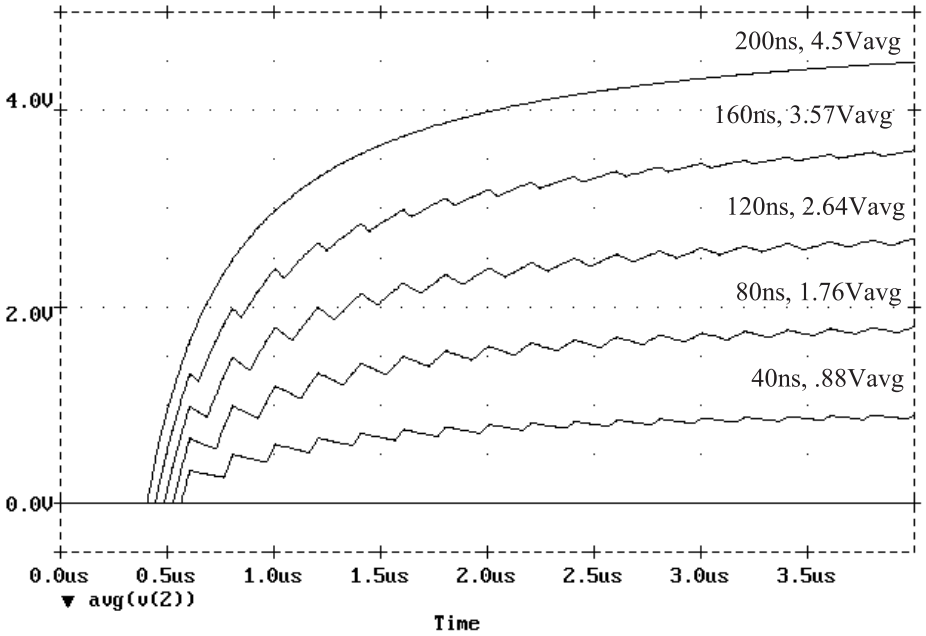


Figure 5.12 Lowpass-filtered output of an exclusive-OR gate versus the variation of input phase error.

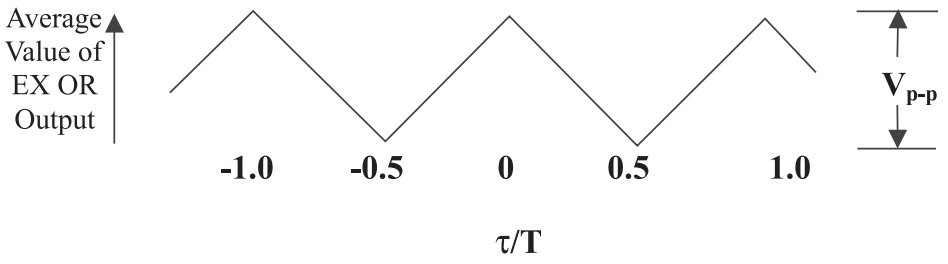


Figure 5.13 Transfer function of exclusive-OR phase detector showing average output voltage versus fractional phase error.

over a range of half a cycle before it starts repeating. For any input phase error, the ideal output does not contain any energy at the fundamental input frequency. At a 90° phase difference for the worst case, the second-harmonic has peak-to-peak amplitude 1.27 times the peak-to-peak range of the phase detector characteristic.

To generate the transfer function for a phase detector, we put in the same frequency 5 MHz with varying phase. This transfer function controls the behavior when the loop is close to lock. When the loop is unlocked, the phase detector has two different input frequencies. Figure 5.14 shows the PSPICE response of the detector with two different input frequencies (5 and 4 MHz). Figure 5.15 shows the unfiltered pulse-width modulation that comes out of the exclusive-OR gate. When this response is seen in other phase detectors, it shows the phase detector acting like an exclusive-OR gate or a multiplier with saturated inputs. A PLL uses the dc average of this waveform to acquire lock. As a rule of thumb, if this frequency difference is 10 times the loop bandwidth, lock will not be achieved, and

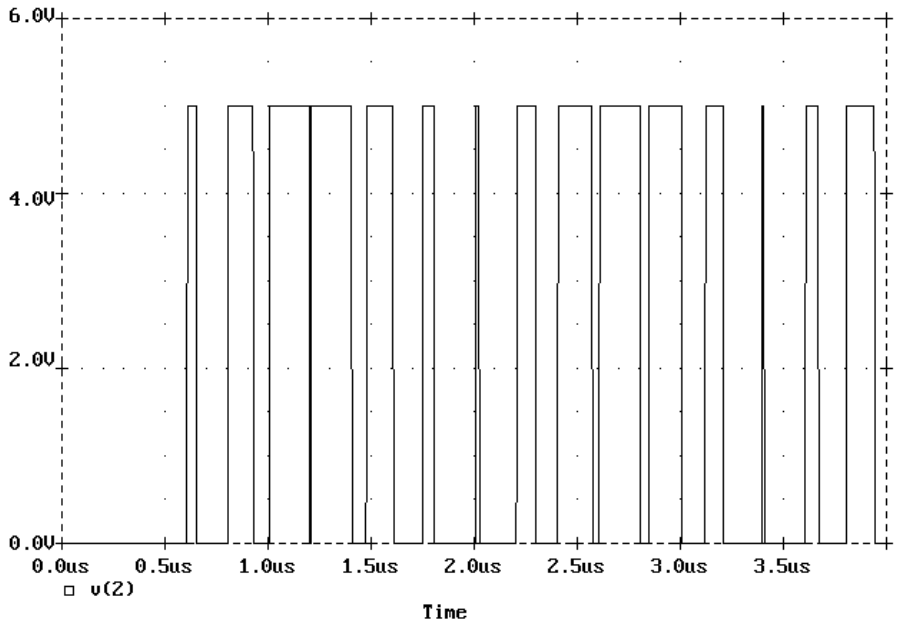


Figure 5.14 Exclusive-OR gate output for inputs with a frequency difference.

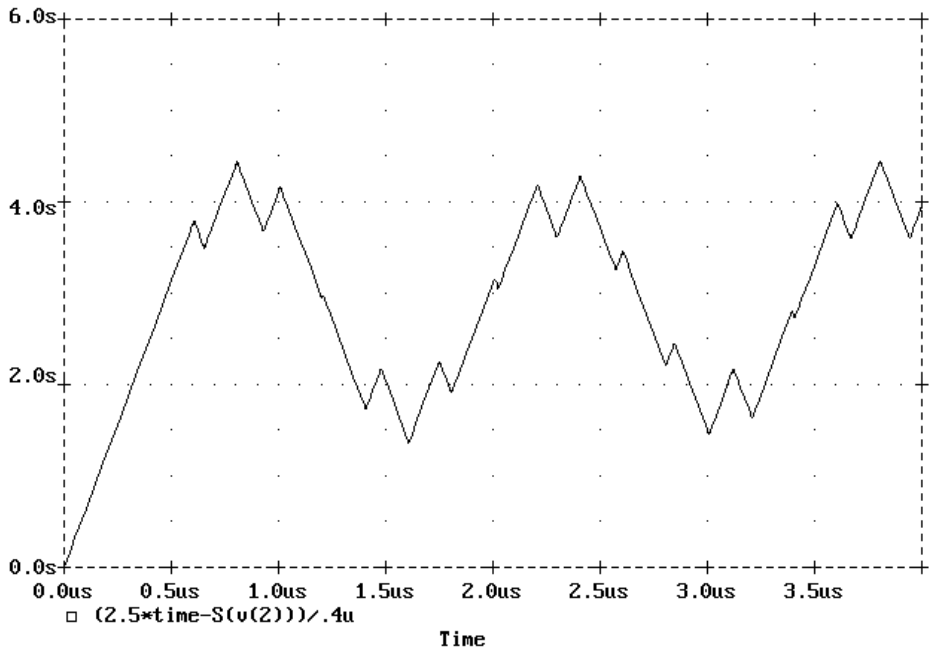


Figure 5.15 Lowpass-filtered (integrated) output of an exclusive-OR detector with a frequency difference at the input.

a frequency-aided acquisition circuit will have to be used. Between 2 and 10 times the bandwidth, the loop will lock in an increasing amount of time, depending on the frequency difference.

Lowpass-filtering the waveform in Figure 5.14 produces the waveform in Figure 5.15. The x-axis is simulation time, and the y-axis is average voltage. The average voltage was computed in PSPICE by integrating the output voltage $[V(2)]$ over the input period (0.2 μs) and offsetting the waveform ($2.5 \times$ time) to make the resulting waveform start at 0. The waveform in the figure shows the sawtooth transfer function and looks similar to the filtered output of the mixer.

So far, we have assumed that the square waves at the input to the detector have a symmetrical shape. Consequently, the input waveforms have a 50% duty cycle. Suppose that A has a duty cycle of 20%, and B has a duty cycle of 40%, as in Figure 5.16. A duty cycle not equal to 50% produces a nonzero, free-running voltage and reduces V_{dm} of the phase detector characteristic. If either, or both, inputs has other than 50% duty cycle, the exclusive-OR phase detector characteristic will have flat spots, as shown in Figure 5.16. The detailed harmonic content of the output of this type can be obtained as a function of duty cycle by Fourier analysis [2]. Using the digital exclusive-OR gate as a phase detector has the advantage of greater gain K_d, less offset V_{io}, and greater linear phase range.

5.1.6 RS Phase Detector (Two States)

An RS latch can be used as a phase detector and have similar characteristics to an exclusive-NOR gate. Figure 5.17 shows a schematic of the RS latch. Figure 5.18

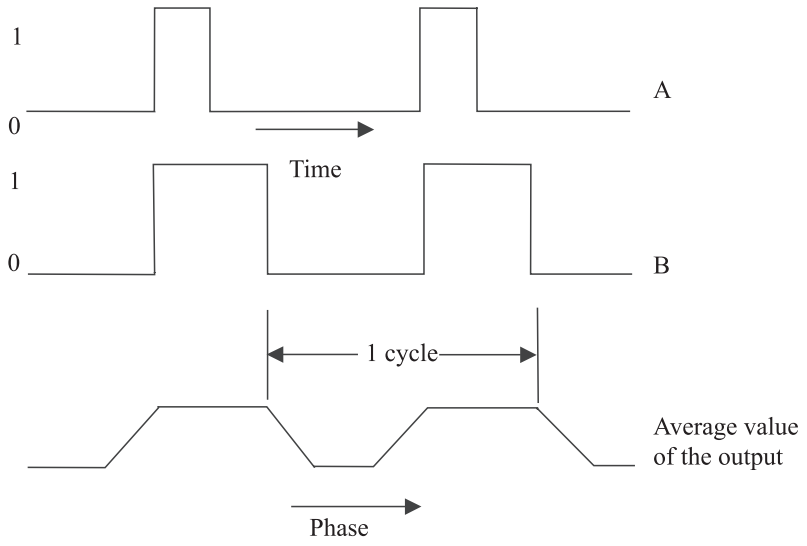
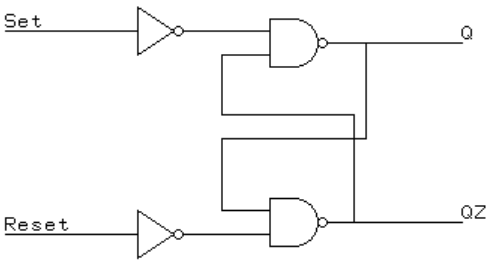


Figure 5.16 Exclusive-OR average output transfer function with non-50% duty-cycle inputs.



Truth Table

Mode of Operation	S	R	Q	QB
Undefined	1	1	1	1
Set	1	0	1	0
Reset	0	1	0	1
Hold	0	0	No change	No change

Figure 5.17 Schematic of an RS latch.

shows the expected waveforms for an RS latch used as a phase detector. The figure shows the input and output signals of the RS-latch phase detector. The input signals *A* and *B* consist of narrow pulses. They connect to the set and reset inputs of a set-reset latch. The average value of the *Q* output is proportional to the phase at *A* relative to *B*. This creates a sawtooth transfer function of voltage versus phase as shown in Figure 5.19. For either input with a finite width, the phase detector transfer function has a flat spot that corresponds to the width at a corner. For both inputs with finite widths, the flat spot, or the sum of two flat spots, will be as wide as the wider input.

Connecting one signal of arbitrary width to the clock input of an edge-triggered D flip-flop will give the same transfer function as the RS latch without causing the flat spot. Consequently, one edge of the waveform defines the switching time. The other input connects to the set or reset input. This signal still must be narrow to minimize the flat spot.

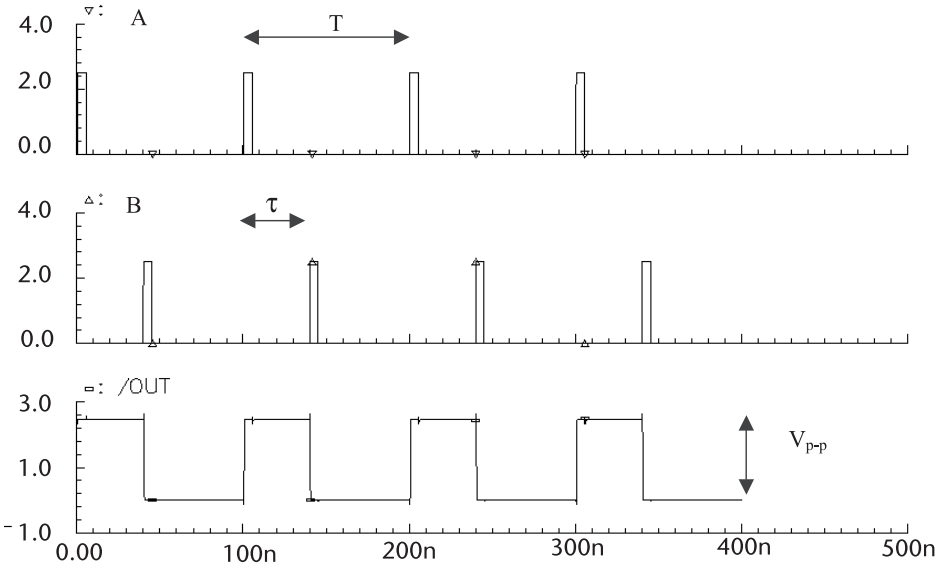


Figure 5.18 Input and output waveforms of an RS latch used as a phase detector.

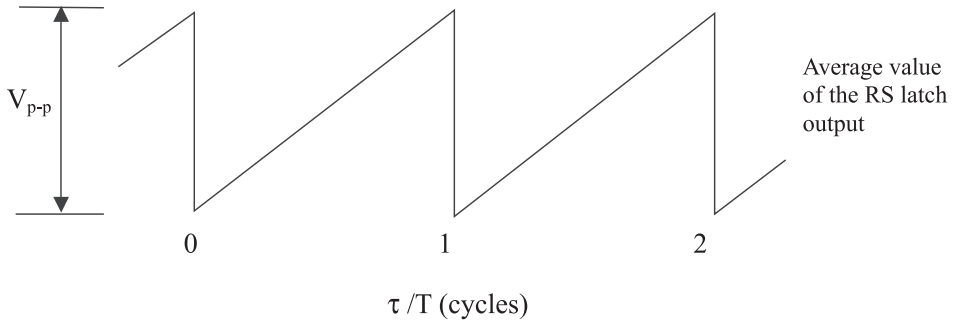


Figure 5.19 Transfer function for an RS latch used as a phase detector.

In the middle of the 360° linear phase range, the Fourier frequency output component at the fundamental frequency of the input signals has a peak-to-peak magnitude equal to 1.27 times the peak-to-peak voltage range of the output characteristic, which is $V_{p\text{-}p}$ in Figure 5.18. The exclusive-OR phase detector has very little spectral energy at the fundamental frequency and has a lot more energy at twice the fundamental frequency. In some applications, this makes filtering out this spurious signal for an exclusive-OR gate easier.

Consequently, the RS latch has the disadvantage of higher spectral energy at the fundamental relative to the exclusive-OR; however, the RS latch has twice the phase-error range for a given gain as shown by comparing Figure 5.19 with Figure 5.13. The exclusive-OR gate and the RS latch are the building blocks for more complicated phase detectors. Understanding their behavior will help us understand the operation of more complicated phase detectors.

Figure 5.20 shows input and output waveforms of an RS latch used as a phase detector for unequal input frequencies (10 and 9.9 MHz). The bottom waveform shows the result of lowpass-filtering the output. This figure shows the pulse-width modulation in an RS flip flop (RSFF) that also occurs in an exclusive-OR gate for two input signals with different input frequencies (10 and 9.9 MHz). This waveform characteristic can be recognized in more complicated phase detectors.

5.1.7 Phase/Frequency Detector

This section studies the phase/frequency detector, which is one of the most commonly used detectors. As you will see, understanding the phase/frequency detector is key to understanding loop performance. First, we will study the gate logic. Next, we will cover the operating conditions. Finally, we will study the transfer function of the phase detector.

Figure 5.21 shows the PSPICE model for the phase/frequency detector, which is one of the most commonly used phase detectors [3, 4]. This model is based on logic gates in the device. The schematic shows that four RS latches make up the phase/frequency detector. FF1 and FF2 control the up and down pulses, and FF3 and FF4 control the reset signal for all the latches. The critical path is limited by just three gate delays, two from the cross-coupled two-input NAND gates and one from the four-input reset NAND gate.

Figure 5.22 shows the relationships of up and down outputs to input waveforms by plotting the average voltage of the individual outputs *u* and *d* and the *u-d* differential combination output versus phase or frequency. The logic in Figure 5.22 shows five possible phase detector relationships.

For the first relationship, the frequency of the VCO is greater than the frequency of the reference. This condition causes the up output to have a low logic level with

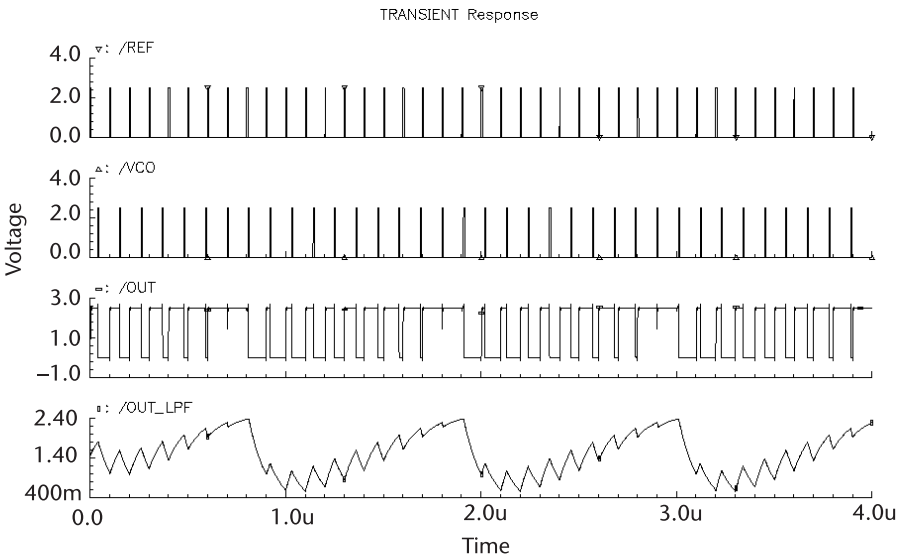


Figure 5.20 Input and output waveforms for RS latch with unequal input frequencies.

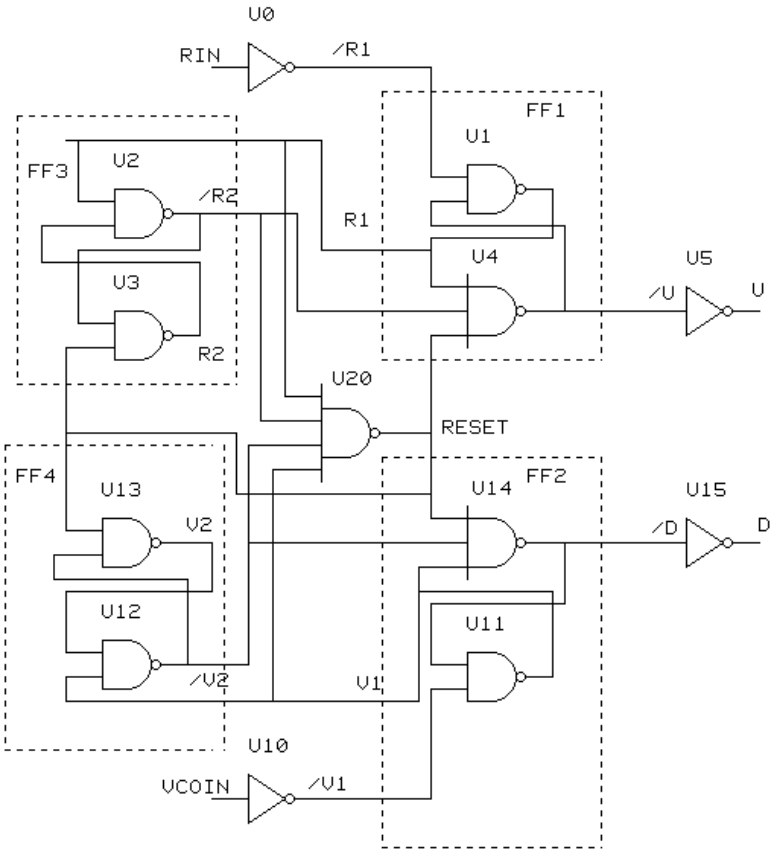


Figure 5.21 PSPICE logic model for the phase/frequency detector.

small positive-going pulses and the down output to have approximately a 50% duty-cycle (pulse-width-modulated) waveform. In this condition, decreasing the VCO frequency will lock the PLL.

For the second relationship, the frequency of the VCO is less than the frequency of the reference. This condition causes the down output to have a low logic level with small positive-going pulses and the up output to have approximately a 50% duty-cycle (pulse-width-modulated) waveform. In this condition, increasing the VCO frequency will lock the PLL.

For the third relationship, the frequency of the reference equals the frequency of the VCO, and the phase of the reference lags the phase of the VCO. This condition causes the up output to have a low logic level with small positive-going pulses and the down output to have positive-going pulses. In this condition, decreasing the VCO phase will lock the PLL.

For the fourth relationship, the frequency of the reference equals the frequency of the VCO, and the phase of the reference leads the phase of the VCO. This condition causes the down output to have a low logic level with small positive-going pulses and the up output to have positive-going pulses. In this condition, increasing the VCO phase will lock the PLL.

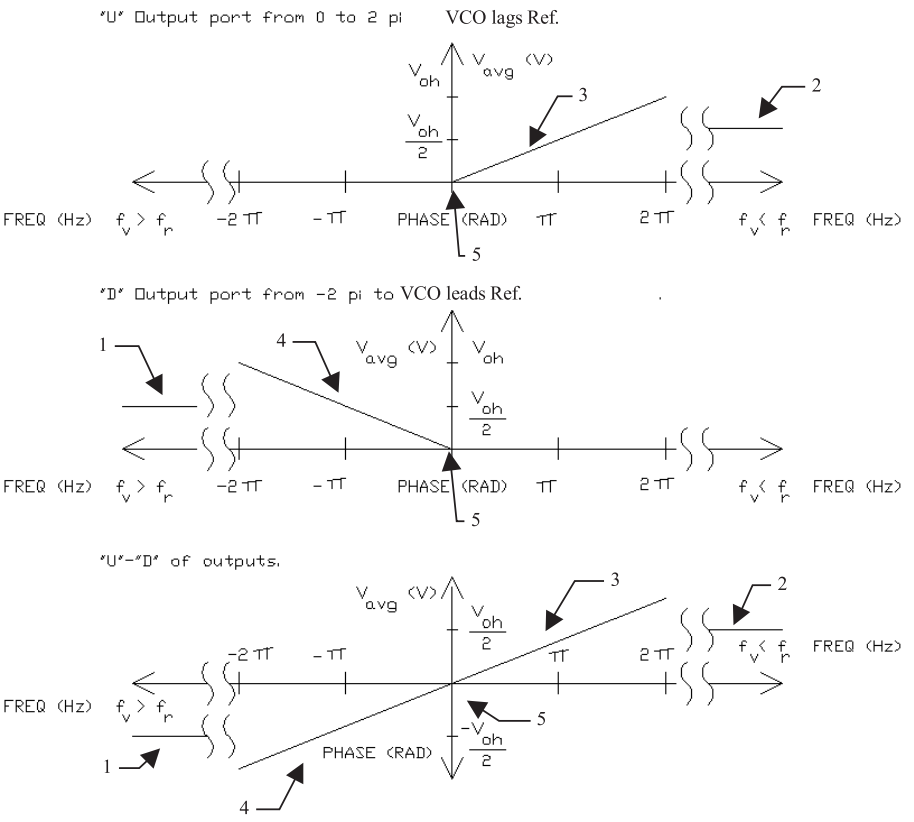


Figure 5.22 Relationships of up and down outputs to input waveforms.

In the third and fourth conditions, the phase difference between the reference and VCO input determines the duty cycle of the positive-going pulses at the down and up outputs. Theory states that a 180° phase difference produces a 50% duty cycle.

In the fifth condition, the frequency of the reference equals the frequency of the VCO, and the phase of the reference equals the phase of the VCO. This condition produces the lowest duty cycle and causes positive-going pulses out of the up and down outputs to occur simultaneously. This condition causes a phase distortion in the transfer function [5].

Let's use a SPICE model to see if we can generate the five relationships and to study the logic more closely. This can be accomplished by varying conditions of the two input sources into the phase/frequency detector. Let's use a reference frequency of 2.5 MHz for the phase detector test. The higher-frequency speeds up the simulation time and make it easier to see the narrow pulses on the plots. The CD that accompanies this book shows the hierarchical SPICE deck for the phase/frequency detector. Now that the SPICE circuit is defined, let's begin understanding the operation of phase/frequency detectors by studying the frequency discriminator function of the detector.

5.1.7.1 Frequency-Difference Response

Let's look at the operation of the phase/frequency detector when the VCO frequency is greater than the reference frequency. Figure 5.23 shows the response of the detector for a reference frequency of 40 MHz and a VCO frequency of 50 MHz, as shown in the first two waveforms at the top of the figure. The up output has narrow pulses and the down output has a pulse-width-modulated output, as shown by the next two waveforms. The loop-compensation processes the pulse-width-modulated down output to push the VCO frequency lower toward the lock condition. The next four waveforms in Figure 5.23 are the inputs to the four-input NAND gate that generates a reset for the latches in the phase detector. The reset signal is the last waveform in the figure. Next, the reset pulse, the up pulse, and the positive edge of the reference are in synch. When the VCO positive edge lags the reference edge by half a period, the reset pulse resets the RS latch (v_1) to get the correct phase detector pulse width.

Figure 5.24 shows the response of the detector to a reference frequency of 50 MHz and a VCO frequency of 40 MHz, as shown in the first two waveforms at the top of the figure. The reset pulse, the down pulse, and the positive edge of the VCO are in synch. When the VCO positive edge lags the reference edge by half a period, the reset pulse resets the RS latch (signal r_1) to get the correct phase detector pulse width. Next, the up output has pulse-width-modulated output, and the down output has narrow pulses, as shown in the next two waveforms. Loop-compensation processes the pulse-width-modulated up output to push the VCO to a higher frequency.

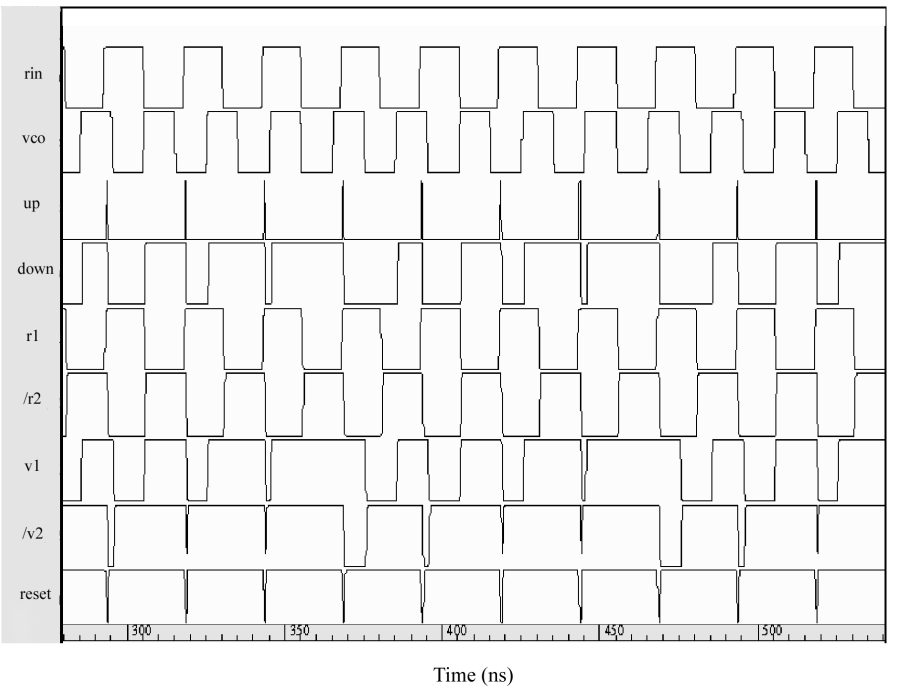


Figure 5.23 VCO frequency greater than the reference frequency.

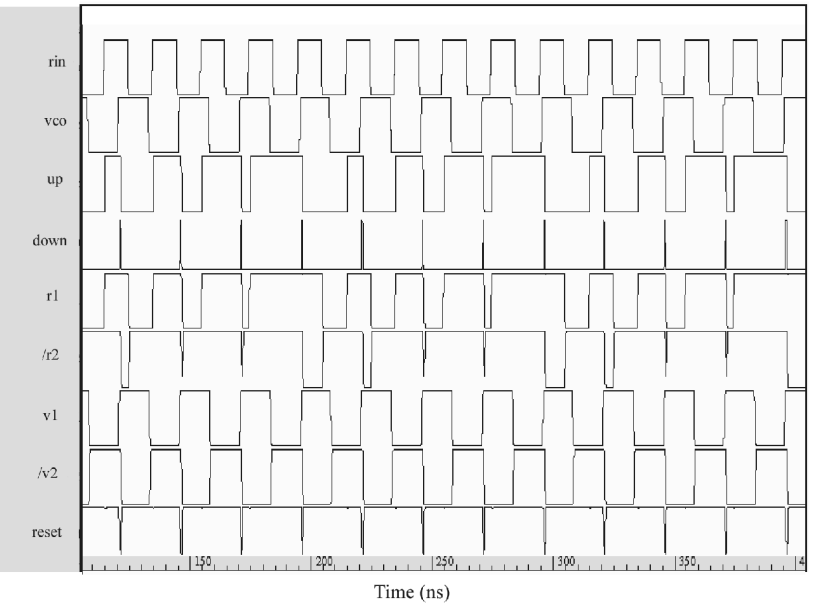


Figure 5.24 VCO frequency less than the reference frequency.

Pulse-width modulation in the up and down outputs of the phase/frequency detector produces the frequency-discrimination mechanism; however, a potential hang up in the transition from frequency detector to phase detector can be caused by the frequency-discriminator mechanism. At high modulation rates, the detector is a frequency discriminator, and the high frequencies are filtered by the loop. However, at low modulation rates and at the edge of the transition from frequency to phase detector, one of the outputs has a slowly varying pulse-width-modulated beat-note output, and the phase frequency detector acts like an exclusive-OR gate. Figure 5.25 shows the pulse-width-modulation output response of an exclusive-OR gate (equivalent to an analog multiplier) to a reference frequency of 2.5 MHz and a VCO frequency of 1.825 MHz. This output is like the down and up responses of the phase/frequency detector in Figures 5.23 and 5.24.

The low-modulation-rate condition can occur for the phase/frequency detector in a PLL with a high damping factor. A low-modulation condition can arise from a slow approach path to lock with only one side (up or down) of the phase detector operating. At the transition from frequency detector to phase detector, it has pulse-width modulation similar to the exclusive-OR gate. If this modulation is less than the modulation bandwidth of the VCO and greater than the loop bandwidth, the loop will have to pull the modulated waveform into lock. This pull into lock is the same mechanism that analog PLLs use to achieve lock. This is a slow process that significantly increases lock time. The phase detector uses the dc average of the modulated signal to pull into lock.

An example measurement of a PLL shows the pull-into-lock mechanism that we have discussed. The PLL has a 270-MHz output frequency, 100-kHz reference frequency, 0.9 damping factor, and 5-kHz bandwidth. Figure 5.26 shows the zoomed-in transient response (output frequency on the *y*-axis and time on the

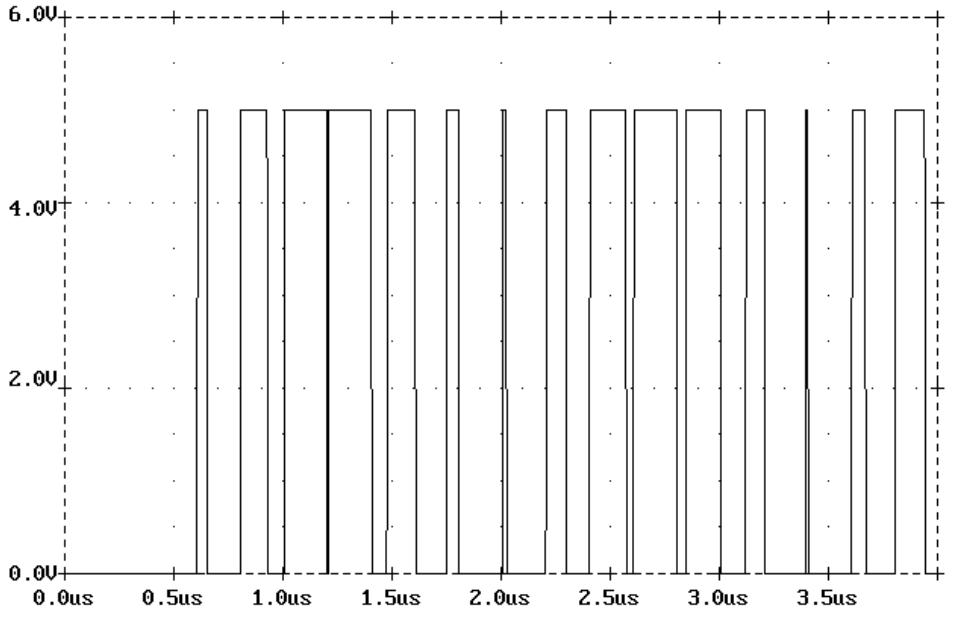


Figure 5.25 Output of exclusive-OR gate for different input frequencies.

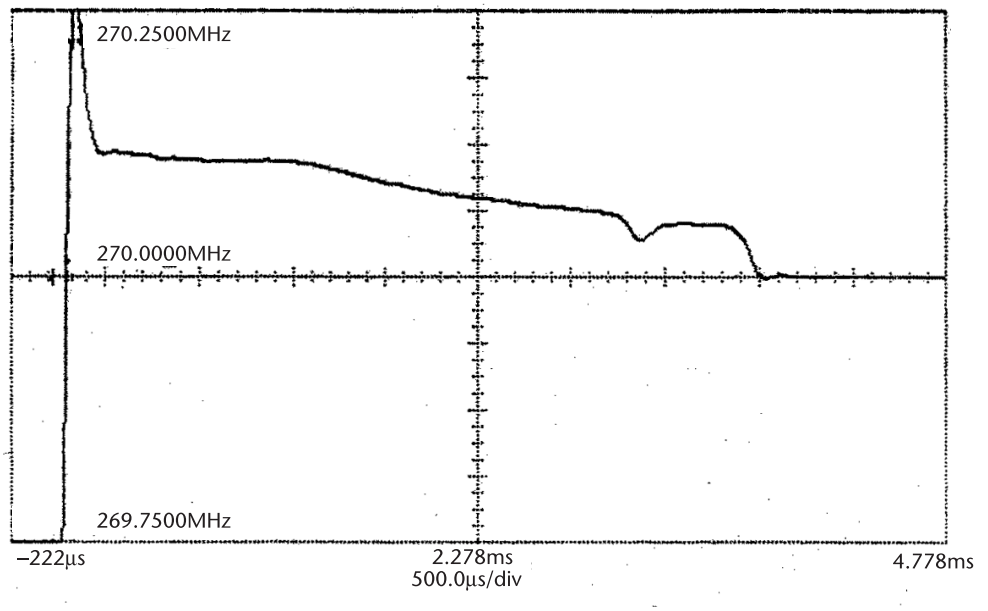


Figure 5.26 Zoomed-in measurement of transient response of a PLL with 0.9 damping factor that shows an analog pull-in mechanism.

x-axis) of the PLL, and it shows that the output frequency remains 50 to 120 kHz above the locked frequency for 3.5 ms before it locks at 270 MHz. The settling time of 3.5 ms is much greater than the 1/5 kHz (200 μs) one would expect for this loop.

Figure 5.27 shows the response of the example PLL with the damping factor changed to 0.5 and a loop bandwidth of 6 kHz. The loop now settles to 270 MHz in 500 μs and has a more classic PLL transient. This is a sevenfold improvement over the previous response. Consequently, this figure shows that the PLL transient response can get hung up in the transition from the frequency-discriminator to phase detector mode on one side of the phase detector and rely on an analog pull-in method to attain lock. Consequently, for fast transient response, a 0.5 damping factor is optimum. This completes the discussion of the frequency-difference response of the phase/frequency detector; we now move on to the phase-difference responses.

5.1.7.2 Phase-Difference Response

Let's study the operation of the phase/frequency detector when the VCO and reference frequency are equal but the phases are different. Figure 5.28 shows the phase/frequency detector output when the VCO phase leads the reference-oscillator phase, and their frequencies are equal to 50 MHz. The down output has a wide pulse width, and the up output has narrow pulses. The down output results from the logic AND of signals V_1 and $/V_2$. Also, the reset pulse, the up pulse, and the positive edge of the reference are in synch. The reset pulse resets the RS latch (ν_1) to get the correct phase detector pulse width.

Figure 5.29 shows the phase/frequency detector output when the VCO phase lags the reference-oscillator phase. The down output has narrow pulses, and the up output has wide pulses. The up output results from the logic AND of signals R_1 and $/R_2$. Also, the reset pulse, the down pulse, and the positive edge of the

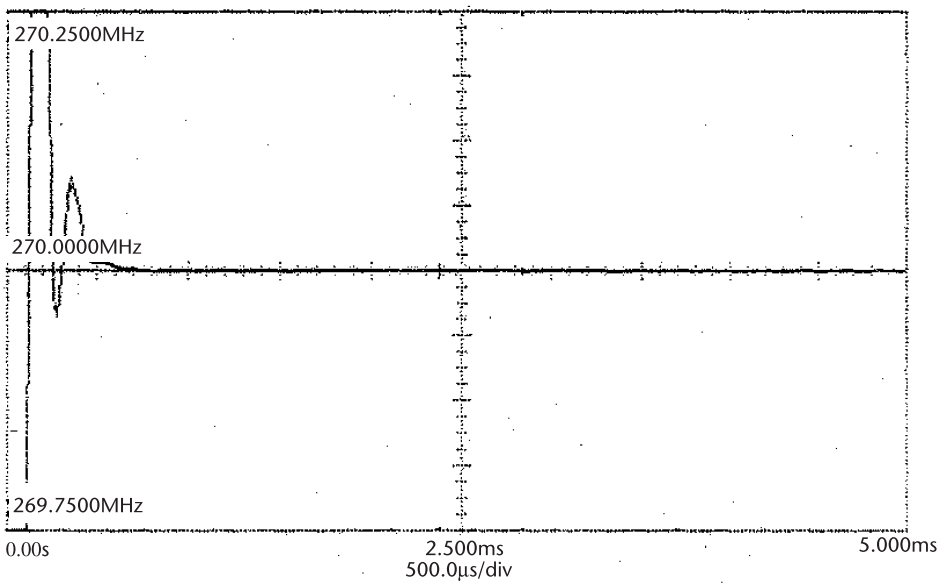


Figure 5.27 Zoomed-in measurement of transient response of example PLL that showed an analog pull-in mechanism with the damping factor changed to 0.5.

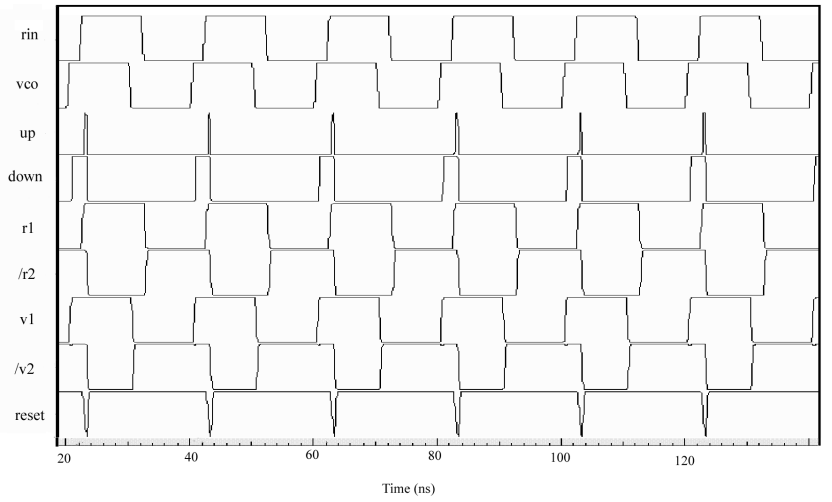


Figure 5.28 Phase/frequency detector output when VCO phase leads reference phase.

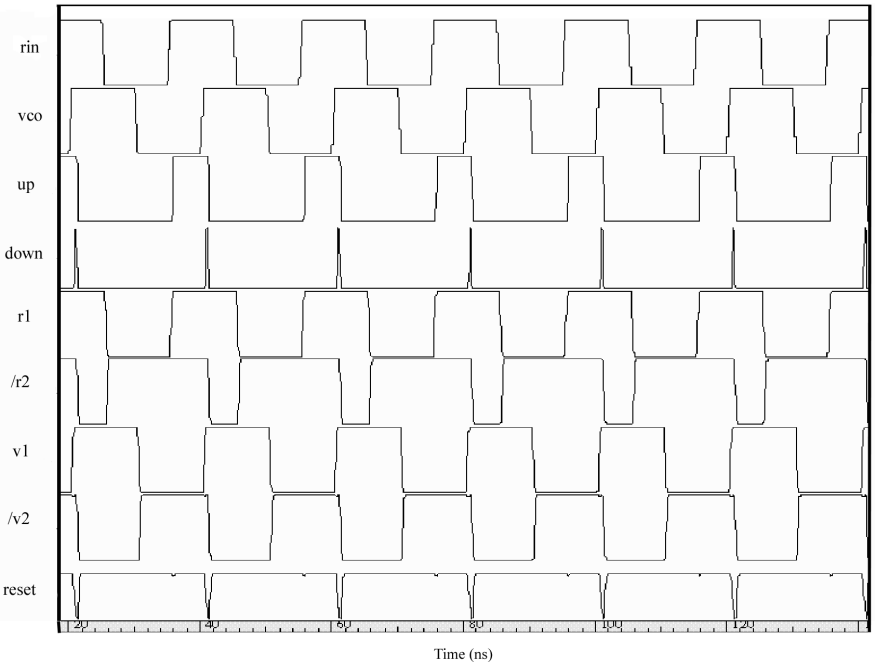


Figure 5.29 Phase/frequency detector output when VCO phase lags reference phase.

VCO are in synch. The reset pulse resets the RS latch (r_1) to get the correct phase detector pulse width.

Figure 5.30 shows that, for equal phase and frequency inputs, the up and down outputs produce narrow pulses. This results from the four-input logic AND of R_1, $/R_2$, V_1, and $/V_2$, which also generates the reset pulse. It is significant that the logic shows that output pulses should be present because measurements of

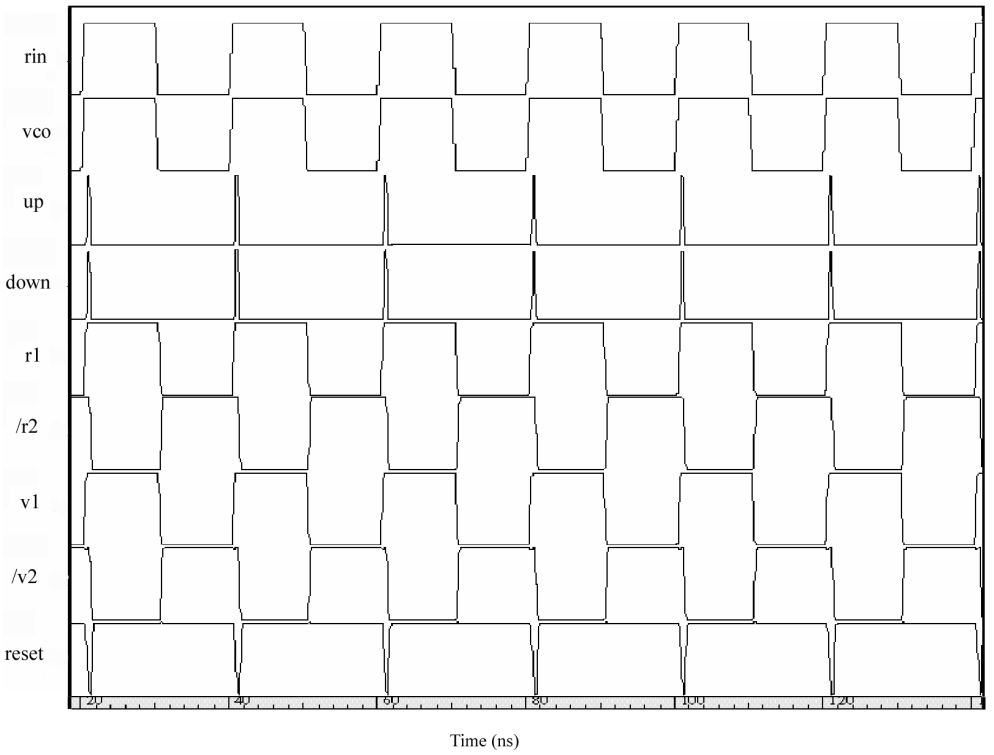


Figure 5.30 Equal phase condition for phase/frequency detector.

some phase detectors do not show these pulses. These zero-output measurements can be explained by the effects of output loading, which eliminates these pulses and causes a dead-zone problem.

5.1.7.3 Generation of Phase Detector Transfer Function

From the PSPICE simulations, the phase detector transfer function can be computed by varying the delay of one of the input signals and computing the average voltage of the resulting waveforms. First, let's compute the output voltage versus the phase of the phase detector by varying the delay (phase) of the VCO input in SPICE.

Figures 5.31 and 5.32 show phase/frequency detector outputs overlayed on top of each other for the variation of the delay of the VCO with respect to the reference of −8 to 8 ns in 4-ns steps. Variation of delay is an equivalent phase shift. Figure 5.31 shows the up output. The y-axis is voltage and the x-axis is simulation time. The falling edge of the up signal depends on the positive edge of the VCO input. The positive edge of the up signal stays fixed with the positive edge of the reference input. For −8-ns, −4-ns, and 0-ns conditions, the up signal has minimum pulse widths of 1 ns that are overlayed on top of each other and centered at the simulation time of 26 ns. This figure shows that for a positive-

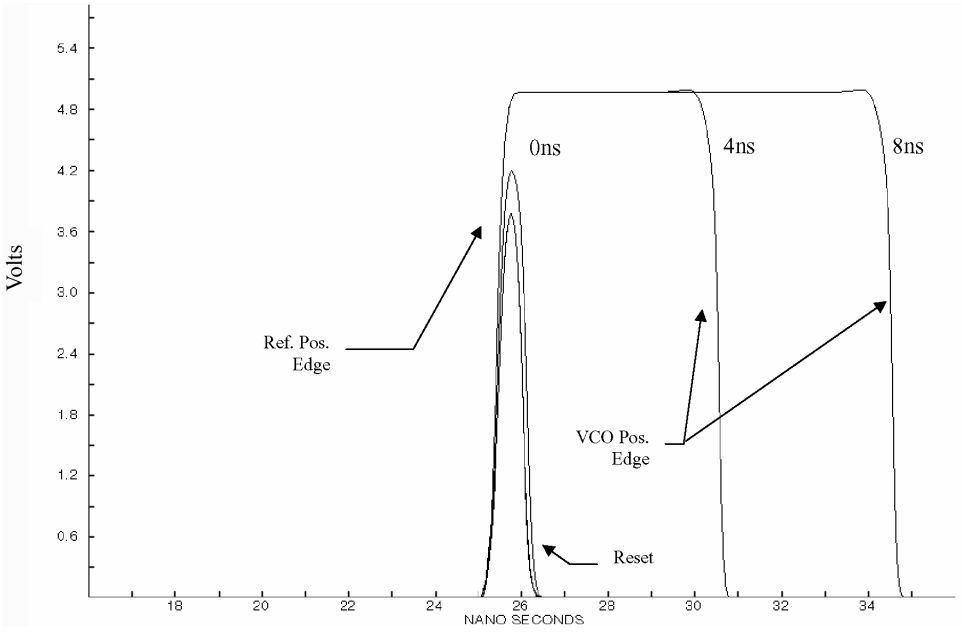


Figure 5.31 Up outputs versus delay in VCO phase.

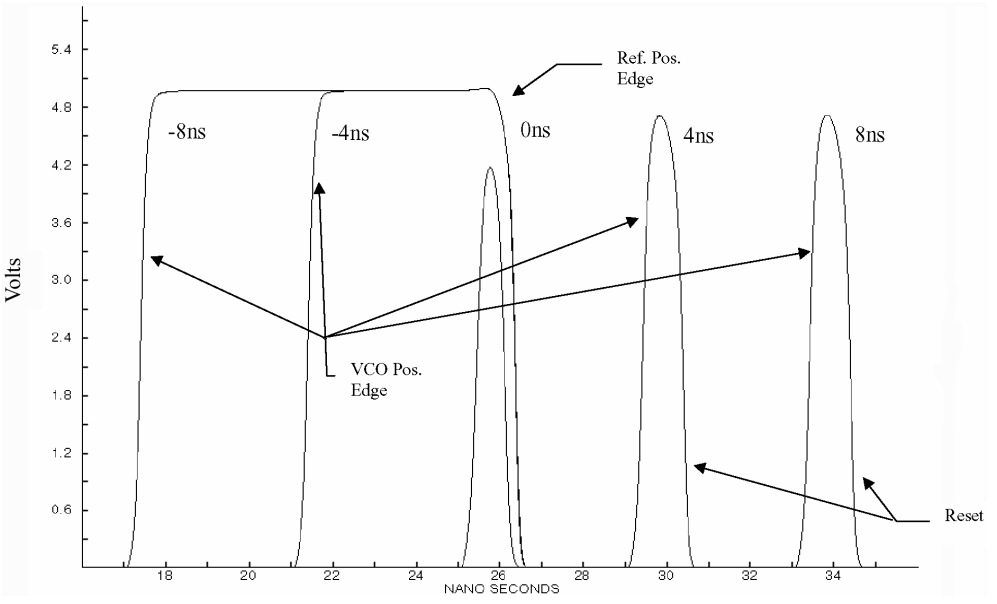


Figure 5.32 Down outputs versus delay in VCO phase.

sloped VCO tune curve, increasing the tune voltage moves the falling up edge from the far right- to the left-hand side of the page and toward the positive reference edge at the simulation time of 25 ns. The time period gets smaller so frequency increases.

Figure 5.32 shows the down output for the variation of the delay of the VCO with respect to the reference of −8 to 8 ns in 4-ns steps. The y-axis is voltage and the x-axis is simulation time. For negative phase errors, the positive edge of the VCO determines the rising edge, and the positive edge of the reference determines the falling edge. For positive phase errors of 0 ns, 4 ns, and 8 ns, the down signal has a minimum pulse of 1 ns with the positive edge following the rising edge of the VCO and centered at simulation times of 26 ns, 30 ns, and 34 ns. This figure shows that, for a positive-sloped VCO tune curve, decreasing the tune voltage moves the rising VCO edge from the far left- to the right-hand side of the page and toward the positive reference edge at the simulation time of 25 ns. The time period gets larger, so frequency decreases.

Figure 5.33 shows the average of the up output voltage waveform minus the average of the down output voltage waveform versus VCO delay. After 0.3 μs of an RC-type time response, the averages have reached a steady-state dc voltage. The average value of the last 100 ns of this voltage is plotted against the delay value of the VCO to produce a phase transfer function. Figure 5.34 plots the previous average dc voltage after 0.3 μs in Figure 5.33 and an additional ±18-ns delay points versus the delay of the VCO. This figure shows a linear transfer function going through zero phase error for the phase detector.

Calculations of the phase detector gain (K_d V/rad) are made from the slope of the phase detector transfer curve in Figure 5.34. The denominator of the gain is $2 \times \pi \times 2$ periods (one reference period = 20 ns) in the x-axis. The numerator is 5V minus −5V in the y-axis. Dividing the numerator by the denominator computes a gain of 0.79 V/rad.

Finally, let's summarize what has been found from the above analysis. First, there is always a pulse coming out of both outputs of the detector from a logic

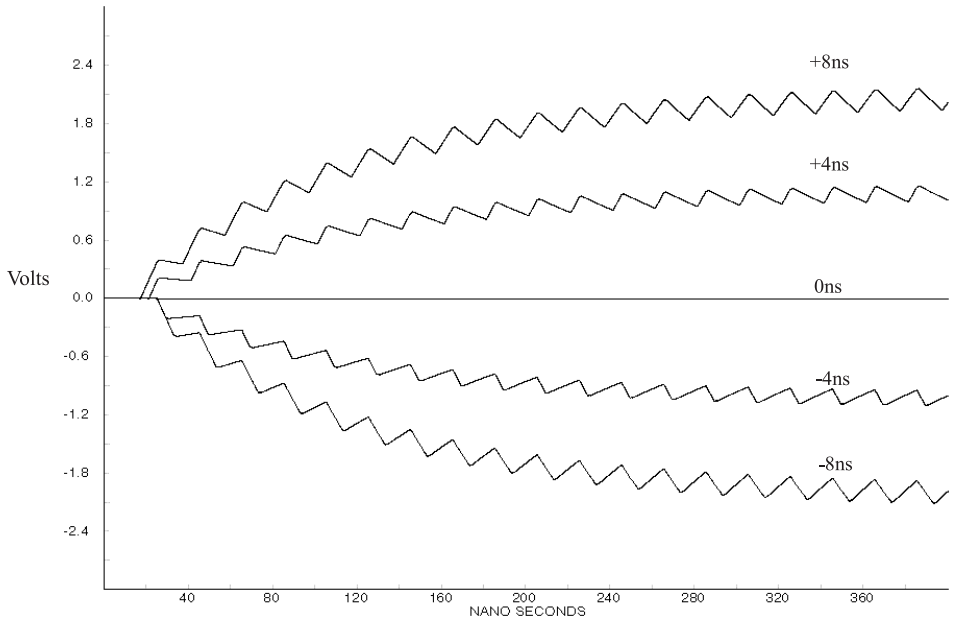


Figure 5.33 Average of the up minus the down waveform versus VCO delay.

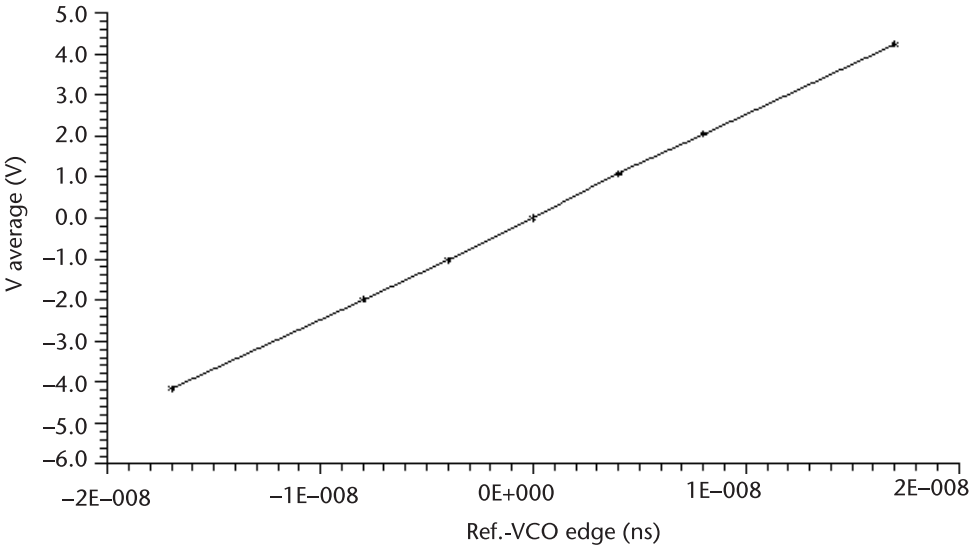


Figure 5.34 Phase transfer function for the phase/frequency detector.

viewpoint. This assumes no loading effects. There is no evidence of a dead zone because pulses are always present at the outputs, and Figure 5.34 shows a linear response around the 0° phase point where the dead zone should appear.

Phase Detector and Loop-Compensation Interface

Earlier we mentioned that loading effects could cause the minimum pulses to be eliminated. Consequently, let's look at loading effects on the phase/frequency detector to see if they cause pulses to be eliminated and a dead zone in the phase detector transfer function. The study of this interface consists of developing a PSPICE model, studying the stored charge on the loop-compensation capacitors, varying the delay between source inputs to vary phase relationship, varying capacitive loading, and computing the phase detector transfer function.

Let's look at the model for the phase/frequency detector and loop-compensation interface. To stay within the parameters of the evaluation version of PSPICE and to speed up calculations, an equivalent ECL output circuit is used and a 2.5-MHz reference frequency is used. The logic of the phase/frequency detector is replaced by voltage sources with a variable delay relationship. Figure 5.35 shows a PSPICE model schematic of the phase/frequency detector and loop-filter combination.

An active lowpass filter is used to model the effects of the loop compensation and also shows the circuitry used to measure the phase transfer function for the phase/frequency detector [6]. The included CD has a PSPICE netlist for studying the loading effects of the loop compensation on the outputs of the phase/frequency detector.

With this circuit, the mechanism that stores the phase error in the loop compensation can be studied, and in Section 5.1.7.4 the dead zone in the phase transfer function will be studied. First, Figure 5.36 shows charge being stored on each capacitor with the output waveform from the phase/frequency detector. Each pulse

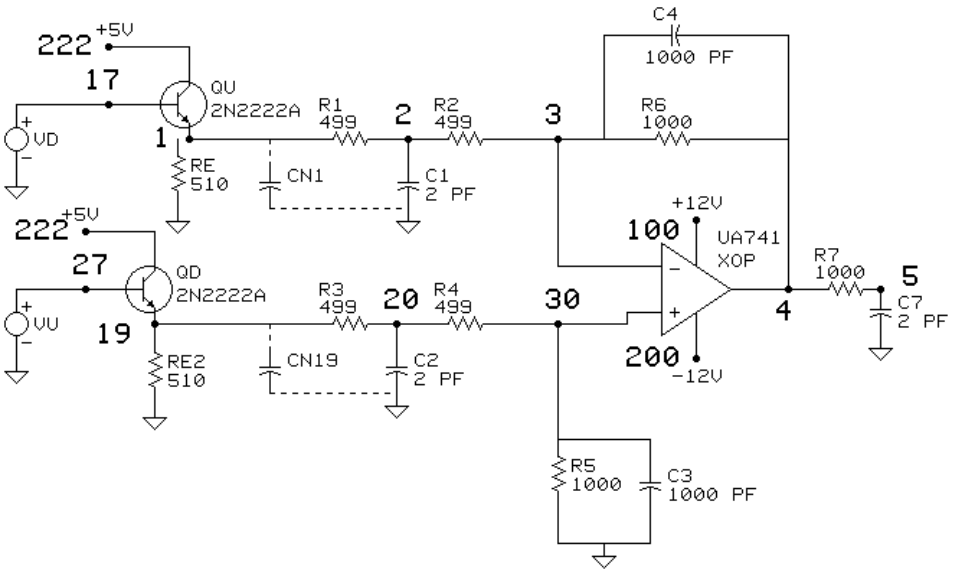


Figure 5.35 PSPICE model of phase/frequency detector and loop-compensation interface.

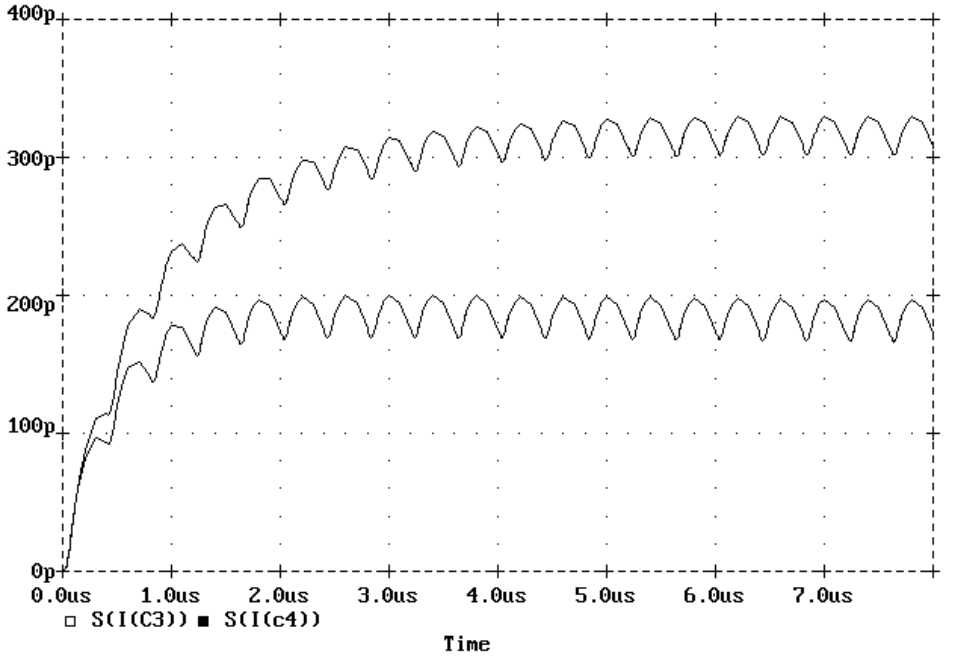


Figure 5.36 Charge stored on feedback and input capacitors in a differential filter.

out of the phase/frequency detector is integrated and stored on the capacitors with each phase comparison. Since the pulse width is a measure of the amount of error, the error is stored in the capacitors.

Figures 5.37 and 5.38 show four positive and three negative averaged-output voltage waveforms versus phase that are created for an ECL phase detector. The

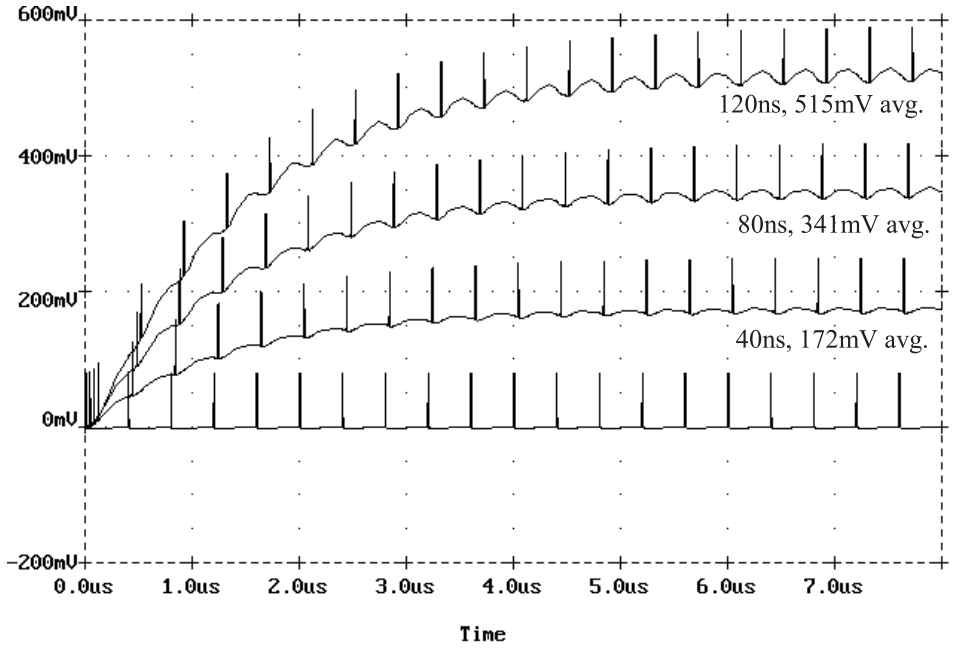


Figure 5.37 For positive delays, averaged output voltage versus phase created from an ECL phase detector.

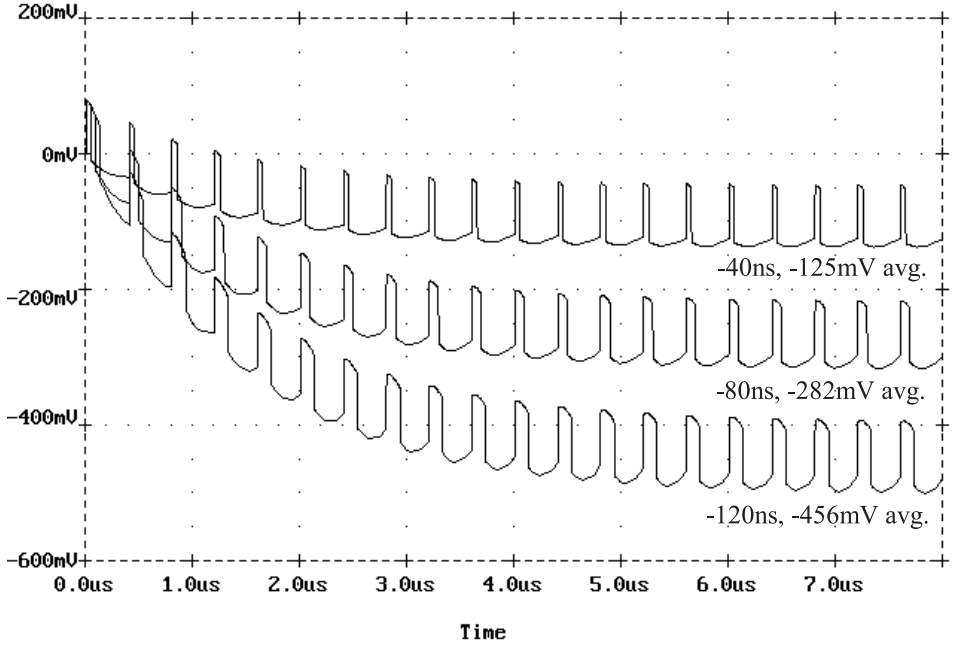


Figure 5.38 For negative delays, averaged output voltage versus phase created from an ECL phase detector.

average voltages of the last 2 ms are used to generate the phase detector transfer function curve. The even voltage spacing shows that a linear transfer function curve will be plotted. Consequently, we can use these plots to study the dead-zone effect on the phase detector transfer function curve.

5.1.7.4 Distortion Zone

The fifth condition of the phase/frequency detector, which has 0° phase difference between the inputs, causes a race condition in the IC. This race condition causes an undetermined state in the logic of the phase detector. In this condition, the output of the detector is sensitive to circuit-loading effects that can produce a nonlinearity in the phase-versus-output-voltage transfer function of the phase detector. This nonlinearity produces higher reference sidebands, loop instability, longer loop settling time, and higher phase noise.

The race condition depends on the rise and fall time and the propagation time of the IC. Consequently, the width of the nonlinear distortion zone depends on the rise and fall time and the propagation time of the IC. Rise and fall times and propagation times decrease with higher-speed digital logic families. Consequently, a high-speed phase detector (MC12040 ECL) has a smaller dead zone than a lower-speed phase detector (MC4044 TTL) [6].

Let's study the effects of loading on the phase detector transfer function by varying the output capacitance. Figure 5.39 shows output voltage variation with capacitive loading on the output level at a constant delay of 10 ns for a 400 ns

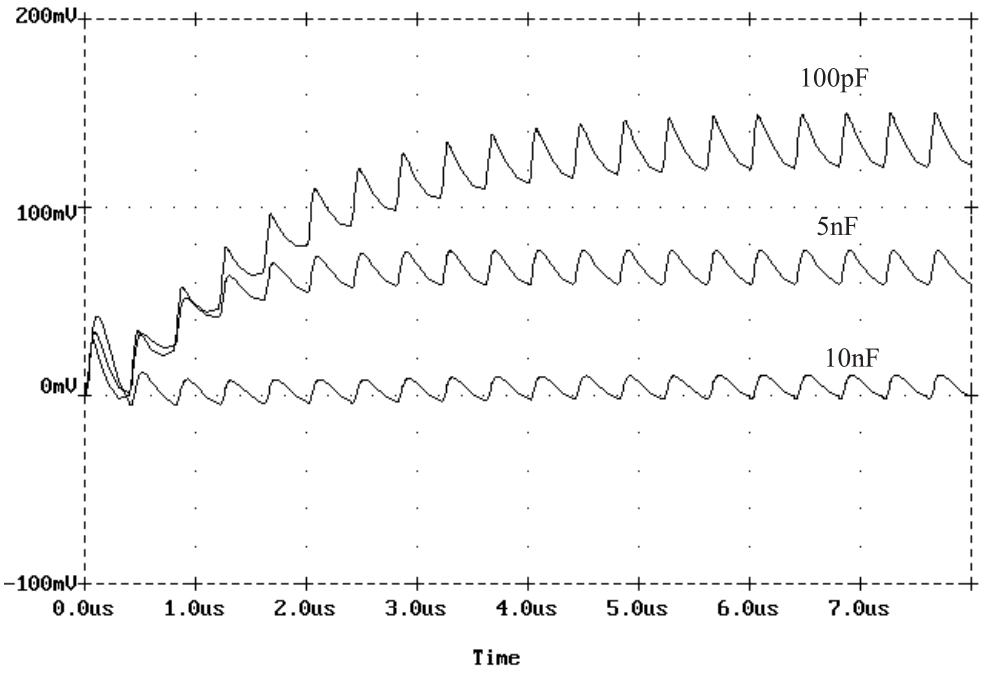


Figure 5.39 Variation of averaged phase detector output voltage for constant delay versus capacitive loading.

reference period. The reduction in output level with increasing load capacitance shows an enhancement of the dead-zone problem.

Next, the phase detector transfer function curve is calculated with 10-*nF* capacitive loading. Figure 5.40 shows the resulting curve, which shows the dead-zone effect on the phase detector transfer function with the output capacitively loaded.

Finally, there are some application and design considerations in using phase/frequency detectors. First, Figure 5.41 shows another form of the three-state phase/frequency detector, which uses D flip-flops [2]. The input reference R_{in} connects to the "clock" input of the top flip-flop. The VCO input connects to the "clock" input of the bottom flip-flop. If R_{in} precedes VCO_{in}, then the data input is logic one when the clock rises, the top flip-flop latches a one, and the output up is asserted. When the VCO edge occurs, the flip-flops are cleared. Similarly, if VCO_{in} precedes R_{in}, the flip-flop latches a one, and the output down is asserted. When the R_{in} edge occurs, the flip-flops are again cleared. The flip-flops are usually a master-slave dynamic topology. They have two transmission gates and two inverters to lower the device count and reduce silicon-area requirements. The conventional CMOS circuit uses an input pass-transistor structure, which gives a longer setup time than hold time, effectively introducing a time offset between R_{in} and VCO_{in}. In addition, the setup and hold timing for the reset signal can cause a dead zone or, in some cases, oscillation. Consequently, the RS flip-flop connection is preferred in most applications.

Next, the phase/frequency detector is an edge-sensitive device. Consequently, under noisy conditions (multiple clocks on rising edges of the input from the reference oscillator) can cause false pulse-width outputs that increase the error in the loop and can eventually cause loss of lock. Laboratory measurements have shown that at –20-dB spurious-to-signal ratio, the phase/frequency detector output produces enough false edges to cause the loop to lose lock. For an exclusive-OR

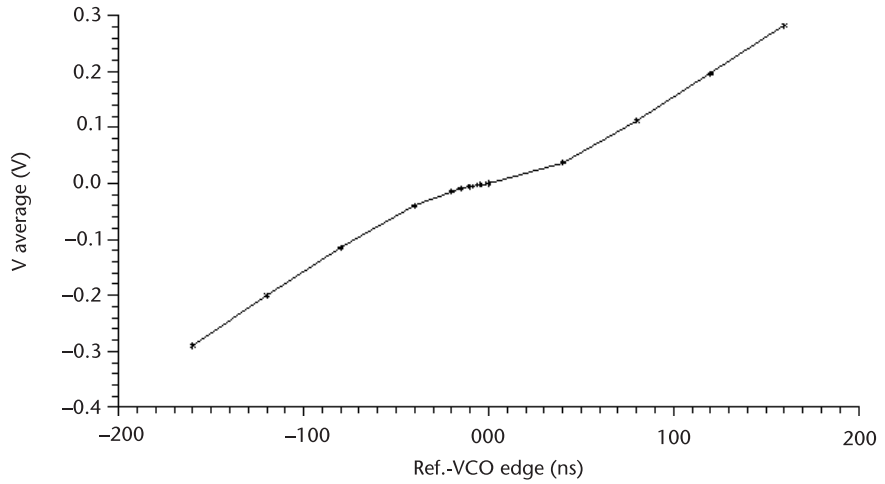


Figure 5.40 Dead-zone effect in phase detector transfer function from capacitive loading.

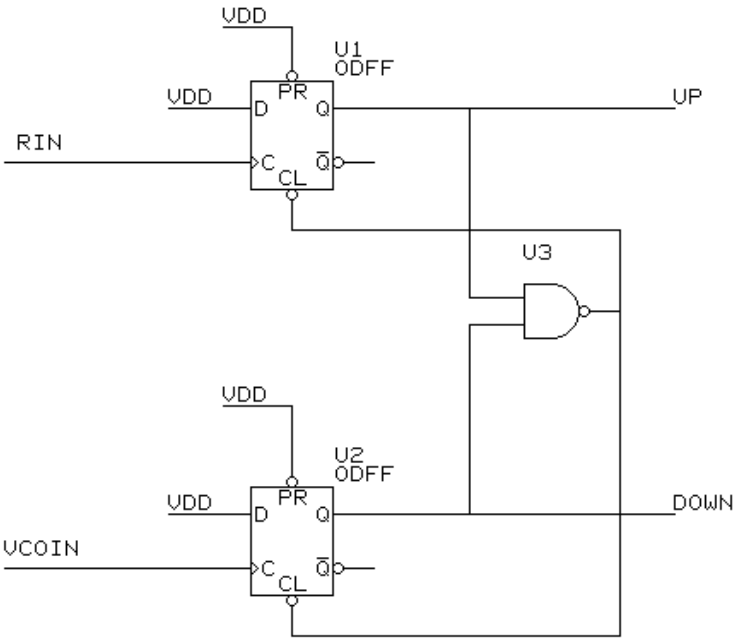


Figure 5.41 Three-state phase/frequency detector with D flip-flops.

phase detector (mixer or multiplier) that is not edge dependent, laboratory measurements have shown that a 0-dB spurious-to-signal ratio into these detectors produces enough error to cause the loop to lose lock. This is a 20-dB improvement. The draw back for the exclusive-OR detector is that frequency acquisition aids are needed initially to lock and maintain lock. Consequently, for most applications, the phase/frequency detector is preferred.

5.1.8 Conclusion

To summarize, modeling of the phase/frequency detector showed that the dead-zone problem is caused by capacitive loading of the output. Improved buffering of the output or increasing the driving capability of the gates can help alleviate this problem. In addition, simulations show that a pulse is always present at the output of the phase/frequency detector.

5.2 Lock Detection

Many systems use a lock-detection circuit to reset the system. This is a disastrous change to the operation of most systems. In a PLL, a reset can start the loop operating at a very low frequency (or with no output), which then acquires lock at the normally much higher output operating frequency. Consequently, a small phase shift in the PLL that would marginally affect the system can cause a huge disruption in the operation of the system if a reset occurs.

The key to lock detection is to alarm on behavior that shows the PLL is broken. A PLL can respond to a disturbance in a manner that makes it look like it is broken. Consequently, the best lock-detection schemes will allow some time for the loop to respond to a disturbance and recover. Otherwise, false alarms may occur. Quadrature phase detector, time-window edge comparison, tune-voltage window comparator, and cycle-slip detection are the most common methods for lock detection.

5.2.1 Quadrature Lock Detection

The quadrature phase detector technique as shown in Figure 5.42 uses two mixers (or analog multipliers) to compare the input reference with the in phase and quadrature phase of the fed-back VCO output. The in-phase comparison has a sin θ_e output relationship with phase error, and the quadrature comparison has a cos θ_e output relationship with phase error. The in-phase comparison is used to lock the loop because sin $\theta_e \approx 0$, and the quadrature comparison is used to detect lock because cos $\theta_e \approx 1$. The quadrature detector output is followed by a lowpass filter and a threshold comparator. A dc level above the threshold indicates that the circuit is locked. An unlocked loop produces a beat-note frequency at the output of the quadrature comparator that is lowpass-filtered to 0-V input to the threshold comparator. Without the proper filter, the lock-detection signal will flicker on and off because of noise, which will give false indications of lock or loss of lock. Too much filtering will cause an excessive delay in the lock or unlock signal. Consequently, the design of the output-smoothing filter is a vital part of a practical lock indicator. A compromise in the amount of smoothing is required. R. C. Tausworthe has performed a detailed analysis of the problem and has produced design curves [7, p. 88; 8, 9].

5.2.2 Tune-Voltage Window Comparator

A PLL can lose lock when the input frequency is to high, which pegs the tune voltage close to the supply rail or when the input frequency is too low, which pegs

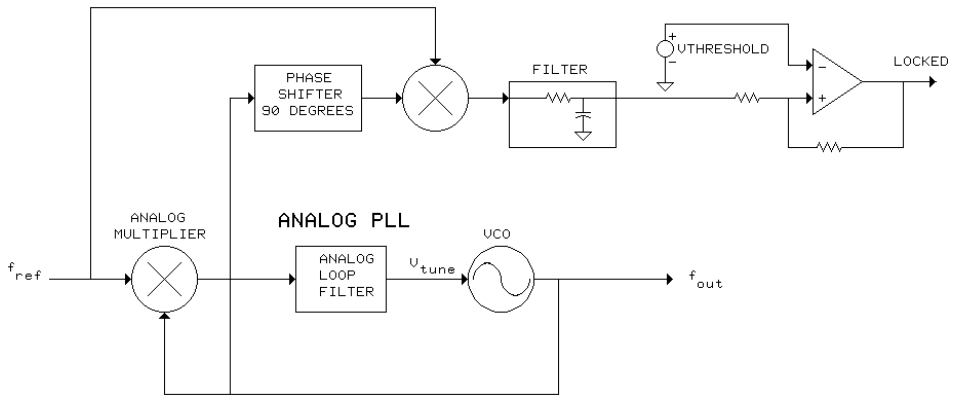


Figure 5.42 Block diagram of quadrature lock detection.

the tune voltage close to the ground supply rail. A tune-voltage window comparator, as shown in Figure 5.43, uses these two voltages to detect the unlocked condition. A tune-voltage window comparator monitors the tune line voltage with a high voltage threshold and a low voltage threshold. Crossing either the high or the low threshold causes an out-of-lock condition. Tune-voltage window comparison requires several operational amplifiers to achieve. Consequently, the size, power consumption, and threshold variation with process makes it impractical for integrated circuit design.

5.2.3 Time-Window Edge Comparison

The time-window edge comparison detector, as shown in Figure 5.44, uses an exclusive-OR gate to combine the up and down pulses out of the phase detector. Following the exclusive-OR gate with a lowpass filter rejects the narrow up and down pulses and takes the dc average of the wider up and down pulses that occur when the loop is unlocked. Monitoring the dc voltage at the output of the lowpass filter with a comparator sets a dc trip point when the loop is determined to be out of lock. Crossing the trip point to higher voltages sets the comparator to a high value (unlocked), and crossing the trip point to lower voltages sets the comparator to a low value (locked).

This detection scheme has several disadvantages. First, the time-window edge comparison (1 to 2 ns) will vary with process, which can cause false unlock conditions. The loop can have a constant phase offset that is out of the time window and will indicate a false unlock condition. A larger capacitor value is needed to increase the time window, which makes it consume area and renders it less integratable. An external disturbance can modulate the PLL so that the detector switches between the locked and unlocked condition. Even worse, the loop control logic may switch bandwidths when the loop is locked or unlocked. Switching bandwidths can disturb the loop enough that the time-window edge-comparison detector toggles, which can cause an oscillation condition to occur.

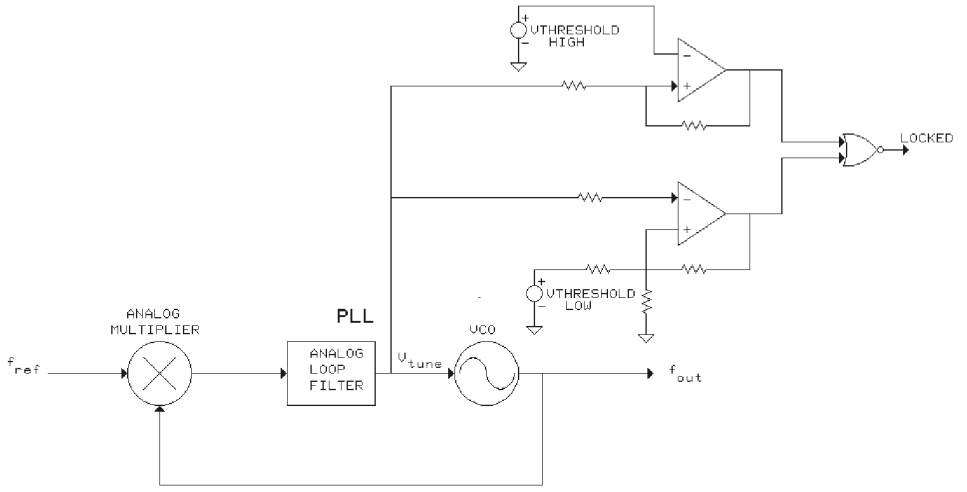


Figure 5.43 Tune-voltage window comparator.

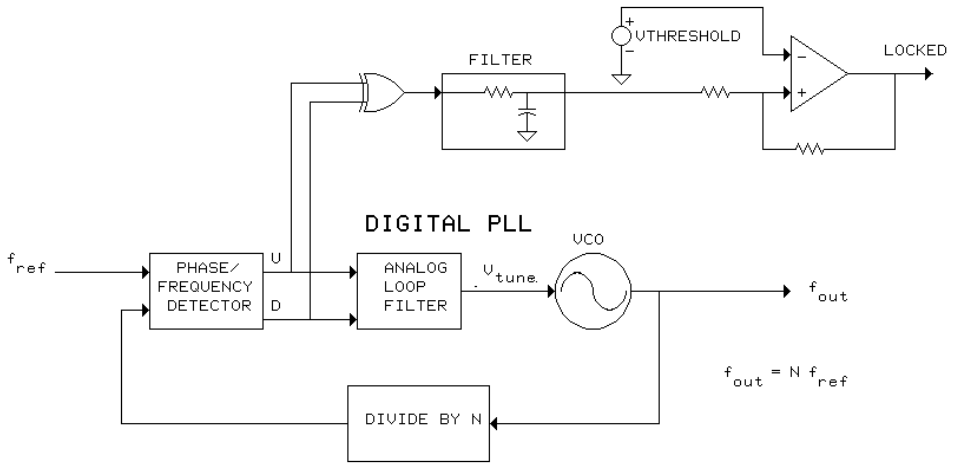


Figure 5.44 Time-window edge comparison.

In summary, the time-window-edge-comparison technique is too sensitive and gives an excessive number of unlocked conditions. Special care must be taken for this to be a successful implementation.

5.2.4 Cycle-Slip Detector

The cycle-slip detector detects frequency differences between its two input clocks that remain different for a time period greater than the inverse of the frequency difference. The detector generates a pulse when the phase/frequency detector output pulse width rolls over from its largest pulse width to its narrowest pulse width. Figure 5.45 shows the schematic for the cycle-slip detector [10]. The cycle-slip detector circuit consists of a phase/frequency detector, two cycle-slip detectors, and a final AND gate. The inputs to the circuit are the divided-down VCO waveform and the reference. The outputs of the phase/frequency detector are up pulses and down pulses. The outputs of the cycle-slip detector are active, low, up cycle slips and down cycle slips. A logical AND of the active, low, up cycle slips and down cycle slips produces an active, low cycle-slip detector output. This output is used to reset a counter and count reference clocks between cycle slips. For example, if 16 reference clocks are counted after a cycle slip, then the loop is set to the locked state by latching the carry out of the counter and disabling any further counts. Figure 5.46 gives an example connection for counting reference clocks after a cycle slip.

The cycle-slip detector does not detect loss of the reference clock or VCO feedback clock. The cycle-slip detector requires that both input clock signals be present. With one clock missing, the output of the cycle-slip detector stays a constant high, which indicates a locked condition to the following circuitry.

Figure 5.47 shows the response of the lock detector with a ramped VCO from below the lock condition to above the lock condition. The x-axis value is 0.1 ns, which makes the minor divisions equal to 5 ns. The VCO ramps from 250 to 400 MHz with the reference frequency set at 300 MHz. The left-hand side of

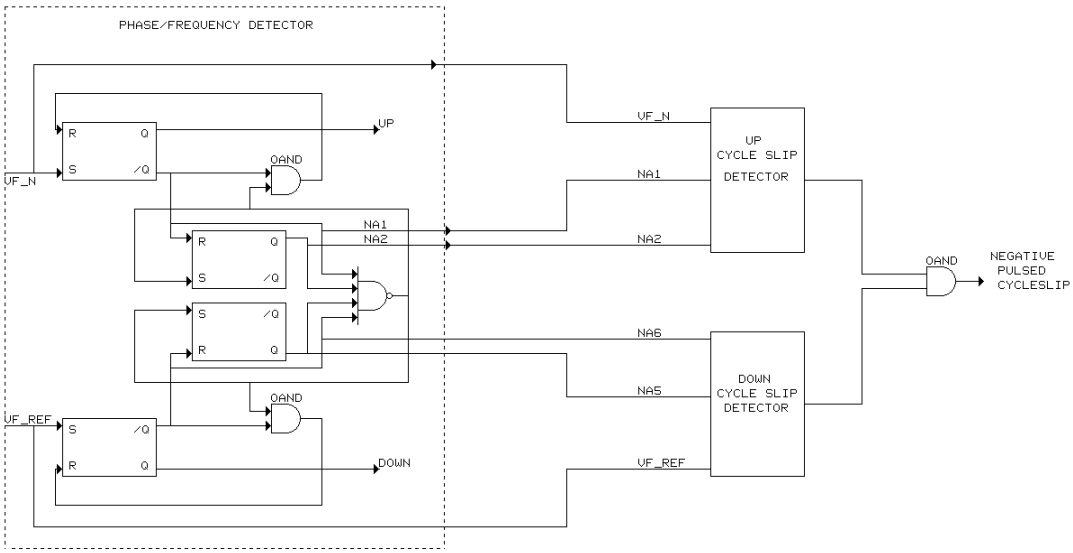


Figure 5.45 Schematic of cycle-slip detector.

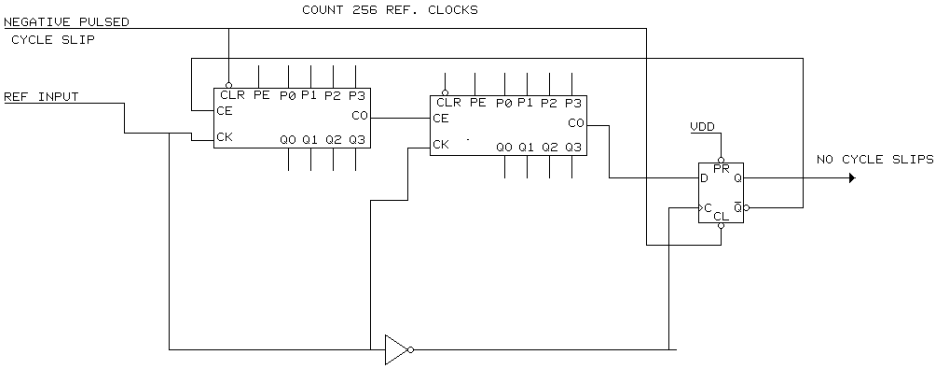


Figure 5.46 Schematic for cycle-slip counter to create lock-detection output signal.

Figure 5.44 shows that the up output of the phase/frequency detector is a pulse-width-modulated signal for a VCO frequency greater than the reference frequency. The down output of the phase/frequency detector has constant narrow pulses, which indicates no response. On the far left-hand side, the 50-MHz difference in input frequency causes a 50-MHz beat note in the pulse-width modulation output of the phase/frequency detector. Using the rising edge of the VCO as a sample clock to the reference waveform outlines a 50-MHz-period beat note. Using the rising edge to rising edge of the VCO waveform as a cycle bin and reflecting these bins on the pulse-width-modulated waveform output (VUP) of the phase/frequency shows a cycle bin where no edges occur. This is a cycle-slip up pulse condition. Sampling this nonresponse latches the cycle slip and causes one pulse per beat note.

The right-hand side of Figure 5.47 shows that the down output of the phase/frequency detector is a pulse-width-modulated signal for a VCO frequency greater

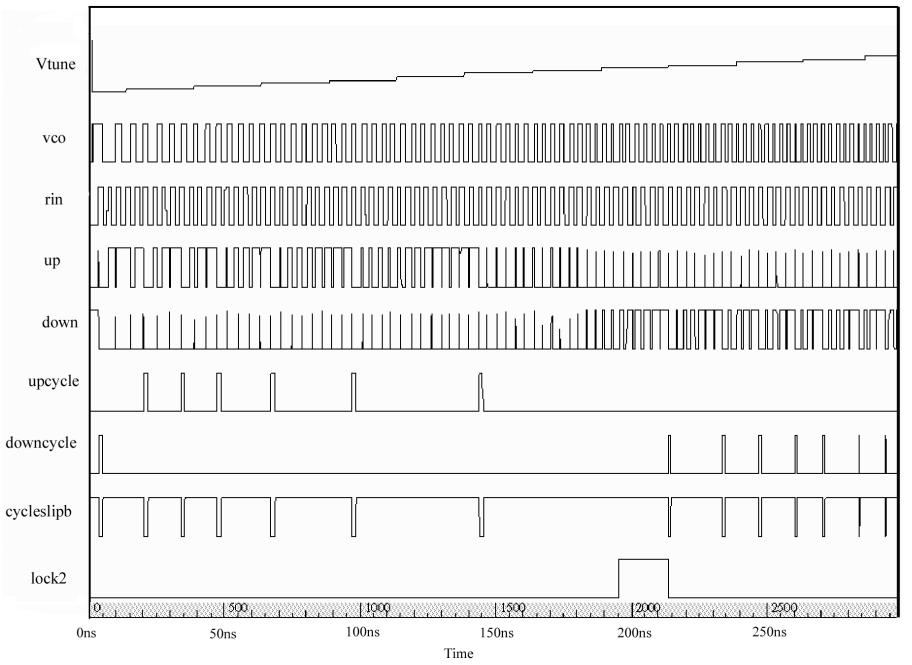


Figure 5.47 Response of the lock detector with a ramped VCO from below the lock condition to above the lock condition.

than the reference frequency. The up output of the phase/frequency detector has constant narrow pulses, which indicates no response. A cycle bin of the down output where no edges occur causes a cycle-slip down pulse to occur. The beat note on the high-frequency side does not represent the frequency difference because of aliasing in the sampling. In the middle of the figure, VCO and reference input frequencies are equal. The up and down cycles have no response. The bottom waveform shows the response of a simple 4-bit counter to generate a lock-detect signal. The wait time for the counter is set to 16. After 16 reference periods, the carry out of the counter goes high, and the counter is disabled until the next cycle slip occurs.

5.2.5 Cycle-Slip Detector Versus Time-Window Comparator

Another example compares the performances of a time-window comparator and a cycle-slip detector. The PLL has a 10-MHz input frequency and multiplies the input frequency by 24. The control system has a natural frequency of 300 kHz and a damping factor of 0.3.

Figure 5.48 shows a normal frequency and phase response of a PLL to a 1-MHz frequency step in the reference frequency. A time-window comparator set to ±10° would give an out-of-lock indication because the 10° threshold would have been crossed. In addition, the time-window comparator would toggle several times because the ±10° threshold would have been crossed several times. The cycle-slip detector would not alarm because 360° phase shift did not accumulate.

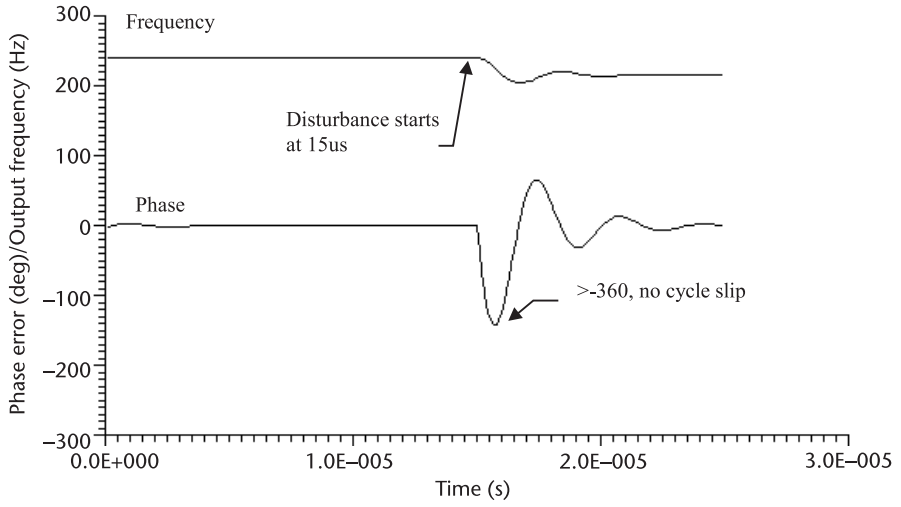


Figure 5.48 Frequency and phase-error response of a PLL to a 1-MHz frequency step in the reference frequency.

Figure 5.49 shows a normal frequency and phase response of a PLL to a 2.5-MHz frequency step in the reference frequency. Here, the cycle-slip detector is on the verge of alarm. Consequently, this figure shows that the cycle-slip detector alarms with frequency steps greater than 2.5 MHz. Figure 5.50 shows a normal frequency and phase response of a PLL to a 50-ns phase step. Here, the time-window comparator would again have multiple alarms, but the cycle-slip-based lock detector would not alarm.

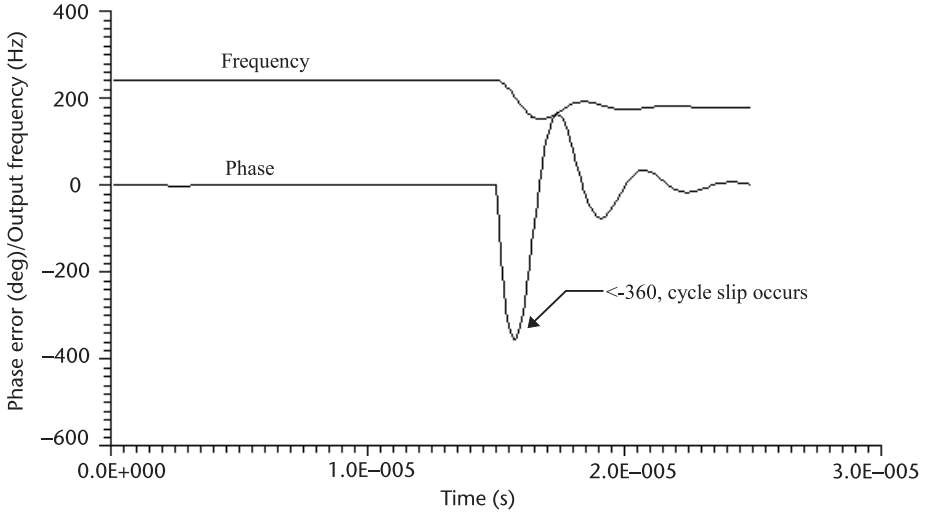


Figure 5.49 Frequency and phase-error response of a PLL to a 2.5-MHz frequency step in the reference frequency.

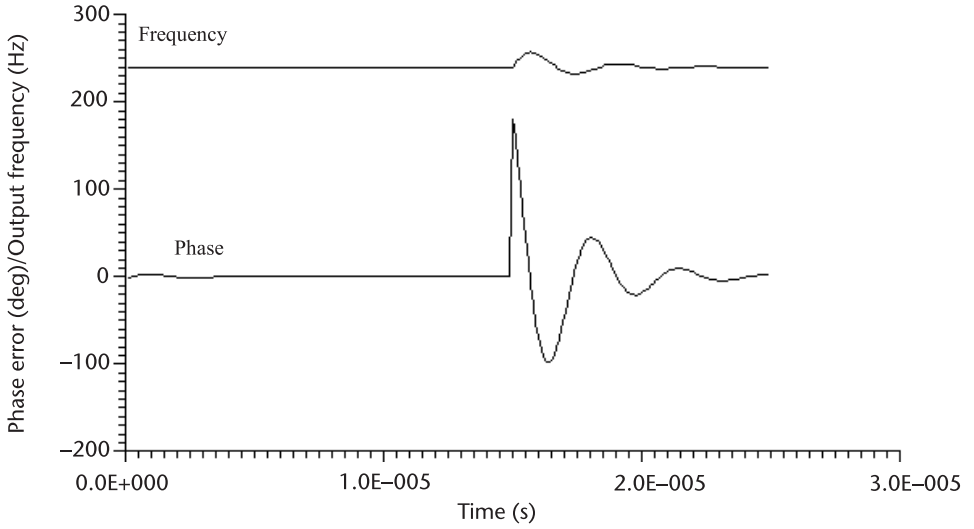


Figure 5.50 Frequency and phase-error response of a PLL to a 50-ns phase step.

Figure 5.51 shows the toggling of a window phase comparator versus solid cycle-slip lock detectors. A PLL with 16-MHz input reference frequency and 128-MHz output frequency shows how the lock detectors operate. The x-axis has the units of nanoseconds. The top waveform shows the tune voltage to the VCO, which shows that the loop locks after 2 μs. The second waveform shows the time-window lock detector. It starts toggling at 1.7 μs and continues to toggle. The bottom waveform shows the response of the cycle-slip detector with a state machine that waits 32 reference clock periods after no cycle slips occur. The cycle-slip detector detects lock at 5.3 μs and does not toggle after detection.

5.3 Acquisition Aids

If you cannot use a phase/frequency detector, then you will need an acquisition aid. One circumstance occurs for clock-recovery applications. In clock recovery,

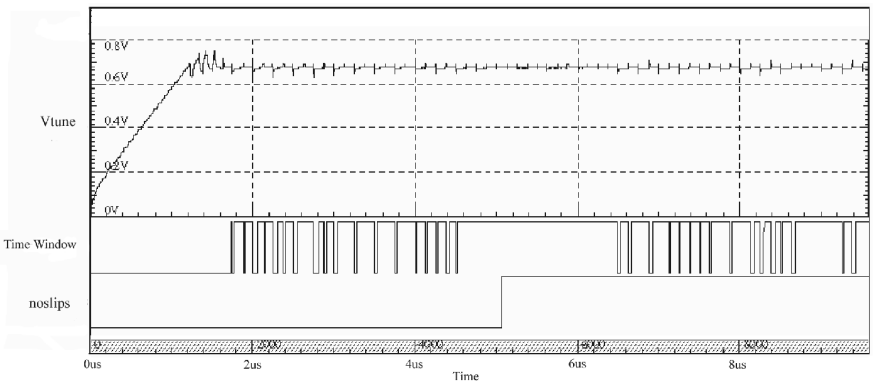


Figure 5.51 PLL transient response that compares a time-window and cycle-slip lock detectors.

multiple false locking conditions and missing clock edges occur. These conditions confuse the phase/frequency detector, and an exclusive-OR gate detector is generally used. Another circumstance occurs in frequency-generation applications. After the other loops are locked, the VCO in the translation loop is tuned to the lock condition. In only a narrow portion of the VCO tune range does the phase detector have an input. Otherwise, there is no input to the phase detector. Consequently, an acquisition aid must be used to tune the VCO until the phase detector gets a response.

In this section, we will study acquisition with an open-loop sweep and a closed-loop sweep and discriminator-aided acquisition. So, let's look at these acquisition strategies in more detail.

5.3.1 Open-Loop Sweep

As shown in Figure 5.52, a sweep can be applied to a type 2 loop in the simple manner of switching a current source in and out of the circuit. When the current source is connected, the voltage sweeps up, and when the current source is disconnected and there is no lock, the voltage sweeps down from the discharging of the capacitor. Otherwise, a separate sawtooth generator must be added to sweep the voltage directly into the VCO [7, pp. 79–87; 11, pp. 227–234; 12].

The phase detector has a maximum output of K_d rad. The output from the phase detector produces a current of K_d rad/R_1 into C in an active filter. This current causes a voltage ramp of slope K_d rad/R_1C. The voltage ramp on the VCO tune line produces a frequency change with a slope that is described by (5.18):

$$K_d K_v/(R_1 C) = \omega_n^2 \tag{5.18}$$

The frequency ramp in (5.18) is related to the natural frequency ω_n from servo mechanical definitions. Ramping the frequency faster will keep the loop unlocked. For a short time, the frequency can move faster due to the zero R_2C in the filter.

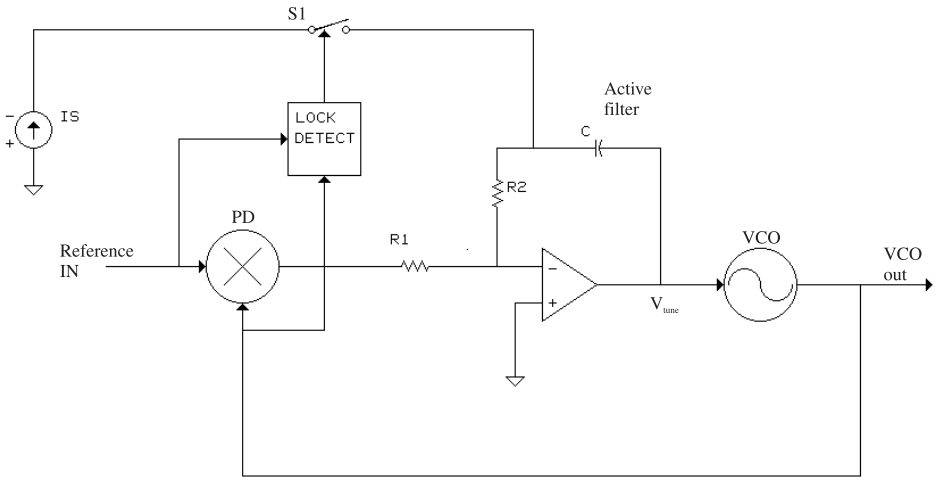


Figure 5.52 Open-loop sweep circuit for lock-acquisition aid.

A sudden change at the input to the active filter will be multiplied by R_2/R_1 and immediately appear at the filter output; however, the sustained ramp cannot move faster than (5.18). A lowpass pole from placing R across C reduces the current into C and the slope. In addition, a loop that cannot hold lock on an input signal will not be able to acquire lock on that input signal. Consequently, the maximum hold lock of ω_n^2 for a swept-input frequency applies to the acquisition limits. The 100% probability of acquiring lock with a swept input depends on the sweep rate and the amount of noise.

The sweep frequency circuit must be shut off once lock has been achieved. Shutting off the sweep circuit prevents loss of lock and reduces reference sidebands from loop-error corrections. In a closed loop, the tracking of the loop allows some leeway in time before turning off the sweeper; however, an open-loop sweep requires a quick detection of frequency agreement and a rapid shut off of the sweep.

5.3.2 Closed-Loop Sweep

One method for closed-loop sweep requires a positive-feedback circuit. Adding low-frequency positive feedback, as shown in Figure 5.53, causes the loop filter to oscillate, which sweeps the VCO frequency. When the loop locks, the large amount of negative feedback dominates the local positive feedback, which suppresses the oscillation and allows the loop to track normally. The feedback network can be a Wien bridge, and the limits of the sweep are set by the supply limits of the operational amplifier.

5.3.3 Discriminator Aided

Figure 5.54 shows a discriminator-aided frequency acquisition. This method has a phase detector loop and a frequency detector loop. With the loop out of lock, the frequency loop controls the VCO, and the phase loop has little effect. After locking, the phase loop has much greater dc gain than the frequency loop to

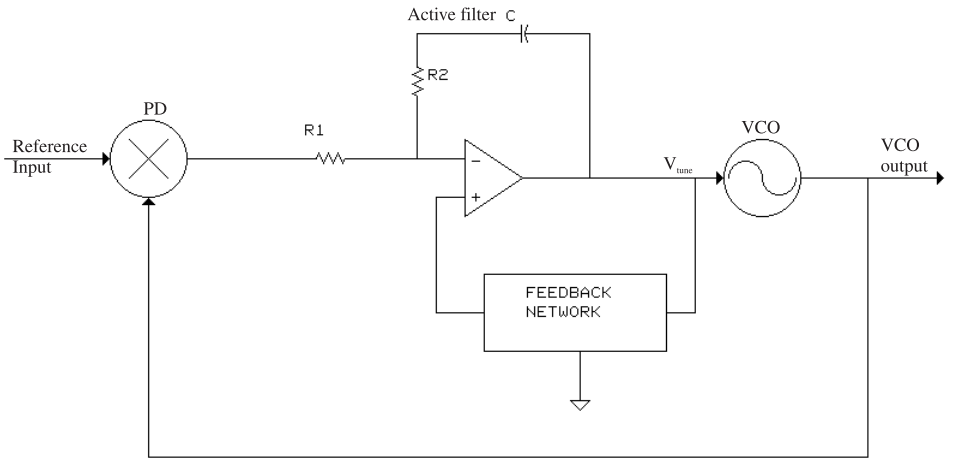


Figure 5.53 Closed-loop, low-frequency, positive-feedback sweep.

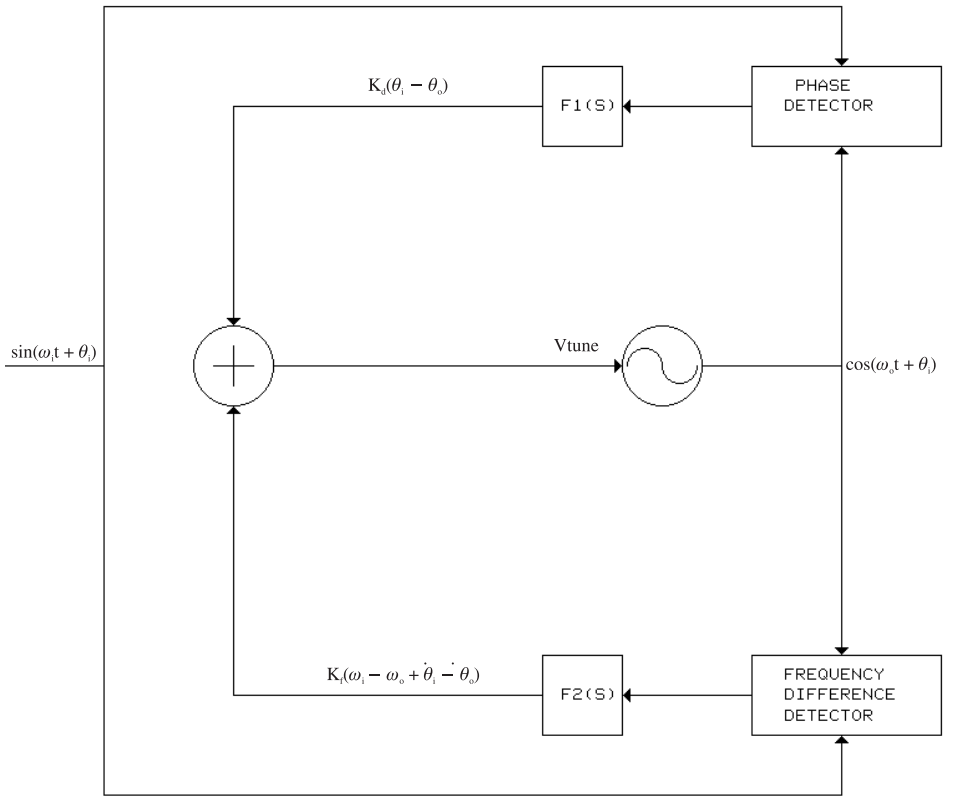


Figure 5.54 Discriminator-aided acquisition with separate phase and frequency detectors. (*From:* [7, pp. 79–87]. © 1979 Wiley Interscience. Reprinted with permission.)

dominate control of the VCO. Consequently, at lock, the discriminator can be disconnected. For a type 2 PLL, the transfer function for the frequency loop can be a type 1, which means function block $F_2(s)$ can be a simple integrator [7, pp. 79–87].

Figure 5.55 shows another discriminator-aided acquisition method. For this method, the frequency loop and phase loop share the same integrator. The response of the loop remains type 2, and the frequency path only adds to the damping factor. The frequency loop can remain connected if the relative contributions between the frequency and phase loops are adjusted to maintain the desired damping factor [7, pp. 79–87]

In a closed loop with frequency sweep activated, the coherent operations in a PLL allow locking to an input signal with low SNR. A discriminator does not distinguish between signal and noise. Consequently, for SNRs less than 6 dB, the sweep search may not successfully lock onto the input signal.

Figure 5.56 shows a frequency-difference detector (quadricorrelator). Equations in the figure describe the signal paths. The quadricorrelator mixes the input signal with an in-phase and quadrature output of the VCO to generate an in-phase and quadrature output of the frequency difference. Differentiating one signal path and mixing the two together produces a product that contains a dc component proportional to the frequency difference. Differentiating one signal path with a

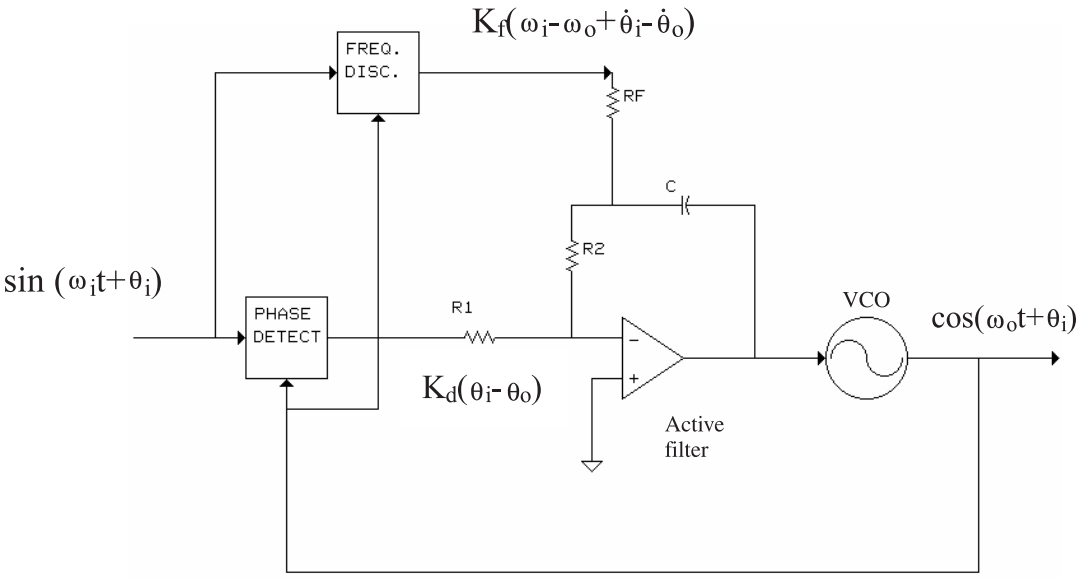


Figure 5.55 Discriminator-aided acquisition with frequency and phase loops sharing the same discriminator. (*From:* [7, pp. 79–87]. © 1979 Wiley Interscience. Reprinted with permission.)

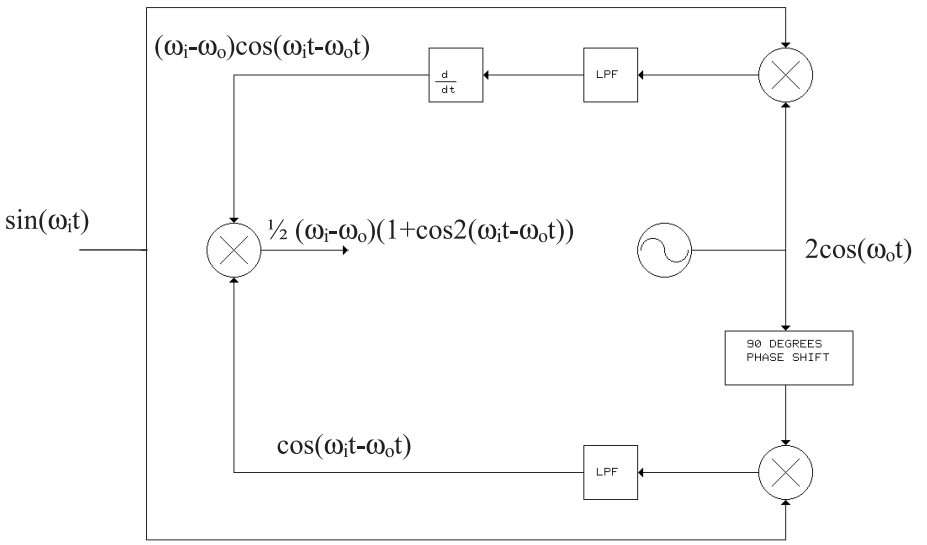


Figure 5.56 Quadricorrelator frequency-difference detector. (*From:* [7, pp. 79–87]. © 1979 Wiley Interscience. Reprinted with permission.)

highpass filter section disconnects the quadricorrelator for very small frequency differences, which allows the phase detector loop to take control of the VCO. The lowpass filters in the in-phase and quadrature signal paths suppress the intermodulation products out of the mixer and limit the operating range of the circuit. Using the in-phase signal path for the phase detector in the PLL reduces the complexity of the circuitry [7, pp. 79–87].

5.4 Charge Pumps

The charge pump in a PLL converts the differential up and down outputs of the phase/frequency detector to a single-ended, switched, positive and negative current source that charges and discharges a capacitor in order to control the VCO in a PLL. The number of its parameters makes the charge pump one of the most important circuits in a PLL (second to the VCO). The linearity of this circuit affects the stability of the loop, the amount of jitter, the amount of noise, the reference sideband levels, the phase tracking error, and the limits of the frequency operating range. The amount of peak charge pump current affects the amount of noise, the loop bandwidth, and the frequency slew rate of the PLL.

A charge pump consists of two switched-current sources driving a capacitive load as shown in Figure 5.57. The left part of Figure 5.57 shows the functional block diagram, and the right part of Figure 5.57 shows a simple implementation in CMOS. An up pulse out of the phase frequency detector turns a p channel MOSFET on to charge the capacitor in the positive voltage direction. A down pulse out of the phase/frequency detector turns an n channel MOSFET on to discharge the capacitor in the negative direction. For a pulse of width T, current I_1 deposits a charge equal to $I \times T$ on the capacitor C_p. As the phase error approaches zero, zero charge accumulates on the capacitor, and the voltage ideally remains constant [13].

Example 5.2

A phase/frequency detector drives a charge pump with a current source of 1 μa. Calculate the phase detector gain. If the charge pump has a figure of merit of 10, calculate the offset current for each current.

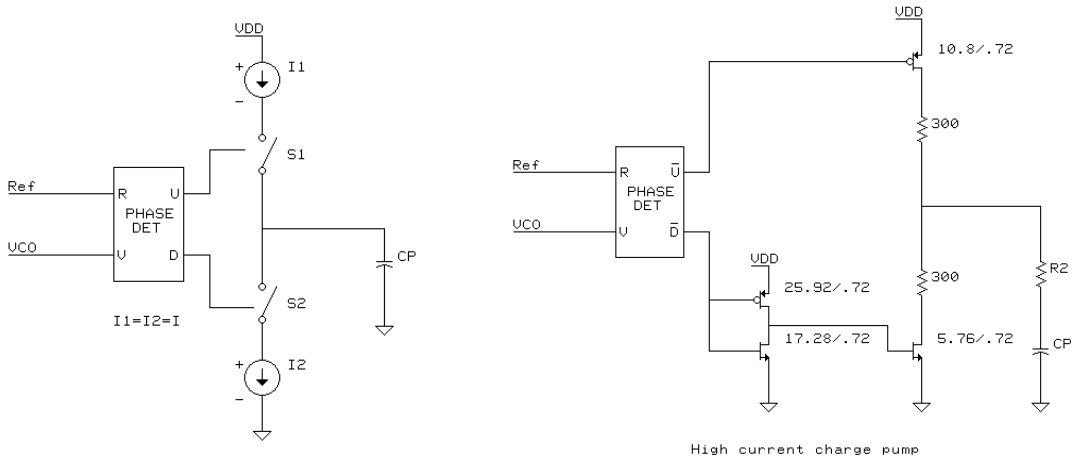


Figure 5.57 (Left) Functional diagram of phase/frequency detector with charge pump combination and (right) simple schematic of phase/frequency detector with a high-current charge pump combination.

The charge pump gain is the charge pump current divided by the range of the phase detector, which is 2π for the phase/frequency detector. Consequently, the charge pump gain is 1 μa/2π = 0.159 μa/rad. Dividing the charge pump gain 0.159 μa/rad by the phase detector figure of merit 10 computes the offset current at zero phase error to be 0.159 μa/rad/10 = 0.0159 μa.

Figure 5.58 shows a test fixture for charge pumps that helps generate the charge pump transfer function. This figure shows an ideal operational amplifier after the charge pump that processes the current out of the charge pump for testing purposes. The operational amplifier presents a high impedance load back to the charge pump output at the voltage that is set by VCPO. The high input impedance of the operational amplifier isolates the voltage source from the charge pump. Consequently, the output voltage to the charge pump can be varied from one supply rail to the next without loading down the charge pump. When switches S_1 or S_2 are closed, the current must go through the R_1 feedback resistor because of the negative feedback around the amplifier. Consequently, measuring the current in R_1 in a SPICE simulation measures the current sourced by the charge pump. Finally, the capacitor C_1 is used to attenuate high-frequency switching spikes that can occur. Figure 5.59 shows a low-current version of the charge pump where transistors are cascoded to make a better current source.

Figure 5.60 shows a differential charge pump, which is another variation. A differential charge pump can help minimize the distortion in the transfer function. In this circuit, the control from the phase detector turns on only pull-down currents. The control signals switch differential pairs $M_1 - M_2$ and $M_3 - M_4$. The pull-up currents *Ip* are always present. Consequently, if up and down controls are in the low state, a common-mode feedback circuit consisting of transistors $M_5 - M_9$ counteracts the pull-up currents to set a proper output common-mode level at

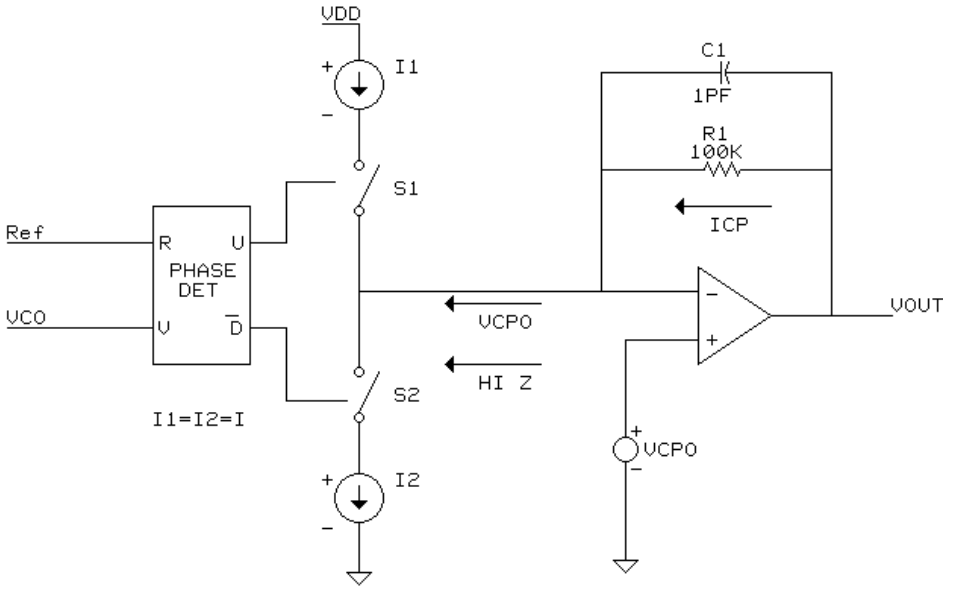


Figure 5.58 Circuit to process the output of a charge pump and generate the transfer function.

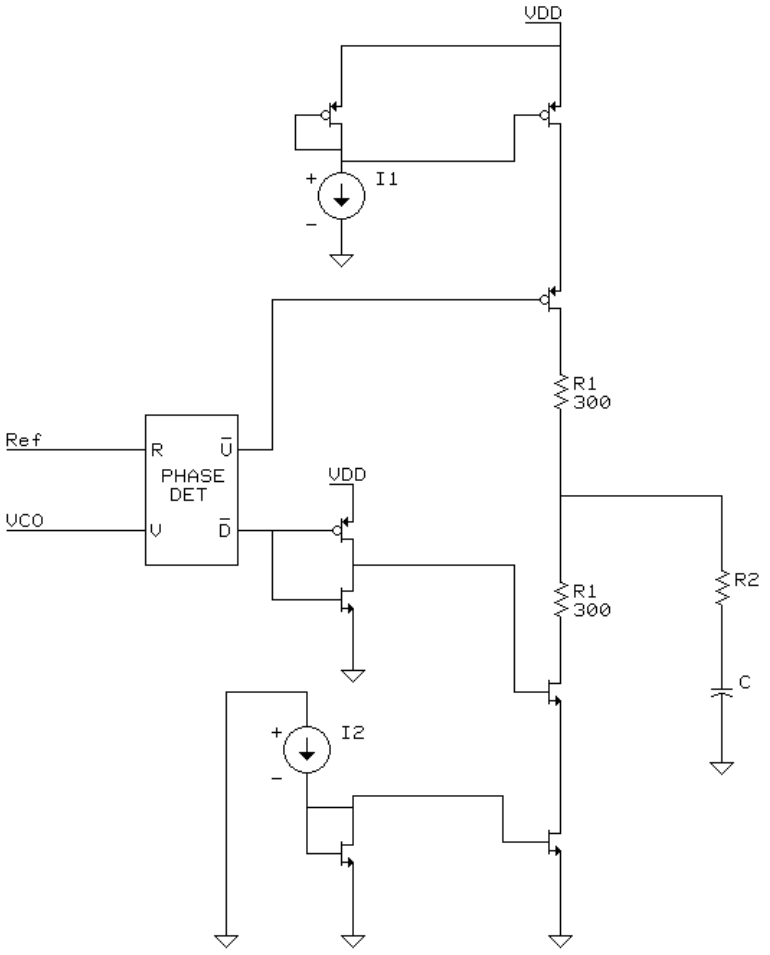


Figure 5.59 Schematic of low-current charge pump.

$V_{GS5} + V_{GS9}$. Each phase comparison momentarily disturbs the common-mode level. Consequently, care must be taken to avoid common-mode transients that can lead to differential settling components.

A dead zone can occur for a charge pump. If the output pulse widths of the phase/frequency detector are small, and there is not enough drive current or there is a high load capacitance, then the logic level will not be high enough to turn the charge pump on. This causes a low-gain time width around the zero phase point where a PLL locks. Zero phase detector gain makes the loop unlock and drift until enough error is generated to cause a correction. Consequently, the amount of jitter this causes is proportional to the time width of the dead-zone area.

Current offsets, transistor mismatches, and charge sharing can cause errors in the transfer characteristics of the charge pump. This can cause an offset and distortion in the transfer characteristics of the charge pump. An offset in the transfer characteristics of the charge pump produces a constant pulse width out of the charge pump when the loop is locked. This pulse width adds to the output jitter of the PLL.

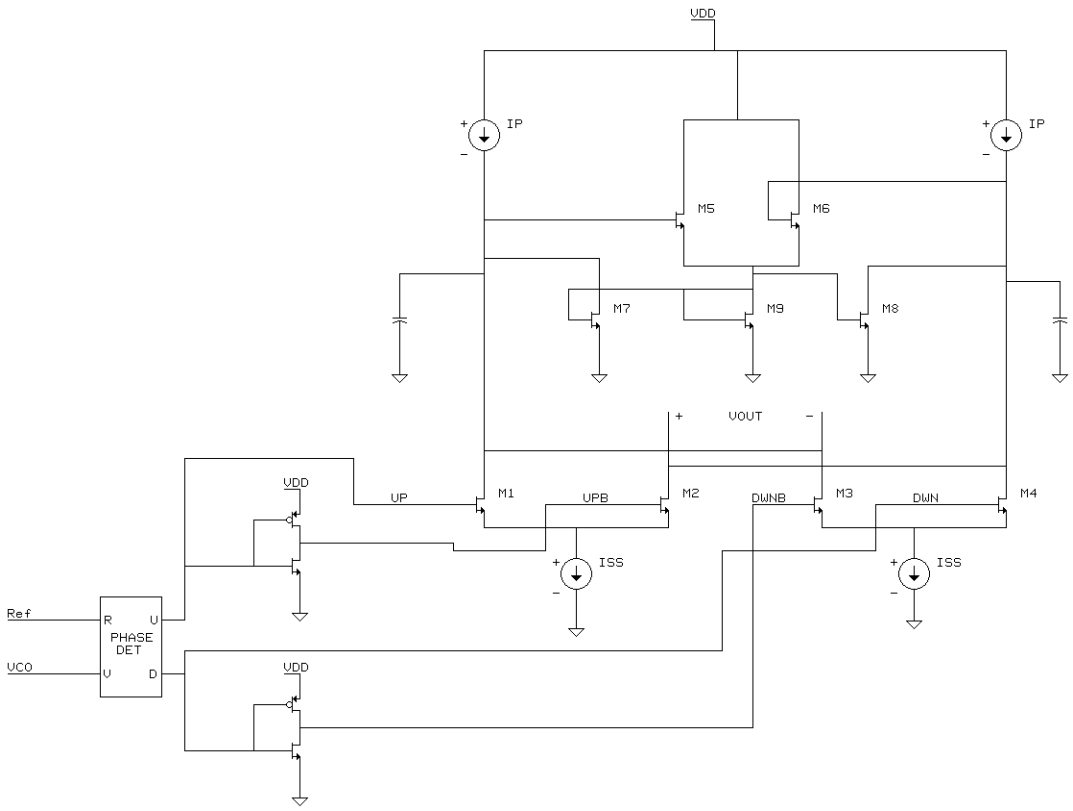


Figure 5.60 Schematic of a differential charge pump.

Using a charge pump has several advantages. Charge pumps have a simple implementation that takes up less area. In addition, this circuit has potential for high-frequency response. Finally, a charge pump is the preferred implementation for a loop filter outside an integrated circuit because it minimizes the number of external components (only needs one large capacitor, a smaller roll-off capacitor, and one resistor.

Using a charge pump also has some disadvantages. Any imbalance of the two transistors can cause a dead zone in the transfer function response. Charge sharing in the parasitic capacitors of the output transistors can be one of the major causes of this imbalance. Furthermore, to get narrow-bandwidth PLLs requires reducing the charge pump gain. At some level this causes a low SNR with these low currents, which adds noise to the PLL over the reference phase noise. Eventually, with a low enough SNR, the loop will not lock.

Next, an ideal charge pump with infinite gain requires an infinite output impedance. A practical charge pump has a finite output impedance, which significantly reduces the gain from the ideal charge pump case. Consequently, the finite output impedance of a practical charge pump gives a low gain when compared to operational amplifiers. This low gain reduces the PLL's tracking effectiveness and insensitivity to disturbances.

Next, as discussed previously, the imbalance of the charge pump transistor can cause an offset in the transfer function, which reduces the figure of merit. The high

output impedance of a charge pump produces a significant slew-rate limit. If a large frequency step occurs, the loop is slew-rate limited by the charge pump current. This would be a disadvantage for frequency-hopping applications.

As discussed earlier, charge sharing is one of the major causes of imbalance in a charge pump. The charge pump circuit in Figure 5.61 shows one method of addressing this problem [14]. Similar to the other charge pump circuits, the up and down signals from a phase frequency detector switch current sources I_{up} and I_{dn} onto node $V_{control}$. The selected current source delivers a charge to move $V_{control}$ up or down. I_{up} and I_{dn} currents need to be equal to minimize offsets. Connecting a unity gain amplifier as shown in Figure 5.61 helps minimize these offsets. The amplifier accomplishes this balance by biasing nodes N_1 and N_2 when they are not switched to $V_{control}$. This bias suppresses any charge sharing from the parasitic capacitance on N_1 or N_2.

Figure 5.62 adds the connection of the integrating capacitor in the loop filter and the parasitic capacitors of the output transistors to the charge pump connection described in Figure 5.61. Figure 5.62 shows the charge-sharing mechanism in the charge pump attached to a loop filter. A pair of matched switched-current sources charges or discharges a dc current I_o into or out of a filter capacitor (a large n channel transistor), depending on the amount of phase error. The up and down switch-control signals add charge or remove charge for a fixed time, which pumps a fixed-size charge packet into or out of the capacitor on each cycle. The operational amplifier connected as a unity-gain buffer provides a low-impedance version of the capacitor voltage, and its output V_{CTRL} is sent to nodes N_1 or N_2.

The unavoidable parasitic capacitance C_p at the current-source output charge-shares with the filter capacitor. This charge sharing produces a charge-error term. Clamping each parasitic capacitor C_p of the current source by using the unity gain amplifier that is not charging the filter capacitor to the $V_{control}$ voltage prevents

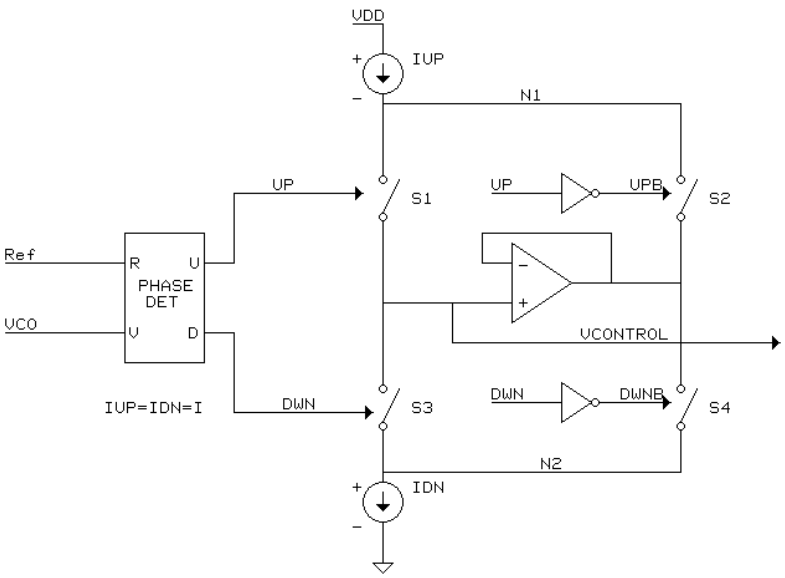


Figure 5.61 Differential charge pump with unity gain feedback to minimize charge sharing.

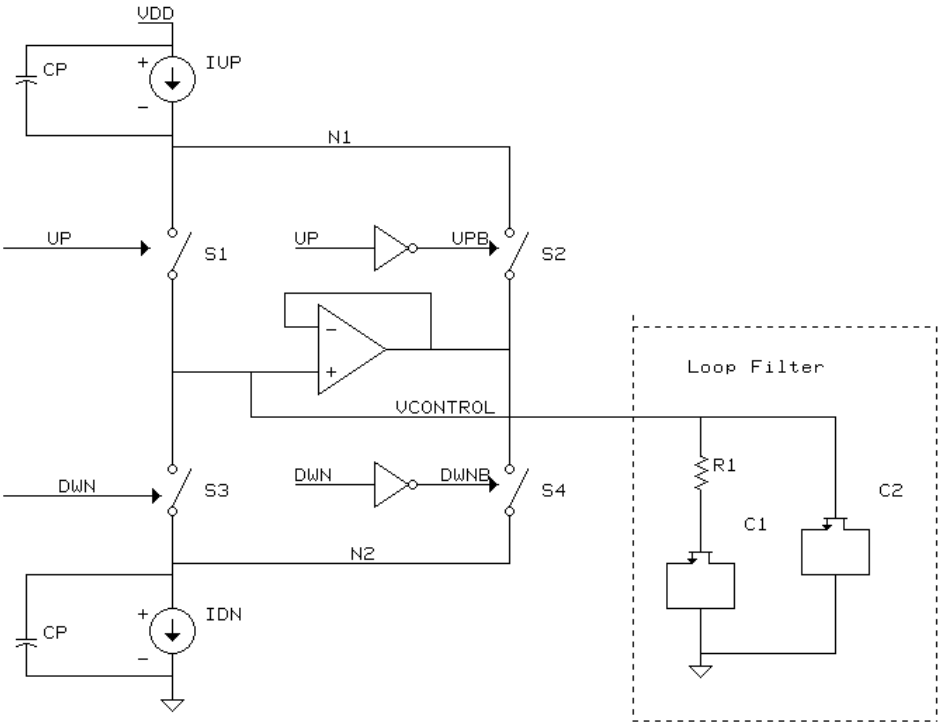


Figure 5.62 Loop-filter and parasitic capacitances that show charge-sharing effects in a differential charge pump with unity-gain feedback.

charge-sharing errors. Keeping the $V_{control}$ voltage on the parasitic capacitor C_p makes a very small ΔV when the parasitic capacitor later connects to the filter capacitor. Consequently, very little charge sharing can occur.

If one were going to use this approach, one might consider using the operational amplifier itself to convert differential to single-ended input. However, if the application requires a 1-μF external capacitor from the IC, a charge pump would be better because only one external capacitor and pad would be necessary, whereas a differential operational amplifier configuration would require two external capacitors and two pads. Many IC customers do not want this extra expense.

To show how the charge pump works, let's use an example. For this example, we will use the simple high-current charge pump circuit shown in Figure 5.57. It will be connected to a test fixture by the method shown in Figure 5.58 in order to get the transfer function.

Figure 5.63 shows the variation of charge pump transfer curve with output voltage. As the voltage approaches one rail or the other one of the output, transistors start to turn off, which causes an offset current. Furthermore, the gain of the charge pump detector varies with voltage and with negative and positive phase error. At the nominal condition (supply midpoint) of 2.5V, the negative phase-error slope equals 295 μa/rad, and the positive phase-error slope equals 390 μa/rad. At 3.5V the negative phase-error slope decreases to 199 μa/rad, and the positive phase error slightly increases to a slope of 429 μa/rad. At 1.0V the negative phase-error slope slightly increases to 356 μa/rad, and the positive phase-error slope decreases

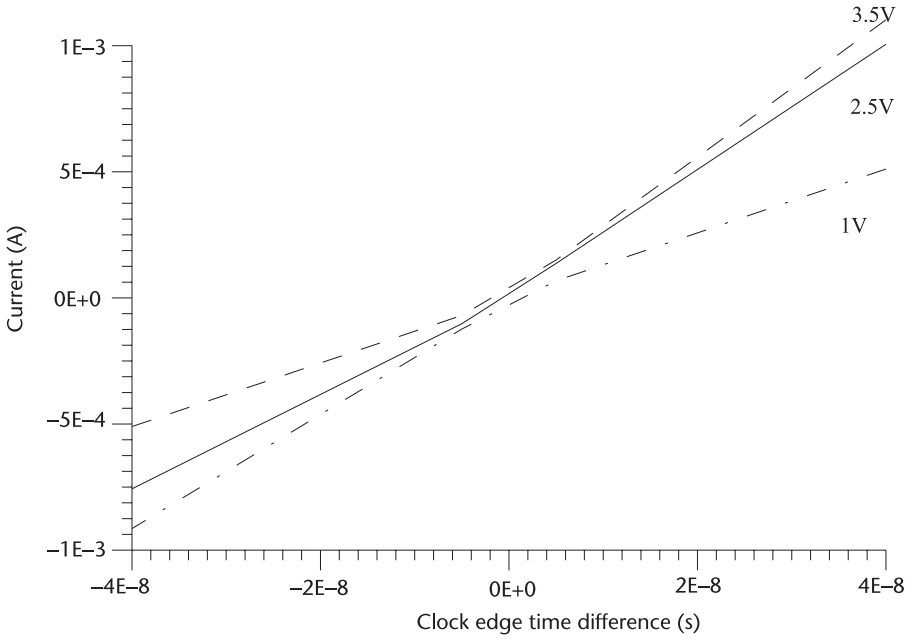


Figure 5.63 Variation of simple charge pump transfer function with output voltage.

to 199 μa/rad. Different gains about the zero-error point can cause oscillations in the loop, so that the loop never locks. A difference of less than 2-to-1 phase detector gain between positive and negative phase-error should be maintained to avoid oscillations.

Figure 5.64 shows the variation of charge pump slope with nominal, weak, and strong process conditions. The transfer function was generated by varying the positive-edge-to-positive-edge time difference between two 10-MHz input clocks with 50% duty cycles. For nominal conditions, the positive current phase-error slope is 390 μa/rad and the negative current phase-error slope is 295 μa/rad. For weak conditions, the positive current phase-error slope decreases to 219 μa/rad, and the negative current phase-error slope decreases to 127 μa/rad. For strong conditions, the positive current phase-error slope increases to 624 μa/rad, and the negative current phase-error slope increases to 644 μa/rad. This is a 490% worst-case variation in-phase detector gain over process, which is a large variation. Furthermore, a 72% variation in positive to negative phase-error slope borders on causing an unstable loop condition.

5.5 Design Considerations for Opamps in a PLL

An operational amplifier provides an alternative method to a charge pump. The operational amplifier in a PLL converts the differential up and down outputs of the phase/frequency detector to a single-ended positive and negative voltage source that charges and discharges capacitors in order to control the VCO in a PLL. The number of PLL parameters that the operational amplifier affects makes it one of the most important circuits in a PLL (second to the VCO).

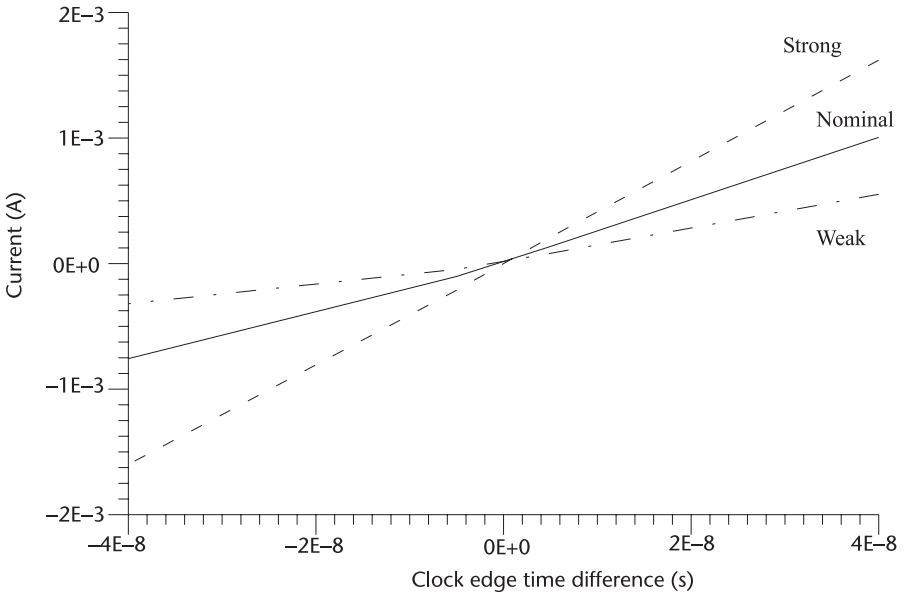


Figure 5.64 Variation of simple charge pump transfer function with process and temperature.

Listed in order of importance, the following operational parameters affect PLL performance:

- Rail-to-rail output voltage swing ≥ (wide PLL frequency range);
- High power-supply rejection ≥ (low jitter and low spurious);
- Low differential offset bias current ≥ (low-jitter and low reference sidebands);
- Wide input common-mode voltage range ≥ (wide PLL frequency range);
- Wide bandwidth ≥ (low noise and jitter);
- High dc gain ≥ (low tracking error and low noise);
- Low-noise figure ≥ (low noise, low jitter, and improved PLL stability);
- Output current loading ≥ (improved stability and low jitter);
- Fast slew rate ≥ (fast PLL switching time).

The linearity of this circuit affects the stability of the loop, the amount of jitter, the amount of noise, the reference sideband levels, the phase tracking error, and the limits of the frequency operating range.

Voltage offset of an operational amplifier is not a problem in PLLs because it operates like a switch capacitor circuit with correlated double-sampling autozeroing. With the PLL close to lock, there are small changes in-phase error at the rate of the reference-clock frequency. The amplifier offset is constant through the reference-clock period and its effect is held on the main integrator capacitor. The effect of the offset causes a onetime phase error (since it is constant) that is subtracted by the next phase-error sampling off the main integrator capacitor, which results in autozeroing of the offset of the amplifier.

We will begin the study of CMOS operational amplifiers for PLLs by studying the baseline two-stage amplifier and then comparing performance to this baseline.

Next, a folded-cascode operational amplifier is studied because of its high power-supply ripple rejection, which is crucial for PLLs. Then, the preferred AB-input, two-stage, folded-cascode operational amplifier is presented because it has high PSRR, low offset voltage, high output drive capability, rail-to-rail input operation, and rail-to-rail output operation. Rail-to-rail operation is the key to preventing the loop from hanging up at either power rail.

5.5.1 Architecture Selection, Comparison to Basic Two-Stage Opamp

For PLL design, we must select the operational amplifier architecture that best fits the list of performances mentioned earlier in this section. We will select and study a basic, two-stage, differential amplifier followed by common-source amplifier-type architectures. The following describes the advantages and disadvantages of some of the differential amplifiers to be considered:

- Folded cascodes and telescopics:
  - Advantages:
    - Good high-frequency power-supply rejection;
  - Disadvantages:
    - Reduced output swing;
    - Higher offset voltage;
    - Reduced voltage gain.
- Class B:
  - Advantages:
    - High output swing;
    - Good slew rate;
    - High gain.

The basic topology used for most CMOS opamps is shown in Figure 5.65. A differential input stage drives an active load, followed by a second gain common-source stage. An output stage may be added for driving heavy loads off-chip. This circuit configuration provides good common-mode range, output swing, voltage gain, and common mode rejection ratio (CMRR) in a simple circuit that can be compensated with a single capacitor.

5.5.2 Basic Opamp

In this section we will analyze the various performance parameters of the CMOS operational amplifier circuit. To do the analysis, we will define the transistor parameters for a 0.8-μm gate length with 5-V supply process and equations to help in the analysis and synthesis. Table 5.3 shows the transistor parameters. We will assume no loading of the first stage by the second stage because of the essentially infinite input resistance of MOS devices. This allows us to separate the two stages in order to find the voltage gain of the amplifier. Let's look at the gain of the first stage.

Using the small-signal equivalent circuit for the transistors allows the voltage gain to be calculated. Equation (5.19) computes the first-stage voltage gain:

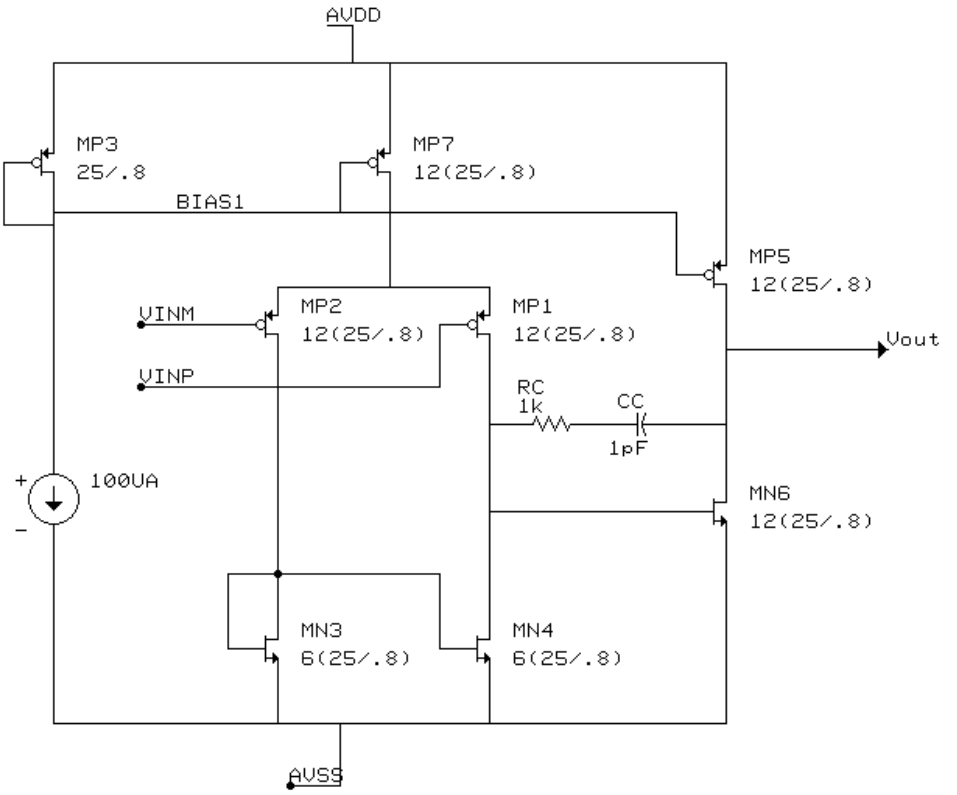


Figure 5.65 Basic two-stage operational amplifier topology.

Table 5.3 List of 0.8-μm Gate-Length Transistor Parameters Used in Studying Opamps

Transistor Parameter	*Value*
U_{ncox}	191 μA/V^2
U_{pcox}	76 μA/V^2
λ_n	0.33 μV
λ_p	0.14 μV

$$A_{v1} = \frac{g_{mp2}}{g_{dsp1} + g_{dsn4}} \tag{5.19}$$

where

g_{mp2} = transconductance of the input transistors;

g_{dsp1} = small-signal device-output conductance of the input transistor;

g_{dsn4} = small-signal device-output conductance of the active load transistor.

Similarly, (5.20) computes the second-stage common-source voltage gain:

$$A_{v2} = \frac{g_{mn6}}{g_{dsp5} + g_{dsn6}} \tag{5.20}$$

where

g_{mn6} = transconductance of the second-stage common source transistor;

g_{dsn6} = small-signal device-output conductance of the second-stage common source amplifier;

g_{dsp5} = small-signal device-output conductance of the active load for the second-stage common-source amplifier.

Consequently, combining gain equations gives (5.21) to compute the overall gain:

$$A_v = \frac{g_{mp2}}{g_{dsp1} + g_{dsn4}} \frac{g_{mn6}}{g_{dsp5} + g_{dsn6}} \tag{5.21}$$

The overall gain is thus related to the quantity $(g_m/g_{ds})^2$ as shown by (5.22) and (5.23).

$$\frac{g_m}{g_{ds}} = \frac{2L}{(V_{gs} - V_t)} \frac{1}{\frac{dX_d}{dV_{ds}}} \tag{5.22}$$

where

$V_{gs} - V_t$ = effective gate source voltage;

V_{ds} = drain to source voltage.

$$\frac{g_m}{g_{ds}} = \frac{2L}{(V_{gs} - V_t)} \frac{1}{\lambda} \tag{5.23}$$

where

λ = the output impedance constant (V^{-1}).

Thus, the overall voltage gain is a strong function of the bias point chosen for the devices and the channel length of the transistors used, and $(V_{gs} - V_t) = 0.2\text{V}$ for all devices.

Example 5.3

For example, consider a typical 0.8-μm gate length that has a channel-length modulation parameter of 0.33 μ/V for an n channel transistor and 0.14 μ/V for a p channel transistor, and set $(V_{gs} - V_t) = 0.2\text{V}$. Let's apply these values to the opamp circuit in Figure 5.65 and calculate the gain for an n channel and p channel transistor and the gain for the whole amplifier. For a typical 0.8-μm process,

λ has a value of 0.33 μ/V for an N-channel MOS transistor and 0.14 μ/V for a P-channel MOS transistor with 0.8-μm channel lengths.

Then (5.23) gives g_m/g_{ds} of $25 = 2 \times 0.8/(0.2 \times 0.14)$ for NMOS devices and 57 for PMOS devices. Equation (5.21) gives $A = -25 \times 57 = -1{,}385$.

Example 5.3 shows that either increasing the channel length of the devices used or reducing the bias current to reduce $(V_{gs} - V_t)$ increases the voltage gain. Unfortunately, both of these changes degrade the frequency response of the amplifier. Equation (5.24) computes the frequency bandwidth of the operational amplifier:

$$\omega_t = \frac{g_{mp2}}{C_c} \tag{5.24}$$

where

$$g_{mp2} = 2I_{dp2}/V_{dsat} \tag{5.25}$$

where

$V_{dsat} = (V_{gs} - V_t)$.

For an I_{d2} current of 55 μa, a V_{dsat} of 0.2, and a miller compensation capacitance C_c of 1 pF, substituting the g_{mp2} (550 μmhos) results from (5.25) into (5.24) computes an 87.5-MHz bandwidth. Next, from high-frequency analysis, the stability of the operational amplifier can be computed as shown by (5.26):

$$\theta_{pm} = \frac{\pi}{2} - \operatorname{atan}\left(\frac{\frac{g_{mp2}}{C_c}}{\frac{g_{mp5}}{C_L}}\right) - \operatorname{atan}\left(\frac{\frac{g_{mp2}}{C_c}}{\frac{g_{mp5}}{C_{gsp5}}}\right) \tag{5.26}$$

where

C_L = the output load capacitance.

Substituting the previous values and a load capacitance of 1 pF, a g_{mp5} of 1.7 ma/V, and a C_{gsp5} of 141 fF into (5.26) computes a phase margin of 69°.

Next, the systematic offset voltage can be computed as shown by (5.27)

$$V_{oscm} = \frac{V_{icm}}{\text{CMRR}} = \frac{V_{icm}}{2g_{mp2}\frac{1}{g_{dsp7}}g_{mn3}\frac{1}{g_{dsp2}}} \tag{5.27}$$

where

V_{icm} = input common mode voltage.

Substituting an input common mode of 2.5V, g_{mn3} of 1.2 ma/V, g_{dsp2} of 19 μmhos, and a g_{dsp7} of 26 μmhos into (5.27) computes an offset of 0.93 mV. Furthermore, (5.27) shows that the CMRR is related to the offset voltage; it is given by (5.28):

$$\text{CMRR} = 2g_{mp2}\frac{1}{g_{dsp7}}g_{mn3}\frac{1}{g_{dsp2}} \tag{5.28}$$

Substituting the previous values into (5.28) computes a CMRR of 2,672. Further degradation in offset can be expected due to the mismatch of the transistors in the process.

With the bandwidth computed, we now compute the slew rate of the amplifier, which depends on the miller capacitance and the loading capacitance of the operational amplifier. Equation (5.29) computes the slew rate for the operational amplifier assuming no capacitive loading:

$$SR = I_{p5}/C_c \tag{5.29}$$

For an I_{p5} bias current of 110 μa and a C_c miller capacitance of 1 pF, (5.29) computes a 110 V/μs slew rate.

Finally, let's look at the PSRR of the operational amplifier. The PSRR to the power supply is a function of the input transistor transconductance, mismatch with the other input transistor transconductance, and the tail-current transistor output conductance. Equation (5.30) shows this relationship:

$$\text{PSRR} = \frac{g_{mp2}}{g_{dsp7}}\frac{2g_{mp2}}{\Delta g_{mp2}} \tag{5.30}$$

where

Δg_{mp2} = mismatch ratio between input transistors.

Using a Δg_{mp2} of 0.01% and the previous values for the other variables computes a PSRR of 47 dB (ratio of 232).

Thus, we find fundamental trade-offs between frequency response, gain, and offset voltage in CMOS operational amplifier design. The above basic, two-stage amplifier with many variations has been widely used in a variety of applications; however, the evolution of several alternative circuits optimizes certain aspects of the performance of the amplifier. In the next section, we consider variations on the basic circuit and alternative architectures.

5.5.3 Folded Cascode

Many modern IC applications need CMOS opamps designed to drive only capacitive loads. Capacitive-only loads make it necessary to use a voltage buffer to obtain a low output impedance for the opamp. Opamp designs that realize this buffer

have higher speeds and larger signal swings than those that must also drive resistive loads. Having only a single high-impedance node at the output of an opamp that drives only capacitive loads yields these improvements. All the other nodes in these opamps have relatively low impedance from the admittance seen at all the other nodes, being on the order of a transistor's transconductance. Having relatively low impedance on all the internal nodes maximizes the speed of the opamp. These low node impedances also result in reduced voltage signals at all nodes other than the output node; however, various transistors can have quite large current signals. With these opamps, the load capacitance compensates the amplifier. Increasing the load capacitance usually makes the opamp more stable, but it also makes it slower. The transconductance parameter (i.e., the ratio of the output current to the input voltage) distinguishes these opamps from the other modern opamps. Consequently, they are sometimes referred to as *operational transconductance amplifiers* or *transconductance opamps*.

Figure 5.66 shows an example of such an amplifier. This circuit is also known as the *folded cascode*. From CMOS amplifier theory, cascode configurations increase the voltage gain of CMOS transistor amplifier stages. A single common-source, common-gate stage gain can provide enough voltage gain for many applications. This opamp configuration also has a high output impedance.

The design converts a differential input to single-ended output. All the current mirrors in the circuit use wide-swing cascode current mirrors. The use of these mirrors results in high-output impedance for the mirrors (compared to simple current mirrors). This higher impedance maximizes the dc gain of the opamp. Even though a folded-cascode amplifier only has a single gain stage, it can have reasonable gain on the order of 700 to 3,000.

A normal cascode would have NMOS input devices M_{P1} and M_{P2} driving M_{N3} and M_{N4}. For ac signals in Figure 5.66, the NMOS devices M_{N3} and M_{N4} fold the cascode up to the PMOS input transistors M_{P1} and M_{P2}. This circuit is a

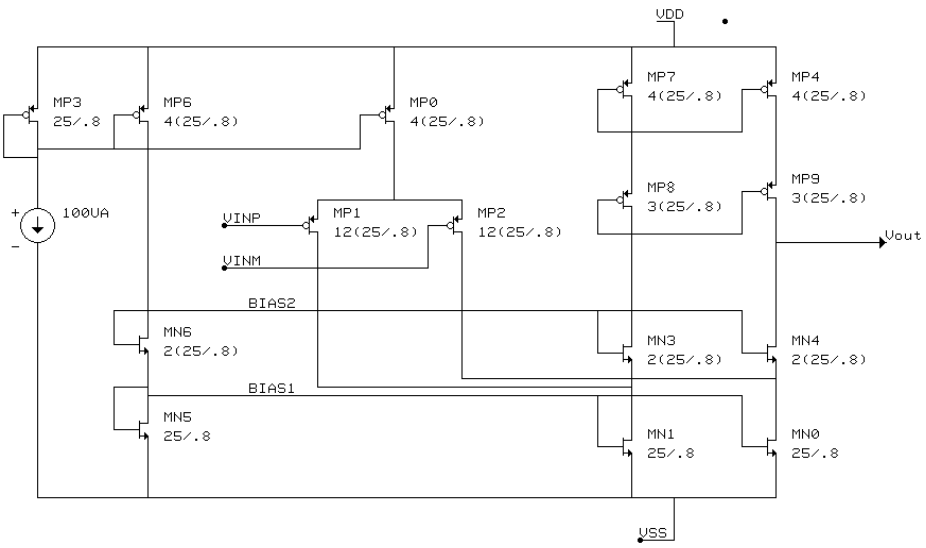


Figure 5.66 Schematic of a folded-cascode operational amplifier.

"folded-up" version of a standard cascode. Additionally, this circuit simultaneously performs a level-shifting function [15].

The folded-cascode opamp applies cascode transistors to the input differential pair, but by using transistors opposite in type from those used in the input stage. For example, the input differential pair has p channel transistors M_P1 and M_{P2} in Figure 5.66, and the cascode transistors have n channel transistors M_{N3} and M_{N4}. This arrangement of opposite-type transistors allows the output of this single gain-stage amplifier to be taken at the same bias-voltage levels as the input signals [16].

Now, for the other transistors, the current mirror composed of M_{P4}, M_{P7}, M_{P8}, and M_{P9} converts differential output to single ended. The circuit in the figure uses a simplified bias network M_{P3}, M_{P8}, M_{N5}, and M_{N6} to simplify matters. The intent here is to show the basic architecture. In practical circuits, the bias for I_{DP0} might be replaced by a constant transconductance bias network.

The load capacitor C_L determines the compensation by setting the dominant pole. In applications where the load capacitance is very small, it is necessary to add additional compensation capacitance in parallel with the load to guarantee stability. If lead compensation is desired, a resistor can be placed in series with load capacitor C_L. In some applications, lead compensation may not be possible because the compensation capacitance is mostly supplied by the load capacitance; however, it is more often possible than many designers realize. For example, it is often possible to include a resistor in series with the load capacitance.

The input differential-pair transistors have bias currents equal to $I_{DP0}/2$. Making the currents in current sources M_{N1} and M_{N0} larger than $I_{DP0}/2$ provides the proper bias to the transistors. The bias current I_{DN3} of one of the n channel cascode transistors M_{N3} or M_{N4}, hence the transistors in the output-summing current mirror as well, equals the drain current of M_{N0} or $M_{N1\ \text{minus}}\, I_{DP0}/2$. Consequently, this bias relationship gives (5.31) and (5.32):

$$I_{DN3} = I_{DN4} = I_{DN0} - I_{DP0}/2 \tag{5.31}$$

$$I_{DN0} = I_{DN1} \tag{5.32}$$

An I_{dp0} of 110 μa and I_{DN0} of 135 μa give an 80-μa current through I_{DN3} and I_{DN4}. The ratio of $(W/L)_{N1}$ or $(W/L)_{N0}$ to bias transistor mirror M_{N5} establishes the drain current I_{DN0}. Since the bias current of one of the cascode transistors is derived by a current addition, for it to be accurately established, it is necessary that both I_{DN1} and I_{DP0} be derived from a single-bias network. In addition, any current mirrors used in deriving these currents should be composed of transistors realized as parallel combinations of unit-size transistors. This approach eliminates inaccuracies due to second-order effects caused by transistors having nonequal widths [16].

Let's look at the two paths of the gain from input to output. A differential ac input voltage V_{in} causes $g_{mp2}\ V_{in}/2$ ac current to flow in the input transistors. This current flows from transistor M_{P2} through transistor M_{N4} to the output. Transistor M_{P2} has a common-source amplifier connection, and transistor M_{N4} has a common-gate amplifier connection. From this connection, this circuit is also known as a common-source, common-gate amplifier. The current through

transistor M_{P1} flows through transistor M_{N3} and is mirrored by transistors M_{P8} and M_{P7} through transistor M_{P4} and M_{P9} to the output.

Equation (5.33) computes the small-signal voltage gain of this circuit at low frequencies, which is a function of the input transistor transconductance and the output conductance contributions from M_{P9} and M_{N4}:

$$A_v = \frac{g_{mp2}}{g_{outp9} + g_{outn4}} \tag{5.33}$$

Equation (5.34) computes the output conductance contribution from M_{P9}:

$$g_{outp9} = \frac{g_{dsp9}}{1 + \dfrac{g_{mp9}}{g_{dsp4}}} \tag{5.34}$$

Equation (5.35) computes the output conductance contribution from M_{N4}:

$$g_{outn4} = \frac{g_{dsn9}}{1 + \dfrac{g_{mn4}}{g_{dsn0} + g_{dsp2}}} \tag{5.35}$$

Substituting (5.33) into (5.35), an g_{mp2} of 1.03 ma/V, a g_{dsp2} of 18.6 μmhos, a g_{mp9} of 0.93 ma/V, a g_{dsp9} of 13.9 μmhos, a g_{mn4} of 1.3 ma/V, a g_{dsn4} of 30.7 μmhos, a g_{dsp4} of 14.3 μmhos, and a g_{dsn0} of 32 μmhos into the equation computes a gain of 57 dB (ratio of 756).

Next, let's look at the stability of the amplifier. The load capacitance C_L performs the function of a compensation capacitor. This gives an important advantage to this circuit versus the previous circuit, which required the additional miller capacitance C_c to keep the amplifier from oscillating in a feedback loop connection. An important disadvantage of single-stage amplifiers is that the output voltage swing is degraded by the presence of the cascode transistors M_{N3}, M_{N4}, M_{P8}, and M_{P9}. *A* high-swing cascode configuration can be directly applied to the single-stage amplifier to improve the swing. The high swing cascode results in an available output voltage swing that extends to within $2(V_{GS} - V_t) = 2\,\Delta V_{GST}$ of each supply.

Analysis of the opamp begins with an expression for the gain. Equation (5.36) computes the gain bandwidth [17]:

$$\omega_t = \frac{g_{mp2}}{C_L + (C_{dbn4} + C_{dbp9})} \tag{5.36}$$

A capacitive load of 0.5 pF, M_{N4} drain capacitance of 26 fF, and M_{P9} drain capacitance of 55 fF substituted into (5.36) gives a 282-MHz unity-gain crossover frequency.

Next, stability is determined by evaluating the nondominant poles. We will use the three-pole approximation for the frequency response as shown by (5.37):

$$\theta_{pm} = 90 - \operatorname{atan}\left(\frac{\omega_t}{p_1}\right) - \operatorname{atan}\left(\frac{\omega_t}{p_2}\right) - \operatorname{atan}\left(\frac{\omega_t}{p_3}\right) \tag{5.37}$$

Pole 1 occurs at the junction of M_{N4} and M_{N0}. Equation (5.38) computes its value:

$$p_1 = \frac{g_{mn4} + g_{mbn4}}{C_{dbn4} + C_{dbn0}} \tag{5.38}$$

Pole 2 occurs at the junction of M_{P4} and M_{P7}. Equation (5.39) computes its value:

$$p_2 = \frac{g_{mp4}}{C_{gsp7} + C_{dbp8}} \tag{5.39}$$

Pole 3 occurs at the junction of M_{P9} and M_{P4}. Equation (5.40) computes its value:

$$p_3 = \frac{g_{mp9}}{C_{dbp9} + C_{dbp4}} \tag{5.40}$$

Other poles are less significant. A g_{mbn4} of 195 μa/V, a C_{dbn0} of 33 fF, a g_{mp4} of 1.01 ma/V, a C_{gsp7} of 53 fF, a C_{dbp8} of 68 fF, and a C_{dbp4} of 79 fF substituted into (5.37) computes a phase margin of 59°. For design purposes, we check that poles 2 and 3 are more than 10 times greater than ω_t so that they do not affect the stability of the amplifier and its crossover frequency point. Then, we adjust pole 1 to give us our phase margin.

Next, we analyze the slew rate. Equation (5.41) computes the slew rate of a folded cascode:

$$\text{SR} = \frac{I_{dp0}}{C_L + (C_{dbn4} + C_{dbp9})} \tag{5.41}$$

Using an I_{dp0} of 110 μa, a C_L of 0.5 pF, and the previous capacitor values computes a slew rate of 183 V/μs.

Figure 5.67 shows an AB-input, two-stage, folded-cascode operational amplifier for rail-to-rail operation. The folded-cascode state is followed with a common-source push-pull output stage for current boosting, higher gain, and output rail-to-rail swing. This circuit has gain from any common-mode input to the operational amplifier. This occurs because either the *n* channel or the *p* channel differential amplifier will be turned on at one of the rails. This is important in PLL designs to prevent the loop from hanging up on either rail. As long as there is gain at the rails, the integrator will operate and move the control voltage to the VCO back toward the locking condition. The equations developed in the earlier designs can also be applied to this design.

Table 5.4 compares the performance of operational amplifiers. This comparison shows the strengths and weaknesses of each design architecture. OP27 and 741 operational amplifiers are individual product ICs and are shown for reference. The AB-input, two-stage, CMOS operational amplifier is preferred for PLLs.

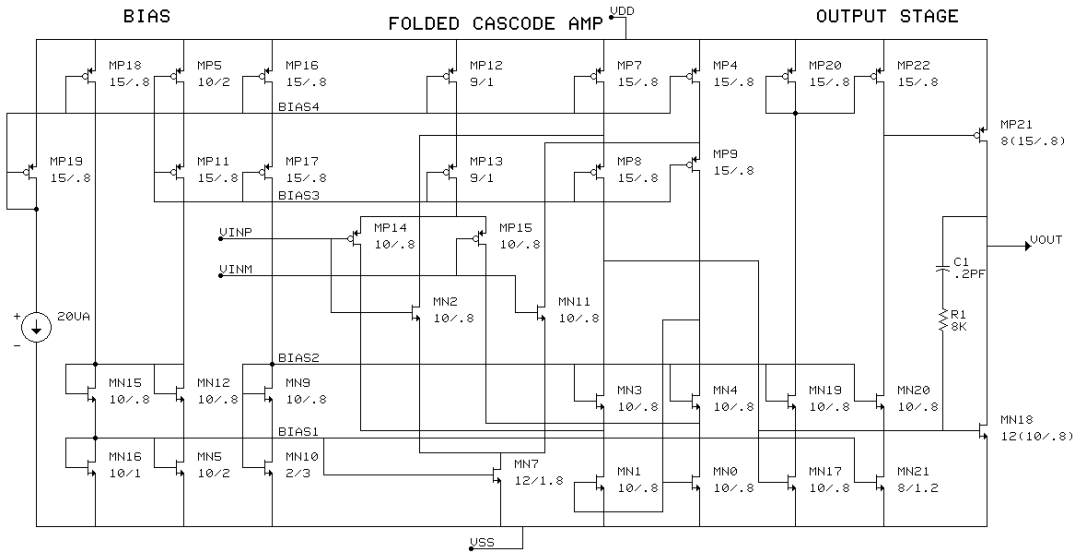


Figure 5.67 AB-input, two-stage, folded-cascode operational amplifier for rail-to-rail operation.

5.6 Differences Between Charge Pump and Operational Amplifier Compensation

One of the most important concepts to understand in PLL design is that synthesis of the compensation circuit only approximates an ideal integrator, which is needed to make an ideal type 2 PLL. A charge pump would have to have infinite output impedance, and an operational amplifier would have to have infinite gain in order for a compensation circuit to have an ideal integrator. Consequently, a decision has to be made as to which circuit makes a better integrator and what the difference in performance is.

Differences in performance show up in the following areas:

- Tracking a swept frequency;
- Noise suppression in phase-noise plots;
- Steady-state phase-error tracking.

5.6.1 Error Tracking of Charge Pump and Active Compensation

Active internal compensation allows better error tracking than charge pump compensation. An example design comparison between charge pump internal compensation and type 2 active compensation makes it easier to show the advantage. Table 5.5 lists the example design parameters. The 75-MHz reference frequency determines the limit for the loop bandwidth because of sampling effects. Consequently, a 1.5-MHz loop bandwidth was chosen because it is far enough away to minimize sampling effects.

Table 5.6 lists the charge pump solution and the type 2 active-compensation solution. For charge pump compensation, charge pump gain and C_1 are used to

Table 5.4 Comparison of Well-Known Opamp Performance Versus Various CMOS Architectures

Key Performance Parameters	*OP27*	*LM741*	*Typical CMOS 3-μm Process*	*CMOS State of the Art*	*Basic Two-Stage CMOS*	*Folded-Cascode CMOS*	*AB-Input Two-Stage CMOS*
Voltage gain	10^6	10^5	10^4	10^6	10^3	10^3	10^5
dc V_{os}	10 μV	2 mV	5 mV	20 μV	2 mV	50 mV	250 μV
Input bias current	10 na	300 na	—	—	0	0	0
Frequency of unity gain	8 MHz	1 MHz	10 MHz	500 MHz	150 MHz	300 MHz	180 MHz
Slew rate	2.8 V/μs	1 V/μs	10 V/μs	1,000 V/μs	44 V/μs	52 V/μs	83 V/μs
Power dissipation	90 mW	50 mW	1 mW	10 μW	1.65 mW	2.75 mW	3.6 mW
PSRR	1 μV/V	—	—	—	60 dB	60 dB	79 dB
Input noise density	3 nV/sqr Hz	20 nV/sqr Hz	—	—	9 nV/sqr Hz	10 nV/sqr Hz	22 nV/sqr Hz

Table 5.5 Example PLL Design Parameters

Design Parameter	*Value*
Reference frequency	75 MHz
K_v	700E6 rad/s/V
N	1
Loop bandwidth	1.5 MHz
Damping factor	0.8

Table 5.6 Charge Pump and Type 2 Active-Compensation Solutions to Example Design

Component	*Charge Pump*	*Type 2 Active Compensation*
K_d	1.3 mA/rad	0.4 V/rad
R_1	0	0.666 Megohms
R_2	22	10 Kohms
C_1	0.12 μF	20 pF
C_2	2,200 pF	0

adjust the bandwidth, and R_2 adjusts phase margin. For type 2 active-compensation phase detector gain, the ratio of R_2/R_1 to C_1 adjusts bandwidth, and R_2 adjusts phase margin.

Next, error tracking for active compensation will be compared with the charge pump compensation. Using a behavioral model and ac SPICE analysis (refer to Section 8.2), Figure 5.68 shows the resulting error transfer function for the charge

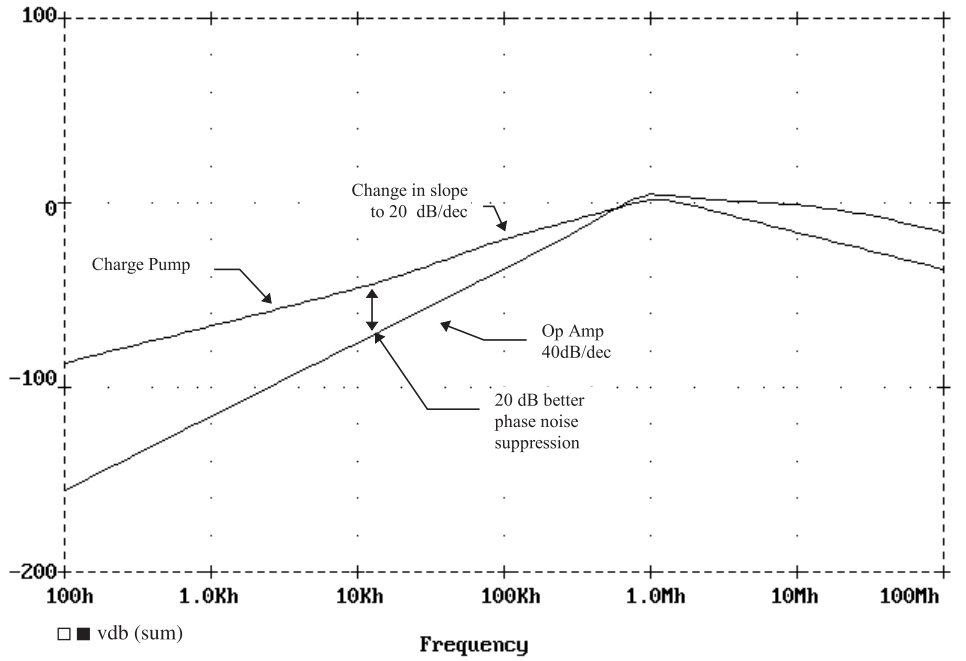


Figure 5.68 Error transfer function for the charge pump and active-based compensation.

pump and active compensation. This figure shows 10–20-dB lower error for active compensation. This is due to the lower gain for the charge pump when compared to an operational amplifier. A parallel 40Ω resistor with the current source was added to model the reduced gain in the charge pump. This accounts for the change in slope at 100 kHz. The difference in control-system response shows up in the amount of phase noise and error tracking. To demonstrate the error-tracking effect on loop performance, a simulation with a sweeping input frequency (triangle wave) will be used.

From doing transient analysis on the behavioral model, Figure 5.69 shows the results for charge pump compensation and active compensation with the swept-input frequency. The frequency of the triangle wave was increased until a significant difference in tracking occurred. Active compensation tracks the triangular modulation closer than charge pump compensation. Closer tracking of the input modulation means the loop will have higher immunity to disturbances. This is a relative measurement of whether the loop is locked with Post-it Note glue that a slight wind can blow off the lock or Super Glue that a strong wind cannot blow off the lock.

5.6.2 Phase-Noise Suppression

Suppression of close-in phase noise is another area where the difference between charge pump– and opamp-based compensation shows up. This occurs at the loop bandwidth of the PLL when the phase noise of the VCO is much greater than the multiplied phase noise of the reference crystal oscillator. This is the usual condition in integrated circuits because of the inherently noisy VCOs in integrated circuits.

As we did before, it is easier to make this phase-noise comparison by using an example. Consequently, we will use a comparison of two example PLLs. One has

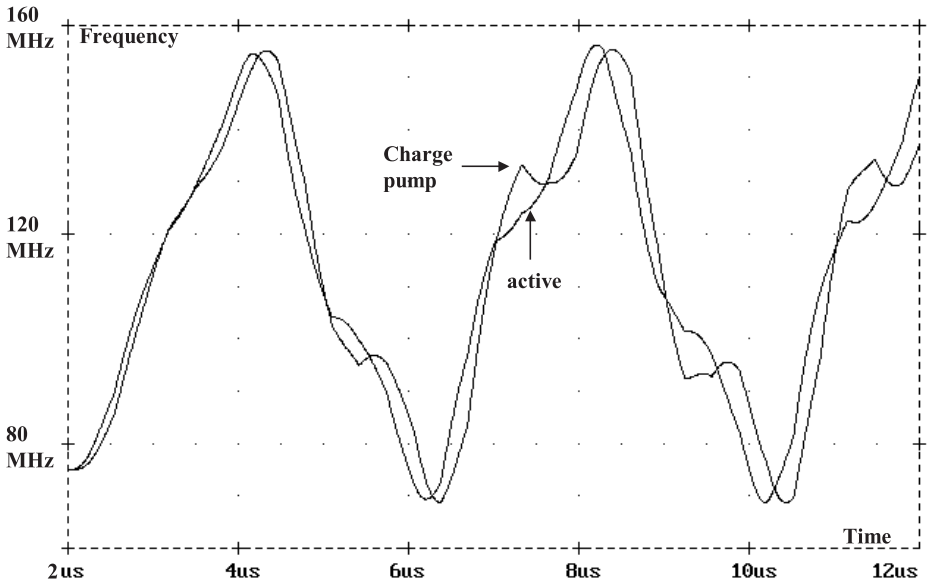


Figure 5.69 Charge pump and active-compensation response to a swept-input frequency.

a charge pump that multiplies 20 MHz by 4 to 80 MHz with a 1-MHz loop bandwidth. The other has an operational amplifier that multiplies 20 MHz by 4 to 80 MHz with a 1-MHz loop bandwidth. In this case, measured phase noise of the examples shows the comparison better than modeling the effects because of the difficulty of taking into account all the nonideal parameters. Figure 5.70 shows the measured comparison results.

This figure shows that the operational amplifier suppresses the phase noise of the VCO from its 1-MHz bandwidth value of –85 dBc/Hz until an offset frequency of 100-kHz value of –95 dBc/Hz. This 10-dB/dec reduction in noise confirms the presence of a type 2, –40-dB/dec slope suppression of the +30-dB/dec increase in noise from the VCO. Consequently, the operational amplifier has produced an ideal integrator over at least the 100-kHz to 1-MHz decade range. From 1 kHz to 100 kHz the loop follows the multiplied reference-oscillator phase noise. In the other example loop, the charge pump does not suppress the phase from its 500-kHz bandwidth value of –85 dBc/Hz to its 10-kHz frequency offset value of –85 dBc/Hz. This flat response shows that the charge pump does not act like an integrator that gives a type 2 PLL response to noise. Consequently, for low output phase noise close to the carrier, operational amplifier compensation is preferred.

5.6.3 Phase-Error Tracking for Changing Input Frequency

Figure 5.71 shows an oscilloscope picture of phase-error tracking for a PLL with an operational amplifier. The top waveform shows the output of the VCO, which multiplies the reference by 2. The bottom waveform shows the reference-oscillator input at 66 MHz. At 20-MHz input frequency, the edge of the VCO that is marked by the dotted line coincided with the *y*-axis. Slowly changing the input frequency

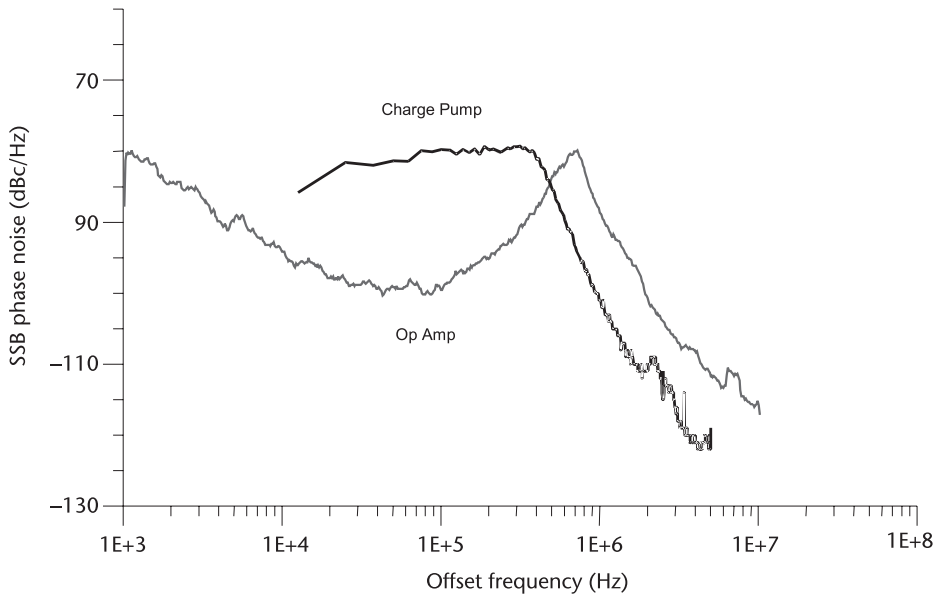


Figure 5.70 Phase-noise suppression comparison between charge pump– and opamp-based compensation.

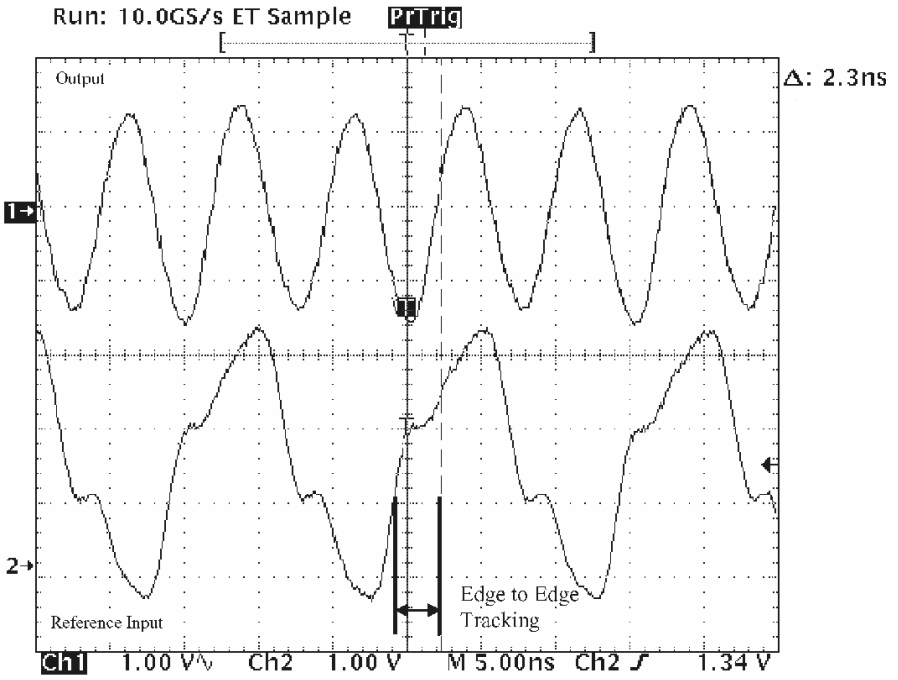


Figure 5.71 Oscilloscope picture of VCO output and reference input of a PLL example for phase tracking.

to its final value of 66 MHz showed the VCO output edge moving slowly to its final value of 2.3 ns from the *y*-axis. Consequently, we had a 50-ps tracking change per 1-MHz change in input frequency. No special phase matching was done to achieve this result. A repeat of this measurement with the charge pump PLL could not be done because the VCO edge moved so quickly across the oscilloscope screen that it was difficult to maintain the identity of each edge.

Another method for quantifying the effectiveness of the compensation is to do an ac SPICE analysis [18]. Figure 5.72 shows an ac SPICE simulation of a charge pump charging capacitors of 1, 10, and 100 pF. The plots show only a decade of integration above the 0-dB gain point.

Figure 5.73 shows an ac SPICE simulation of an operational amplifier with feedback capacitors of 10 pF and 100 pF. This plot shows 2.5 decades of integration above the 0-dB gain point. This increase should improve suppression of phase noise when compared to a charge pump integrator.

5.7 Summary

In the previous chapter we discussed dividers and oscillators. In this chapter, we discussed detectors and other circuit designs of the individual components in a PLL. Detailed designs of phase detectors, lock detectors, and acquisition aids were studied.

Phase detectors were studied because understanding how phase detectors work is one of the major keys to understanding how PLLs work. Next, lock detection

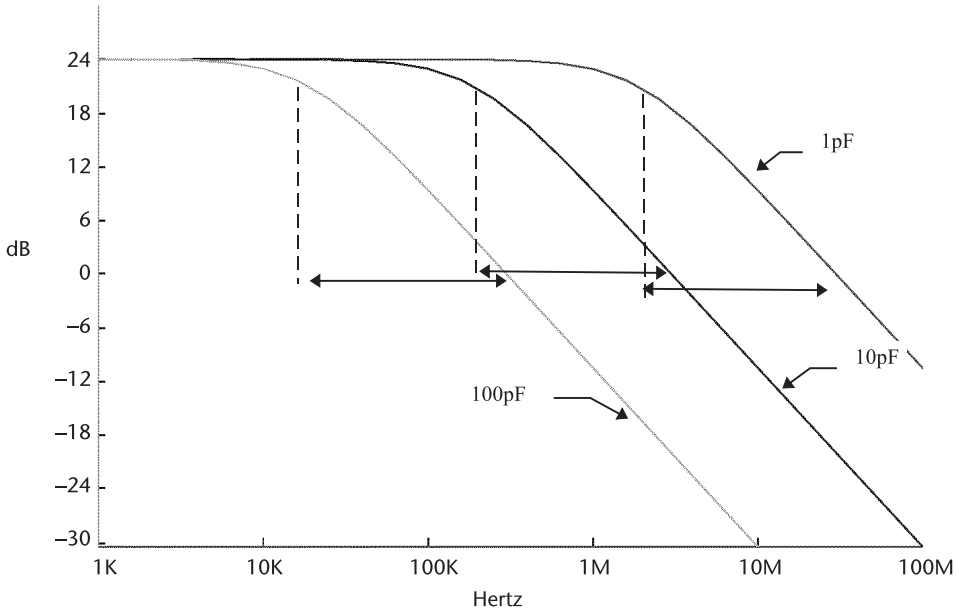


Figure 5.72 Integrator frequency range versus integrating capacitor for a charge pump.

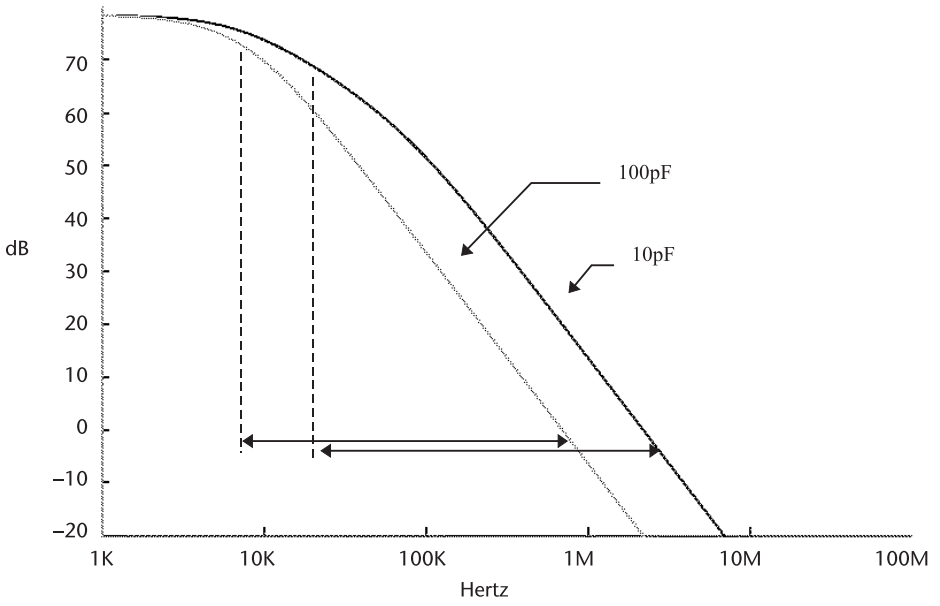


Figure 5.73 Integrator frequency range versus integrating capacitor for an operational amplifier.

was studied. Many systems use the lock detector to reset the system. This is a disastrous change to the operation of most systems. In a PLL, a reset can start the loop operating at a very low frequency (or with no output), which then acquires lock at the normally much higher output operating frequency. Consequently, a small phase shift in a PLL that would marginally affect the system can cause a

huge disruption in the operation of the system if a reset occurs. The key to lock detection is to alarm on behavior that shows the PLL is broken. Quadrature phase detection, time-window edge comparison, tune-voltage window comparator, and cycle-slip detection are the lock-detection methods that were covered.

Then, acquisition techniques were studied. Open-loop sweep, closed-loop sweep, and discriminator-aided acquisitions were the methods covered. The phase/frequency detector uses discriminator-aided acquisition and is the most popular choice. Clock-recovery circuits cannot use phase/frequency detectors. Consequently, these circuits require an acquisition aid.

Next, single-ended and differential charge pumps were studied. The number of parameters that the charge pump affects makes it one of the most important circuits in a PLL. The linearity of the circuit affects the stability of the loop, the amount of jitter, the amount of noise, the reference sideband levels, the phase tracking error, and the limits of the frequency range. The amount of peak charge pump current affects the amount of noise, the loop bandwidth, and the frequency slew rate. Next, basic and other opamp variations were studied as an alternative to charge pumps. An opamp affects the same parameters as the charge pump. Basic opamp design was covered. Folded-cascode and other variations were studied and compared in order to find the best configuration for a PLL. Finally, the trade-offs between operational amplifiers and charge pumps were studied in order to decide which circuit to use. Understanding the design details and trade-offs in these detector and supporting components is critical in designing monolithic PLLs.

Questions

5.1 A phase detector has a maximum voltage of 3.3V for a 2π phase error and 13.3 mV at zero phase error. Calculate the phase detector gain and the figure of merit M. Is this a reasonable phase detector?

5.2 A sinusoidal phase detector has 0.1V average output for a 0° phase error. What is the gain of the phase detector at 0° phase error? Is this a reasonable phase detector at 0° phase error?

5.3 A sinusoidal phase detector has a maximum output voltage of 0.6V and an offset voltage of 1 mV. Calculate the phase detector gain and the figure of merit M. Is this a reasonable phase detector?

5.4 A exclusive-OR phase detector has a maximum output voltage of 1.8V and an offset voltage of 11.1 mV. Calculate the phase detector gain and the figure of merit M. Is this a reasonable phase detector?

5.5 An RSFF phase detector has a maximum output voltage of 1.1V and an offset voltage of 21.1 mV. Calculate the phase detector gain and the figure of merit M. Is this a reasonable phase detector?

5.6 The Gilbert multiplier circuit in Figure 5.6 has a current $I = 2$ mA and resistance $R = 5$ kΩ. R_1 and R_2 differ by 2%, and $V_{io} = 5$ mV. Find V_{do}, K_d, and the figure of merit.

5.7 Run a simulation for an RSFF with a 10-MHz reference frequency and 50% duty cycle and one with a 9-MHz VCO frequency and 50% duty

cycle. Draw the output waveform after it has been filtered. Describe any problems with this waveform.

5.8 How many regions of operation does a phase/frequency detector have? Describe the regions.

5.9 In a phase/frequency detector, what is the dead zone? What is one condition that can cause a dead zone? What can be done to the phase detector to minimize the dead zone? Can a type 2 PLL stay locked in the dead zone?

5.10 What happens to the transient response of a PLL with a phase/frequency detector and a damping factor of 3? What can be done to improve the transient response.

5.11 Why are there equal up-down pulses at 0° phase error in a phase/frequency detector? What would happen if we filtered the output pulses at 0° phase error so that there would be no output?

5.12 Your customer wants you to choose between a NAND gate and a D flip-flop phase/frequency detector that he plans to use over several process (0.8μ to 0.15μ gate lengths). Which one would you choose and why?

5.13 A PLL with 100-kHz loop bandwidth uses a quadrature lock detector and has a 3.3-V supply. The mixer has x gain. What bandwidth do you set the lowpass filter to in the detector and what voltage threshold would you use in the comparator?

5.14 A PLL with 10-kHz bandwidth uses a tune-voltage window comparator lock detector. What would you set the low-voltage and high-voltage thresholds to?

5.15 $K_d = 0.4$, $K_v = 1E9$, $R_1 = 300\ k\Omega$, and $C = 100$ pF. What is the maximum sweep rate and the natural frequency? For a 3-V supply, what is the fastest ramp time of the tune line that can be achieved?

5.16 $K_d = 0.16$, $K_v = 3E8$, $R_1 = 10\ k\Omega$, $R_2 = 1\ k\Omega$, and $C = 3300$ pF. What is the maximum sweep rate and the natural frequency? For a 5-V supply, what is the fastest ramp time of the tune line that can be achieved? What pulse width should you make the one shot?

5.17 What are the advantages and disadvantages of using a charge pump in a PLL?

5.18 Name and describe two variations of a charge pump?

5.19 What is the advantage of using an operational amplifier to feed back the voltage to the other leg in a differential charge pump?

5.20 A phase/frequency detector drives a charge pump with a programmable current source of 100 μa and 1 ma. Calculate the phase detector gains? If the charge pump has a figure of merit of 10, calculate the offset current for each current.

5.21 What opamp has the widest swing and largest PSRR?

5.22 Name a few operational amplifier configurations.

5.23 Name a few operational amplifier characteristics that pertain to PLLs.

5.24 Why do you use cascode transistors in a current mirror?

5.25 Would you use a charge pump or an operational amplifier to convert a differential signal to a single-ended signal?

5.26 Which has more flexibility in synthesizing compensation configurations, a charge pump or operational amplifier?

5.27 For which IC applications would charge pump compensation be a good choice?

5.28 What noise specification is significantly improved by using an operational amplifier?

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