



Figure 1, Dr. C

Phase Lock Loop Design

INTRODUCTION

The specifications for this Design included.

- Build VCO using discrete components
- Build diode ring mixer or use (ADE-1)
- No specified frequency
- Measure Capture, and Lock Range

The purpose of this paper is to describe the process taken to design a phase lock loop (PLL), the PLL is an essential control system tool used in many applications for demodulation, synchronization, and frequency synthesis. A simple block diagram of the loop can be seen below in figure 2; in this project I built the VCO with the design provide by Dr. Campbell, the goal of the VCO was to oscillate at 10MHz but having non ideal components this VCO began oscillating at 13MHz. The phase detector was built using a diode ring mixer to multiply the signals from the LO

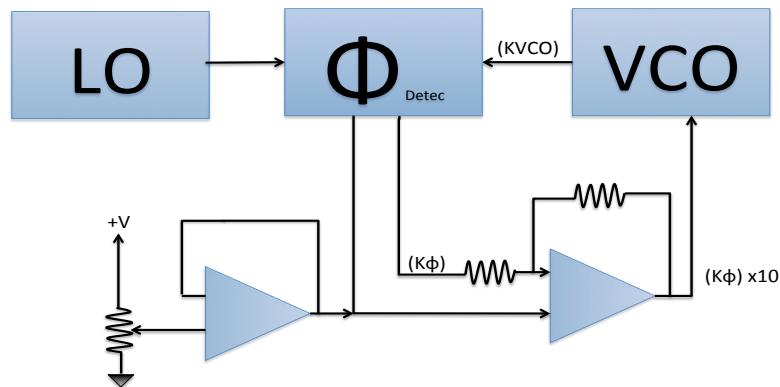
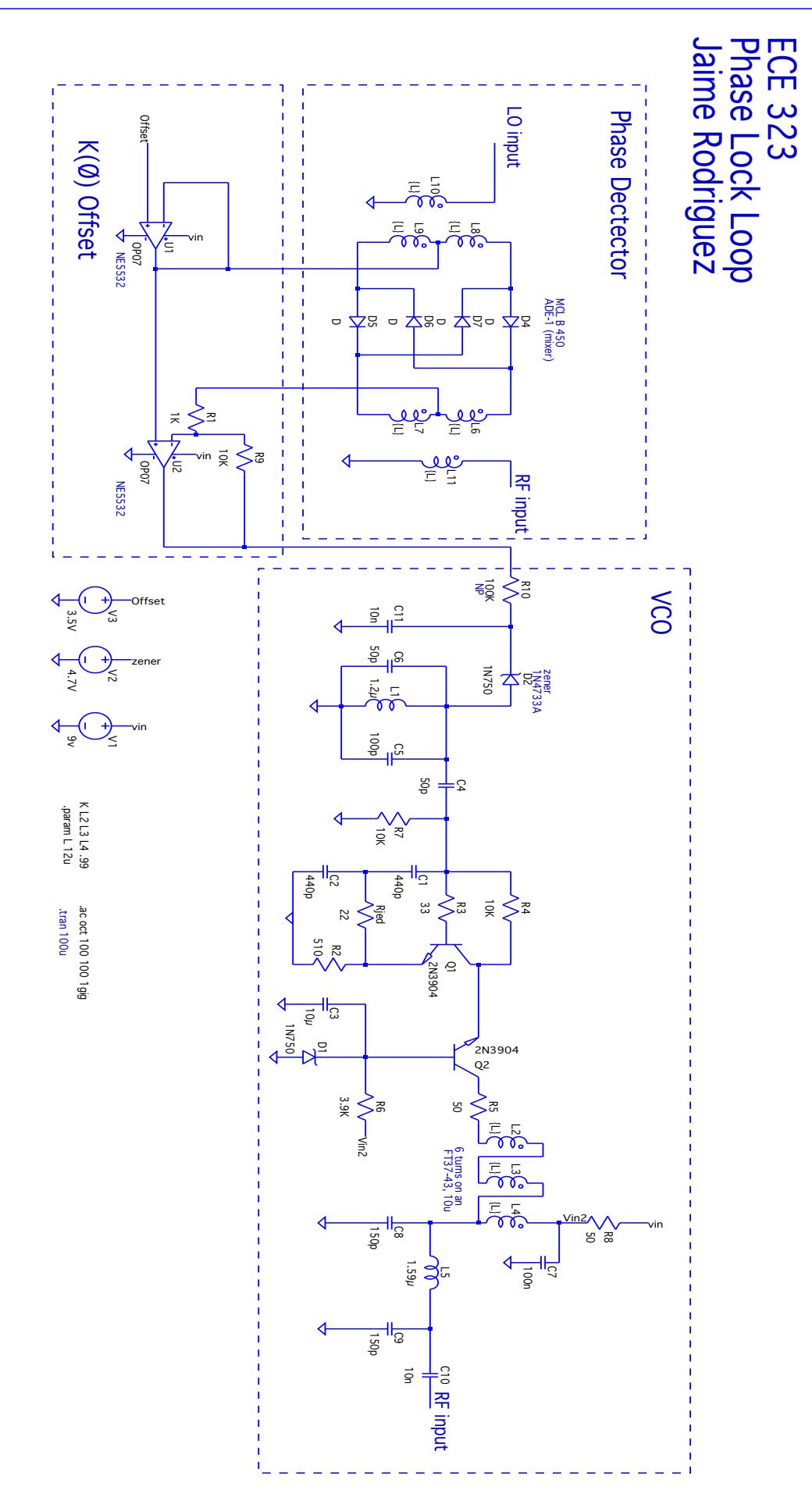


Figure 2, Block diagram of PLL

and the VCO which produces a dc offset when the two signals are out of phase that is fed back to the VCO to lock the signals to the same frequency. A full schematic of the phase lock loop can be seen in figure 3.

ECE 323
Phase Lock Loop
Jaime Rodriguez



For the phase detector I built an earlier version out of discrete components, but in this design I wanted a more compact PLL so I used the off the shelf ADE-1 from Mini Circuits, which measured a ($K\phi$) of about 30mV per radian with a signal of about 300mVpeak as the RF input.

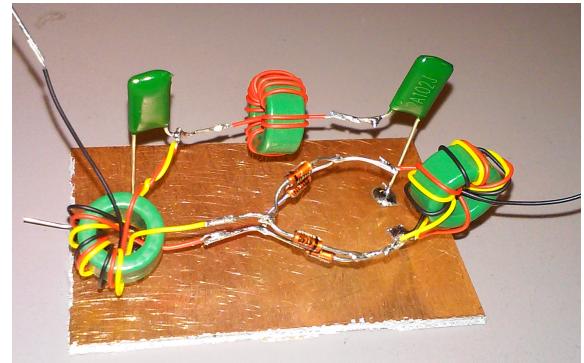


Figure 4, diode ring mixer

F (MHZ)	Volt in	Amp (mV)
11.2	0	320
11.43	0.5	356
11.65	1	384
12	1.5	412
12.25	2	412
12.4	2.5	392
12.55	3	388
12.6	3.5	376
12.65	4	376
12.7	4.5	368
12.73	5	360
12.77	5.5	356
12.82	6	348
12.85	6.5	336
12.86	7	336
12.88	7.5	325
12.9	8	320
12.95	8.5	303
13	9	284
13.1	9.5	248
~	10	No more
~	10.5	No more

Table 1, KVCO measurements

Next I characterized the gain of the VCO (KVCO) having only the input at the varactor (actually zener 4.7V, 1W) diode connected to the power supply and measuring the output frequency.

KVCO:

$$13.1\text{MHz} - 11.2\text{MHz} = 1.9\text{MHz}$$

$$\frac{1.9\text{MHz}}{9.5\text{V}} = 200\text{KHz per Volt}$$

The VCO was able to take an input voltage up to about 9.5 volts before having the output die out I believe this was because I was using a bigger 1watt zener vs. the standard $\frac{1}{4}$ watt, after getting a range I took the difference of the max and min frequencies and divided that by the input voltage range and found KVCO to be 200KHz per Volt .

After having measured KVCO I decided to go ahead and close the loop using the two-opamp network to raise the dc offset and add a gain of 10, after achieving

freq@13.8MHz	Capture (MHz)			Lock (MHz)		
Dc Offset (V)	Min	Max	Range	Min	Max	Range
0-2.5	12.42	12.46	0.04	12.4	12.46	0.06
3	13.13	13.6	0.47	13.06	13.76	0.7
3.5	13.23	13.77	0.54	12.79	13.78	0.99
3.75	13.31	13.78	0.47	12.94	13.79	0.85
4	13.45	13.81	0.36	13.1	13.82	0.72
4.5	13.72	13.8	0.08	13.3	13.8	0.5

Table 2, DC offset measurements

lock for the first time I made several more measurements varying the dc offset, the table above shows the different capture and lock ranges that where measured in the lab. The best results occurred when the dc offset was set at 3.5 Volts achieving a capture range of around 500KHz and a lock range of 990MHz.

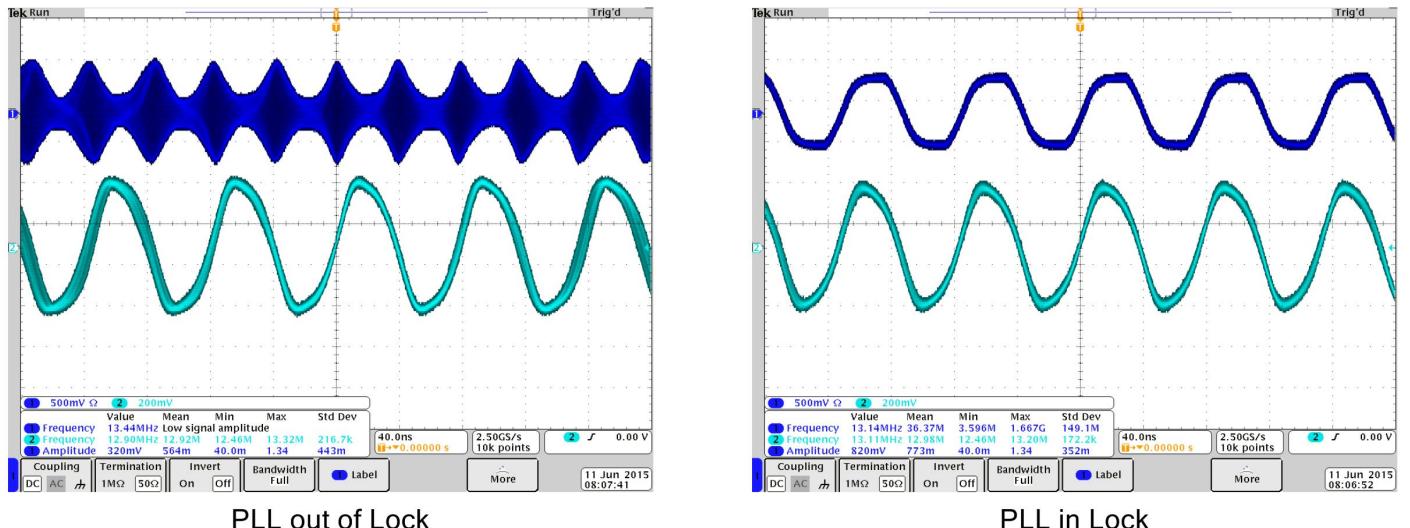


Figure 5, Waveforms of PLL in and out of lock

The above waveforms in figure 5 demonstrate the locking and unlocking of the reference signal (blue) to the VCO (green), the capture range was measured by having the PLL out of lock and then varying the reference signal until the signals synchronized at both max and min frequencies, the lock range was done the same but instead in lock and measuring when the lock was broken.

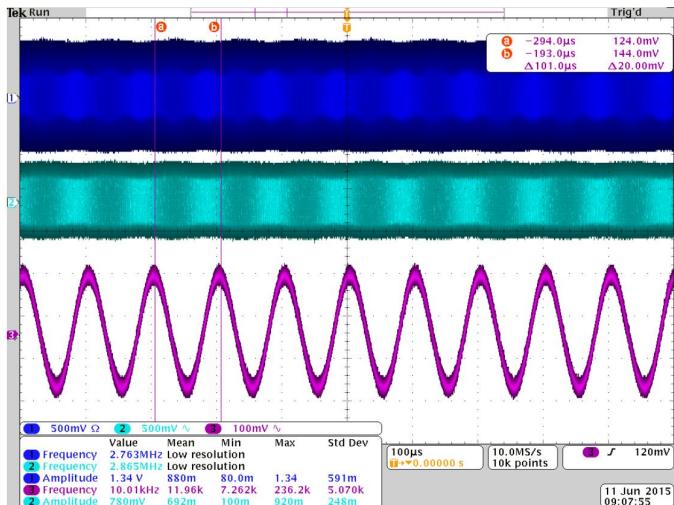
CONCLUSION

After making measurements and determining a capture range of 500KHz was too high for the RC lowpass filter on the input of the VCO I did some debugging and found that I had made a mistake in my wiring instead of having my input go through the resistor, it was connected straight to the zener diode and nothing was being filtered out. After fixing this issue I made some more measurements and found that the performance of the PLL was a lot worse with the resistor so I chose to disconnect the resistor. The PLL performed as expected but the signals were slightly distorted because there was no filtering in the loop, there was also a second oscillation seen at around 10Hz. To finish up the project I placed the whole circuit in an Altoids tin to make the PLL easy to test and care.

In my testing I also played with the FM modulation on the reference signal, I was able to use the PLL to demodulate a 10KHz sine wave with up to 200KHz deviation, this output had some high frequency noise that was cleaned up using an RC filter on the output of the gain opamp as can be seen in figure.



Figure 6, Phase Lock Loop in can



PLL FM Modulation @ 10KHz

Figure 7, FM demodulation with 200KHz deviation

