Jaime Rodriguez
ECE 421

Head Phone Amplifier Design

INTRODUCTION

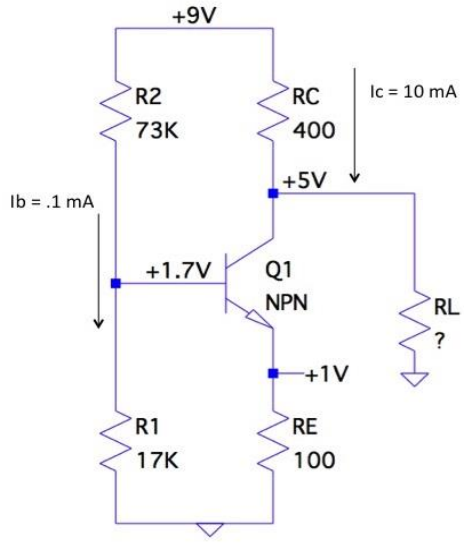
The specifications for this amplifier included.

- Input resistance of 1K ohm's or greater.
- Output resistance of 32 ohm's
- Power out of 100 mWatt's or greater.
- Gain of 10dB
- Bandwidth of 100 Hz – 20K Hz.

Note: please skip to page 5 for Final report unless you need to review.

Gain Stage

I began this problem by thinking about the difficulties that this amplifier design needed to overcome. The gain needed is very easy to achieve using a C-E npn transistor but being able to drive a load of 32 ohms with just one transistor seems pretty difficult, so I immediately knew that this would be a two stage amplifier design. I began by creating the gain stage first and turning on the transistor, I arbitrarily chose values that would make my calculations easy. I also picked 9V as my voltage source because if my design was successful I would eventually like to realize my design and build it as a portable amplifier.



In all my calculations I used standard values for β, V_A and V_t. I picked my Ic to be 10mA to ease my calculations and I also chose my output swing to be from 5v to 1v. This made it easy to find values for Rc and Re. knowing that I need the base to be .7V higher than at Ve and that ib = (Ic/100) I was able to create a voltage divider to meet this need. Now that I had the transistor turned on, I knew that gain was dependent on RL because of:

$$Av = \frac{gm*(Rc//RL)}{1+gm*Re}$$

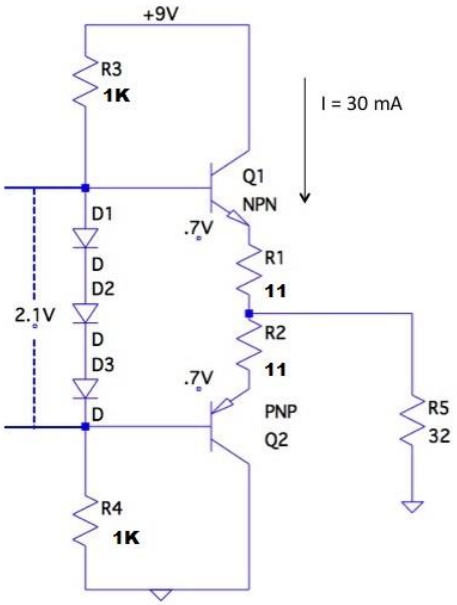
I already have all the values needed in the equation above except for RL, so I set this equation equal to 3.2 which is around the gain of about 10dB, and solved for RL (2K ohms). This value of RL needs to be the Input resistance of my output stage for my gain to be 10dB.

Output Stage

In creating my output stage, I decided to go with complementary push pull pair discussed in class, this topology works off the concept that when an Ac input signal is coming in, the positive voltages from that signal, begin turning on the NPN transistor and in contrast the PNP transistor begins turning off, These behavior is also reversed as the input signal hits negative voltages pushing and pulling the transistors more on or off.

The resistors R3, and R4 need to equal each other and in series they define the input resistance of this stage, which from my previous calculations needs to be around 2K to give me the desired gain of 10dB, so I decided to make each one around 1K. There needs to be a power output of 100mW, and with a source of 9V the output current needs to be i=11mA using (P=VI).

The efficiency of the amplifier will probably loss two thirds of its power so I decided to design this stage with 30mA for my Iq (current through Q1, and Q2), because there is a voltage drop of about 2.1V between the three diodes and about 1.4V through the transistor pair that difference needs to be made up across R1 and R2 so (.7V = R*30mA). R becomes 23 ohms divided into 2. Capacitors where also added to this design to lock ac signals but omitted to simplify figures.



Ltspice Simulation

In simulating my design I quickly found that my design didn't work out exactly as I expected mostly because the models in Ltspice had differently characteristic values like beta then the ones values I used for my calculations and the diode also had different voltage drops then what I used, these required me to play around with some of my resistor values, I found that the current values that I chose where very close to what I picked. Using two tone simulation I also found that the distortion was reasonable as my 3rd order products where about -40dBc, but I found that adjusting the gain could would also greatly affect distortion so the higher gain the more distortion as the output signal began reaching its clipping voltage. All required specifications where meet the only problem I wasn't able to solve was a small offset of around 100mV at a high amplitude of 800mV, I was able to adjust the voltage diver in my gain stage to decrease the offset but not enough to completely remove it.

--- Bipolar Transistors ---

Name:	q3	q2	q1
Model:	2n3906	2n3904	2n3904
Ib:	-1.55e-04	1.04e-04	2.97e-05
Ic:	-3.01e-02	3.02e-02	9.06e-03
Vbe:	-7.50e-01	7.49e-01	7.13e-01
Vbc:	3.98e+00	-3.46e+00	-3.85e+00
Vce:	-4.73e+00	4.21e+00	4.56e+00
BetaDC:	1.94e+02	2.89e+02	3.05e+02
Gm:	1.09e+00	1.09e+00	3.43e-01
Rpi:	1.66e+02	2.48e+02	8.71e+02
Rx:	2.00e+01	2.00e+01	2.00e+01
Ro:	3.45e+03	3.43e+03	1.15e+04
Cbe:	4.00e-10	3.97e-10	1.33e-10
Cbc:	2.45e-12	2.26e-12	2.20e-12
Cjs:	0.00e+00	0.00e+00	0.00e+00
BetaAC:	1.82e+02	2.71e+02	2.98e+02
Cbx:	0.00e+00	0.00e+00	0.00e+00
Ft:	4.32e+08	4.36e+08	4.03e+08

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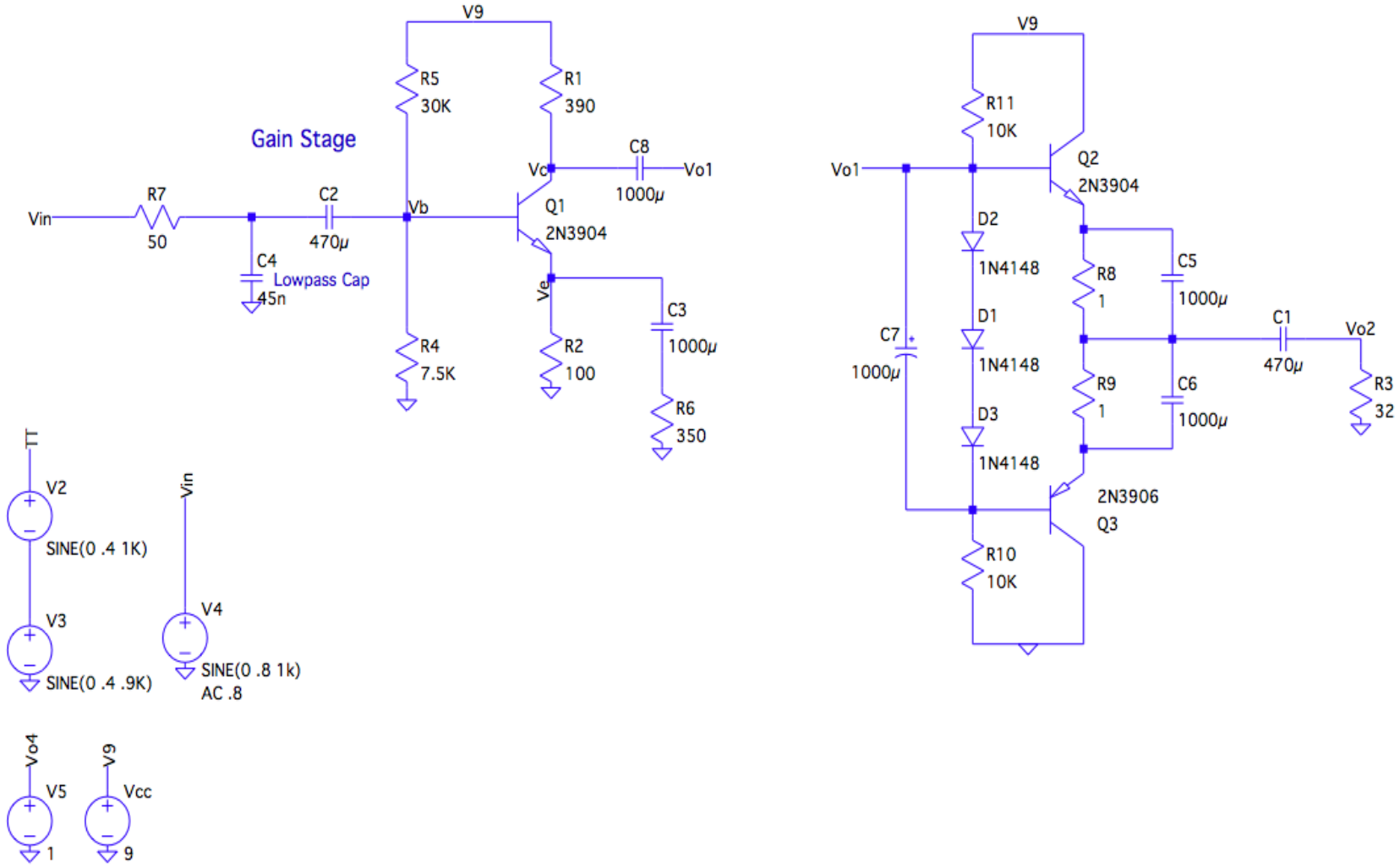
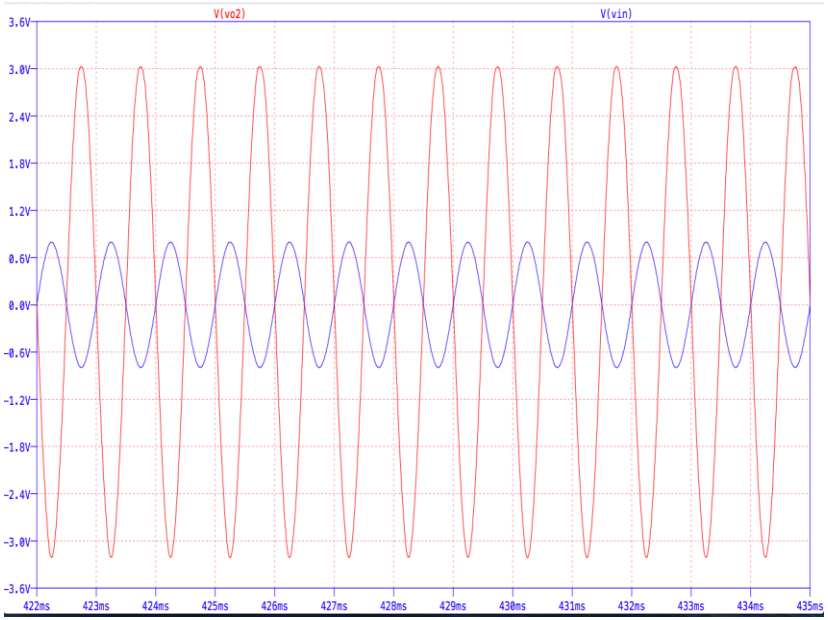
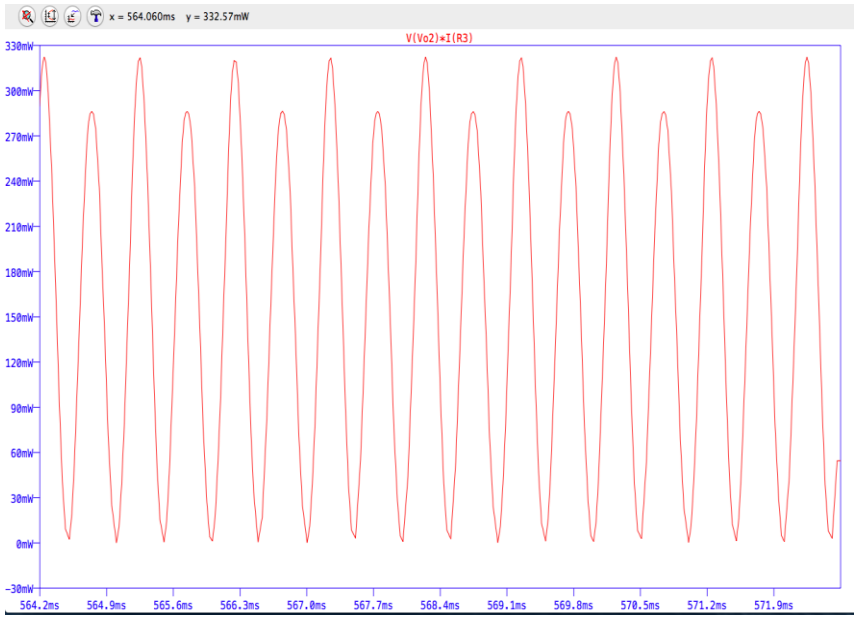
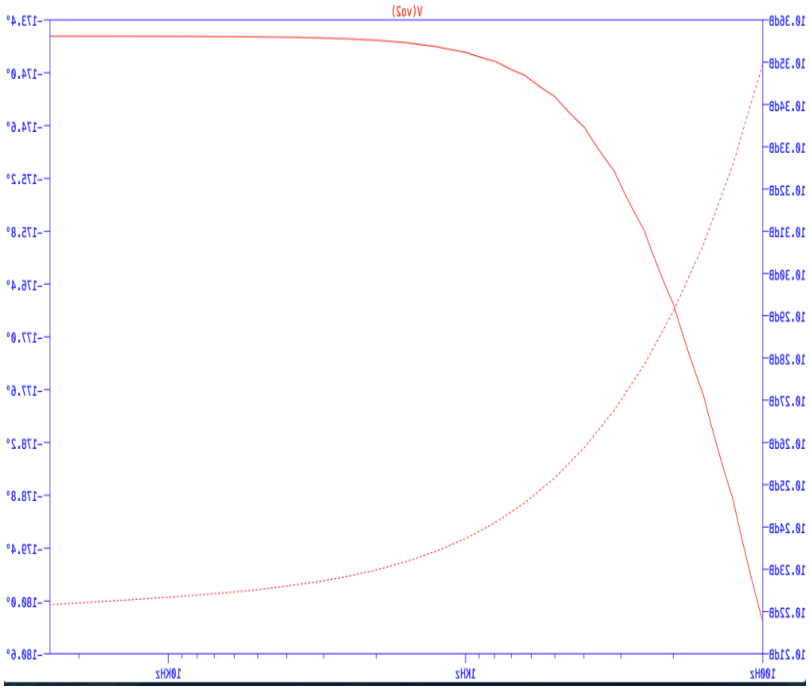
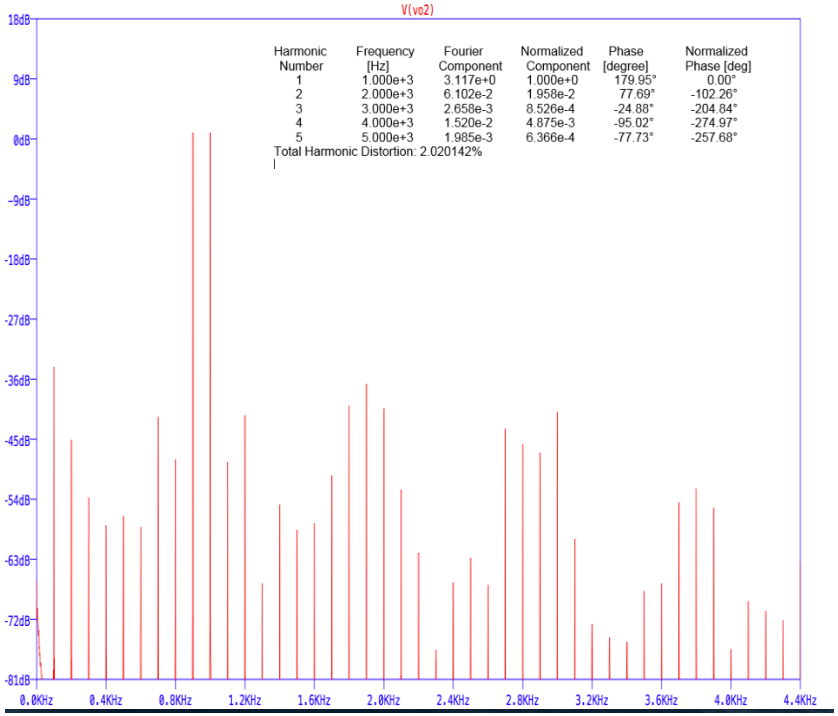
.tran 1
.ac dec .001 100 100K
.step param R 1K 2K 200











Harmonic Number	Frequency [Hz]	Fourier Component	Normalized Component	Phase [degree]	Normalized Phase [deg]
1	1.000e+3	3.117e+0	1.000e+0	179.95°	0.00°
2	2.000e+3	6.102e-2	1.958e-2	77.69°	-102.26°
3	3.000e+3	2.658e-3	8.526e-4	-24.88°	-204.84°
4	4.000e+3	1.520e-2	4.875e-3	-95.02°	-274.97°
5	5.000e+3	1.985e-3	6.366e-4	-77.73°	-257.68°

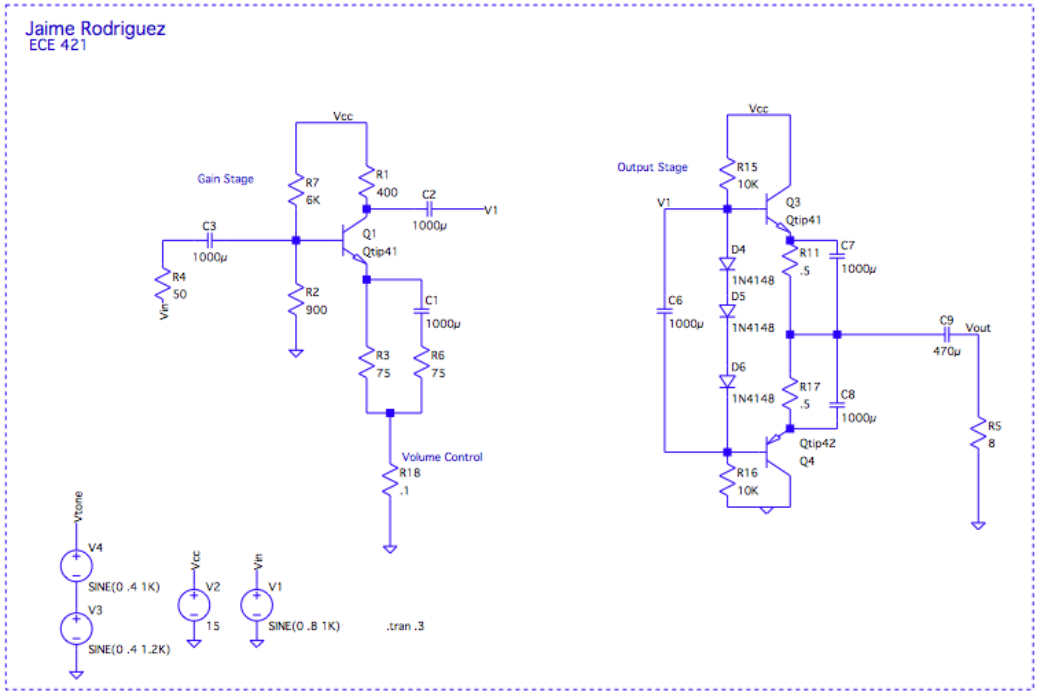
Total Harmonic Distortion: 2.020142%

Part 2 Final Report

Introduction:

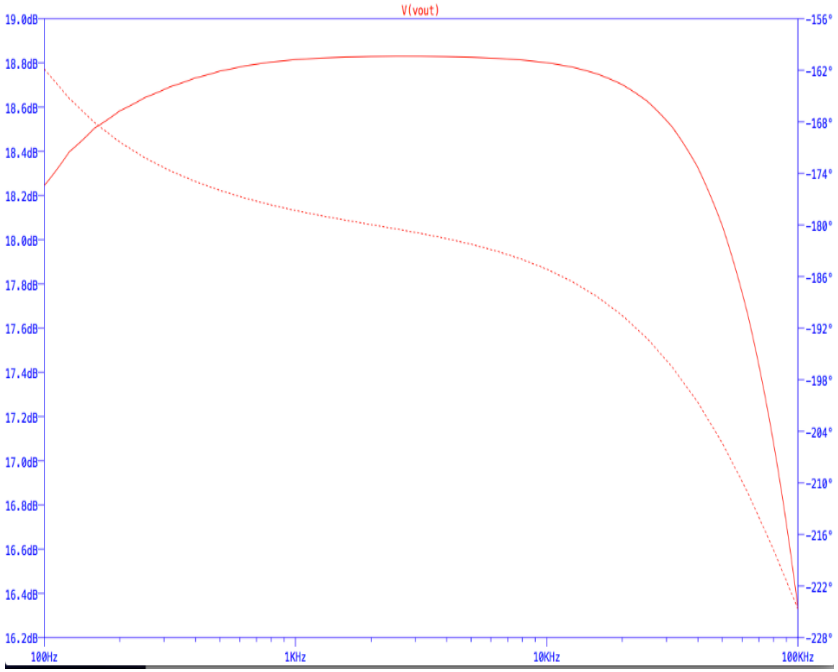
Up to this point all previous work was completed for the ECE 421 midterm but to continue where I left off I began by building and testing the designed amplifier discussed above, this turned out to be pretty straight forward and my prototype worked as expected with the exception of changing a couple resistor values to increase and match performance, I was able to achieve desired gain of 10 dB and power output of around 300mWatts. I also decided to swap out the three diodes in the output stage for a blue LED and lowering the pair of resistors in the same series was able to get it to turn on but this also lowered my gain, but I was able to balance this out by lowering the resistance in RE of my gain stage.

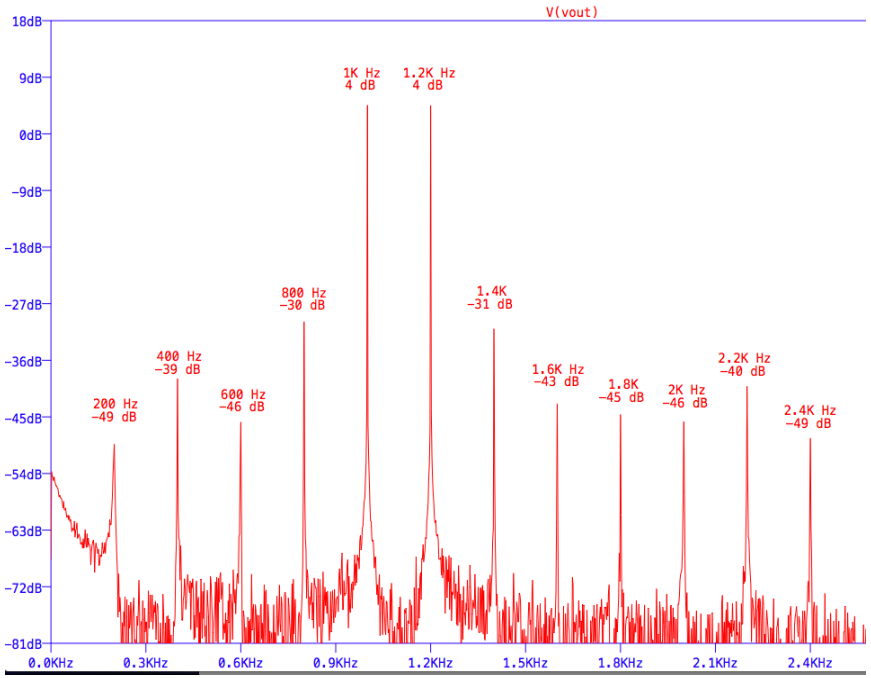
After getting to the point where I was happy with this amplifier, I started becoming greedy for more power and as I started rising the gain and power the 3904 and 3906 transistors in my output stage started burning out, so I began to experiment with Tip41 and Tip42 transistors using the same topology. First in simulation I found the model and began playing with resistor values.

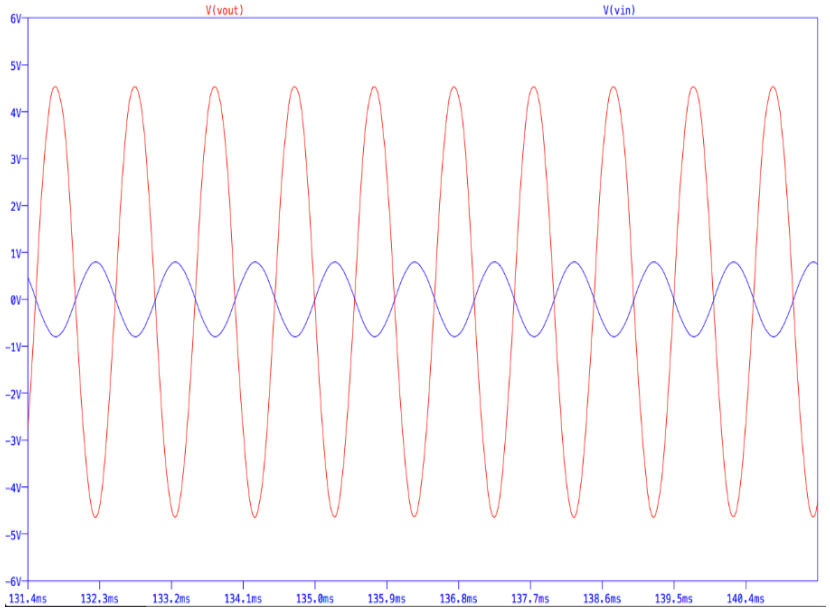


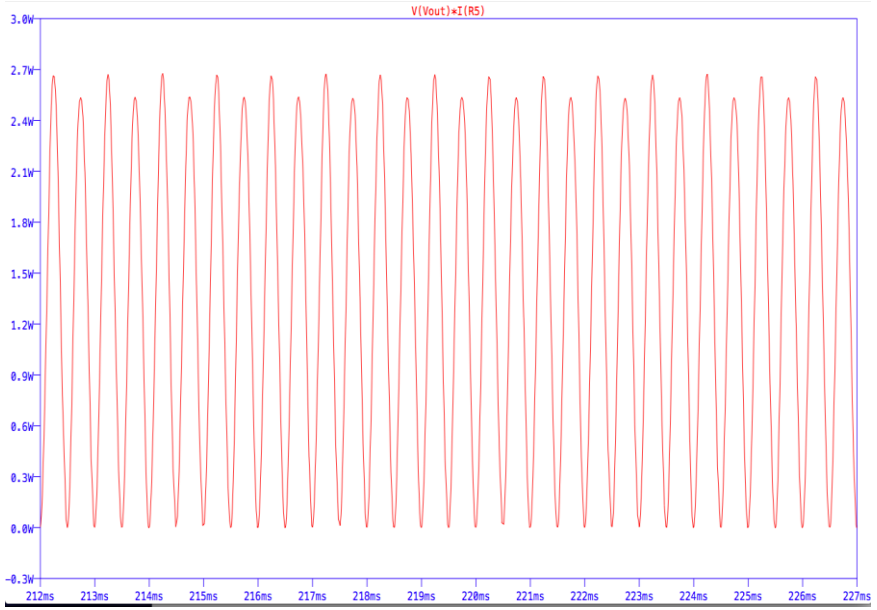
.model Qtip41 NPN(IS=7.6E-11 VAF=100 Bf=260.5 IKF=.5 XTB=.1 BR=26 CJC=1.09E-10 CJE=1.93E-10 RB=4.6 RC=0.081 RE=0.016 TR=9E-08 TF=1E-08 ITF=.001 VTF=7.15 XTF=4.07 Vceo=100 Icrating=6
.model Qtip42 PNP(IS=5.65E-10 VAF=90.67 BF=120.07 IKF=1.46 XTB=3.2 BR=2.83 CJC=1.09E-10 CJE=1.93E-10 RB=4.7 RC=0.09 RE=0.00066 TR=1E-7 TF=9.99E-09 ITF=.001 VTF=6.53 XTF=4.4 Vceo=10

This design is very similar to the previous except for the Tips and resistor values used, I was able to get a gain of around 18 dB and Power of around 2.7 Watts

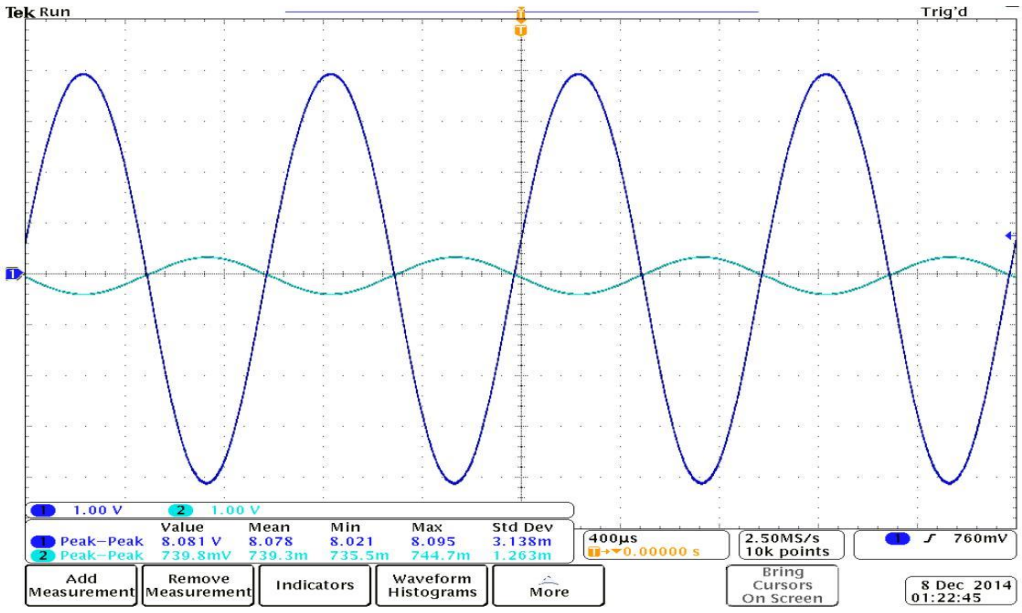

V(vout)
19.0dB
18.8dB
18.6dB
18.4dB
18.2dB
18.0dB
17.8dB
17.6dB
17.4dB
17.2dB
17.0dB
16.8dB
16.6dB
16.4dB
16.2dB
-156°
-162°
-168°
-174°
-180°
-186°
-192°
-198°
-204°
-210°
-216°
-222°
-228°
100Hz
1KHz
10KHz
100KHz


V(vout)
18dB
9dB
0dB
-9dB
-18dB
-27dB
-36dB
-45dB
-54dB
-63dB
-72dB
-81dB
200 Hz
-49 dB
400 Hz
-39 dB
600 Hz
-46 dB
800 Hz
-30 dB
1K Hz
4 dB
1.2K Hz
4 dB
1.4K
-31 dB
1.6K Hz
-43 dB
1.8K
-45 dB
2K Hz
-46 dB
2.2K Hz
-40 dB
2.4K Hz
-49 dB
0.0KHz
0.3KHz
0.6KHz
0.9KHz
1.2KHz
1.5KHz
1.8KHz
2.1KHz
2.4KHz

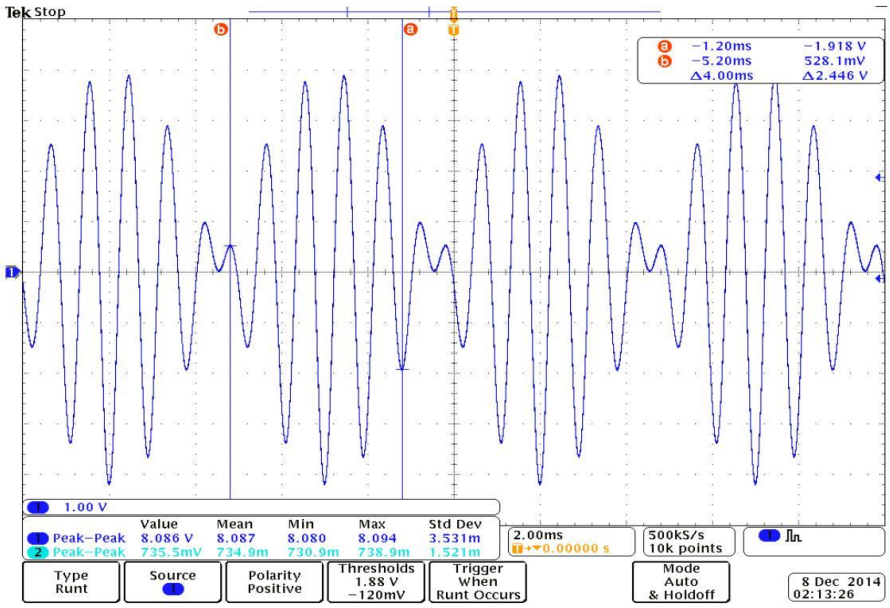

V(vout)
V(vin)
6V
5V
4V
3V
2V
1V
0V
-1V
-2V
-3V
-4V
-5V
-6V
131.4ms
132.3ms
133.2ms
134.1ms
135.0ms
135.9ms
136.8ms
137.7ms
138.6ms
139.5ms
140.4ms


V(Vout)*I(R5)
3.0W
2.7W
2.4W
2.1W
1.8W
1.5W
1.2W
0.9W
0.6W
0.3W
0.0W
-0.3W
212ms
213ms
214ms
215ms
216ms
217ms
218ms
219ms
220ms
221ms
222ms
223ms
224ms
225ms
226ms
227ms

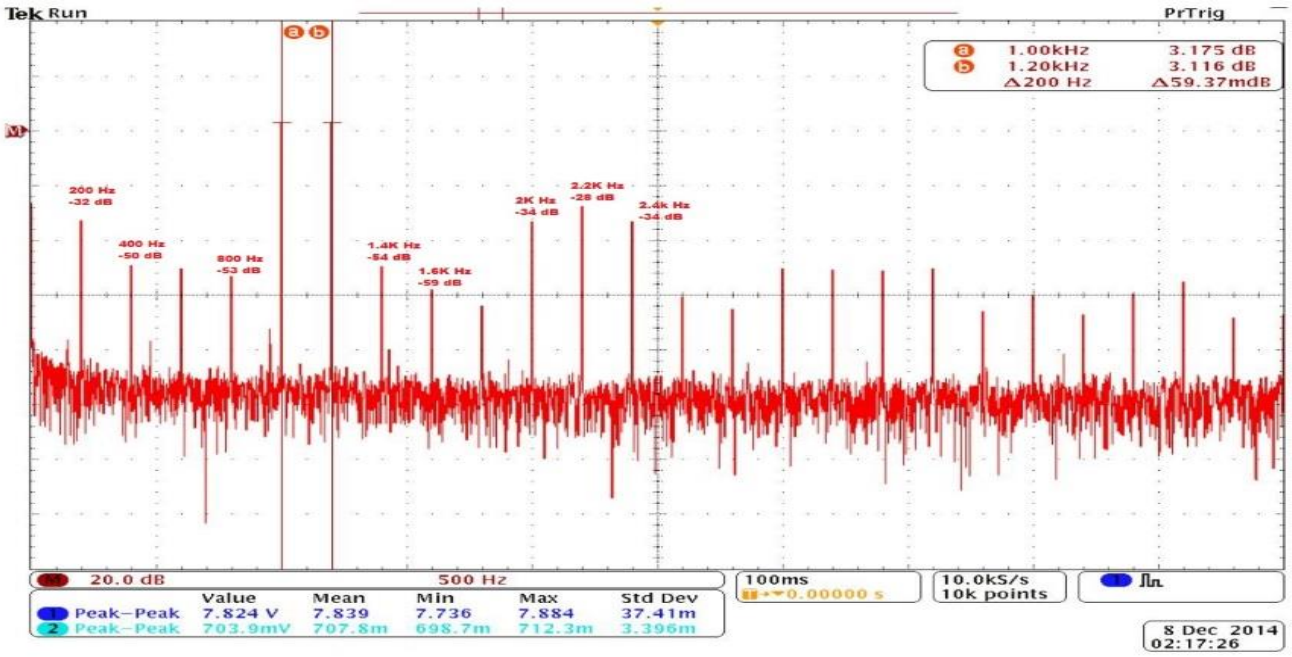
I decided to go ahead and build and test my amplifier and found to have a gain of around 20 dB power of around 1 Watt using $P = \frac{Vp^2}{2*R}$ with an 8 ohm speaker, the whole circuit is drawing about 200 mA at 15 Watts so the efficiency is about 30% not very good but I can live with this . I also tried doing a two tone distortion test like in my Ltspice simulation and found the perfomance to be very similar the 3rd harmonic is down at -56 dBc, and the 2nd is about -35dBc in my prototype vs the simulation which has -34dBc for the 3rd and -53 dBc for the 2nd ?



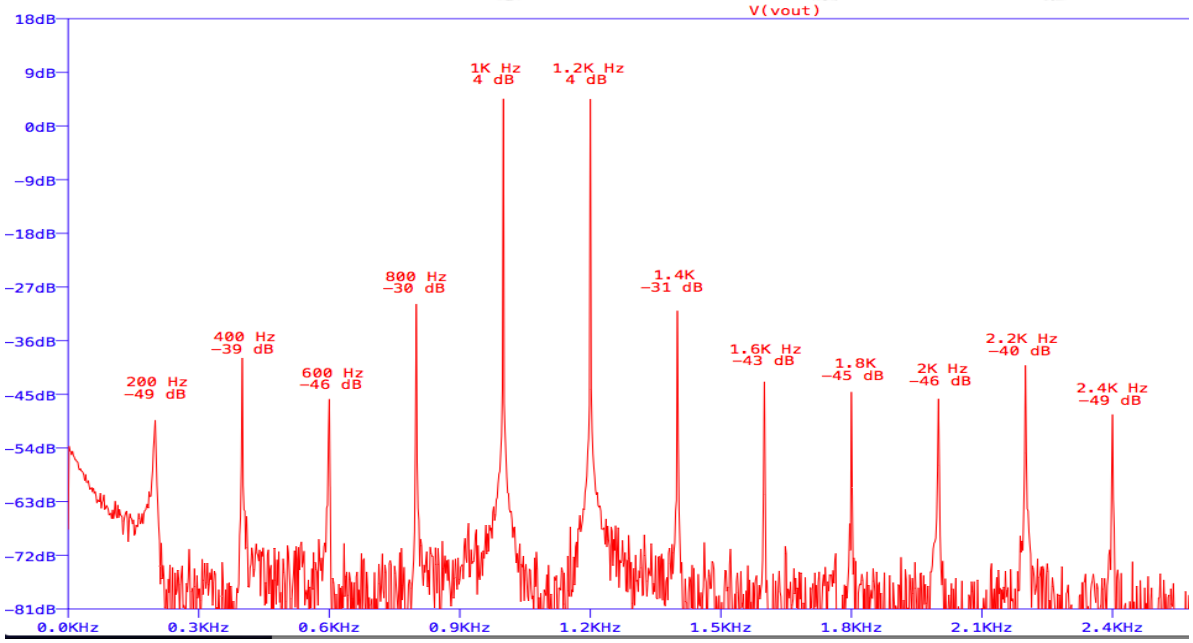
Jaime Rodriguez - 1 Watt Amp



Jaime Rodriguez- 2 tone(1K, 1.2K)



Jaime Rodriguez-2 tone (1K, 1.2K)



Conclusion

In the end I was pretty pleased with my design it sounds really great and it's too loud if turned up all the way when indoors, one thing I'm still trying to work out is getting the Led to turn on without comprising the same performance (Power Output), If I can get this to work I plan to create a more finished amplifier and solder my circuit in a Manhattan style and letting it set in a clear resin block as the picture below, the Tips get pretty warm but hopefully the resin material will act as some sort of heat sink instead of creating some funky smells!. Please give me some feedback on this because it seems like a pretty cool idea.