一、单项选择题（本大题共 10 小题，每小题 2 分，共 20 分）

提示：在每小题列出的四个备选项中只有一个是符合题目要求的，请将其代码填写在下表中。错选、多选或未选均无分。

1. The code that has an even-parity error is

(a) 1010011 (b) 1101000 (c) 1001000 (d) 1110111

2. The number 1011 in BCD is

(a). equal to decimal eight (b). equal to decimal ten (c). equal to decimal twelve (d). invalid

3. The decimal number 250 is equivalent to the binary number

(a) 11111010 (b) 11110110 (c) 11111000 (d) 11111011

4. The difference of 1000 - 100 equals

(a) 100 (b) 101 (c) 110 (d) 111

5. The BCD number for decimal 473 is

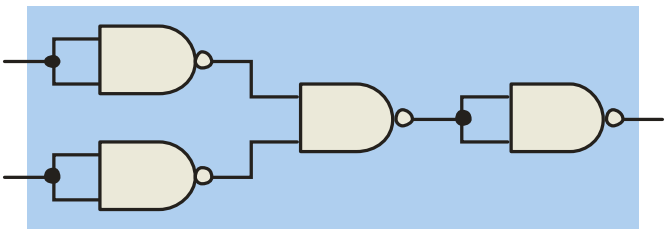
(a) 111011010 (b) 110001110011 (c) 010001110011 (d) 010011110011

6. The binary number 1000110101000110111 1 can be written in hexadecimal as

(a) AD467 (b) 8C46F (c) 8D46F (d) AE46F

7. The circuit shown is equivalent to an

(a). AND gate (b). XOR gate (c). NOR gate (d). none of the above



8. The expression A'BCD + ABCD' + AB'C'D

(a) cannot be simplified (b) can be simplified to A'BC + AB'

(c) can be simplified to ABCD' + A'BC' (d) None of these answers is correct

9. An exclusive-OR(XOR) function is expressed as

(a) A'B' + AB (b) A'B + AB' (c) (A' + B)(A + B') (d) (A' + B')(A + B)

10. A flip-flop is Toggle when

(a) J = 0, K = 0 (b) J = 0, K = 1 (c) J = 1, K = 0 (d) J = 1, K = 1

二、填空题（本大题共 9 空，每空 2 分，共 18 分）。

1. (18pts) Complete the following table of equivalent values. Use binary numbers with a sign bit and 7 bits for the value.

Decimal	Signed Magnitude	2's Complement code	1's Complement code
+56			
-32			
	10011001		

三、分析计算题（本大题共 6 小题，共 42 分）。

1. (共 5 分) Reduce the following using the Boolean algebra rules and draw the logic diagram using only NAND gates:

$$\overline{AB + AC} + \overline{A}\,\overline{B}C$$

2. (共 6 分) Implement the basic logic gates (AND, OR, NOT) only by the NOR gates respectively.

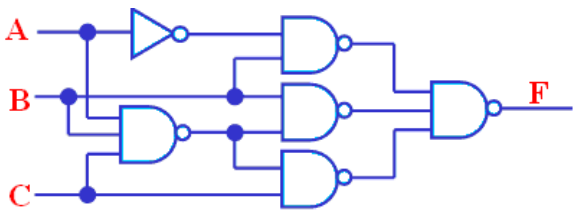
3. (共 15 分)Simplify the following expressions using Karnaugh maps.

a: f(a,b,c,d)=Σ(0,4,6,7,8,9,11,12,13,15)

b: f(w,x,y,z)= ∑(0,3,4,7,8)+ ∑d(10,11,12,13,14,15)

c: f(a,b,c,d)= a'b'c'+a'c'd+ac'd'+bc'd'+b'd'

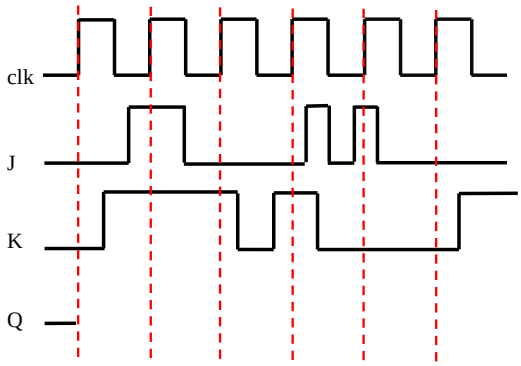
4. (共 6 分) Write the switching expressions for the following logic circuits and Simplify it.



5. (共 5 分) Using 4-1 Multiplexer to implement following expressions

$$f(a,b,c) = (a+b'+c)(a'+b)$$

6. (共 5 分) Complete the positive edge triggered JK flip-flop' timing diagram. The initial state of Q equals to 0.



四、设计题（本大题共 2 小题，共 20 分）。

1. (共 8 分) Design a two-bits adder that implements addition of two two-bits binary numbers, Construct the truth table, write out the reduced switch expressions and draw the logic diagram.

2. (共 12 分) Complete the design for the state machine described in the state diagram below.

   a) Write out the state table.

   b) Assign states using a simple binary order (ex. S0 = ABC = 000) and assign the unused states to go to State S2 as their next state if X=1 and S1 if X=0. The write out the transition table.

   c) Write out the flip-flop input excitation table assuming JK flip-flops are used.

   d) Sketch the circuit diagram.