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//
// Verilog description for cell TopLevel,
// Sun Sep 4 23:13:00 2022
//
// Precision RTL Synthesis, 64-bit 2021.2.0.8//


module TopLevel ( Reset, Start, Clk, Ack ) ;

input Reset ;
input Start ;
input Clk ;
output Ack ;

wire \PCTarg(7) , \PCTarg(0) ;
wire MemWrite;
wire RegWrEn, Jump, BranchEn, LoadInst, nx41793z13, nx31097z9, nx44004z7,
nx15592z17, nx20243z6, nx17197z11, nx10072z19, nx11069z23,
\Registers[15]_s114_rtlcGen_CrossHier_n84 ,
\Registers[14]_s115_rtlcGen_CrossHier_n85 ,
\Registers[13]_s116_rtlcGen_CrossHier_n86 ,
\Registers[12]_s117_rtlcGen_CrossHier_n87 ,
\Registers[11]_s118_rtlcGen_CrossHier_n88 ,
\Registers[10]_s119_rtlcGen_CrossHier_n89 ,
\Registers[9]_s120_rtlcGen_CrossHier_n90 ,
\Registers[8]_s121_rtlcGen_CrossHier_n91 ,
\Registers[23]_s124_rtlcGen_CrossHier_n93 ,
\Registers[22]_s125_rtlcGen_CrossHier_n94 ,
\Registers[21]_s126_rtlcGen_CrossHier_n95 ,
\Registers[20]_s127_rtlcGen_CrossHier_n96 ,
\Registers[19]_s128_rtlcGen_CrossHier_n97 ,
\Registers[18]_s129_rtlcGen_CrossHier_n98 ,
\Registers[17]_s130_rtlcGen_CrossHier_n99 ,
\Registers[16]_s131_rtlcGen_CrossHier_n100 ,
\Registers[55]_s165_rtlcGen_CrossHier_n129 ,
\Registers[54]_s166_rtlcGen_CrossHier_n130 ,
\Registers[53]_s167_rtlcGen_CrossHier_n131 ,
\Registers[52]_s168_rtlcGen_CrossHier_n132 ,
\Registers[51]_s169_rtlcGen_CrossHier_n133 ,
\Registers[50]_s170_rtlcGen_CrossHier_n134 ,
\Registers[49]_s171_rtlcGen_CrossHier_n135 ,
\Registers[48]_s172_rtlcGen_CrossHier_n136 ,
\Registers[63]_s175_rtlcGen_CrossHier_n138 ,
\Registers[62]_s176_rtlcGen_CrossHier_n139 ,
\Registers[61]_s177_rtlcGen_CrossHier_n140 ,
\Registers[60]_s178_rtlcGen_CrossHier_n141 ,
\Registers[59]_s179_rtlcGen_CrossHier_n142 ,
\Registers[58]_s180_rtlcGen_CrossHier_n143 ,
\Registers[57]_s181_rtlcGen_CrossHier_n144 ,
\Registers[56]_s182_rtlcGen_CrossHier_n145 ,
\Registers[71]_s185_rtlcGen_CrossHier_n147 ,
\Registers[70]_s186_rtlcGen_CrossHier_n148 ,
\Registers[69]_s187_rtlcGen_CrossHier_n149 ,
\Registers[68]_s188_rtlcGen_CrossHier_n150 ,
\Registers[67]_s189_rtlcGen_CrossHier_n151 ,
\Registers[66]_s190_rtlcGen_CrossHier_n152 ,
\Registers[65]_s191_rtlcGen_CrossHier_n153 ,
\Registers[64]_s192_rtlcGen_CrossHier_n154 ,
\Registers[79]_s195_rtlcGen_CrossHier_n156 ,
\Registers[78]_s196_rtlcGen_CrossHier_n157 ,
\Registers[77]_s197_rtlcGen_CrossHier_n158 ,
\Registers[76]_s198_rtlcGen_CrossHier_n159 ,
\Registers[75]_s199_rtlcGen_CrossHier_n160 ,
\Registers[74]_s200_rtlcGen_CrossHier_n161 ,
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\Registers[73]_s201_rtlcGen_CrossHier_n162 ,
\Registers[72]_s202_rtlcGen_CrossHier_n163 ,
\Registers[87]_s205_rtlcGen_CrossHier_n165 ,
\Registers[86]_s206_rtlcGen_CrossHier_n166 ,
\Registers[85]_s207_rtlcGen_CrossHier_n167 ,
\Registers[84]_s208_rtlcGen_CrossHier_n168 ,
\Registers[83]_s209_rtlcGen_CrossHier_n169 ,
\Registers[82]_s210_rtlcGen_CrossHier_n170 ,
\Registers[81]_s211_rtlcGen_CrossHier_n171 ,
\Registers[80]_s212_rtlcGen_CrossHier_n172 ,
\Registers[95]_s215_rtlcGen_CrossHier_n174 ,
\Registers[94]_s216_rtlcGen_CrossHier_n175 ,
\Registers[93]_s217_rtlcGen_CrossHier_n176 ,
\Registers[92]_s218_rtlcGen_CrossHier_n177 ,
\Registers[91]_s219_rtlcGen_CrossHier_n178 ,
\Registers[90]_s220_rtlcGen_CrossHier_n179 ,
\Registers[89]_s221_rtlcGen_CrossHier_n180 ,
\Registers[88]_s222_rtlcGen_CrossHier_n181 ,
\Registers[103]_s225_rtlcGen_CrossHier_n183 ,
\Registers[102]_s226_rtlcGen_CrossHier_n184 ,
\Registers[101]_s227_rtlcGen_CrossHier_n185 ,
\Registers[100]_s228_rtlcGen_CrossHier_n186 ,
\Registers[99]_s229_rtlcGen_CrossHier_n187 ,
\Registers[98]_s230_rtlcGen_CrossHier_n188 ,
\Registers[97]_s231_rtlcGen_CrossHier_n189 ,
\Registers[96]_s232_rtlcGen_CrossHier_n190 ,
\Registers[111]_s235_rtlcGen_CrossHier_n192 ,
\Registers[110]_s236_rtlcGen_CrossHier_n193 ,
\Registers[109]_s237_rtlcGen_CrossHier_n194 ,
\Registers[108]_s238_rtlcGen_CrossHier_n195 ,
\Registers[107]_s239_rtlcGen_CrossHier_n196 ,
\Registers[106]_s240_rtlcGen_CrossHier_n197 ,
\Registers[105]_s241_rtlcGen_CrossHier_n198 ,
\Registers[104]_s242_rtlcGen_CrossHier_n199 ,
\Registers[119]_s245_rtlcGen_CrossHier_n201 ,
\Registers[118]_s246_rtlcGen_CrossHier_n202 ,
\Registers[117]_s247_rtlcGen_CrossHier_n203 ,
\Registers[116]_s248_rtlcGen_CrossHier_n204 ,
\Registers[115]_s249_rtlcGen_CrossHier_n205 ,
\Registers[114]_s250_rtlcGen_CrossHier_n206 ,
\Registers[113]_s251_rtlcGen_CrossHier_n207 ,
\Registers[112]_s252_rtlcGen_CrossHier_n208 , \ALU1_Out_0n1s2(8) ;
wire [7:0]ALU1_Out_0n1s6;
wire sload_mux_0_dup_123, nx8474z1, sload_mux_1_dup_124, nx8475z1,
sload_mux_2_dup_125, nx8476z1, sload_mux_3_dup_126, nx8477z1,
sload_mux_4_dup_127, nx8478z1, sload_mux_5_dup_128, nx8479z1,
sload_mux_6_dup_129, nx51681z1, sload_mux_7_dup_130, nx8481z1,
sload_mux_8_dup_131, nx51679z1, sload_mux_9_dup_132, nx2749z1, nx2748z1,
nx2747z1, nx2746z1, nx2745z1, nx2744z1, nx2743z1, nx2633z1, Reset_int,
Start_int;
wire Clk_int;
wire CrossHierIn_0, CrossHierIn_1, CrossHierIn_2, CrossHierIn_3,
CrossHierIn_4, CrossHierIn_5, CrossHierIn_6, CrossHierIn_7, nx9884z1,
nx31097z1, nx44004z1, nx15592z1, nx20243z1, nx17197z1, nx10072z1,
nx11069z6, nx2633z2, nx2747z2, nx2748z2, nx2750z1, nx61537z1, nx50058z1,
nx36542z1, nx43600z1, nx55451z1, nx42063z1, nx8480z1, nx8480z2,
nx51682z1, nx51684z1, nx51685z1, nx51687z1, nx51688z1, nx53265z1,
nx26451z17, nx26451z16, nx26451z14, nx26451z13, nx26451z12, nx26451z11,
nx26451z10, nx26451z9, nx26451z3, nx50624z1, nx38036z1, nx38036z5,
nx38036z6, nx38036z9, nx38036z7, nx38036z8, nx38036z10, nx55346z1,
nx11069z1, nx9652z1, nx57760z1, nx31844z1, nx19493z1, nx4575z1,
nx4450z1, nx53557z1, nx36047z1, nx5421z1, nx21647z1, nx41793z1,
nx41793z2, nx41793z12, nx31097z2, nx31097z8, nx31097z5, nx31097z7,
nx44004z2, nx44004z3, nx44004z6, nx15592z2, nx15592z16, nx15592z11,
nx15592z12, nx20243z2, nx20243z3, nx17197z2, nx17197z10, nx10072z2,
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nx10072z13, nx10072z18, nx38036z2, nx41793z11, nx38036z3, nx38036z4,
nx31097z6, nx11069z7, nx11069z22, nx11069z21, nx11069z20, nx49419z1,
nx31844z2, nx49419z2, nx2743z2, nx50624z2, nx2631z1, nx10072z3,
nx2745z2, nx2745z3, nx2746z2, nx2747z3, nx2749z2, nx2750z2, nx50624z3,
nx50624z4, nx50624z6, nx50624z5, nx36542z8, nx36542z10, nx36542z12,
nx36542z11, nx36542z9, nx11069z2, nx11069z3, nx11069z5, nx11069z4,
nx36542z2, nx36542z3, nx36542z7, nx36542z6, nx36542z13, nx36542z15,
nx36542z14, nx45966z1, nx51679z2, nx51680z1, nx10072z12, nx51683z1,
nx2746z3, nx51686z1, nx2748z3, nx2749z8, nx8473z1, nx26451z8, nx31097z3,
nx41793z7, nx41793z10, nx41793z9, nx41793z8, nx41793z3, nx41793z5,
nx41793z4, nx41793z6, nx31097z4, nx26451z7, nx2749z3, nx2749z6,
nx2749z7, nx2749z4, nx2749z5, nx44004z4, nx44004z5, nx26451z6,
nx15592z3, nx15592z9, nx15592z10, nx15592z7, nx15592z6, nx15592z5,
nx15592z4, nx26451z5, nx20243z4, nx15592z15, nx15592z14, nx15592z13,
nx20243z5, nx2747z4, nx2747z5, nx26451z4, nx17197z3, nx17197z8,
nx17197z7, nx17197z9, nx17197z6, nx17197z4, nx17197z5, nx11069z15,
nx10072z14, nx10072z17, nx10072z16, nx10072z15, nx11069z16, nx11069z19,
nx11069z18, nx11069z17, nx26451z2, nx26451z15, nx10072z8, nx10072z11,
nx10072z10, nx10072z9, nx10072z5, nx10072z7, nx10072z6, nx10072z4,
nx26451z1, nx11069z8, nx51685z2, nx45966z4, nx45966z6, nx45966z5,
nx51685z3, nx51685z5, nx11069z13, nx15592z8, nx11069z12, nx11069z11,
nx11069z9, nx11069z10, nx45966z2, nx51684z2, nx11069z14, nx45966z3,
nx51684z3, nx51684z9, nx51684z8, nx51684z7, nx51684z6, nx51684z5,
nx51684z4, nx51683z2, nx51683z3, nx51683z5, nx2747z6, nx51683z4,
nx51687z2, nx51682z2, nx36542z5, nx51687z4, nx36542z4, nx55346z2,
nx51687z3, nx51685z4, nx51682z3, nx42063z2, nx1629;
wire [9:0]PgmCtr;
wire \DM1_MSR__DataMem_core_5_rtlc_sync_msr_n3_rtlcGen2(128) ;
wire Zq, SCq;
wire [34:0] \$dummy ;




ram_dq_8_0 core (.wr_data1 ({nx26451z1,nx26451z2,nx26451z3,nx26451z4,
nx26451z5,nx26451z6,nx26451z7,nx26451z8}), .addr1 ({\$dummy [0],
nx26451z9,\$dummy [1],nx26451z10,nx26451z11,nx26451z12,nx26451z13
,nx26451z14}), .wr_clk1 (Clk_int), .rd_data2 ({nx11069z23,
nx10072z19,nx17197z11,nx20243z6,nx15592z17,nx44004z7,nx31097z9,
nx41793z13}), .addr2 ({nx11069z8,nx26451z15,nx11069z15,nx17197z3,
nx26451z16,nx15592z3,nx26451z17,nx31097z3}), .p_MemWrite (
MemWrite), .p_Reset_int (Reset_int)) ;
XORCY xorcy_0 (.O (sload_mux_0_dup_123), .CI (nx8473z1), .LI (nx51688z1)) ;
XORCY xorcy_1 (.O (sload_mux_1_dup_124), .CI (nx8474z1), .LI (nx51687z1)) ;
XORCY xorcy_2 (.O (sload_mux_2_dup_125), .CI (nx8475z1), .LI (nx51686z1)) ;
XORCY xorcy_3 (.O (sload_mux_3_dup_126), .CI (nx8476z1), .LI (nx51685z1)) ;
XORCY xorcy_4 (.O (sload_mux_4_dup_127), .CI (nx8477z1), .LI (nx51684z1)) ;
XORCY xorcy_5 (.O (sload_mux_5_dup_128), .CI (nx8478z1), .LI (nx51683z1)) ;
XORCY xorcy_6 (.O (sload_mux_6_dup_129), .CI (nx8479z1), .LI (nx51682z1)) ;
XORCY xorcy_7 (.O (sload_mux_7_dup_130), .CI (nx51681z1), .LI (nx8480z2)) ;
XORCY xorcy_8 (.O (sload_mux_8_dup_131), .CI (nx8481z1), .LI (nx51680z1)) ;
XORCY xorcy_9 (.O (sload_mux_9_dup_132), .CI (nx51679z1), .LI (nx51679z2)) ;
(* IS_INTERNAL_DONT_TOUCH = "true" *)
INV \ix406_PCTarg(7) (.O (\PCTarg(7) ), .I (nx42063z1)) ;
(* IS_INTERNAL_DONT_TOUCH = "true" *)
INV \ix448_PCTarg(0) (.O (\PCTarg(0) ), .I (nx45966z1)) ;
(* IS_INTERNAL_DONT_TOUCH = "true" *)
INV ix454_LoadInst (.O (LoadInst), .I (nx55451z1)) ;
(* IS_INTERNAL_DONT_TOUCH = "true" *)
INV ix460_MemWrite (.O (MemWrite), .I (nx43600z1)) ;
(* IS_INTERNAL_DONT_TOUCH = "true" *)
INV ix466_RegWrEn (.O (RegWrEn), .I (nx36542z1)) ;
(* IS_INTERNAL_DONT_TOUCH = "true" *)
INV ix472_BranchEn (.O (BranchEn), .I (nx50058z1)) ;
(* IS_INTERNAL_DONT_TOUCH = "true" *)
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INV ix478_Jump (.O (Jump), .I (nx61537z1)) ;
XORCY ALU1_Out_addsub9_0i1_xorcy_0 (.O (ALU1_Out_0n1s6[0]), .CI (nx2750z1),
.LI (nx2750z2)) ;
XORCY ALU1_Out_addsub9_0i1_xorcy_1 (.O (ALU1_Out_0n1s6[1]), .CI (nx2749z1),
.LI (nx2749z2)) ;
XORCY ALU1_Out_addsub9_0i1_xorcy_2 (.O (ALU1_Out_0n1s6[2]), .CI (nx2748z1),
.LI (nx2748z2)) ;
XORCY ALU1_Out_addsub9_0i1_xorcy_3 (.O (ALU1_Out_0n1s6[3]), .CI (nx2747z1),
.LI (nx2747z2)) ;
XORCY ALU1_Out_addsub9_0i1_xorcy_4 (.O (ALU1_Out_0n1s6[4]), .CI (nx2746z1),
.LI (nx2746z2)) ;
XORCY ALU1_Out_addsub9_0i1_xorcy_5 (.O (ALU1_Out_0n1s6[5]), .CI (nx2745z1),
.LI (nx2745z2)) ;
XORCY ALU1_Out_addsub9_0i1_xorcy_6 (.O (ALU1_Out_0n1s6[6]), .CI (nx2744z1),
.LI (nx2631z1)) ;
XORCY ALU1_Out_addsub9_0i1_xorcy_7 (.O (ALU1_Out_0n1s6[7]), .CI (nx2743z1),
.LI (nx2743z2)) ;
XORCY ALU1_Out_addsub9_0i1_xorcy_8 (.O (\ALU1_Out_0n1s2(8) ), .CI (nx2633z1
), .LI (nx2633z2)) ;
FDRE \reg_Registers[15]_s114_rtlcGen_CrossHier_n84 (.Q (
\Registers[15]_s114_rtlcGen_CrossHier_n84 ), .C (Clk_int), .CE (
nx49419z1), .D (nx11069z6), .R (Reset_int)) ;
FDRE \reg_Registers[14]_s115_rtlcGen_CrossHier_n85 (.Q (
\Registers[14]_s115_rtlcGen_CrossHier_n85 ), .C (Clk_int), .CE (
nx49419z1), .D (nx10072z1), .R (Reset_int)) ;
FDRE \reg_Registers[13]_s116_rtlcGen_CrossHier_n86 (.Q (
\Registers[13]_s116_rtlcGen_CrossHier_n86 ), .C (Clk_int), .CE (
nx49419z1), .D (nx17197z1), .R (Reset_int)) ;
FDRE \reg_Registers[12]_s117_rtlcGen_CrossHier_n87 (.Q (
\Registers[12]_s117_rtlcGen_CrossHier_n87 ), .C (Clk_int), .CE (
nx49419z1), .D (nx20243z1), .R (Reset_int)) ;
FDRE \reg_Registers[11]_s118_rtlcGen_CrossHier_n88 (.Q (
\Registers[11]_s118_rtlcGen_CrossHier_n88 ), .C (Clk_int), .CE (
nx49419z1), .D (nx15592z1), .R (Reset_int)) ;
FDRE \reg_Registers[10]_s119_rtlcGen_CrossHier_n89 (.Q (
\Registers[10]_s119_rtlcGen_CrossHier_n89 ), .C (Clk_int), .CE (
nx49419z1), .D (nx44004z1), .R (Reset_int)) ;
FDRE \reg_Registers[9]_s120_rtlcGen_CrossHier_n90 (.Q (
\Registers[9]_s120_rtlcGen_CrossHier_n90 ), .C (Clk_int), .CE (
nx49419z1), .D (nx31097z1), .R (Reset_int)) ;
FDRE \reg_Registers[8]_s121_rtlcGen_CrossHier_n91 (.Q (
\Registers[8]_s121_rtlcGen_CrossHier_n91 ), .C (Clk_int), .CE (
nx49419z1), .D (nx41793z1), .R (Reset_int)) ;
FDRE \reg_Registers[23]_s124_rtlcGen_CrossHier_n93 (.Q (
\Registers[23]_s124_rtlcGen_CrossHier_n93 ), .C (Clk_int), .CE (
nx21647z1), .D (nx11069z6), .R (Reset_int)) ;
FDRE \reg_Registers[22]_s125_rtlcGen_CrossHier_n94 (.Q (
\Registers[22]_s125_rtlcGen_CrossHier_n94 ), .C (Clk_int), .CE (
nx21647z1), .D (nx10072z1), .R (Reset_int)) ;
FDRE \reg_Registers[21]_s126_rtlcGen_CrossHier_n95 (.Q (
\Registers[21]_s126_rtlcGen_CrossHier_n95 ), .C (Clk_int), .CE (
nx21647z1), .D (nx17197z1), .R (Reset_int)) ;
FDRE \reg_Registers[20]_s127_rtlcGen_CrossHier_n96 (.Q (
\Registers[20]_s127_rtlcGen_CrossHier_n96 ), .C (Clk_int), .CE (
nx21647z1), .D (nx20243z1), .R (Reset_int)) ;
FDRE \reg_Registers[19]_s128_rtlcGen_CrossHier_n97 (.Q (
\Registers[19]_s128_rtlcGen_CrossHier_n97 ), .C (Clk_int), .CE (
nx21647z1), .D (nx15592z1), .R (Reset_int)) ;
FDRE \reg_Registers[18]_s129_rtlcGen_CrossHier_n98 (.Q (
\Registers[18]_s129_rtlcGen_CrossHier_n98 ), .C (Clk_int), .CE (
nx21647z1), .D (nx44004z1), .R (Reset_int)) ;
FDRE \reg_Registers[17]_s130_rtlcGen_CrossHier_n99 (.Q (
\Registers[17]_s130_rtlcGen_CrossHier_n99 ), .C (Clk_int), .CE (
nx21647z1), .D (nx31097z1), .R (Reset_int)) ;
FDRE \reg_Registers[16]_s131_rtlcGen_CrossHier_n100 (.Q (
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  \Registers[16]_s131_rtlcGen_CrossHier_n100 ), .C (Clk_int), .CE (
  nx21647z1), .D (nx41793z1), .R (Reset_int)) ;
  FDRE \reg_Registers[55]_s165_rtlcGen_CrossHier_n129 (.Q (
  \Registers[55]_s165_rtlcGen_CrossHier_n129 ), .C (Clk_int), .CE (
  nx5421z1), .D (nx11069z6), .R (Reset_int)) ;
  FDRE \reg_Registers[54]_s166_rtlcGen_CrossHier_n130 (.Q (
  \Registers[54]_s166_rtlcGen_CrossHier_n130 ), .C (Clk_int), .CE (
  nx5421z1), .D (nx10072z1), .R (Reset_int)) ;
  FDRE \reg_Registers[53]_s167_rtlcGen_CrossHier_n131 (.Q (
  \Registers[53]_s167_rtlcGen_CrossHier_n131 ), .C (Clk_int), .CE (
  nx5421z1), .D (nx17197z1), .R (Reset_int)) ;
  FDRE \reg_Registers[52]_s168_rtlcGen_CrossHier_n132 (.Q (
  \Registers[52]_s168_rtlcGen_CrossHier_n132 ), .C (Clk_int), .CE (
  nx5421z1), .D (nx20243z1), .R (Reset_int)) ;
  FDRE \reg_Registers[51]_s169_rtlcGen_CrossHier_n133 (.Q (
  \Registers[51]_s169_rtlcGen_CrossHier_n133 ), .C (Clk_int), .CE (
  nx5421z1), .D (nx15592z1), .R (Reset_int)) ;
  FDRE \reg_Registers[50]_s170_rtlcGen_CrossHier_n134 (.Q (
  \Registers[50]_s170_rtlcGen_CrossHier_n134 ), .C (Clk_int), .CE (
  nx5421z1), .D (nx44004z1), .R (Reset_int)) ;
  FDRE \reg_Registers[49]_s171_rtlcGen_CrossHier_n135 (.Q (
  \Registers[49]_s171_rtlcGen_CrossHier_n135 ), .C (Clk_int), .CE (
  nx5421z1), .D (nx31097z1), .R (Reset_int)) ;
  FDRE \reg_Registers[48]_s172_rtlcGen_CrossHier_n136 (.Q (
  \Registers[48]_s172_rtlcGen_CrossHier_n136 ), .C (Clk_int), .CE (
  nx5421z1), .D (nx41793z1), .R (Reset_int)) ;
  FDRE \reg_Registers[63]_s175_rtlcGen_CrossHier_n138 (.Q (
  \Registers[63]_s175_rtlcGen_CrossHier_n138 ), .C (Clk_int), .CE (
  nx36047z1), .D (nx11069z6), .R (Reset_int)) ;
  FDRE \reg_Registers[62]_s176_rtlcGen_CrossHier_n139 (.Q (
  \Registers[62]_s176_rtlcGen_CrossHier_n139 ), .C (Clk_int), .CE (
  nx36047z1), .D (nx10072z1), .R (Reset_int)) ;
  FDRE \reg_Registers[61]_s177_rtlcGen_CrossHier_n140 (.Q (
  \Registers[61]_s177_rtlcGen_CrossHier_n140 ), .C (Clk_int), .CE (
  nx36047z1), .D (nx17197z1), .R (Reset_int)) ;
  FDRE \reg_Registers[60]_s178_rtlcGen_CrossHier_n141 (.Q (
  \Registers[60]_s178_rtlcGen_CrossHier_n141 ), .C (Clk_int), .CE (
  nx36047z1), .D (nx20243z1), .R (Reset_int)) ;
  FDRE \reg_Registers[59]_s179_rtlcGen_CrossHier_n142 (.Q (
  \Registers[59]_s179_rtlcGen_CrossHier_n142 ), .C (Clk_int), .CE (
  nx36047z1), .D (nx15592z1), .R (Reset_int)) ;
  FDRE \reg_Registers[58]_s180_rtlcGen_CrossHier_n143 (.Q (
  \Registers[58]_s180_rtlcGen_CrossHier_n143 ), .C (Clk_int), .CE (
  nx36047z1), .D (nx44004z1), .R (Reset_int)) ;
  FDRE \reg_Registers[57]_s181_rtlcGen_CrossHier_n144 (.Q (
  \Registers[57]_s181_rtlcGen_CrossHier_n144 ), .C (Clk_int), .CE (
  nx36047z1), .D (nx31097z1), .R (Reset_int)) ;
  FDRE \reg_Registers[56]_s182_rtlcGen_CrossHier_n145 (.Q (
  \Registers[56]_s182_rtlcGen_CrossHier_n145 ), .C (Clk_int), .CE (
  nx36047z1), .D (nx41793z1), .R (Reset_int)) ;
  FDRE \reg_Registers[71]_s185_rtlcGen_CrossHier_n147 (.Q (
  \Registers[71]_s185_rtlcGen_CrossHier_n147 ), .C (Clk_int), .CE (
  nx53557z1), .D (nx11069z6), .R (Reset_int)) ;
  FDRE \reg_Registers[70]_s186_rtlcGen_CrossHier_n148 (.Q (
  \Registers[70]_s186_rtlcGen_CrossHier_n148 ), .C (Clk_int), .CE (
  nx53557z1), .D (nx10072z1), .R (Reset_int)) ;
  FDRE \reg_Registers[69]_s187_rtlcGen_CrossHier_n149 (.Q (
  \Registers[69]_s187_rtlcGen_CrossHier_n149 ), .C (Clk_int), .CE (
  nx53557z1), .D (nx17197z1), .R (Reset_int)) ;
  FDRE \reg_Registers[68]_s188_rtlcGen_CrossHier_n150 (.Q (
  \Registers[68]_s188_rtlcGen_CrossHier_n150 ), .C (Clk_int), .CE (
  nx53557z1), .D (nx20243z1), .R (Reset_int)) ;
  FDRE \reg_Registers[67]_s189_rtlcGen_CrossHier_n151 (.Q (
  \Registers[67]_s189_rtlcGen_CrossHier_n151 ), .C (Clk_int), .CE (
  nx53557z1), .D (nx15592z1), .R (Reset_int)) ;
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FDRE \reg_Registers[66]_s190_rtlcGen_CrossHier_n152 (.Q (
\Registers[66]_s190_rtlcGen_CrossHier_n152 ), .C (Clk_int), .CE (
nx53557z1), .D (nx44004z1), .R (Reset_int)) ;
FDRE \reg_Registers[65]_s191_rtlcGen_CrossHier_n153 (.Q (
\Registers[65]_s191_rtlcGen_CrossHier_n153 ), .C (Clk_int), .CE (
nx53557z1), .D (nx31097z1), .R (Reset_int)) ;
FDSE \reg_Registers[64]_s192_rtlcGen_CrossHier_n154 (.Q (
\Registers[64]_s192_rtlcGen_CrossHier_n154 ), .C (Clk_int), .CE (
nx53557z1), .D (nx41793z1), .S (Reset_int)) ;
FDRE \reg_Registers[79]_s195_rtlcGen_CrossHier_n156 (.Q (
\Registers[79]_s195_rtlcGen_CrossHier_n156 ), .C (Clk_int), .CE (
nx4450z1), .D (nx11069z6), .R (Reset_int)) ;
FDRE \reg_Registers[78]_s196_rtlcGen_CrossHier_n157 (.Q (
\Registers[78]_s196_rtlcGen_CrossHier_n157 ), .C (Clk_int), .CE (
nx4450z1), .D (nx10072z1), .R (Reset_int)) ;
FDRE \reg_Registers[77]_s197_rtlcGen_CrossHier_n158 (.Q (
\Registers[77]_s197_rtlcGen_CrossHier_n158 ), .C (Clk_int), .CE (
nx4450z1), .D (nx17197z1), .R (Reset_int)) ;
FDRE \reg_Registers[76]_s198_rtlcGen_CrossHier_n159 (.Q (
\Registers[76]_s198_rtlcGen_CrossHier_n159 ), .C (Clk_int), .CE (
nx4450z1), .D (nx20243z1), .R (Reset_int)) ;
FDRE \reg_Registers[75]_s199_rtlcGen_CrossHier_n160 (.Q (
\Registers[75]_s199_rtlcGen_CrossHier_n160 ), .C (Clk_int), .CE (
nx4450z1), .D (nx15592z1), .R (Reset_int)) ;
FDRE \reg_Registers[74]_s200_rtlcGen_CrossHier_n161 (.Q (
\Registers[74]_s200_rtlcGen_CrossHier_n161 ), .C (Clk_int), .CE (
nx4450z1), .D (nx44004z1), .R (Reset_int)) ;
FDRE \reg_Registers[73]_s201_rtlcGen_CrossHier_n162 (.Q (
\Registers[73]_s201_rtlcGen_CrossHier_n162 ), .C (Clk_int), .CE (
nx4450z1), .D (nx31097z1), .R (Reset_int)) ;
FDRE \reg_Registers[72]_s202_rtlcGen_CrossHier_n163 (.Q (
\Registers[72]_s202_rtlcGen_CrossHier_n163 ), .C (Clk_int), .CE (
nx4450z1), .D (nx41793z1), .R (Reset_int)) ;
FDSE \reg_Registers[87]_s205_rtlcGen_CrossHier_n165 (.Q (
\Registers[87]_s205_rtlcGen_CrossHier_n165 ), .C (Clk_int), .CE (
nx4575z1), .D (nx11069z6), .S (Reset_int)) ;
FDSE \reg_Registers[86]_s206_rtlcGen_CrossHier_n166 (.Q (
\Registers[86]_s206_rtlcGen_CrossHier_n166 ), .C (Clk_int), .CE (
nx4575z1), .D (nx10072z1), .S (Reset_int)) ;
FDSE \reg_Registers[85]_s207_rtlcGen_CrossHier_n167 (.Q (
\Registers[85]_s207_rtlcGen_CrossHier_n167 ), .C (Clk_int), .CE (
nx4575z1), .D (nx17197z1), .S (Reset_int)) ;
FDSE \reg_Registers[84]_s208_rtlcGen_CrossHier_n168 (.Q (
\Registers[84]_s208_rtlcGen_CrossHier_n168 ), .C (Clk_int), .CE (
nx4575z1), .D (nx20243z1), .S (Reset_int)) ;
FDSE \reg_Registers[83]_s209_rtlcGen_CrossHier_n169 (.Q (
\Registers[83]_s209_rtlcGen_CrossHier_n169 ), .C (Clk_int), .CE (
nx4575z1), .D (nx15592z1), .S (Reset_int)) ;
FDSE \reg_Registers[82]_s210_rtlcGen_CrossHier_n170 (.Q (
\Registers[82]_s210_rtlcGen_CrossHier_n170 ), .C (Clk_int), .CE (
nx4575z1), .D (nx44004z1), .S (Reset_int)) ;
FDSE \reg_Registers[81]_s211_rtlcGen_CrossHier_n171 (.Q (
\Registers[81]_s211_rtlcGen_CrossHier_n171 ), .C (Clk_int), .CE (
nx4575z1), .D (nx31097z1), .S (Reset_int)) ;
FDSE \reg_Registers[80]_s212_rtlcGen_CrossHier_n172 (.Q (
\Registers[80]_s212_rtlcGen_CrossHier_n172 ), .C (Clk_int), .CE (
nx4575z1), .D (nx41793z1), .S (Reset_int)) ;
FDRE \reg_Registers[95]_s215_rtlcGen_CrossHier_n174 (.Q (
\Registers[95]_s215_rtlcGen_CrossHier_n174 ), .C (Clk_int), .CE (
nx19493z1), .D (nx11069z6), .R (Reset_int)) ;
FDSE \reg_Registers[94]_s216_rtlcGen_CrossHier_n175 (.Q (
\Registers[94]_s216_rtlcGen_CrossHier_n175 ), .C (Clk_int), .CE (
nx19493z1), .D (nx10072z1), .S (Reset_int)) ;
FDRE \reg_Registers[93]_s217_rtlcGen_CrossHier_n176 (.Q (
\Registers[93]_s217_rtlcGen_CrossHier_n176 ), .C (Clk_int), .CE (
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nx19493z1), .D (nx17197z1), .R (Reset_int)) ;
FDRE \reg_Registers[92]_s218_rtlcGen_CrossHier_n177 (.Q (
\Registers[92]_s218_rtlcGen_CrossHier_n177 ), .C (Clk_int), .CE (
nx19493z1), .D (nx20243z1), .R (Reset_int)) ;
FDRE \reg_Registers[91]_s219_rtlcGen_CrossHier_n178 (.Q (
\Registers[91]_s219_rtlcGen_CrossHier_n178 ), .C (Clk_int), .CE (
nx19493z1), .D (nx15592z1), .R (Reset_int)) ;
FDRE \reg_Registers[90]_s220_rtlcGen_CrossHier_n179 (.Q (
\Registers[90]_s220_rtlcGen_CrossHier_n179 ), .C (Clk_int), .CE (
nx19493z1), .D (nx44004z1), .R (Reset_int)) ;
FDRE \reg_Registers[89]_s221_rtlcGen_CrossHier_n180 (.Q (
\Registers[89]_s221_rtlcGen_CrossHier_n180 ), .C (Clk_int), .CE (
nx19493z1), .D (nx31097z1), .R (Reset_int)) ;
FDRE \reg_Registers[88]_s222_rtlcGen_CrossHier_n181 (.Q (
\Registers[88]_s222_rtlcGen_CrossHier_n181 ), .C (Clk_int), .CE (
nx19493z1), .D (nx41793z1), .R (Reset_int)) ;
FDRE \reg_Registers[103]_s225_rtlcGen_CrossHier_n183 (.Q (
\Registers[103]_s225_rtlcGen_CrossHier_n183 ), .C (Clk_int), .CE (
nx31844z1), .D (nx11069z6), .R (Reset_int)) ;
FDRE \reg_Registers[102]_s226_rtlcGen_CrossHier_n184 (.Q (
\Registers[102]_s226_rtlcGen_CrossHier_n184 ), .C (Clk_int), .CE (
nx31844z1), .D (nx10072z1), .R (Reset_int)) ;
FDSE \reg_Registers[101]_s227_rtlcGen_CrossHier_n185 (.Q (
\Registers[101]_s227_rtlcGen_CrossHier_n185 ), .C (Clk_int), .CE (
nx31844z1), .D (nx17197z1), .S (Reset_int)) ;
FDSE \reg_Registers[100]_s228_rtlcGen_CrossHier_n186 (.Q (
\Registers[100]_s228_rtlcGen_CrossHier_n186 ), .C (Clk_int), .CE (
nx31844z1), .D (nx20243z1), .S (Reset_int)) ;
FDSE \reg_Registers[99]_s229_rtlcGen_CrossHier_n187 (.Q (
\Registers[99]_s229_rtlcGen_CrossHier_n187 ), .C (Clk_int), .CE (
nx31844z1), .D (nx15592z1), .S (Reset_int)) ;
FDSE \reg_Registers[98]_s230_rtlcGen_CrossHier_n188 (.Q (
\Registers[98]_s230_rtlcGen_CrossHier_n188 ), .C (Clk_int), .CE (
nx31844z1), .D (nx44004z1), .S (Reset_int)) ;
FDSE \reg_Registers[97]_s231_rtlcGen_CrossHier_n189 (.Q (
\Registers[97]_s231_rtlcGen_CrossHier_n189 ), .C (Clk_int), .CE (
nx31844z1), .D (nx31097z1), .S (Reset_int)) ;
FDSE \reg_Registers[96]_s232_rtlcGen_CrossHier_n190 (.Q (
\Registers[96]_s232_rtlcGen_CrossHier_n190 ), .C (Clk_int), .CE (
nx31844z1), .D (nx41793z1), .S (Reset_int)) ;
FDRE \reg_Registers[111]_s235_rtlcGen_CrossHier_n192 (.Q (
\Registers[111]_s235_rtlcGen_CrossHier_n192 ), .C (Clk_int), .CE (
nx57760z1), .D (nx11069z6), .R (Reset_int)) ;
FDRE \reg_Registers[110]_s236_rtlcGen_CrossHier_n193 (.Q (
\Registers[110]_s236_rtlcGen_CrossHier_n193 ), .C (Clk_int), .CE (
nx57760z1), .D (nx10072z1), .R (Reset_int)) ;
FDSE \reg_Registers[109]_s237_rtlcGen_CrossHier_n194 (.Q (
\Registers[109]_s237_rtlcGen_CrossHier_n194 ), .C (Clk_int), .CE (
nx57760z1), .D (nx17197z1), .S (Reset_int)) ;
FDSE \reg_Registers[108]_s238_rtlcGen_CrossHier_n195 (.Q (
\Registers[108]_s238_rtlcGen_CrossHier_n195 ), .C (Clk_int), .CE (
nx57760z1), .D (nx20243z1), .S (Reset_int)) ;
FDSE \reg_Registers[107]_s239_rtlcGen_CrossHier_n196 (.Q (
\Registers[107]_s239_rtlcGen_CrossHier_n196 ), .C (Clk_int), .CE (
nx57760z1), .D (nx15592z1), .S (Reset_int)) ;
FDSE \reg_Registers[106]_s240_rtlcGen_CrossHier_n197 (.Q (
\Registers[106]_s240_rtlcGen_CrossHier_n197 ), .C (Clk_int), .CE (
nx57760z1), .D (nx44004z1), .S (Reset_int)) ;
FDSE \reg_Registers[105]_s241_rtlcGen_CrossHier_n198 (.Q (
\Registers[105]_s241_rtlcGen_CrossHier_n198 ), .C (Clk_int), .CE (
nx57760z1), .D (nx31097z1), .S (Reset_int)) ;
FDRE \reg_Registers[104]_s242_rtlcGen_CrossHier_n199 (.Q (
\Registers[104]_s242_rtlcGen_CrossHier_n199 ), .C (Clk_int), .CE (
nx57760z1), .D (nx41793z1), .R (Reset_int)) ;
FDRE \reg_Registers[119]_s245_rtlcGen_CrossHier_n201 (.Q (
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    \Registers[119]_s245_rtlcGen_CrossHier_n201 ), .C (Clk_int), .CE (
    nx9652z1), .D (nx11069z6), .R (Reset_int)) ;
    FDRE \reg_Registers[118]_s246_rtlcGen_CrossHier_n202 (.Q (
    \Registers[118]_s246_rtlcGen_CrossHier_n202 ), .C (Clk_int), .CE (
    nx9652z1), .D (nx10072z1), .R (Reset_int)) ;
    FDSE \reg_Registers[117]_s247_rtlcGen_CrossHier_n203 (.Q (
    \Registers[117]_s247_rtlcGen_CrossHier_n203 ), .C (Clk_int), .CE (
    nx9652z1), .D (nx17197z1), .S (Reset_int)) ;
    FDSE \reg_Registers[116]_s248_rtlcGen_CrossHier_n204 (.Q (
    \Registers[116]_s248_rtlcGen_CrossHier_n204 ), .C (Clk_int), .CE (
    nx9652z1), .D (nx20243z1), .S (Reset_int)) ;
    FDSE \reg_Registers[115]_s249_rtlcGen_CrossHier_n205 (.Q (
    \Registers[115]_s249_rtlcGen_CrossHier_n205 ), .C (Clk_int), .CE (
    nx9652z1), .D (nx15592z1), .S (Reset_int)) ;
    FDSE \reg_Registers[114]_s250_rtlcGen_CrossHier_n206 (.Q (
    \Registers[114]_s250_rtlcGen_CrossHier_n206 ), .C (Clk_int), .CE (
    nx9652z1), .D (nx44004z1), .S (Reset_int)) ;
    FDRE \reg_Registers[113]_s251_rtlcGen_CrossHier_n207 (.Q (
    \Registers[113]_s251_rtlcGen_CrossHier_n207 ), .C (Clk_int), .CE (
    nx9652z1), .D (nx31097z1), .R (Reset_int)) ;
    FDSE \reg_Registers[112]_s252_rtlcGen_CrossHier_n208 (.Q (
    \Registers[112]_s252_rtlcGen_CrossHier_n208 ), .C (Clk_int), .CE (
    nx9652z1), .D (nx41793z1), .S (Reset_int)) ;
    FDRE \reg_InA(7) (.Q (CrossHierIn_0), .C (Clk_int), .CE (nx11069z1), .D (
    nx11069z6), .R (Reset_int)) ;
    FDRE \reg_InA(6) (.Q (CrossHierIn_1), .C (Clk_int), .CE (nx11069z1), .D (
    nx10072z1), .R (Reset_int)) ;
    FDRE \reg_InA(5) (.Q (CrossHierIn_2), .C (Clk_int), .CE (nx11069z1), .D (
    nx17197z1), .R (Reset_int)) ;
    FDRE \reg_InA(4) (.Q (CrossHierIn_3), .C (Clk_int), .CE (nx11069z1), .D (
    nx20243z1), .R (Reset_int)) ;
    FDRE \reg_InA(3) (.Q (CrossHierIn_4), .C (Clk_int), .CE (nx11069z1), .D (
    nx15592z1), .R (Reset_int)) ;
    FDRE \reg_InA(2) (.Q (CrossHierIn_5), .C (Clk_int), .CE (nx11069z1), .D (
    nx44004z1), .R (Reset_int)) ;
    FDRE \reg_InA(1) (.Q (CrossHierIn_6), .C (Clk_int), .CE (nx11069z1), .D (
    nx31097z1), .R (Reset_int)) ;
    FDRE \reg_InA(0) (.Q (CrossHierIn_7), .C (Clk_int), .CE (nx11069z1), .D (
    nx41793z1), .R (Reset_int)) ;
    OBUF Ack_obuf (.O (Ack), .I (nx55346z1)) ;
    IBUF Start_ibuf (.O (Start_int), .I (Start)) ;
    IBUF Reset_ibuf (.O (Reset_int), .I (Reset)) ;
    (* HLUTNM = "LUT62_2_19" *)
    LUT4 ix9884z1170 (.O (nx9884z1), .I0 (nx11069z7), .I1 (MemWrite), .I2 (
    \DM1_MSR__DataMem_core_5_rtlc_sync_msr_n3_rtlcGen2(128) ), .I3 (
    Reset_int)) ;
    defparam ix9884z1170.INIT = 16'hFF70;
    LUT4 ix31097z24878 (.O (nx31097z1), .I0 (nx11069z7), .I1 (nx31097z2), .I2 (
    LoadInst), .I3 (nx31097z9)) ;
    defparam ix31097z24878.INIT = 16'h5C0C;
    LUT4 ix44004z22565 (.O (nx44004z1), .I0 (nx11069z7), .I1 (nx44004z2), .I2 (
    LoadInst), .I3 (nx44004z7)) ;
    defparam ix44004z22565.INIT = 16'h5303;
    LUT4 ix15592z22565 (.O (nx15592z1), .I0 (nx11069z7), .I1 (nx15592z2), .I2 (
    LoadInst), .I3 (nx15592z17)) ;
    defparam ix15592z22565.INIT = 16'h5303;
    LUT4 ix20243z22565 (.O (nx20243z1), .I0 (nx11069z7), .I1 (nx20243z2), .I2 (
    LoadInst), .I3 (nx20243z6)) ;
    defparam ix20243z22565.INIT = 16'h5303;
    LUT5 ix17197z1557 (.O (nx17197z1), .I0 (nx11069z7), .I1 (nx17197z2), .I2 (
    nx17197z10), .I3 (LoadInst), .I4 (nx17197z11)) ;
    defparam ix17197z1557.INIT = 32'h55F300F3;
    LUT4 ix10072z22565 (.O (nx10072z1), .I0 (nx11069z7), .I1 (nx10072z2), .I2 (
    LoadInst), .I3 (nx10072z19)) ;
    defparam ix10072z22565.INIT = 16'h5303;
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LUT4 ix11069z22570 (.O (nx11069z6), .I0 (nx11069z7), .I1 (nx38036z2), .I2 (
LoadInst), .I3 (nx11069z23)) ;
defparam ix11069z22570.INIT = 16'h5303;
LUT5 ix2633z32 (.O (nx2633z2), .I0 (nx36542z3), .I1 (nx36542z4), .I2 (
nx36542z5), .I3 (nx36542z6), .I4 (nx36542z7)) ;
defparam ix2633z32.INIT = 32'hAAEEFAFE;
LUT3 ix2747z1419 (.O (nx2747z2), .I0 (nx2747z3), .I1 (nx36542z2), .I2 (
CrossHierIn_4)) ;
defparam ix2747z1419.INIT = 8'h69;
LUT5 ix2748z43614 (.O (nx2748z2), .I0 (nx15592z3), .I1 (nx2748z3), .I2 (
nx36542z2), .I3 (nx50624z3), .I4 (CrossHierIn_5)) ;
defparam ix2748z43614.INIT = 32'h5AC3A53C;
LUT6 ix2750z32 (.O (nx2750z1), .I0 (SCq), .I1 (nx36542z4), .I2 (nx36542z5),
.I3 (nx36542z6), .I4 (nx36542z7), .I5 (nx36542z3)) ;
defparam ix2750z32.INIT = 64'hFFFFFFFFAAEEFAFE;
LUT6 ix61537z5409 (.O (nx61537z1), .I0 (PgmCtr[6]), .I1 (PgmCtr[5]), .I2 (
nx42063z2), .I3 (nx11069z2), .I4 (nx36542z9), .I5 (nx36542z10)) ;
defparam ix61537z5409.INIT = 64'hFFFFEFFF0FFF0FFF;
LUT6 ix50058z1073 (.O (nx50058z1), .I0 (PgmCtr[6]), .I1 (PgmCtr[5]), .I2 (
nx42063z2), .I3 (nx11069z2), .I4 (nx36542z9), .I5 (nx36542z10)) ;
defparam ix50058z1073.INIT = 64'hFFFFFFEFFF0FFF0F;
(* HLUTNM = "LUT62_2_21" *)
LUT3 ix36542z1534 (.O (nx36542z1), .I0 (nx36542z2), .I1 (nx36542z8), .I2 (
nx36542z13)) ;
defparam ix36542z1534.INIT = 8'hDC;
(* HLUTNM = "LUT62_2_11" *)
LUT3 ix43600z1553 (.O (nx43600z1), .I0 (nx36542z2), .I1 (nx11069z2), .I2 (
nx36542z13)) ;
defparam ix43600z1553.INIT = 8'hEF;
(* HLUTNM = "LUT62_2_12" *)
LUT3 ix55451z1565 (.O (nx55451z1), .I0 (nx36542z2), .I1 (nx11069z2), .I2 (
nx36542z13)) ;
defparam ix55451z1565.INIT = 8'hFB;
LUT6 ix42063z1313 (.O (nx42063z1), .I0 (nx42063z2), .I1 (nx51687z2), .I2 (
nx51683z2), .I3 (nx51684z2), .I4 (nx51685z3), .I5 (nx45966z4)) ;
defparam ix42063z1313.INIT = 64'hFF7FFF7FFF7FFFFF;
GND ps_gnd (.G (nx8480z1)) ;
LUT5 ix8480z53228 (.O (nx8480z2), .I0 (PgmCtr[7]), .I1 (\PCTarg(7) ), .I2 (
Jump), .I3 (BranchEn), .I4 (Zq)) ;
defparam ix8480z53228.INIT = 32'hCCCACACA;
LUT6 ix51682z63570 (.O (nx51682z1), .I0 (PgmCtr[6]), .I1 (nx51682z2), .I2 (
nx51683z2), .I3 (nx45966z2), .I4 (nx51685z2), .I5 (nx8473z1)) ;
defparam ix51682z63570.INIT = 64'hAAAAAAAA00F0F330;
LUT6 ix51684z53742 (.O (nx51684z1), .I0 (PgmCtr[4]), .I1 (nx51682z2), .I2 (
nx51683z2), .I3 (nx51684z2), .I4 (nx51685z2), .I5 (nx8473z1)) ;
defparam ix51684z53742.INIT = 64'hAAAAAAAAF300CCCC;
LUT6 ix51685z9644 (.O (nx51685z1), .I0 (nx51683z2), .I1 (nx51684z2), .I2 (
nx51685z2), .I3 (nx51682z2), .I4 (nx8473z1), .I5 (PgmCtr[3])) ;
defparam ix51685z9644.INIT = 64'hFFFF208A0000208A;
LUT6 ix51687z62946 (.O (nx51687z1), .I0 (PgmCtr[1]), .I1 (nx51687z2), .I2 (
nx51683z2), .I3 (nx51684z2), .I4 (nx51685z2), .I5 (nx8473z1)) ;
defparam ix51687z62946.INIT = 64'hAAAAAAAAFFCFF0C0;
LUT5 ix51688z53228 (.O (nx51688z1), .I0 (PgmCtr[0]), .I1 (\PCTarg(0) ), .I2 (
Jump), .I3 (BranchEn), .I4 (Zq)) ;
defparam ix51688z53228.INIT = 32'hCCCACACA;
(* HLUTNM = "LUT62_2_31" *)
LUT2 ix53265z1328 (.O (nx53265z1), .I0 (Reset_int), .I1 (Start_int)) ;
defparam ix53265z1328.INIT = 4'hE;
LUT6 ix26451z1841 (.O (nx26451z17), .I0 (PgmCtr[9]), .I1 (PgmCtr[8]), .I2 (
nx51683z3), .I3 (nx44004z4), .I4 (nx2749z4), .I5 (nx2749z6)) ;
defparam ix26451z1841.INIT = 64'h000000FE010101FF;
LUT5 ix26451z1330 (.O (nx26451z16), .I0 (PgmCtr[9]), .I1 (PgmCtr[8]), .I2 (
nx51683z3), .I3 (nx2747z4), .I4 (nx20243z4)) ;
defparam ix26451z1330.INIT = 32'hFEFF0001;
(* HLUTNM = "LUT62_2_2" *)
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LUT5 ix26451z1294 (.O (nx26451z14), .I0 (MemWrite), .I1 (Reset_int), .I2 (
nx31097z4), .I3 (nx41793z3), .I4 (nx41793z7)) ;
defparam ix26451z1294.INIT = 32'hDDDDFFDF;
LUT6 ix26451z813 (.O (nx26451z13), .I0 (MemWrite), .I1 (Reset_int), .I2 (
nx51683z2), .I3 (nx44004z4), .I4 (nx2749z4), .I5 (nx2749z6)) ;
defparam ix26451z813.INIT = 64'hDDDDDDDFFDFDFDFF;
LUT3 ix26451z1576 (.O (nx26451z12), .I0 (nx15592z3), .I1 (MemWrite), .I2 (
Reset_int)) ;
defparam ix26451z1576.INIT = 8'hFB;
LUT6 ix26451z58153 (.O (nx26451z11), .I0 (MemWrite), .I1 (Reset_int), .I2 (
nx42063z2), .I3 (nx51683z3), .I4 (nx2747z4), .I5 (nx20243z4)) ;
defparam ix26451z58153.INIT = 64'hFFDFFFFFDDDDDDFD;
(* HLUTNM = "LUT62_2_20" *)
LUT3 ix26451z1574 (.O (nx26451z10), .I0 (nx17197z3), .I1 (MemWrite), .I2 (
Reset_int)) ;
defparam ix26451z1574.INIT = 8'hFB;
(* HLUTNM = "LUT62_2_3" *)
LUT5 ix26451z58121 (.O (nx26451z9), .I0 (MemWrite), .I1 (Reset_int), .I2 (
nx10072z4), .I3 (nx10072z5), .I4 (nx10072z8)) ;
defparam ix26451z58121.INIT = 32'hDDDDDDDF;
(* HLUTNM = "LUT62_2_16" *)
LUT4 ix26451z58115 (.O (nx26451z3), .I0 (MemWrite), .I1 (Reset_int), .I2 (
nx11069z16), .I3 (nx10072z14)) ;
defparam ix26451z58115.INIT = 16'hDDDF;
LUT5 ix50624z1315 (.O (nx50624z1), .I0 (nx50624z2), .I1 (nx36542z2), .I2 (
nx11069z2), .I3 (nx36542z13), .I4 (\ALU1_Out_0n1s2(8) )) ;
defparam ix50624z1315.INIT = 32'h00C10001;
LUT6 ix38036z1314 (.O (nx38036z1), .I0 (nx38036z2), .I1 (nx10072z2), .I2 (
nx15592z2), .I3 (nx44004z2), .I4 (nx31097z2), .I5 (nx38036z5)) ;
defparam ix38036z1314.INIT = 64'h0000800000000000;
LUT5 ix38036z1319 (.O (nx38036z5), .I0 (nx17197z3), .I1 (nx17197z10), .I2 (
nx41793z2), .I3 (nx38036z6), .I4 (nx38036z10)) ;
defparam ix38036z1319.INIT = 32'h00030001;
LUT6 ix38036z17702 (.O (nx38036z6), .I0 (nx17197z4), .I1 (nx31097z6), .I2 (
nx15592z12), .I3 (nx41793z12), .I4 (nx38036z7), .I5 (nx38036z9)) ;
defparam ix38036z17702.INIT = 64'hAAAAFFFF00FF3FFF;
(* HLUTNM = "LUT62_2_21" *)
LUT3 ix38036z1450 (.O (nx38036z9), .I0 (nx36542z2), .I1 (nx36542z13), .I2 (
CrossHierIn_3)) ;
defparam ix38036z1450.INIT = 8'h80;
LUT6 ix38036z1060 (.O (nx38036z7), .I0 (nx36542z2), .I1 (nx11069z2), .I2 (
nx36542z13), .I3 (nx38036z8), .I4 (ALU1_Out_0n1s6[5]), .I5 (
ALU1_Out_0n1s6[4])) ;
defparam ix38036z1060.INIT = 64'hB6B4B6B4B6B4FEFC;
(* HLUTNM = "LUT62_2_29" *)
LUT2 ix38036z1322 (.O (nx38036z8), .I0 (CrossHierIn_2), .I1 (CrossHierIn_3)
) ;
defparam ix38036z1322.INIT = 4'h1;
(* HLUTNM = "LUT62_2_13" *)
LUT4 ix38036z58281 (.O (nx38036z10), .I0 (nx36542z2), .I1 (nx11069z2), .I2 (
nx36542z13), .I3 (CrossHierIn_3)) ;
defparam ix38036z58281.INIT = 16'hDE7E;
LUT6 ix55346z1314 (.O (nx55346z1), .I0 (nx55346z2), .I1 (nx36542z4), .I2 (
PgmCtr[7]), .I3 (PgmCtr[4]), .I4 (PgmCtr[1]), .I5 (PgmCtr[0])) ;
defparam ix55346z1314.INIT = 64'h0000004000000000;
(* HLUTNM = "LUT62_2_1" *)
LUT5 ix11069z44972 (.O (nx11069z1), .I0 (RegWrEn), .I1 (nx36542z13), .I2 (
nx36542z2), .I3 (nx11069z2), .I4 (nx36542z8)) ;
defparam ix11069z44972.INIT = 32'hAAAAAA8A;
LUT6 ix9652z1314 (.O (nx9652z1), .I0 (nx42063z2), .I1 (nx51683z2), .I2 (
nx45966z2), .I3 (nx51685z3), .I4 (nx45966z4), .I5 (nx31844z2)) ;
defparam ix9652z1314.INIT = 64'h0101010300000000;
LUT5 ix57760z1442 (.O (nx57760z1), .I0 (nx31844z2), .I1 (nx45966z2), .I2 (
nx51682z2), .I3 (nx45966z4), .I4 (PgmCtr[2])) ;
defparam ix57760z1442.INIT = 32'h00000080;
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LUT6 ix31844z1314 (.O (nx31844z1), .I0 (nx42063z2), .I1 (nx51682z2), .I2 (
nx45966z2), .I3 (nx51685z3), .I4 (nx45966z4), .I5 (nx31844z2)) ;
defparam ix31844z1314.INIT = 64'h1010103000000000;
LUT4 ix19493z9506 (.O (nx19493z1), .I0 (nx31844z2), .I1 (nx45966z2), .I2 (
nx51682z2), .I3 (nx51683z3)) ;
defparam ix19493z9506.INIT = 16'h2000;
LUT5 ix4575z1314 (.O (nx4575z1), .I0 (nx31844z2), .I1 (nx51684z2), .I2 (
nx51685z2), .I3 (nx51682z2), .I4 (nx51683z3)) ;
defparam ix4575z1314.INIT = 32'h00800000;
LUT5 ix4450z1314 (.O (nx4450z1), .I0 (nx31844z2), .I1 (nx51684z2), .I2 (
nx51685z2), .I3 (nx51687z2), .I4 (nx51683z3)) ;
defparam ix4450z1314.INIT = 32'h20000000;
LUT6 ix53557z1314 (.O (nx53557z1), .I0 (nx42063z2), .I1 (nx51682z2), .I2 (
nx51684z2), .I3 (nx51685z3), .I4 (nx45966z4), .I5 (nx31844z2)) ;
defparam ix53557z1314.INIT = 64'h0202020000000000;
LUT6 ix36047z1314 (.O (nx36047z1), .I0 (nx42063z2), .I1 (nx51682z2), .I2 (
nx51683z2), .I3 (nx51685z3), .I4 (nx45966z4), .I5 (nx31844z2)) ;
defparam ix36047z1314.INIT = 64'h404040C000000000;
LUT6 ix5421z1314 (.O (nx5421z1), .I0 (nx42063z2), .I1 (nx51682z2), .I2 (
nx51683z2), .I3 (nx51685z3), .I4 (nx45966z4), .I5 (nx31844z2)) ;
defparam ix5421z1314.INIT = 64'h1010103000000000;
LUT6 ix21647z1314 (.O (nx21647z1), .I0 (PgmCtr[9]), .I1 (PgmCtr[8]), .I2 (
nx51683z3), .I3 (nx45966z2), .I4 (nx45966z4), .I5 (nx31844z2)) ;
defparam ix21647z1314.INIT = 64'h0001000000000000;
LUT5 ix41793z1521 (.O (nx41793z1), .I0 (nx11069z7), .I1 (nx41793z2), .I2 (
nx41793z12), .I3 (LoadInst), .I4 (nx41793z13)) ;
defparam ix41793z1521.INIT = 32'h55CF00CF;
LUT6 ix41793z1315 (.O (nx41793z2), .I0 (nx31097z4), .I1 (nx41793z3), .I2 (
nx41793z7), .I3 (nx41793z11), .I4 (nx11069z2), .I5 (CrossHierIn_7)) ;
defparam ix41793z1315.INIT = 64'h22008D008D000000;
LUT6 ix41793z1068 (.O (nx41793z12), .I0 (nx36542z2), .I1 (nx11069z2), .I2 (
nx36542z13), .I3 (SCq), .I4 (ALU1_Out_0n1s6[0]), .I5 (CrossHierIn_7)) ;
defparam ix41793z1068.INIT = 64'hB4B5FCFDB6B7FEFF;
LUT6 ix31097z14626 (.O (nx31097z2), .I0 (nx31097z3), .I1 (nx31097z5), .I2 (
nx31097z6), .I3 (nx41793z11), .I4 (nx31097z7), .I5 (nx31097z8)) ;
defparam ix31097z14626.INIT = 64'h80A020A0CCFF33FF;
(* HLUTNM = "LUT62_2_11" *)
LUT5 ix31097z15528 (.O (nx31097z8), .I0 (nx36542z2), .I1 (nx11069z2), .I2 (
nx36542z13), .I3 (ALU1_Out_0n1s6[1]), .I4 (CrossHierIn_6)) ;
defparam ix31097z15528.INIT = 32'h155D377F;
LUT6 ix31097z1319 (.O (nx31097z5), .I0 (PgmCtr[9]), .I1 (PgmCtr[8]), .I2 (
\Registers[57]_s181_rtlcGen_CrossHier_n144 ), .I3 (nx51683z3), .I4 (
nx44004z4), .I5 (nx2749z4)) ;
defparam ix31097z1319.INIT = 64'hFFFEFFFEFFFEF0001;
LUT6 ix31097z44874 (.O (nx31097z7), .I0 (CrossHierIn_6), .I1 (nx36542z4), .I2 (
nx36542z5), .I3 (nx11069z4), .I4 (nx11069z5), .I5 (nx11069z3)) ;
defparam ix31097z44874.INIT = 64'h000000000A02AA22;
LUT6 ix44004z34082 (.O (nx44004z2), .I0 (CrossHierIn_5), .I1 (nx15592z3), .I2 (
nx36542z13), .I3 (nx36542z2), .I4 (nx11069z2), .I5 (nx44004z3)) ;
defparam ix44004z34082.INIT = 64'h000000009FFF7FFF;
LUT6 ix44004z17460 (.O (nx44004z3), .I0 (nx44004z4), .I1 (nx2749z4), .I2 (
nx49419z2), .I3 (nx44004z6), .I4 (nx36542z2), .I5 (CrossHierIn_5)) ;
defparam ix44004z17460.INIT = 64'hFFFF03F10FF003F10;
(* HLUTNM = "LUT62_2_13" *)
LUT4 ix44004z19751 (.O (nx44004z6), .I0 (nx36542z2), .I1 (nx11069z2), .I2 (
nx36542z13), .I3 (ALU1_Out_0n1s6[2])) ;
defparam ix44004z19751.INIT = 16'h4800;
LUT6 ix15592z1315 (.O (nx15592z2), .I0 (nx15592z3), .I1 (nx36542z13), .I2 (
nx36542z2), .I3 (nx11069z2), .I4 (nx15592z11), .I5 (nx15592z16)) ;
defparam ix15592z1315.INIT = 64'h0000FFFD00000000;
LUT6 ix15592z50480 (.O (nx15592z16), .I0 (nx15592z12), .I1 (nx36542z2), .I2 (
nx11069z2), .I3 (nx36542z13), .I4 (ALU1_Out_0n1s6[3]), .I5 (
CrossHierIn_4)) ;
defparam ix15592z50480.INIT = 64'hCB33FBF38F3FBFFF;
LUT6 ix15592z1324 (.O (nx15592z11), .I0 (CrossHierIn_4), .I1 (nx2747z4), .I2 (
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nx36542z13), .I3 (nx36542z2), .I4 (nx11069z2), .I5 (nx15592z12)) ;
defparam ix15592z1324.INIT = 64'h9000000010000000;
LUT5 ix15592z31326 (.O (nx15592z12), .I0 (nx45966z2), .I1 (nx51685z2), .I2 (
nx15592z13), .I3 (nx15592z14), .I4 (nx15592z15)) ;
defparam ix15592z31326.INIT = 32'hFDB97531;
LUT6 ix20243z1315 (.O (nx20243z2), .I0 (CrossHierIn_3), .I1 (nx17197z3), .I2 (
nx36542z13), .I3 (nx36542z2), .I4 (nx11069z2), .I5 (nx20243z3)) ;
defparam ix20243z1315.INIT = 64'h9FFF7FFF00000000;
LUT6 ix20243z1313 (.O (nx20243z3), .I0 (nx20243z4), .I1 (nx36542z2), .I2 (
nx11069z2), .I3 (nx36542z13), .I4 (ALU1_Out_0n1s6[4]), .I5 (
CrossHierIn_3)) ;
defparam ix20243z1313.INIT = 64'hCF31FFF1CF3DFFFD;
LUT6 ix17197z1312 (.O (nx17197z2), .I0 (nx17197z3), .I1 (nx36542z2), .I2 (
nx11069z2), .I3 (nx36542z13), .I4 (ALU1_Out_0n1s6[5]), .I5 (
CrossHierIn_2)) ;
defparam ix17197z1312.INIT = 64'hCF31FFF1CF3DFFFD;
LUT6 ix17197z1323 (.O (nx17197z10), .I0 (CrossHierIn_2), .I1 (nx11069z16), .I2 (
nx10072z14), .I3 (nx36542z13), .I4 (nx36542z2), .I5 (nx11069z2)) ;
defparam ix17197z1323.INIT = 64'h2100000002000000;
LUT6 ix10072z1315 (.O (nx10072z2), .I0 (CrossHierIn_1), .I1 (nx36542z13), .I2 (
nx36542z2), .I3 (nx11069z2), .I4 (nx10072z3), .I5 (nx10072z13)) ;
defparam ix10072z1315.INIT = 64'h7FFFBF7F00000000;
LUT6 ix10072z1326 (.O (nx10072z13), .I0 (nx11069z16), .I1 (nx10072z14), .I2 (
nx36542z13), .I3 (nx36542z2), .I4 (nx11069z2), .I5 (nx10072z18)) ;
defparam ix10072z1326.INIT = 64'hFFFFFFFE00000000;
(* HLUTNM = "LUT62_2_10" *)
LUT5 ix10072z48434 (.O (nx10072z18), .I0 (nx36542z2), .I1 (nx11069z2), .I2 (
nx36542z13), .I3 (ALU1_Out_0n1s6[6]), .I4 (CrossHierIn_1)) ;
defparam ix10072z48434.INIT = 32'hB5FDB7FF;
LUT6 ix38036z1315 (.O (nx38036z2), .I0 (CrossHierIn_0), .I1 (nx11069z8), .I2 (
nx36542z13), .I3 (nx36542z2), .I4 (nx11069z2), .I5 (nx38036z3)) ;
defparam ix38036z1315.INIT = 64'h9FFF7FFF00000000;
LUT6 ix41793z13628 (.O (nx41793z11), .I0 (nx36542z4), .I1 (nx36542z5), .I2 (
nx36542z13), .I3 (nx36542z6), .I4 (nx36542z7), .I5 (nx36542z3)) ;
defparam ix41793z13628.INIT = 64'h00000000F0503010;
LUT6 ix38036z1316 (.O (nx38036z3), .I0 (nx10072z5), .I1 (nx10072z8), .I2 (
nx36542z13), .I3 (nx36542z2), .I4 (nx11069z2), .I5 (nx38036z4)) ;
defparam ix38036z1316.INIT = 64'hFFFFFFFE00000000;
(* HLUTNM = "LUT62_2_12" *)
LUT5 ix38036z48420 (.O (nx38036z4), .I0 (nx36542z2), .I1 (nx11069z2), .I2 (
nx36542z13), .I3 (ALU1_Out_0n1s6[7]), .I4 (CrossHierIn_0)) ;
defparam ix38036z48420.INIT = 32'hB5FDB7FF;
(* HLUTNM = "LUT62_2_10" *)
LUT3 ix31097z1320 (.O (nx31097z6), .I0 (nx36542z2), .I1 (nx11069z2), .I2 (
nx36542z13)) ;
defparam ix31097z1320.INIT = 8'h01;
LUT6 ix11069z1320 (.O (nx11069z7), .I0 (nx11069z8), .I1 (nx11069z15), .I2 (
nx17197z3), .I3 (nx11069z20), .I4 (nx11069z21), .I5 (nx11069z22)) ;
defparam ix11069z1320.INIT = 64'h0002000000000000;
LUT6 ix11069z823 (.O (nx11069z22), .I0 (nx10072z4), .I1 (nx10072z5), .I2 (
nx10072z8), .I3 (nx31097z4), .I4 (nx41793z3), .I5 (nx41793z7)) ;
defparam ix11069z823.INIT = 64'hFEFEFEFE0000FE00;
LUT6 ix11069z1334 (.O (nx11069z21), .I0 (nx15592z4), .I1 (nx15592z5), .I2 (
nx15592z6), .I3 (nx15592z7), .I4 (nx15592z9), .I5 (
\DM1_MSR__DataMem_core_5_rtlc_sync_msr_n3_rtlcGen2(128) )) ;
defparam ix11069z1334.INIT = 64'h1010FF1000000000;
LUT6 ix11069z53764 (.O (nx11069z20), .I0 (nx2747z4), .I1 (nx20243z4), .I2 (
nx44004z4), .I3 (nx2749z4), .I4 (nx2749z6), .I5 (nx51683z2)) ;
defparam ix11069z53764.INIT = 64'h5555FFFFCCCFCCCF;
LUT6 ix49419z1314 (.O (nx49419z1), .I0 (RegWrEn), .I1 (nx51683z2), .I2 (
nx51684z2), .I3 (nx36542z2), .I4 (nx36542z8), .I5 (nx49419z2)) ;
defparam ix49419z1314.INIT = 64'h0000080000000000;
(* HLUTNM = "LUT62_2_1" *)
LUT5 ix31844z1347 (.O (nx31844z2), .I0 (RegWrEn), .I1 (nx36542z13), .I2 (
nx36542z2), .I3 (nx11069z2), .I4 (nx36542z8)) ;
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defparam ix31844z1347.INIT = 32'h00000020;
LUT6 ix49419z1325 (.O (nx49419z2), .I0 (nx36542z4), .I1 (nx36542z5), .I2 (
nx36542z13), .I3 (nx11069z4), .I4 (nx11069z5), .I5 (nx11069z3)) ;
defparam ix49419z1325.INIT = 64'h0F0F0F0F0C0E000A;
LUT5 ix2743z27579 (.O (nx2743z2), .I0 (\PCTarg(7) ), .I1 (CrossHierIn_0), .I2 (
nx11069z8), .I3 (nx36542z2), .I4 (nx50624z3)) ;
defparam ix2743z27579.INIT = 32'h3CC36699;
(* HLUTNM = "LUT62_2_31" *)
LUT3 ix50624z1386 (.O (nx50624z2), .I0 (nx11069z8), .I1 (nx50624z3), .I2 (
\PCTarg(7) )) ;
defparam ix50624z1386.INIT = 8'h47;
LUT3 ix2631z1464 (.O (nx2631z1), .I0 (nx10072z3), .I1 (nx36542z2), .I2 (
CrossHierIn_1)) ;
defparam ix2631z1464.INIT = 8'h96;
(* HLUTNM = "LUT62_2_9" *)
LUT5 ix10072z1571 (.O (nx10072z3), .I0 (nx10072z4), .I1 (nx10072z5), .I2 (
nx10072z8), .I3 (nx10072z12), .I4 (nx50624z3)) ;
defparam ix10072z1571.INIT = 32'hFEFE00FF;
LUT3 ix2745z1464 (.O (nx2745z2), .I0 (nx2745z3), .I1 (nx36542z2), .I2 (
CrossHierIn_2)) ;
defparam ix2745z1464.INIT = 8'h96;
LUT6 ix2745z17020 (.O (nx2745z3), .I0 (nx51682z2), .I1 (nx51683z2), .I2 (
nx51684z2), .I3 (nx51685z2), .I4 (nx11069z15), .I5 (nx50624z3)) ;
defparam ix2745z17020.INIT = 64'h0000FFFB3D593D59;
LUT5 ix2746z43749 (.O (nx2746z2), .I0 (nx17197z3), .I1 (nx2746z3), .I2 (
nx36542z2), .I3 (nx50624z3), .I4 (CrossHierIn_3)) ;
defparam ix2746z43749.INIT = 32'h5A3CA5C3;
LUT6 ix2747z22035 (.O (nx2747z3), .I0 (nx2747z4), .I1 (nx20243z4), .I2 (
nx51683z2), .I3 (nx51685z2), .I4 (nx50624z3), .I5 (nx2747z6)) ;
defparam ix2747z22035.INIT = 64'h5C5CF0005C5C50F0;
LUT5 ix2749z24549 (.O (nx2749z2), .I0 (nx2749z3), .I1 (nx2749z8), .I2 (
nx36542z2), .I3 (nx50624z3), .I4 (CrossHierIn_6)) ;
defparam ix2749z24549.INIT = 32'hA53C5AC3;
LUT5 ix2750z41398 (.O (nx2750z2), .I0 (nx31097z3), .I1 (nx36542z2), .I2 (
nx50624z3), .I3 (\PCTarg(0) ), .I4 (CrossHierIn_7)) ;
defparam ix2750z41398.INIT = 32'h636C9C93;
LUT5 ix50624z2597 (.O (nx50624z3), .I0 (nx50624z4), .I1 (nx36542z4), .I2 (
nx36542z5), .I3 (nx50624z5), .I4 (nx50624z6)) ;
defparam ix50624z2597.INIT = 32'h55110501;
LUT6 ix50624z1317 (.O (nx50624z4), .I0 (PgmCtr[4]), .I1 (PgmCtr[3]), .I2 (
PgmCtr[2]), .I3 (PgmCtr[1]), .I4 (PgmCtr[0]), .I5 (nx51682z3)) ;
defparam ix50624z1317.INIT = 64'h2A53008800000000;
LUT6 ix50624z1278 (.O (nx50624z6), .I0 (PgmCtr[5]), .I1 (PgmCtr[4]), .I2 (
PgmCtr[3]), .I3 (PgmCtr[2]), .I4 (PgmCtr[1]), .I5 (PgmCtr[0])) ;
defparam ix50624z1278.INIT = 64'hFD63799DFFE6FFD7;
LUT6 ix50624z1269 (.O (nx50624z5), .I0 (PgmCtr[7]), .I1 (PgmCtr[4]), .I2 (
PgmCtr[3]), .I3 (PgmCtr[2]), .I4 (PgmCtr[1]), .I5 (PgmCtr[0])) ;
defparam ix50624z1269.INIT = 64'hBBFFFFFFDEBDFFFCF;
LUT6 ix36542z5690 (.O (nx36542z8), .I0 (PgmCtr[9]), .I1 (PgmCtr[8]), .I2 (
PgmCtr[6]), .I3 (PgmCtr[5]), .I4 (nx36542z9), .I5 (nx36542z10)) ;
defparam ix36542z5690.INIT = 64'h0000000111111111;
LUT6 ix36542z1322 (.O (nx36542z10), .I0 (nx36542z11), .I1 (nx36542z12), .I2 (
PgmCtr[7]), .I3 (PgmCtr[6]), .I4 (PgmCtr[5]), .I5 (PgmCtr[0])) ;
defparam ix36542z1322.INIT = 64'hFAFCFAFFFFFFCFFFF;
(* HLUTNM = "LUT62_2_4" *)
LUT5 ix36542z1188 (.O (nx36542z12), .I0 (PgmCtr[4]), .I1 (PgmCtr[3]), .I2 (
PgmCtr[2]), .I3 (PgmCtr[1]), .I4 (PgmCtr[0])) ;
defparam ix36542z1188.INIT = 32'hFDFEFF77;
(* HLUTNM = "LUT62_2_14" *)
LUT5 ix36542z33035 (.O (nx36542z11), .I0 (PgmCtr[5]), .I1 (PgmCtr[4]), .I2 (
PgmCtr[3]), .I3 (PgmCtr[2]), .I4 (PgmCtr[1])) ;
defparam ix36542z33035.INIT = 32'hFDE77BDF;
LUT6 ix36542z1305 (.O (nx36542z9), .I0 (PgmCtr[7]), .I1 (PgmCtr[4]), .I2 (
PgmCtr[3]), .I3 (PgmCtr[2]), .I4 (PgmCtr[1]), .I5 (PgmCtr[0])) ;
defparam ix36542z1305.INIT = 64'hFBFFFFFFFFFDFFFEF;
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LUT5 ix11069z23092 (.O (nx11069z2), .I0 (nx11069z3), .I1 (nx36542z4), .I2 (
nx36542z5), .I3 (nx11069z4), .I4 (nx11069z5)) ;
defparam ix11069z23092.INIT = 32'h05015511;
LUT6 ix11069z34726 (.O (nx11069z3), .I0 (nx51682z3), .I1 (PgmCtr[4]), .I2 (
PgmCtr[3]), .I3 (PgmCtr[2]), .I4 (PgmCtr[1]), .I5 (PgmCtr[0])) ;
defparam ix11069z34726.INIT = 64'h822208202A088282;
LUT6 ix11069z41466 (.O (nx11069z5), .I0 (PgmCtr[5]), .I1 (PgmCtr[4]), .I2 (
PgmCtr[3]), .I3 (PgmCtr[2]), .I4 (PgmCtr[1]), .I5 (PgmCtr[0])) ;
defparam ix11069z41466.INIT = 64'hC55978381B429CD4;
LUT6 ix11069z49362 (.O (nx11069z4), .I0 (PgmCtr[7]), .I1 (PgmCtr[4]), .I2 (
PgmCtr[3]), .I3 (PgmCtr[2]), .I4 (PgmCtr[1]), .I5 (PgmCtr[0])) ;
defparam ix11069z49362.INIT = 64'hEBE8F89EFFB9BBAD;
LUT5 ix36542z2596 (.O (nx36542z2), .I0 (nx36542z3), .I1 (nx36542z4), .I2 (
nx36542z5), .I3 (nx36542z6), .I4 (nx36542z7)) ;
defparam ix36542z2596.INIT = 32'h55110501;
LUT6 ix36542z3364 (.O (nx36542z3), .I0 (nx51682z3), .I1 (PgmCtr[4]), .I2 (
PgmCtr[3]), .I3 (PgmCtr[2]), .I4 (PgmCtr[1]), .I5 (PgmCtr[0])) ;
defparam ix36542z3364.INIT = 64'hAA80808000220800;
LUT6 ix36542z60422 (.O (nx36542z7), .I0 (PgmCtr[5]), .I1 (PgmCtr[4]), .I2 (
PgmCtr[3]), .I3 (PgmCtr[2]), .I4 (PgmCtr[1]), .I5 (PgmCtr[0])) ;
defparam ix36542z60422.INIT = 64'hFFBDDF7B1BC7E6DE;
LUT6 ix36542z62433 (.O (nx36542z6), .I0 (PgmCtr[7]), .I1 (PgmCtr[4]), .I2 (
PgmCtr[3]), .I3 (PgmCtr[2]), .I4 (PgmCtr[1]), .I5 (PgmCtr[0])) ;
defparam ix36542z62433.INIT = 64'hFECDBFEFF8FEEEBA;
LUT6 ix36542z1583 (.O (nx36542z13), .I0 (PgmCtr[9]), .I1 (PgmCtr[8]), .I2 (
PgmCtr[7]), .I3 (PgmCtr[6]), .I4 (nx36542z14), .I5 (nx36542z15)) ;
defparam ix36542z1583.INIT = 64'h0000010000010101;
LUT6 ix36542z303 (.O (nx36542z15), .I0 (PgmCtr[5]), .I1 (PgmCtr[4]), .I2 (
PgmCtr[3]), .I3 (PgmCtr[2]), .I4 (PgmCtr[1]), .I5 (PgmCtr[0])) ;
defparam ix36542z303.INIT = 64'h762FFFFF7BABFBFF;
LUT6 ix36542z58622 (.O (nx36542z14), .I0 (PgmCtr[5]), .I1 (PgmCtr[4]), .I2 (
PgmCtr[3]), .I3 (PgmCtr[2]), .I4 (PgmCtr[1]), .I5 (PgmCtr[0])) ;
defparam ix36542z58622.INIT = 64'hE7FFDFFFE6E7DFCF;
LUT6 ix45966z1118 (.O (nx45966z1), .I0 (nx42063z2), .I1 (nx51682z2), .I2 (
nx51683z2), .I3 (nx45966z2), .I4 (nx51685z3), .I5 (nx45966z4)) ;
defparam ix45966z1118.INIT = 64'h5DB65DB65DB6FF3C;
(* HLUTNM = "LUT62_2_22" *)
LUT4 ix51679z1860 (.O (nx51679z2), .I0 (PgmCtr[9]), .I1 (Jump), .I2 (
BranchEn), .I3 (Zq)) ;
defparam ix51679z1860.INIT = 16'h0222;
LUT4 ix51680z1860 (.O (nx51680z1), .I0 (PgmCtr[8]), .I1 (Jump), .I2 (
BranchEn), .I3 (Zq)) ;
defparam ix51680z1860.INIT = 16'h0222;
LUT6 ix10072z63581 (.O (nx10072z12), .I0 (nx42063z2), .I1 (nx51682z2), .I2 (
nx51683z2), .I3 (nx45966z2), .I4 (nx51685z3), .I5 (nx45966z4)) ;
defparam ix10072z63581.INIT = 64'h51B051B051B0F330;
LUT6 ix51683z16878 (.O (nx51683z1), .I0 (PgmCtr[5]), .I1 (nx51682z2), .I2 (
nx51683z2), .I3 (nx45966z2), .I4 (nx51685z2), .I5 (nx8473z1)) ;
defparam ix51683z16878.INIT = 64'hAAAAAAAA0CF03CCC;
LUT6 ix2746z53743 (.O (nx2746z3), .I0 (nx42063z2), .I1 (nx51682z2), .I2 (
nx51683z2), .I3 (nx51684z2), .I4 (nx51685z3), .I5 (nx45966z4)) ;
defparam ix2746z53743.INIT = 64'hE644E644E644CCCC;
LUT6 ix51686z53742 (.O (nx51686z1), .I0 (PgmCtr[2]), .I1 (nx51682z2), .I2 (
nx51683z2), .I3 (nx51684z2), .I4 (nx51685z2), .I5 (nx8473z1)) ;
defparam ix51686z53742.INIT = 64'hAAAAAAAA3F03CCCC;
LUT6 ix2748z14422 (.O (nx2748z3), .I0 (nx42063z2), .I1 (nx51682z2), .I2 (
nx51683z2), .I3 (nx51684z2), .I4 (nx51685z3), .I5 (nx45966z4)) ;
defparam ix2748z14422.INIT = 64'h91B991B991B93333;
LUT6 ix2749z62952 (.O (nx2749z8), .I0 (nx42063z2), .I1 (nx51687z2), .I2 (
nx51683z2), .I3 (nx51684z2), .I4 (nx51685z3), .I5 (nx45966z4)) ;
defparam ix2749z62952.INIT = 64'hFACAFACAFACAF0C0;
LUT3 ix8473z1335 (.O (nx8473z1), .I0 (Jump), .I1 (BranchEn), .I2 (Zq)) ;
defparam ix8473z1335.INIT = 8'h15;
(* HLUTNM = "LUT62_2_2" *)
LUT5 ix26451z10027 (.O (nx26451z8), .I0 (MemWrite), .I1 (Reset_int), .I2 (
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nx31097z4), .I3 (nx41793z3), .I4 (nx41793z7)) ;
defparam ix26451z10027.INIT = 32'h00002202;
(* HLUTNM = "LUT62_2_29" *)
LUT3 ix31097z1329 (.O (nx31097z3), .I0 (nx31097z4), .I1 (nx41793z3), .I2 (
nx41793z7)) ;
defparam ix31097z1329.INIT = 8'h0D;
LUT6 ix41793z17704 (.O (nx41793z7), .I0 (nx51683z2), .I1 (nx51684z2), .I2 (
nx51685z2), .I3 (nx41793z8), .I4 (nx41793z9), .I5 (nx41793z10)) ;
defparam ix41793z17704.INIT = 64'hF0B0E0A050104000;
LUT5 ix41793z25386 (.O (nx41793z10), .I0 (nx51687z2), .I1 (nx51684z3), .I2 (
nx11069z14), .I3 (\Registers[8]_s121_rtlcGen_CrossHier_n91 ), .I4 (
\Registers[16]_s131_rtlcGen_CrossHier_n100 )) ;
defparam ix41793z25386.INIT = 32'h59FB5DFF;
(* HLUTNM = "LUT62_2_28" *)
LUT3 ix41793z1349 (.O (nx41793z9), .I0 (nx51687z2), .I1 (
\Registers[64]_s192_rtlcGen_CrossHier_n154 ), .I2 (
\Registers[72]_s202_rtlcGen_CrossHier_n163 )) ;
defparam ix41793z1349.INIT = 8'h1B;
(* HLUTNM = "LUT62_2_28" *)
LUT3 ix41793z1348 (.O (nx41793z8), .I0 (nx51687z2), .I1 (
\Registers[80]_s212_rtlcGen_CrossHier_n172 ), .I2 (
\Registers[88]_s222_rtlcGen_CrossHier_n181 )) ;
defparam ix41793z1348.INIT = 8'h1B;
LUT6 ix41793z2084 (.O (nx41793z3), .I0 (nx51684z2), .I1 (nx41793z4), .I2 (
nx41793z5), .I3 (nx51682z2), .I4 (
\Registers[96]_s232_rtlcGen_CrossHier_n190 ), .I5 (
\Registers[112]_s252_rtlcGen_CrossHier_n208 )) ;
defparam ix41793z2084.INIT = 64'h0303030203010300;
LUT6 ix41793z44846 (.O (nx41793z5), .I0 (nx51687z2), .I1 (nx51684z3), .I2 (
nx11069z14), .I3 (nx41793z6), .I4 (PgmCtr[6]), .I5 (CrossHierIn_7)) ;
defparam ix41793z44846.INIT = 64'hA000A200AA0AAA08;
(* HLUTNM = "LUT62_2_18" *)
LUT4 ix41793z4932 (.O (nx41793z4), .I0 (PgmCtr[9]), .I1 (PgmCtr[8]), .I2 (
CrossHierIn_7), .I3 (nx51683z3)) ;
defparam ix41793z4932.INIT = 16'h0E1F;
(* HLUTNM = "LUT62_2_18" *)
LUT3 ix41793z1320 (.O (nx41793z6), .I0 (PgmCtr[9]), .I1 (PgmCtr[8]), .I2 (
\Registers[104]_s242_rtlcGen_CrossHier_n199 )) ;
defparam ix41793z1320.INIT = 8'h01;
LUT6 ix31097z5172 (.O (nx31097z4), .I0 (nx51683z2), .I1 (nx51684z2), .I2 (
nx51685z2), .I3 (nx51687z2), .I4 (
\Registers[48]_s172_rtlcGen_CrossHier_n136 ), .I5 (
\Registers[56]_s182_rtlcGen_CrossHier_n145 )) ;
defparam ix31097z5172.INIT = 64'h0707070F0F070F0F;
LUT6 ix26451z9546 (.O (nx26451z7), .I0 (MemWrite), .I1 (Reset_int), .I2 (
nx51683z2), .I3 (nx44004z4), .I4 (nx2749z4), .I5 (nx2749z6)) ;
defparam ix26451z9546.INIT = 64'h0000000220202022;
LUT6 ix2749z803 (.O (nx2749z3), .I0 (PgmCtr[9]), .I1 (PgmCtr[8]), .I2 (
nx51683z3), .I3 (nx44004z4), .I4 (nx2749z4), .I5 (nx2749z6)) ;
defparam ix2749z803.INIT = 64'hFFFFFF01FEFEFE00;
LUT6 ix2749z63769 (.O (nx2749z6), .I0 (nx45966z2), .I1 (nx51685z2), .I2 (
nx2749z7), .I3 (nx51687z2), .I4 (
\Registers[49]_s171_rtlcGen_CrossHier_n135 ), .I5 (
\Registers[57]_s181_rtlcGen_CrossHier_n144 )) ;
defparam ix2749z63769.INIT = 64'hE2E2E2F3F3E2F3F3;
LUT5 ix2749z25382 (.O (nx2749z7), .I0 (nx51687z2), .I1 (nx51684z3), .I2 (
nx11069z14), .I3 (\Registers[9]_s120_rtlcGen_CrossHier_n90 ), .I4 (
\Registers[17]_s130_rtlcGen_CrossHier_n99 )) ;
defparam ix2749z25382.INIT = 32'h59FB5DFF;
LUT6 ix2749z50672 (.O (nx2749z4), .I0 (nx51684z2), .I1 (nx51685z2), .I2 (
nx2749z5), .I3 (nx51687z2), .I4 (
\Registers[65]_s191_rtlcGen_CrossHier_n153 ), .I5 (
\Registers[81]_s211_rtlcGen_CrossHier_n171 )) ;
defparam ix2749z50672.INIT = 64'hC000C044C088C0CC;
LUT6 ix44004z13910 (.O (nx44004z4), .I0 (nx45966z2), .I1 (nx51685z2), .I2 (
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   nx44004z5), .I3 (nx51682z2), .I4 (
   \Registers[113]_s251_rtlcGen_CrossHier_n207 ), .I5 (CrossHierIn_6)) ;
   defparam ix44004z13910.INIT = 64'h2020203131203131;
   (* HLUTNM = "LUT62_2_30" *)
   LUT3 ix44004z1345 (.O (nx44004z5), .I0 (nx51687z2), .I1 (
   \Registers[97]_s231_rtlcGen_CrossHier_n189 ), .I2 (
   \Registers[105]_s241_rtlcGen_CrossHier_n198 )) ;
   defparam ix44004z1345.INIT = 8'h1B;
   (* HLUTNM = "LUT62_2_20" *)
   LUT3 ix26451z1327 (.O (nx26451z6), .I0 (nx15592z3), .I1 (MemWrite), .I2 (
   Reset_int)) ;
   defparam ix26451z1327.INIT = 8'h08;
   LUT5 ix15592z1555 (.O (nx15592z3), .I0 (nx15592z4), .I1 (nx15592z5), .I2 (
   nx15592z6), .I3 (nx15592z7), .I4 (nx15592z9)) ;
   defparam ix15592z1555.INIT = 32'hEFEF00EF;
   LUT6 ix15592z2602 (.O (nx15592z9), .I0 (nx51683z2), .I1 (nx51684z2), .I2 (
   nx15592z10), .I3 (nx51687z2), .I4 (
   \Registers[66]_s190_rtlcGen_CrossHier_n152 ), .I5 (
   \Registers[82]_s210_rtlcGen_CrossHier_n170 )) ;
   defparam ix15592z2602.INIT = 64'h0555054405110500;
   LUT6 ix15592z53748 (.O (nx15592z7), .I0 (nx15592z8), .I1 (nx51685z2), .I2 (
   nx51687z2), .I3 (nx51683z3), .I4 (
   \Registers[10]_s119_rtlcGen_CrossHier_n89 ), .I5 (
   \Registers[18]_s129_rtlcGen_CrossHier_n98 )) ;
   defparam ix15592z53748.INIT = 64'hCC84CCC4CC8CCCCC;
   LUT6 ix15592z5174 (.O (nx15592z6), .I0 (nx51683z2), .I1 (nx51684z2), .I2 (
   nx51685z2), .I3 (nx51682z2), .I4 (
   \Registers[98]_s230_rtlcGen_CrossHier_n188 ), .I5 (
   \Registers[114]_s250_rtlcGen_CrossHier_n206 )) ;
   defparam ix15592z5174.INIT = 64'h0F0A0F0B0F0E0F0F;
   LUT6 ix15592z4390 (.O (nx15592z5), .I0 (
   \Registers[106]_s240_rtlcGen_CrossHier_n197 ), .I1 (CrossHierIn_5), .I2 (
   nx42063z2), .I3 (nx51682z2), .I4 (nx51683z3), .I5 (nx45966z2)) ;
   defparam ix15592z4390.INIT = 64'hAA000A00CC000C00;
   LUT6 ix15592z1317 (.O (nx15592z4), .I0 (
   \Registers[50]_s170_rtlcGen_CrossHier_n134 ), .I1 (
   \Registers[58]_s180_rtlcGen_CrossHier_n143 ), .I2 (nx42063z2), .I3 (
   nx51687z2), .I4 (nx51683z3), .I5 (nx51684z2)) ;
   defparam ix15592z1317.INIT = 64'h0000C0A000000000;
   LUT6 ix26451z1350 (.O (nx26451z5), .I0 (MemWrite), .I1 (Reset_int), .I2 (
   nx42063z2), .I3 (nx51683z3), .I4 (nx2747z4), .I5 (nx20243z4)) ;
   defparam ix26451z1350.INIT = 64'h2202222200000020;
   LUT6 ix20243z54036 (.O (nx20243z4), .I0 (nx45966z2), .I1 (nx51685z2), .I2 (
   nx20243z5), .I3 (nx15592z13), .I4 (nx15592z14), .I5 (nx15592z15)) ;
   defparam ix20243z54036.INIT = 64'h0123456789ABCDEF;
   (* HLUTNM = "LUT62_2_27" *)
   LUT3 ix15592z1355 (.O (nx15592z15), .I0 (nx51687z2), .I1 (
   \Registers[67]_s189_rtlcGen_CrossHier_n151 ), .I2 (
   \Registers[75]_s199_rtlcGen_CrossHier_n160 )) ;
   defparam ix15592z1355.INIT = 8'h1B;
   (* HLUTNM = "LUT62_2_26" *)
   LUT3 ix15592z1354 (.O (nx15592z14), .I0 (nx51687z2), .I1 (
   \Registers[83]_s209_rtlcGen_CrossHier_n169 ), .I2 (
   \Registers[91]_s219_rtlcGen_CrossHier_n178 )) ;
   defparam ix15592z1354.INIT = 8'h1B;
   (* HLUTNM = "LUT62_2_26" *)
   LUT3 ix15592z1353 (.O (nx15592z13), .I0 (nx51687z2), .I1 (
   \Registers[99]_s229_rtlcGen_CrossHier_n187 ), .I2 (
   \Registers[107]_s239_rtlcGen_CrossHier_n196 )) ;
   defparam ix15592z1353.INIT = 8'h1B;
   (* HLUTNM = "LUT62_2_23" *)
   LUT3 ix20243z1345 (.O (nx20243z5), .I0 (nx51682z2), .I1 (
   \Registers[115]_s249_rtlcGen_CrossHier_n205 ), .I2 (CrossHierIn_4)) ;
   defparam ix20243z1345.INIT = 8'h1B;
   LUT6 ix2747z801 (.O (nx2747z4), .I0 (nx51684z2), .I1 (nx51685z2), .I2 (
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nx2747z5), .I3 (nx51682z2), .I4 (
\Registers[11]_s118_rtlcGen_CrossHier_n88 ), .I5 (
\Registers[19]_s128_rtlcGen_CrossHier_n97 )) ;
defparam ix2747z801.INIT = 64'hB975FD75B9FDFDFD;
(* HLUTNM = "LUT62_2_27" *)
LUT3 ix2747z1344 (.O (nx2747z5), .I0 (nx51687z2), .I1 (
\Registers[51]_s169_rtlcGen_CrossHier_n133 ), .I2 (
\Registers[59]_s179_rtlcGen_CrossHier_n142 )) ;
defparam ix2747z1344.INIT = 8'h1B;
(* HLUTNM = "LUT62_2_19" *)
LUT3 ix26451z1325 (.O (nx26451z4), .I0 (nx17197z3), .I1 (MemWrite), .I2 (
Reset_int)) ;
defparam ix26451z1325.INIT = 8'h08;
LUT5 ix17197z5685 (.O (nx17197z3), .I0 (nx17197z4), .I1 (nx17197z6), .I2 (
nx17197z7), .I3 (nx17197z8), .I4 (nx51685z2)) ;
defparam ix17197z5685.INIT = 32'h11101111;
LUT6 ix17197z13609 (.O (nx17197z8), .I0 (nx51684z2), .I1 (nx17197z9), .I2 (
nx51687z2), .I3 (nx51683z3), .I4 (
\Registers[68]_s188_rtlcGen_CrossHier_n150 ), .I5 (
\Registers[84]_s208_rtlcGen_CrossHier_n168 )) ;
defparam ix17197z13609.INIT = 64'h3300320031003000;
LUT6 ix17197z1480 (.O (nx17197z7), .I0 (
\Registers[12]_s117_rtlcGen_CrossHier_n87 ), .I1 (
\Registers[20]_s127_rtlcGen_CrossHier_n96 ), .I2 (nx51687z2), .I3 (
nx51683z3), .I4 (nx51684z3), .I5 (nx11069z14)) ;
defparam ix17197z1480.INIT = 64'h00A000A0000C00A0;
LUT6 ix17197z45012 (.O (nx17197z9), .I0 (nx51682z2), .I1 (nx51684z3), .I2 (
nx11069z14), .I3 (PgmCtr[6]), .I4 (
\Registers[76]_s198_rtlcGen_CrossHier_n159 ), .I5 (
\Registers[92]_s218_rtlcGen_CrossHier_n177 )) ;
defparam ix17197z45012.INIT = 64'h0000A0A20A08AAAA;
LUT5 ix17197z5463 (.O (nx17197z6), .I0 (nx45966z2), .I1 (nx10072z7), .I2 (
nx51682z2), .I3 (\Registers[108]_s238_rtlcGen_CrossHier_n195 ), .I4 (
CrossHierIn_3)) ;
defparam ix17197z5463.INIT = 32'h00201030;
LUT6 ix17197z2100 (.O (nx17197z4), .I0 (nx51683z2), .I1 (nx51684z2), .I2 (
nx51685z2), .I3 (nx17197z5), .I4 (nx51682z2), .I5 (
\Registers[100]_s228_rtlcGen_CrossHier_n186 )) ;
defparam ix17197z2100.INIT = 64'h020A020E020A030F;
LUT5 ix17197z14134 (.O (nx17197z5), .I0 (nx51687z2), .I1 (nx51683z3), .I2 (
\Registers[52]_s168_rtlcGen_CrossHier_n132 ), .I3 (
\Registers[60]_s178_rtlcGen_CrossHier_n141 ), .I4 (
\Registers[116]_s248_rtlcGen_CrossHier_n204 )) ;
defparam ix17197z14134.INIT = 32'hFEDC3210;
LUT2 ix11069z1329 (.O (nx11069z15), .I0 (nx11069z16), .I1 (nx10072z14)) ;
defparam ix11069z1329.INIT = 4'h1;
LUT6 ix10072z4153 (.O (nx10072z14), .I0 (nx51683z2), .I1 (nx45966z2), .I2 (
nx51685z2), .I3 (nx10072z15), .I4 (nx10072z16), .I5 (nx10072z17)) ;
defparam ix10072z4153.INIT = 64'h050401000F0E0B0A;
LUT6 ix10072z42452 (.O (nx10072z17), .I0 (nx51687z2), .I1 (nx51684z3), .I2 (
nx11069z14), .I3 (PgmCtr[6]), .I4 (
\Registers[53]_s167_rtlcGen_CrossHier_n131 ), .I5 (
\Registers[61]_s177_rtlcGen_CrossHier_n140 )) ;
defparam ix10072z42452.INIT = 64'hAFAEAAAAA5A6A0A2;
(* HLUTNM = "LUT62_2_24" *)
LUT3 ix10072z1356 (.O (nx10072z16), .I0 (nx51687z2), .I1 (
\Registers[101]_s227_rtlcGen_CrossHier_n185 ), .I2 (
\Registers[109]_s237_rtlcGen_CrossHier_n194 )) ;
defparam ix10072z1356.INIT = 8'h1B;
(* HLUTNM = "LUT62_2_23" *)
LUT3 ix10072z1355 (.O (nx10072z15), .I0 (nx51682z2), .I1 (
\Registers[117]_s247_rtlcGen_CrossHier_n203 ), .I2 (CrossHierIn_2)) ;
defparam ix10072z1355.INIT = 8'h1B;
LUT6 ix11069z17713 (.O (nx11069z16), .I0 (nx51683z2), .I1 (nx51684z2), .I2 (
nx51685z2), .I3 (nx11069z17), .I4 (nx11069z18), .I5 (nx11069z19)) ;
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defparam ix11069z17713.INIT = 64'hF0B0E0A050104000;
LUT5 ix11069z25395 (.O (nx11069z19), .I0 (nx51687z2), .I1 (nx51684z3), .I2 (
nx11069z14), .I3 (\Registers[13]_s116_rtlcGen_CrossHier_n86 ), .I4 (
\Registers[21]_s126_rtlcGen_CrossHier_n95 )) ;
defparam ix11069z25395.INIT = 32'h59FB5DFF;
(* HLUTNM = "LUT62_2_25" *)
LUT3 ix11069z1358 (.O (nx11069z18), .I0 (nx51687z2), .I1 (
\Registers[69]_s187_rtlcGen_CrossHier_n149 ), .I2 (
\Registers[77]_s197_rtlcGen_CrossHier_n158 )) ;
defparam ix11069z1358.INIT = 8'h1B;
(* HLUTNM = "LUT62_2_25" *)
LUT3 ix11069z1357 (.O (nx11069z17), .I0 (nx51687z2), .I1 (
\Registers[85]_s207_rtlcGen_CrossHier_n167 ), .I2 (
\Registers[93]_s217_rtlcGen_CrossHier_n176 )) ;
defparam ix11069z1357.INIT = 8'h1B;
(* HLUTNM = "LUT62_2_3" *)
LUT5 ix26451z1317 (.O (nx26451z2), .I0 (MemWrite), .I1 (Reset_int), .I2 (
nx10072z4), .I3 (nx10072z5), .I4 (nx10072z8)) ;
defparam ix26451z1317.INIT = 32'h00000002;
(* HLUTNM = "LUT62_2_9" *)
LUT3 ix26451z1329 (.O (nx26451z15), .I0 (nx10072z4), .I1 (nx10072z5), .I2 (
nx10072z8)) ;
defparam ix26451z1329.INIT = 8'h01;
LUT6 ix10072z44841 (.O (nx10072z8), .I0 (nx51685z2), .I1 (nx10072z9), .I2 (
nx10072z10), .I3 (nx10072z11), .I4 (nx51687z2), .I5 (nx51683z3)) ;
defparam ix10072z44841.INIT = 64'hA0008888AA00AA00;
LUT6 ix10072z1323 (.O (nx10072z11), .I0 (nx51687z2), .I1 (nx51683z3), .I2 (
nx51684z3), .I3 (nx11069z14), .I4 (
\Registers[14]_s115_rtlcGen_CrossHier_n85 ), .I5 (
\Registers[22]_s125_rtlcGen_CrossHier_n94 )) ;
defparam ix10072z1323.INIT = 64'hDDADFFAFDDFDFFFF;
LUT6 ix10072z4658 (.O (nx10072z5), .I0 (nx45966z2), .I1 (nx10072z6), .I2 (
nx10072z7), .I3 (nx51682z2), .I4 (
\Registers[102]_s226_rtlcGen_CrossHier_n184 ), .I5 (CrossHierIn_1)) ;
defparam ix10072z4658.INIT = 64'h0804080C0D040D0C;
(* HLUTNM = "LUT62_2_6" *)
LUT5 ix10072z5673 (.O (nx10072z7), .I0 (PgmCtr[9]), .I1 (PgmCtr[8]), .I2 (
nx51683z3), .I3 (nx51685z3), .I4 (nx45966z4)) ;
defparam ix10072z5673.INIT = 32'h11111101;
LUT6 ix10072z1318 (.O (nx10072z6), .I0 (nx51687z2), .I1 (nx51684z3), .I2 (
nx11069z14), .I3 (PgmCtr[6]), .I4 (
\Registers[110]_s236_rtlcGen_CrossHier_n193 ), .I5 (
\Registers[118]_s246_rtlcGen_CrossHier_n202 )) ;
defparam ix10072z1318.INIT = 64'h5A59FAFB5F5DFFFF;
LUT6 ix10072z3887 (.O (nx10072z4), .I0 (nx51683z2), .I1 (nx51684z2), .I2 (
nx51685z2), .I3 (nx51687z2), .I4 (
\Registers[54]_s166_rtlcGen_CrossHier_n130 ), .I5 (
\Registers[62]_s176_rtlcGen_CrossHier_n139 )) ;
defparam ix10072z3887.INIT = 64'h0202020A0A020A0A;
(* HLUTNM = "LUT62_2_16" *)
LUT3 ix26451z1322 (.O (nx26451z1), .I0 (nx11069z8), .I1 (MemWrite), .I2 (
Reset_int)) ;
defparam ix26451z1322.INIT = 8'h08;
LUT6 ix11069z62487 (.O (nx11069z8), .I0 (nx11069z9), .I1 (nx11069z11), .I2 (
nx11069z12), .I3 (nx11069z13), .I4 (nx51683z2), .I5 (nx51685z2)) ;
defparam ix11069z62487.INIT = 64'hFF00F0F0CCCCEEEE;
(* HLUTNM = "LUT62_2_6" *)
LUT4 ix51685z5683 (.O (nx51685z2), .I0 (PgmCtr[9]), .I1 (PgmCtr[8]), .I2 (
nx51685z3), .I3 (nx45966z4)) ;
defparam ix51685z5683.INIT = 16'h1110;
LUT6 ix45966z1404 (.O (nx45966z4), .I0 (nx45966z5), .I1 (nx45966z6), .I2 (
PgmCtr[7]), .I3 (PgmCtr[6]), .I4 (PgmCtr[5]), .I5 (PgmCtr[4])) ;
defparam ix45966z1404.INIT = 64'h0003000300030057;
LUT6 ix45966z54880 (.O (nx45966z6), .I0 (PgmCtr[5]), .I1 (PgmCtr[4]), .I2 (
PgmCtr[3]), .I3 (PgmCtr[2]), .I4 (PgmCtr[1]), .I5 (PgmCtr[0])) ;
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defparam ix45966z54880.INIT = 64'h5BF1272D901DD139;
(* HLUTNM = "LUT62_2_15" *)
LUT5 ix45966z58083 (.O (nx45966z5), .I0 (PgmCtr[7]), .I1 (PgmCtr[3]), .I2 (
PgmCtr[2]), .I3 (PgmCtr[1]), .I4 (PgmCtr[0])) ;
defparam ix45966z58083.INIT = 32'hB3BBDDBD;
LUT6 ix51685z4388 (.O (nx51685z3), .I0 (nx51685z4), .I1 (nx51685z5), .I2 (
PgmCtr[7]), .I3 (PgmCtr[6]), .I4 (PgmCtr[3]), .I5 (PgmCtr[2])) ;
defparam ix51685z4388.INIT = 64'h0C000C0004000C00;
LUT6 ix51685z41593 (.O (nx51685z5), .I0 (PgmCtr[5]), .I1 (PgmCtr[4]), .I2 (
PgmCtr[3]), .I3 (PgmCtr[2]), .I4 (PgmCtr[1]), .I5 (PgmCtr[0])) ;
defparam ix51685z41593.INIT = 64'hA5ABB8ADFCFE9D53;
LUT5 ix11069z4573 (.O (nx11069z13), .I0 (
\Registers[15]_s114_rtlcGen_CrossHier_n84 ), .I1 (
\Registers[23]_s124_rtlcGen_CrossHier_n93 ), .I2 (nx51687z2), .I3 (
nx51684z3), .I4 (nx11069z14)) ;
defparam ix11069z4573.INIT = 32'hAFAF0CAF;
(* HLUTNM = "LUT62_2_8" *)
LUT4 ix15592z62937 (.O (nx15592z8), .I0 (PgmCtr[7]), .I1 (PgmCtr[6]), .I2 (
nx51684z3), .I3 (nx45966z3)) ;
defparam ix15592z62937.INIT = 16'hF0B0;
LUT6 ix11069z22845 (.O (nx11069z12), .I0 (nx51684z2), .I1 (nx51687z2), .I2 (
\Registers[71]_s185_rtlcGen_CrossHier_n147 ), .I3 (
\Registers[79]_s195_rtlcGen_CrossHier_n156 ), .I4 (
\Registers[87]_s205_rtlcGen_CrossHier_n165 ), .I5 (
\Registers[95]_s215_rtlcGen_CrossHier_n174 )) ;
defparam ix11069z22845.INIT = 64'hFEBADC9876325410;
LUT6 ix11069z1324 (.O (nx11069z11), .I0 (
\Registers[55]_s165_rtlcGen_CrossHier_n129 ), .I1 (
\Registers[63]_s175_rtlcGen_CrossHier_n138 ), .I2 (nx42063z2), .I3 (
nx51687z2), .I4 (nx51683z3), .I5 (nx51684z2)) ;
defparam ix11069z1324.INIT = 64'h0000C0A000000000;
LUT5 ix11069z11340 (.O (nx11069z9), .I0 (nx45966z2), .I1 (nx11069z10), .I2 (
nx51682z2), .I3 (\Registers[119]_s245_rtlcGen_CrossHier_n201 ), .I4 (
CrossHierIn_0)) ;
defparam ix11069z11340.INIT = 32'h77722722;
(* HLUTNM = "LUT62_2_24" *)
LUT3 ix11069z1350 (.O (nx11069z10), .I0 (nx51687z2), .I1 (
\Registers[103]_s225_rtlcGen_CrossHier_n183 ), .I2 (
\Registers[111]_s235_rtlcGen_CrossHier_n192 )) ;
defparam ix11069z1350.INIT = 8'h1B;
LUT6 ix45966z1588 (.O (nx45966z2), .I0 (PgmCtr[9]), .I1 (PgmCtr[8]), .I2 (
PgmCtr[7]), .I3 (PgmCtr[6]), .I4 (nx51684z3), .I5 (nx45966z3)) ;
defparam ix45966z1588.INIT = 64'h0000001101000111;
(* HLUTNM = "LUT62_2_8" *)
LUT4 ix51684z475 (.O (nx51684z2), .I0 (PgmCtr[7]), .I1 (PgmCtr[6]), .I2 (
nx51684z3), .I3 (nx45966z3)) ;
defparam ix51684z475.INIT = 16'hFCB8;
(* HLUTNM = "LUT62_2_17" *)
LUT3 ix11069z1343 (.O (nx11069z14), .I0 (nx45966z3), .I1 (PgmCtr[7]), .I2 (
PgmCtr[6])) ;
defparam ix11069z1343.INIT = 8'h10;
LUT6 ix45966z18354 (.O (nx45966z3), .I0 (PgmCtr[5]), .I1 (PgmCtr[4]), .I2 (
PgmCtr[3]), .I3 (PgmCtr[2]), .I4 (PgmCtr[1]), .I5 (PgmCtr[0])) ;
defparam ix45966z18354.INIT = 64'h7A8DA65B0203428E;
LUT6 ix51684z50403 (.O (nx51684z3), .I0 (nx51684z4), .I1 (nx51684z5), .I2 (
nx51684z6), .I3 (nx51684z7), .I4 (nx51684z8), .I5 (nx51684z9)) ;
defparam ix51684z50403.INIT = 64'h000000BFBFBFBFBF;
LUT6 ix51684z31905 (.O (nx51684z9), .I0 (PgmCtr[7]), .I1 (PgmCtr[4]), .I2 (
PgmCtr[3]), .I3 (PgmCtr[2]), .I4 (PgmCtr[1]), .I5 (PgmCtr[0])) ;
defparam ix51684z31905.INIT = 64'h0427676747377777;
(* HLUTNM = "LUT62_2_14" *)
LUT2 ix51684z1325 (.O (nx51684z8), .I0 (PgmCtr[5]), .I1 (PgmCtr[1])) ;
defparam ix51684z1325.INIT = 4'h4;
LUT6 ix51684z5722 (.O (nx51684z7), .I0 (PgmCtr[7]), .I1 (PgmCtr[5]), .I2 (
PgmCtr[4]), .I3 (PgmCtr[3]), .I4 (PgmCtr[2]), .I5 (PgmCtr[0])) ;
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 defparam ix51684z5722.INIT = 64'h1103111001111132;
 (* HLUTNM = "LUT62_2_30" *)
 LUT2 ix51684z1323 (.O (nx51684z6), .I0 (PgmCtr[7]), .I1 (PgmCtr[5])) ;
 defparam ix51684z1323.INIT = 4'h4;
 (* HLUTNM = "LUT62_2_5" *)
 LUT5 ix51684z56099 (.O (nx51684z5), .I0 (PgmCtr[4]), .I1 (PgmCtr[3]), .I2 (
 PgmCtr[2]), .I3 (PgmCtr[1]), .I4 (PgmCtr[0])) ;
 defparam ix51684z56099.INIT = 32'hF5CCD5FD;
 (* HLUTNM = "LUT62_2_5" *)
 LUT5 ix51684z17769 (.O (nx51684z4), .I0 (PgmCtr[4]), .I1 (PgmCtr[3]), .I2 (
 PgmCtr[2]), .I3 (PgmCtr[1]), .I4 (PgmCtr[0])) ;
 defparam ix51684z17769.INIT = 32'h8CC04044;
 LUT3 ix51683z1316 (.O (nx51683z2), .I0 (PgmCtr[9]), .I1 (PgmCtr[8]), .I2 (
 nx51683z3)) ;
 defparam ix51683z1316.INIT = 8'h01;
 LUT6 ix51683z53744 (.O (nx51683z3), .I0 (nx51683z4), .I1 (nx2747z6), .I2 (
 nx51683z5), .I3 (PgmCtr[7]), .I4 (PgmCtr[6]), .I5 (PgmCtr[5])) ;
 defparam ix51683z53744.INIT = 64'hFFF0FF55FFF0CCCC;
 LUT6 ix51683z15776 (.O (nx51683z5), .I0 (PgmCtr[5]), .I1 (PgmCtr[4]), .I2 (
 PgmCtr[3]), .I3 (PgmCtr[2]), .I4 (PgmCtr[1]), .I5 (PgmCtr[0])) ;
 defparam ix51683z15776.INIT = 64'h21C57B4B195B387A;
 LUT6 ix2747z45857 (.O (nx2747z6), .I0 (PgmCtr[7]), .I1 (PgmCtr[4]), .I2 (
 PgmCtr[3]), .I3 (PgmCtr[2]), .I4 (PgmCtr[1]), .I5 (PgmCtr[0])) ;
 defparam ix2747z45857.INIT = 64'hFD9FBBDFBCDFADFB;
 (* HLUTNM = "LUT62_2_4" *)
 LUT5 ix51683z19732 (.O (nx51683z4), .I0 (PgmCtr[4]), .I1 (PgmCtr[3]), .I2 (
 PgmCtr[2]), .I3 (PgmCtr[1]), .I4 (PgmCtr[0])) ;
 defparam ix51683z19732.INIT = 32'h452847EF;
 LUT6 ix51687z14422 (.O (nx51687z2), .I0 (nx51687z3), .I1 (nx55346z2), .I2 (
 nx51687z4), .I3 (PgmCtr[7]), .I4 (PgmCtr[6]), .I5 (PgmCtr[5])) ;
 defparam ix51687z14422.INIT = 64'hFF0FFF55FF0F3333;
 LUT6 ix51682z3226 (.O (nx51682z2), .I0 (nx51682z3), .I1 (nx51687z3), .I2 (
 nx55346z2), .I3 (nx36542z4), .I4 (nx51687z4), .I5 (nx36542z5)) ;
 defparam ix51682z3226.INIT = 64'h0000077707770777;
 (* HLUTNM = "LUT62_2_17" *)
 LUT4 ix36542z1574 (.O (nx36542z5), .I0 (PgmCtr[9]), .I1 (PgmCtr[8]), .I2 (
 PgmCtr[7]), .I3 (PgmCtr[6])) ;
 defparam ix36542z1574.INIT = 16'h0100;
 LUT6 ix51687z16544 (.O (nx51687z4), .I0 (PgmCtr[5]), .I1 (PgmCtr[4]), .I2 (
 PgmCtr[3]), .I3 (PgmCtr[2]), .I4 (PgmCtr[1]), .I5 (PgmCtr[0])) ;
 defparam ix51687z16544.INIT = 64'h00CE5FC6E67B3B7B;
 (* HLUTNM = "LUT62_2_7" *)
 LUT4 ix36542z1318 (.O (nx36542z4), .I0 (PgmCtr[9]), .I1 (PgmCtr[8]), .I2 (
 PgmCtr[6]), .I3 (PgmCtr[5])) ;
 defparam ix36542z1318.INIT = 16'h0001;
 LUT6 ix55346z6794 (.O (nx55346z2), .I0 (PgmCtr[7]), .I1 (PgmCtr[4]), .I2 (
 PgmCtr[3]), .I3 (PgmCtr[2]), .I4 (PgmCtr[1]), .I5 (PgmCtr[0])) ;
 defparam ix55346z6794.INIT = 64'h4322437717721567;
 LUT5 ix51687z1302 (.O (nx51687z3), .I0 (PgmCtr[4]), .I1 (PgmCtr[3]), .I2 (
 PgmCtr[2]), .I3 (PgmCtr[1]), .I4 (PgmCtr[0])) ;
 defparam ix51687z1302.INIT = 32'h70FFFFF2;
 (* HLUTNM = "LUT62_2_15" *)
 LUT2 ix51685z1325 (.O (nx51685z4), .I0 (PgmCtr[1]), .I1 (PgmCtr[0])) ;
 defparam ix51685z1325.INIT = 4'h8;
 (* HLUTNM = "LUT62_2_7" *)
 LUT5 ix51682z1316 (.O (nx51682z3), .I0 (PgmCtr[9]), .I1 (PgmCtr[8]), .I2 (
 PgmCtr[7]), .I3 (PgmCtr[6]), .I4 (PgmCtr[5])) ;
 defparam ix51682z1316.INIT = 32'h00010000;
 (* HLUTNM = "LUT62_2_22" *)
 LUT2 ix42063z1316 (.O (nx42063z2), .I0 (PgmCtr[9]), .I1 (PgmCtr[8])) ;
 defparam ix42063z1316.INIT = 4'h1;
 BUFGP Clk_ibuf (.O (Clk_int), .I (Clk)) ;
 LUT6 ix2749z14456 (.O (nx2749z5), .I0 (
 \Registers[89]_s221_rtlcGen_CrossHier_n180 ), .I1 (
 \Registers[73]_s201_rtlcGen_CrossHier_n162 ), .I2 (nx51684z3), .I3 (
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PgmCtr[6]), .I4 (PgmCtr[7]), .I5 (nx45966z3)) ;
defparam ix2749z14456.INIT = 64'h5553555355533353;
LUT6 ix15592z14462 (.O (nx15592z10), .I0 (
\Registers[90]_s220_rtlcGen_CrossHier_n179 ), .I1 (
\Registers[74]_s200_rtlcGen_CrossHier_n161 ), .I2 (nx51684z3), .I3 (
PgmCtr[6]), .I4 (PgmCtr[7]), .I5 (nx45966z3)) ;
defparam ix15592z14462.INIT = 64'h5553555355533353;
LUT6 ix10072z14462 (.O (nx10072z10), .I0 (
\Registers[94]_s216_rtlcGen_CrossHier_n175 ), .I1 (
\Registers[78]_s196_rtlcGen_CrossHier_n157 ), .I2 (nx51684z3), .I3 (
PgmCtr[6]), .I4 (PgmCtr[7]), .I5 (nx45966z3)) ;
defparam ix10072z14462.INIT = 64'h5553555355533353;
LUT6 ix10072z14461 (.O (nx10072z9), .I0 (
\Registers[86]_s206_rtlcGen_CrossHier_n166 ), .I1 (
\Registers[70]_s186_rtlcGen_CrossHier_n148 ), .I2 (nx51684z3), .I3 (
PgmCtr[6]), .I4 (PgmCtr[7]), .I5 (nx45966z3)) ;
defparam ix10072z14461.INIT = 64'h5553555355533353;
VCC ps_vcc (.P (nx1629)) ;
FDRE \reg_q(9) (.Q (PgmCtr[9]), .C (Clk_int), .CE (nx1629), .D (
sload_mux_9_dup_132), .R (nx53265z1)) ;
FDRE \reg_q(8) (.Q (PgmCtr[8]), .C (Clk_int), .CE (nx1629), .D (
sload_mux_8_dup_131), .R (nx53265z1)) ;
FDRE \reg_q(7) (.Q (PgmCtr[7]), .C (Clk_int), .CE (nx1629), .D (
sload_mux_7_dup_130), .R (nx53265z1)) ;
FDRE \reg_q(6) (.Q (PgmCtr[6]), .C (Clk_int), .CE (nx1629), .D (
sload_mux_6_dup_129), .R (nx53265z1)) ;
FDRE \reg_q(5) (.Q (PgmCtr[5]), .C (Clk_int), .CE (nx1629), .D (
sload_mux_5_dup_128), .R (nx53265z1)) ;
FDRE \reg_q(4) (.Q (PgmCtr[4]), .C (Clk_int), .CE (nx1629), .D (
sload_mux_4_dup_127), .R (nx53265z1)) ;
FDRE \reg_q(3) (.Q (PgmCtr[3]), .C (Clk_int), .CE (nx1629), .D (
sload_mux_3_dup_126), .R (nx53265z1)) ;
FDRE \reg_q(2) (.Q (PgmCtr[2]), .C (Clk_int), .CE (nx1629), .D (
sload_mux_2_dup_125), .R (nx53265z1)) ;
FDRE \reg_q(1) (.Q (PgmCtr[1]), .C (Clk_int), .CE (nx1629), .D (
sload_mux_1_dup_124), .R (nx53265z1)) ;
FDRE \reg_q(0) (.Q (PgmCtr[0]), .C (Clk_int), .CE (nx1629), .D (
sload_mux_0_dup_123), .R (nx53265z1)) ;
FDRE \DM1_reg_MSR__DataMem_core_5_rtlc_sync_msr_n3_rtlcGen2(128) (.Q (
\DM1_MSR__DataMem_core_5_rtlc_sync_msr_n3_rtlcGen2(128) ), .C (Clk_int
), .CE (nx1629), .D (nx9884z1), .R (nx8480z1)) ;
FDRE reg_Zq (.Q (Zq), .C (Clk_int), .CE (nx1629), .D (nx38036z1), .R (
nx8480z1)) ;
FDRE reg_SCq (.Q (SCq), .C (Clk_int), .CE (nx1629), .D (nx50624z1), .R (
nx8480z1)) ;
MUXCY muxcy_0 (.O (nx8474z1), .CI (nx8473z1), .DI (nx8480z1), .S (nx51688z1)
) ;
MUXCY muxcy_1 (.O (nx8475z1), .CI (nx8474z1), .DI (nx8480z1), .S (nx51687z1)
) ;
MUXCY muxcy_2 (.O (nx8476z1), .CI (nx8475z1), .DI (nx8480z1), .S (nx51686z1)
) ;
MUXCY muxcy_3 (.O (nx8477z1), .CI (nx8476z1), .DI (nx8480z1), .S (nx51685z1)
) ;
MUXCY muxcy_4 (.O (nx8478z1), .CI (nx8477z1), .DI (nx8480z1), .S (nx51684z1)
) ;
MUXCY muxcy_5 (.O (nx8479z1), .CI (nx8478z1), .DI (nx8480z1), .S (nx51683z1)
) ;
MUXCY muxcy_6 (.O (nx51681z1), .CI (nx8479z1), .DI (nx8480z1), .S (nx51682z1
)) ;
MUXCY muxcy_7 (.O (nx8481z1), .CI (nx51681z1), .DI (nx8480z1), .S (nx8480z2)
) ;
MUXCY muxcy_8 (.O (nx51679z1), .CI (nx8481z1), .DI (nx8480z1), .S (nx51680z1
)) ;
MUXCY ALU1_Out_addsub9_0i1_muxcy_0 (.O (nx2749z1), .CI (nx2750z1), .DI (
CrossHierIn_7), .S (nx2750z2)) ;
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MUXCY ALU1_Out_addsub9_0i1_muxcy_1 (.O (nx2748z1), .CI (nx2749z1), .DI (
CrossHierIn_6), .S (nx2749z2)) ;
MUXCY ALU1_Out_addsub9_0i1_muxcy_2 (.O (nx2747z1), .CI (nx2748z1), .DI (
CrossHierIn_5), .S (nx2748z2)) ;
MUXCY ALU1_Out_addsub9_0i1_muxcy_3 (.O (nx2746z1), .CI (nx2747z1), .DI (
CrossHierIn_4), .S (nx2747z2)) ;
MUXCY ALU1_Out_addsub9_0i1_muxcy_4 (.O (nx2745z1), .CI (nx2746z1), .DI (
CrossHierIn_3), .S (nx2746z2)) ;
MUXCY ALU1_Out_addsub9_0i1_muxcy_5 (.O (nx2744z1), .CI (nx2745z1), .DI (
CrossHierIn_2), .S (nx2745z2)) ;
MUXCY ALU1_Out_addsub9_0i1_muxcy_6 (.O (nx2743z1), .CI (nx2744z1), .DI (
CrossHierIn_1), .S (nx2631z1)) ;
MUXCY ALU1_Out_addsub9_0i1_muxcy_7 (.O (nx2633z1), .CI (nx2743z1), .DI (
CrossHierIn_0), .S (nx2743z2)) ;
endmodule


module ram_dq_8_0 ( wr_data1, rd_data1, addr1, wr_clk1, rd_clk1, wr_ena1,
rd_ena1, ena1, rst1, regce1, regrst1, rd_access1, wr_data2,
rd_data2, addr2, wr_clk2, rd_clk2, wr_ena2, rd_ena2, ena2,
rst2, regce2, regrst2, rd_access2, p_MemWrite, p_Reset_int
) ;

input [7:0]wr_data1 ;
output [7:0]rd_data1 ;
input [7:0]addr1 ;
input wr_clk1 ;
input rd_clk1 ;
input wr_ena1 ;
input rd_ena1 ;
input ena1 ;
input rst1 ;
input regce1 ;
input regrst1 ;
output rd_access1 ;
input [7:0]wr_data2 ;
output [7:0]rd_data2 ;
input [7:0]addr2 ;
input wr_clk2 ;
input rd_clk2 ;
input wr_ena2 ;
input rd_ena2 ;
input ena2 ;
input rst2 ;
input regce2 ;
input regrst2 ;
output rd_access2 ;
input p_MemWrite ;
input p_Reset_int ;

wire nx16878z1, nx15881z1, nx14884z1, nx13887z1, nx12890z1, nx11893z1,
nx10896z1, nx9899z1, nx16878z2, nx15881z2, nx14884z2, nx13887z2,
nx12890z2, nx11893z2, nx10896z2, nx9899z2, nx16878z3, nx15881z3,
nx14884z3, nx13887z3, nx12890z3, nx11893z3, nx10896z3, nx9899z3,
nx16878z4, nx15881z4, nx14884z4, nx13887z4, nx12890z4, nx11893z4,
nx10896z4, nx9899z4, nx16083z1, nx16083z2, nx16086z1, nx16089z1,
nx23513z1;
wire [15:0] \$dummy ;



RAM64M core_1 (.DOA (nx16878z1), .DOB (nx15881z1), .DOC (nx14884z1), .ADDRA (
{addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRB ({
addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRC ({
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addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRD ({
wr_data1[5],addr1[4],addr1[3],addr1[2],addr1[1],addr1[0]}), .DIA (
wr_data1[0]), .DIB (wr_data1[1]), .DIC (wr_data1[2]), .DID (nx16083z1
), .WCLK (wr_clk1), .WE (nx16083z2)) ;
RAM64M core_2 (.DOA (nx13887z1), .DOB (nx12890z1), .DOC (nx11893z1), .ADDRA (
{addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRB ({
addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRC ({
addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRD ({
wr_data1[5],addr1[4],addr1[3],addr1[2],addr1[1],addr1[0]}), .DIA (
wr_data1[3]), .DIB (wr_data1[4]), .DIC (wr_data1[5]), .DID (nx16083z1
), .WCLK (wr_clk1), .WE (nx16083z2)) ;
RAM64M core_3 (.DOA (nx10896z1), .DOB (nx9899z1), .ADDRA ({addr2[5],addr2[4]
,addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRB ({addr2[5],addr2[4],
addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRC ({addr2[5],addr2[4],
addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRD ({wr_data1[5],addr1[4],
addr1[3],addr1[2],addr1[1],addr1[0]}), .DIA (wr_data1[6]), .DIB (
wr_data1[7]), .DIC (nx16083z1), .DID (nx16083z1), .WCLK (wr_clk1), .WE (
nx16083z2)) ;
RAM64M core_4 (.DOA (nx16878z2), .DOB (nx15881z2), .DOC (nx14884z2), .ADDRA (
{addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRB ({
addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRC ({
addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRD ({
wr_data1[5],addr1[4],addr1[3],addr1[2],addr1[1],addr1[0]}), .DIA (
wr_data1[0]), .DIB (wr_data1[1]), .DIC (wr_data1[2]), .DID (nx16083z1
), .WCLK (wr_clk1), .WE (nx16086z1)) ;
RAM64M core_5 (.DOA (nx13887z2), .DOB (nx12890z2), .DOC (nx11893z2), .ADDRA (
{addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRB ({
addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRC ({
addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRD ({
wr_data1[5],addr1[4],addr1[3],addr1[2],addr1[1],addr1[0]}), .DIA (
wr_data1[3]), .DIB (wr_data1[4]), .DIC (wr_data1[5]), .DID (nx16083z1
), .WCLK (wr_clk1), .WE (nx16086z1)) ;
RAM64M core_6 (.DOA (nx10896z2), .DOB (nx9899z2), .ADDRA ({addr2[5],addr2[4]
,addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRB ({addr2[5],addr2[4],
addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRC ({addr2[5],addr2[4],
addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRD ({wr_data1[5],addr1[4],
addr1[3],addr1[2],addr1[1],addr1[0]}), .DIA (wr_data1[6]), .DIB (
wr_data1[7]), .DIC (nx16083z1), .DID (nx16083z1), .WCLK (wr_clk1), .WE (
nx16086z1)) ;
RAM64M core_7 (.DOA (nx16878z3), .DOB (nx15881z3), .DOC (nx14884z3), .ADDRA (
{addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRB ({
addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRC ({
addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRD ({
wr_data1[5],addr1[4],addr1[3],addr1[2],addr1[1],addr1[0]}), .DIA (
wr_data1[0]), .DIB (wr_data1[1]), .DIC (wr_data1[2]), .DID (nx16083z1
), .WCLK (wr_clk1), .WE (nx16089z1)) ;
RAM64M core_8 (.DOA (nx13887z3), .DOB (nx12890z3), .DOC (nx11893z3), .ADDRA (
{addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRB ({
addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRC ({
addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRD ({
wr_data1[5],addr1[4],addr1[3],addr1[2],addr1[1],addr1[0]}), .DIA (
wr_data1[3]), .DIB (wr_data1[4]), .DIC (wr_data1[5]), .DID (nx16083z1
), .WCLK (wr_clk1), .WE (nx16089z1)) ;
RAM64M core_9 (.DOA (nx10896z3), .DOB (nx9899z3), .ADDRA ({addr2[5],addr2[4]
,addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRB ({addr2[5],addr2[4],
addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRC ({addr2[5],addr2[4],
addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRD ({wr_data1[5],addr1[4],
addr1[3],addr1[2],addr1[1],addr1[0]}), .DIA (wr_data1[6]), .DIB (
wr_data1[7]), .DIC (nx16083z1), .DID (nx16083z1), .WCLK (wr_clk1), .WE (
nx16089z1)) ;
RAM64M core_10 (.DOA (nx16878z4), .DOB (nx15881z4), .DOC (nx14884z4), .ADDRA (
{addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRB ({
addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRC ({
addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRD ({
wr_data1[5],addr1[4],addr1[3],addr1[2],addr1[1],addr1[0]}), .DIA (
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wr_data1[0]), .DIB (wr_data1[1]), .DIC (wr_data1[2]), .DID (nx16083z1
), .WCLK (wr_clk1), .WE (nx23513z1)) ;
RAM64M core_11 (.DOA (nx13887z4), .DOB (nx12890z4), .DOC (nx11893z4), .ADDRA (
{addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRB ({
addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRC ({
addr2[5],addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRD ({
wr_data1[5],addr1[4],addr1[3],addr1[2],addr1[1],addr1[0]}), .DIA (
wr_data1[3]), .DIB (wr_data1[4]), .DIC (wr_data1[5]), .DID (nx16083z1
), .WCLK (wr_clk1), .WE (nx23513z1)) ;
RAM64M core_12 (.DOA (nx10896z4), .DOB (nx9899z4), .ADDRA ({addr2[5],
addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRB ({addr2[5],
addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRC ({addr2[5],
addr2[4],addr2[3],addr2[2],addr2[1],addr2[0]}), .ADDRD ({wr_data1[5],
addr1[4],addr1[3],addr1[2],addr1[1],addr1[0]}), .DIA (wr_data1[6]), .DIB (
wr_data1[7]), .DIC (nx16083z1), .DID (nx16083z1), .WCLK (wr_clk1), .WE (
nx23513z1)) ;
GND ps_gnd (.G (nx16083z1)) ;
LUT6 ix16878z22834 (.O (rd_data2[0]), .I0 (addr2[7]), .I1 (addr2[6]), .I2 (
nx16878z1), .I3 (nx16878z2), .I4 (nx16878z3), .I5 (nx16878z4)) ;
defparam ix16878z22834.INIT = 64'hFEBADC9876325410;
LUT6 ix15881z22834 (.O (rd_data2[1]), .I0 (addr2[7]), .I1 (addr2[6]), .I2 (
nx15881z1), .I3 (nx15881z2), .I4 (nx15881z3), .I5 (nx15881z4)) ;
defparam ix15881z22834.INIT = 64'hFEBADC9876325410;
LUT6 ix14884z22834 (.O (rd_data2[2]), .I0 (addr2[7]), .I1 (addr2[6]), .I2 (
nx14884z1), .I3 (nx14884z2), .I4 (nx14884z3), .I5 (nx14884z4)) ;
defparam ix14884z22834.INIT = 64'hFEBADC9876325410;
LUT6 ix13887z22834 (.O (rd_data2[3]), .I0 (addr2[7]), .I1 (addr2[6]), .I2 (
nx13887z1), .I3 (nx13887z2), .I4 (nx13887z3), .I5 (nx13887z4)) ;
defparam ix13887z22834.INIT = 64'hFEBADC9876325410;
LUT6 ix12890z22834 (.O (rd_data2[4]), .I0 (addr2[7]), .I1 (addr2[6]), .I2 (
nx12890z1), .I3 (nx12890z2), .I4 (nx12890z3), .I5 (nx12890z4)) ;
defparam ix12890z22834.INIT = 64'hFEBADC9876325410;
LUT6 ix11893z22834 (.O (rd_data2[5]), .I0 (addr2[7]), .I1 (addr2[6]), .I2 (
nx11893z1), .I3 (nx11893z2), .I4 (nx11893z3), .I5 (nx11893z4)) ;
defparam ix11893z22834.INIT = 64'hFEBADC9876325410;
LUT6 ix10896z22834 (.O (rd_data2[6]), .I0 (addr2[7]), .I1 (addr2[6]), .I2 (
nx10896z1), .I3 (nx10896z2), .I4 (nx10896z3), .I5 (nx10896z4)) ;
defparam ix10896z22834.INIT = 64'hFEBADC9876325410;
LUT6 ix9899z22834 (.O (rd_data2[7]), .I0 (addr2[7]), .I1 (addr2[6]), .I2 (
nx9899z1), .I3 (nx9899z2), .I4 (nx9899z3), .I5 (nx9899z4)) ;
defparam ix9899z22834.INIT = 64'hFEBADC9876325410;
(* HLUTNM = "LUT62_1_1" *)
LUT4 ix16083z1571 (.O (nx16083z2), .I0 (addr2[7]), .I1 (addr1[6]), .I2 (
p_Reset_int), .I3 (p_MemWrite)) ;
defparam ix16083z1571.INIT = 16'h0100;
(* HLUTNM = "LUT62_1_1" *)
LUT4 ix16086z2338 (.O (nx16086z1), .I0 (addr2[7]), .I1 (addr1[6]), .I2 (
p_Reset_int), .I3 (p_MemWrite)) ;
defparam ix16086z2338.INIT = 16'h0400;
(* HLUTNM = "LUT62_1_2" *)
LUT4 ix16089z14162 (.O (nx16089z1), .I0 (addr2[7]), .I1 (addr1[6]), .I2 (
p_Reset_int), .I3 (p_MemWrite)) ;
defparam ix16089z14162.INIT = 16'h3230;
(* HLUTNM = "LUT62_1_2" *)
LUT4 ix23513z52706 (.O (nx23513z1), .I0 (addr2[7]), .I1 (addr1[6]), .I2 (
p_Reset_int), .I3 (p_MemWrite)) ;
defparam ix23513z52706.INIT = 16'hC8C0;
endmodule
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