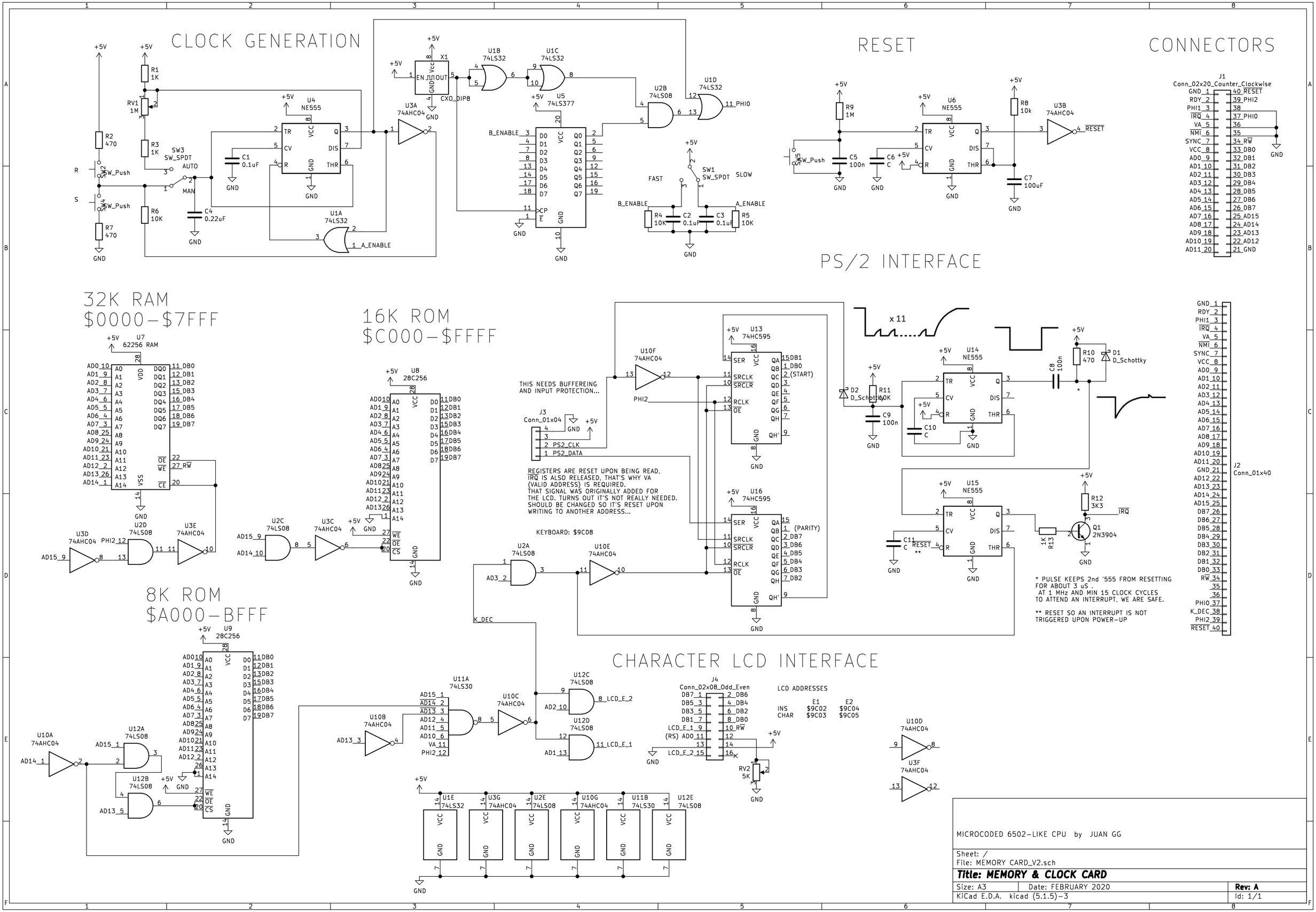
CLOCK GENERATION
RESET
CONNECTORS
PS/2 INTERFACE
32K RAM
$0000–$7FFF
16K ROM
$C000–$FFFF
8K ROM
$A000–BFFF
CHARACTER LCD INTERFACE
THIS NEEDS BUFFEREING AND INPUT PROTECTION...
REGISTERS ARE RESET UPON BEING READ, IRQ IS ALSO RELEASED. THAT'S WHY VA (VALID ADDRESS) IS REQUIRED. THAT SIGNAL WAS ORIGINALLY ADDED FOR THE LCD. TURNS OUT IT'S NOT REALLY NEEDED. SHOULD BE CHANGED SO IT'S RESET UPON WRITING TO ANOTHER ADDRESS...
KEYBOARD: $9C08
LCD ADDRESSES
INS $9C02 $9C04
CHAR $9C03 $9C05
* PULSE KEEPS 2nd '555 FROM RESETTING FOR ABOUT 3 uS . AT 1 MHz AND MIN 15 CLOCK CYCLES TO ATTEND AN INTERRUPT, WE ARE SAFE.
** RESET SO AN INTERRUPT IS NOT TRIGGERED UPON POWER–UP
MICROCODED 6502–LIKE CPU by JUAN GG
Sheet: /
File: MEMORY CARD_V2.sch
Title: MEMORY & CLOCK CARD
Size: A3
Date: FEBRUARY 2020
Rev: A
KiCad E.D.A. kicad (5.1.5)–3
Id: 1/1