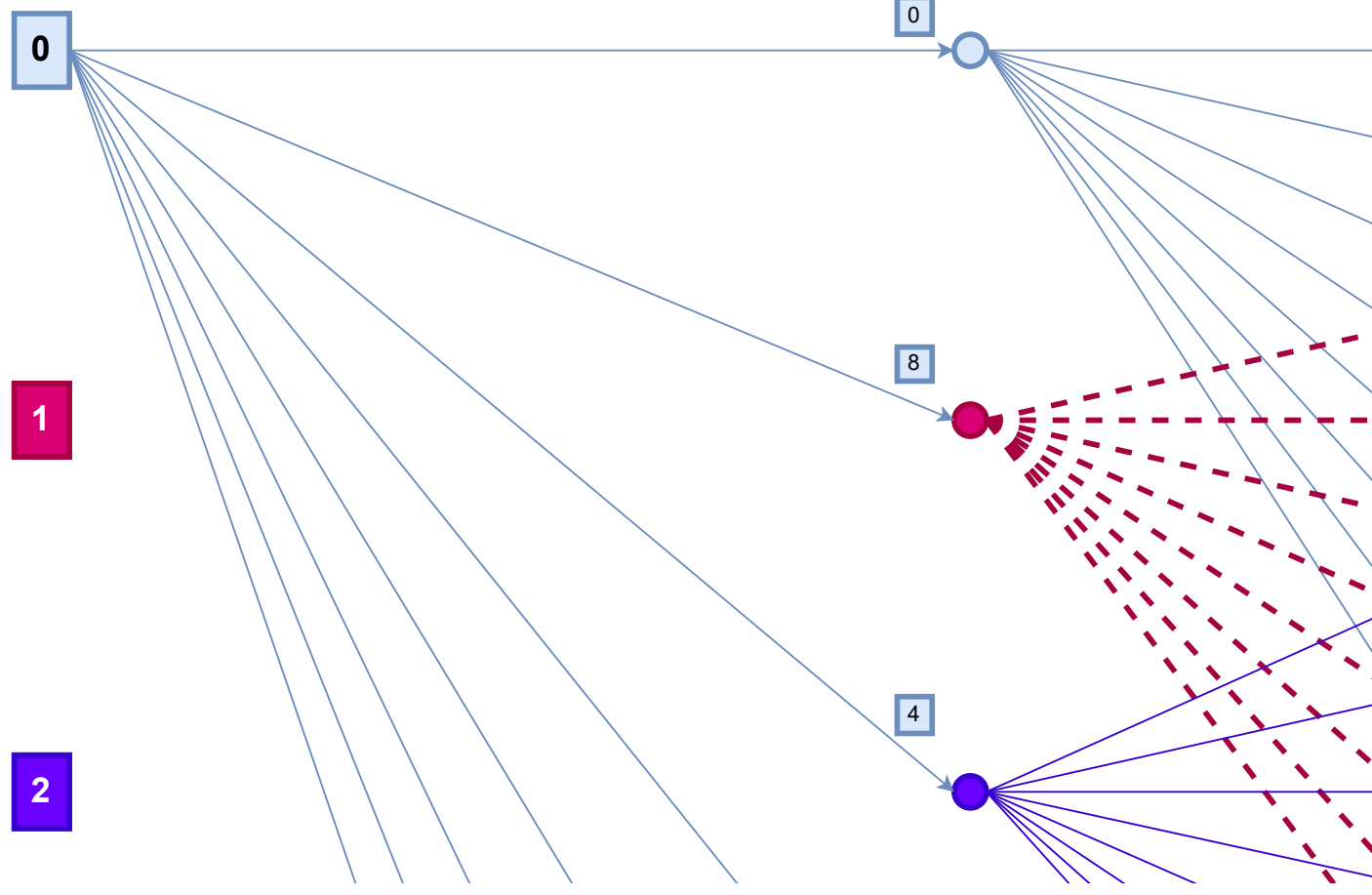
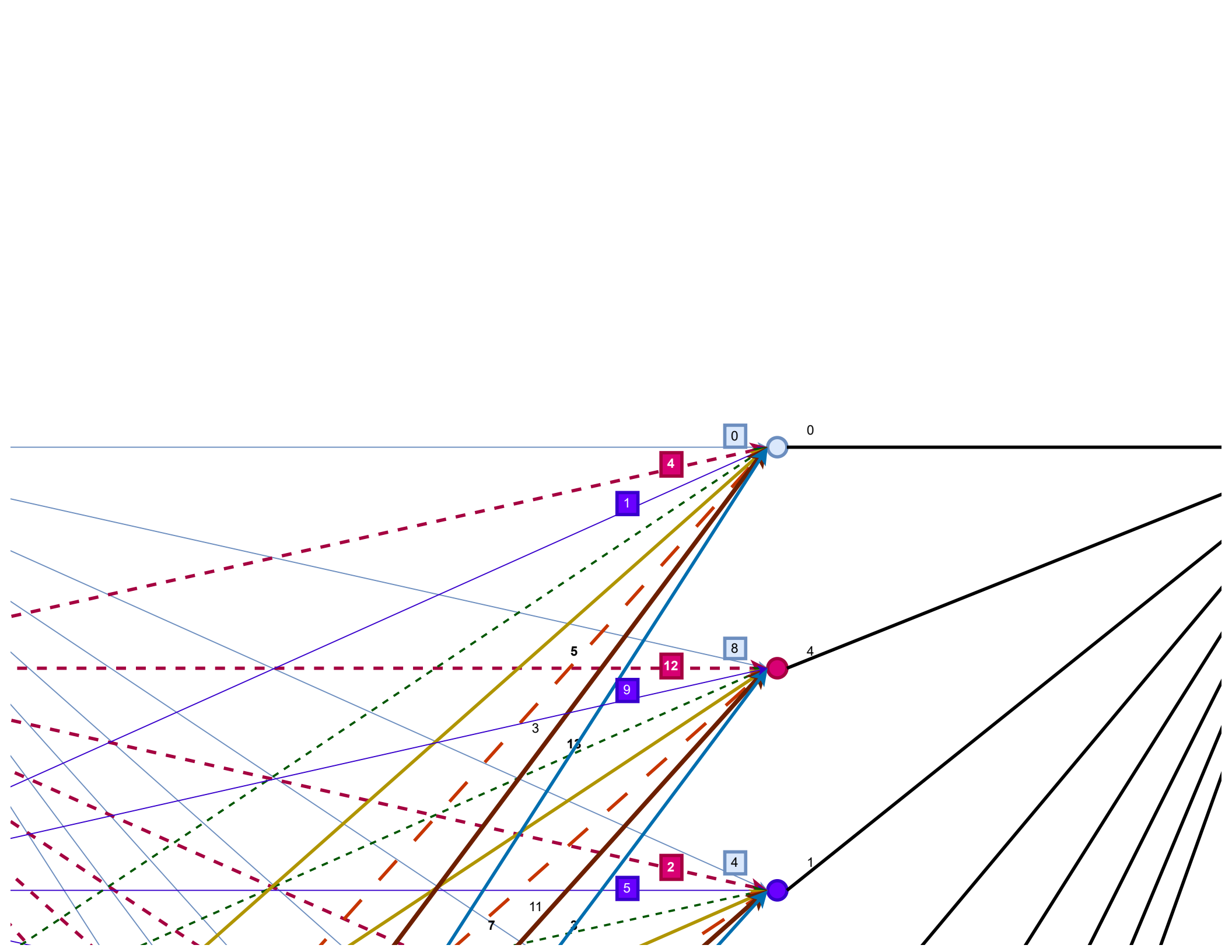


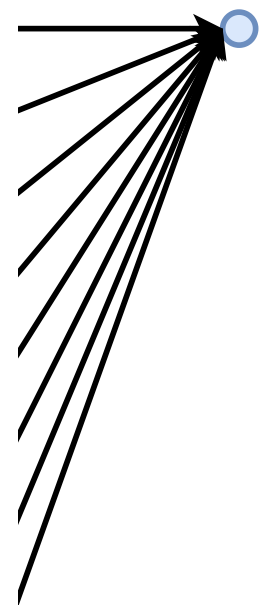
		input							
		0	1	2	3	4	5	6	7
FSM state	0	0000	1000	0100	1100	0010	1010	0110	1110
	1	0100	1100	0010	1010	0110	1110	0000	1000
	2	0001	1001	0101	1101	0011	1011	0111	1111
	3	0101	1101	0011	1011	0111	1111	0001	1001
	4	0011	1011	0111	1111	0001	1001	0101	1101
	5	0111	1111	0001	1001	0101	1101	0011	1011
	6	0010	1010	0110	1110	0000	1000	0100	1100
	7	0110	1110	0000	1000	0100	1100	0010	1010

		input							
		0	1	2	3	4	5	6	7
FSM state	0	0	8	4	12	2	10	6	14
	1	4	12	2	10	6	14	0	8
	2	1	9	5	13	3	11	7	15
	3	5	13	3	11	7	15	1	9
	4	3	11	7	15	1	9	5	13
	5	7	15	1	9	5	13	3	11
	6	2	10	6	14	0	8	4	12
	7	6	14	0	8	4	12	2	10

		input							
		0	1	2	3	4	5	6	7
FSM state	0	0000	1000	0100	1100	0010	1010	0110	1110
	1	0100	1100	0010	1010	0110	1110	0000	1000
	2	0001	1001	0101	1101	0011	1011	0111	1111
	3	0101	1101	0011	1011	0111	1111	0001	1001
	4	0011	1011	0111	1111	0001	1001	0101	1101
	5	0111	1111	0001	1001	0101	1101	0011	1011
	6	0010	1010	0110	1110	0000	1000	0100	1100
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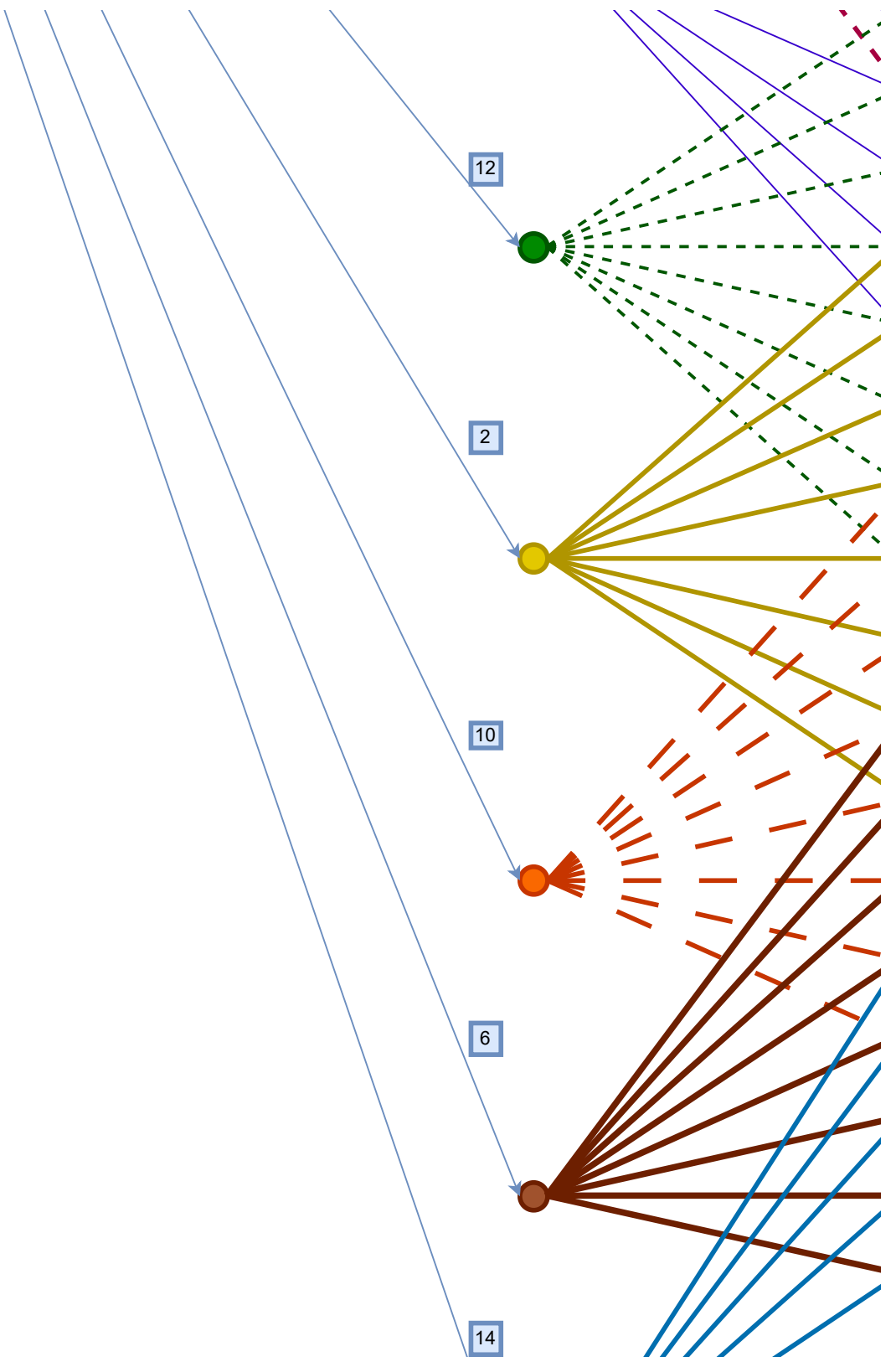


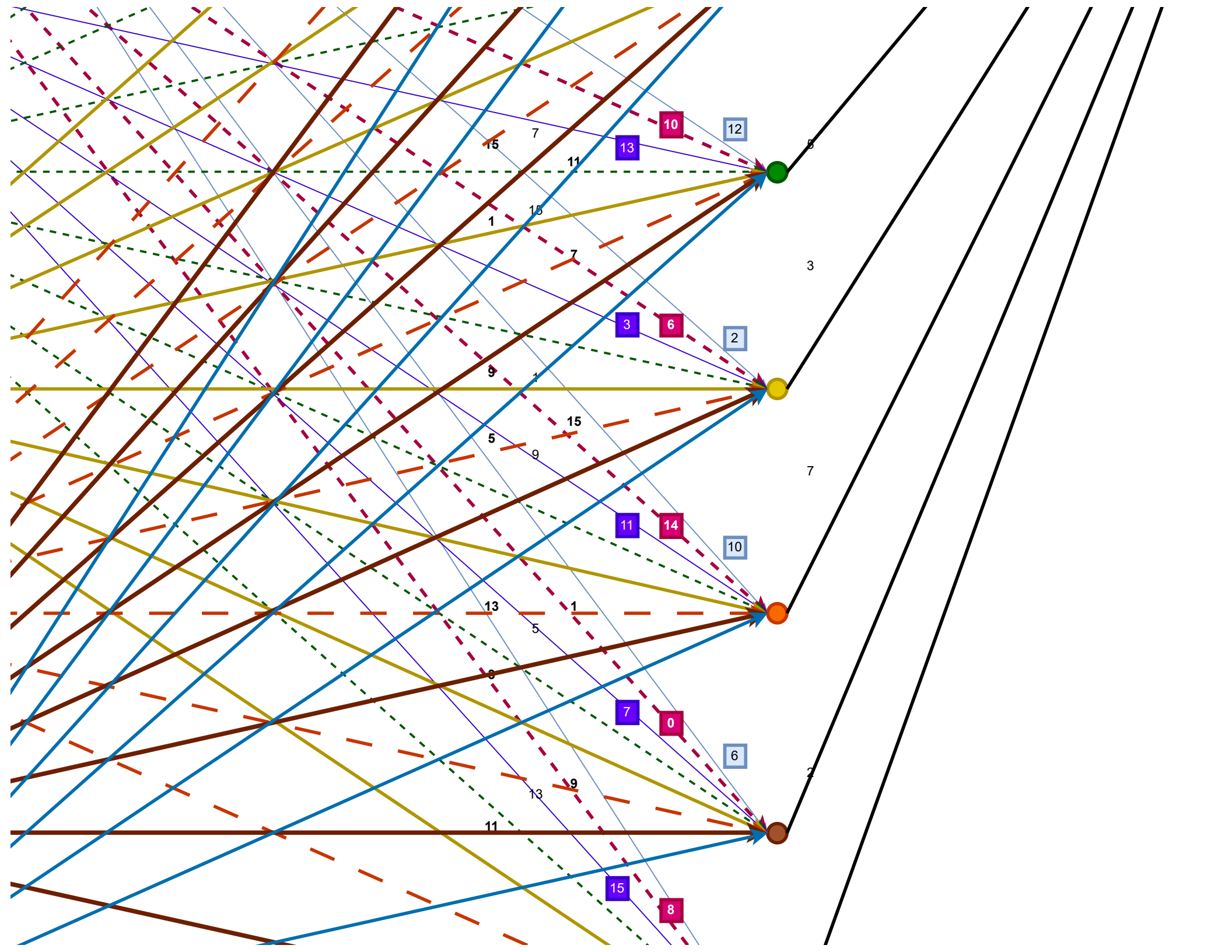
3

4

5

6



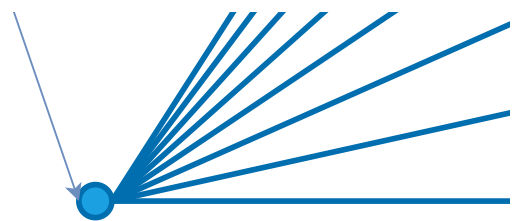


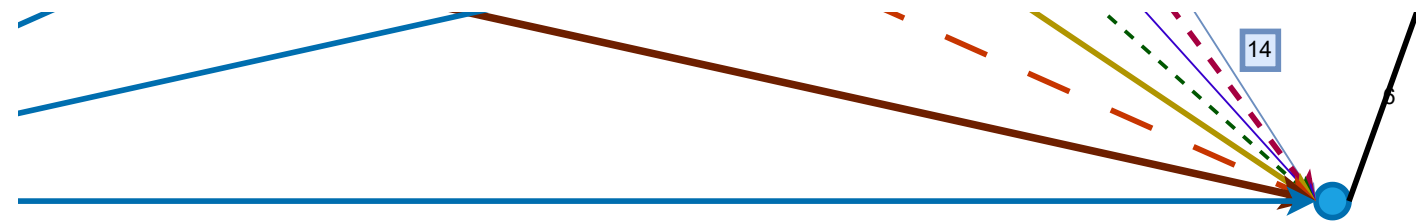




7

$t_0$





$$t_n \leq t_{i-1}$$

$$t_i$$

