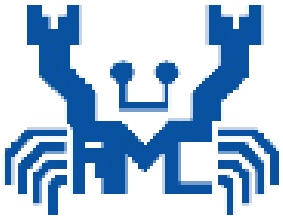

REALTEK

RTL8735BDM-VA3-CG **RTL8735BM-VA3-CG**
RTL8735BDM-VL3-CG **RTL8735BM-VL3-CG**
RTL8735BDM-VA4-CG **RTL8735BM-VA4-CG**
RTL8735BDM-VL4-CG **RTL8735BM-VL4-CG**

AmebaPro-II
Highly Integrated, Ultra-Low-Power IEEE 802.11a/b/g/n Compatible 1T1R WLAN + Bluetooth Camera SoC

DATASHEET

(CONFIDENTIAL: For AmebaIoT registered user Only)

Rev. 1.0 Lite
2022

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
1.0 Lite		First lite release.

Table of Contents

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1. General Description

The Realtek RTL8735B (also named AmebaPro-II) is a highly integrated low-power 802.11a/b/g/n Wireless LAN (WLAN) and Bluetooth camera SoC. It combines ARM v8M MCUs (500MHz and 2.23 DMIPS/MHz), WLAN MAC, a 1T1R capable WLAN baseband, Bluetooth MAC, RF, audio codec, ISP and H264/H265 encoder in a single chip. It provides useful high speed connectivity interfaces, such as USB 2.0 host, USB 2.0 device, SD host and Ethernet interfaces. It also provides a bunch of configurable GPIOs which are configured as digital peripherals for different application and control usage.

The AmebaPro-II series integrates internal memory for full Wi-Fi protocol functions. The embedded memory configuration also enables various application development.

2. Features

MCU Features

- Real-M500 (TM9) clock frequency up to 500MHz
- I-Cache 32KB/D-Cache 32KB
- eXecute In Place (XIP) on NOR flash
- Internal Memory
- Supports 768KB ROM
- Supports 512KB RAM
- Supports external flash interface
- Supports MCM embedded 64MB/128MB DDR2 Memory
- Supports MCM embedded 64MB/128MB DDR3L Memory

ISP Features

- Advanced temporal and spatial noise reduction(3DNR)
- Supports major brands of DOL-HDR or Staggered-HDR sensors
- Supports 12bit Bayer pattern input and 8bit YUY2 input from CMOS sensor
- Supports MIPI CSI-2 four data lane
- Supports Auto Banding, Auto Exposure, Auto White Balance
- Black level compensation and dead pixel cancellation
- Lens shading compensation
- Lens distortion correction
- High dynamic range fusion and tone mapping for HDR sensor input
- Advanced Contrast Adjustment and Sharpness Enhancement
- Programmable color matrix and gamma table
- Digital WDR
- Image enhancement(brightness, contrast, saturation, hue and sharpness)
- ISP tuning tool

Graphic Processing

- Digital resolution scaling up and down
- Multiple stream outputs and various formats: NV12, RGB888
- Each stream has individual OSD overlay
- Supports motion detection and private mask

Video Encoding

- Max 5-megapixel resolution for H.264/H.265 encoding
- H.264 Baseline/Main/High profiles, levels 4.1
- H.265 Main and Main Still profiles, levels 4
- JPEG/MJPEG Baseline and Max 5-megapixel resolution for JPEG encoding
- Multiple streams real-time H.265/H.264/JPEG encoding
- H265 2M@30fps + H265 1M@30fps
- CBR/VBR rate control

Intelligent Engine

- 0.384 TOPS
- 384 MAC
- Engine Precision: INT8/INT16

Wi-Fi Features

- 802.11 a/b/g/n compatible 1x1, 2.4GHz/5GHz
- 802.11e QoS Enhancement (WMM)
- Wi-Fi WEP, WPA, WPA2, WPA3, WPS. Open, shared key, and pair-wise key authentication services
- Supports low-power Tx/Rx for short-range application
- Supports Antenna diversity
- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- Long NAV for media reservation with CF-End for NAV release
- Integrated Balun, PA/LNA

Bluetooth Low Energy

- Bluetooth Low Energy (BLE) 5.1
- Supports LE secure connections
- Supports LE scatternet
- Supports 1 Master/1 Slave

Security

- Supports secure boot
- Crypto engine: MD5, SHA-1, SHA2-224, SHA2-256, HMAC, AES
- ECDSA, ED25519
- RSA

Peripheral Interfaces

- Maximum 4 UART interface, baud rate up to 4MHz and all of them can be configurable as log UART
- Maximum 4 I2C interface, Max clock 400Kbps
- Maximum 2 SPI interface, Master clock up to 25Mbps/Slave clock up to 31.25Mbps
- Maximum 12 PWM interface with configurable duration and duty cycle from 0 ~ 100%
- Maximum 8 ADC channel with 12-bit mode with maximum 31.5KHz
- Maximum 59 programmable GPIOs
- 2 GDMA and each with maximum 6 channels
- Maximum 4 Comparator channel
- Supports Watchdog Timer

Clock Source

- 40MHz crystal oscillator

Package Type

- 10mm x 10mm x 1.5mm
- QFN128 pins

3. Block Diagram

The AmebaPro-II diagram shown below provides a general application scenario. External devices can be connected with the various peripheral interfaces. The PMU and related blocks for low power application are also elaborated on this diagram.

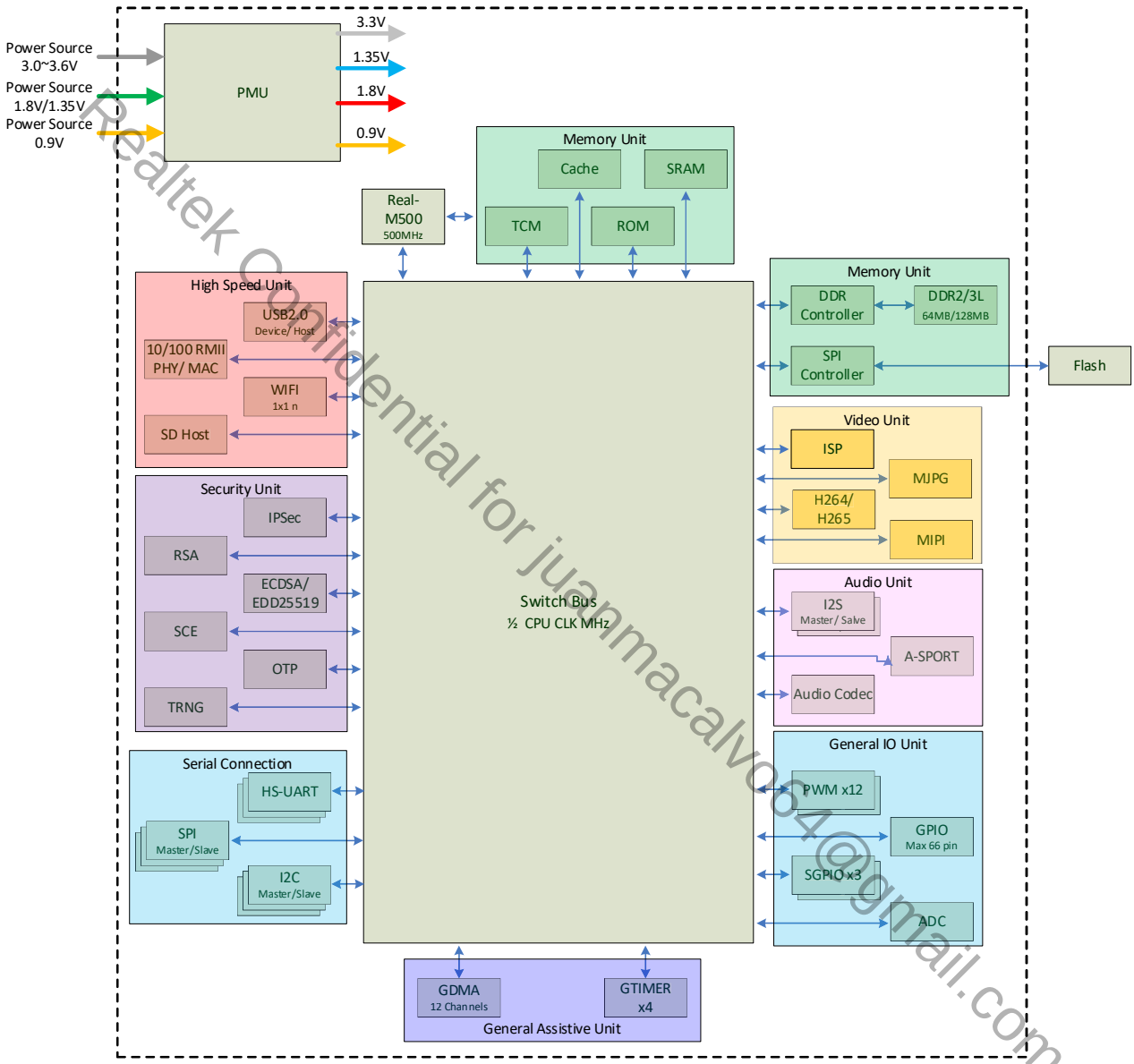


Figure 1. Block Diagram of AmebaPro-II

3.1. Power Architecture

Figure 2 shows the AmebaPro-II power management control unit architecture.

The PMU provides the following functions:

- SWR 1.35V output from 3.3V for RF units
- LDO 1.8V output from 3.3V for SD interface
- Wakeup system detector to resume from low power state

3.1.1. AmebaPro-II Regulator Architecture

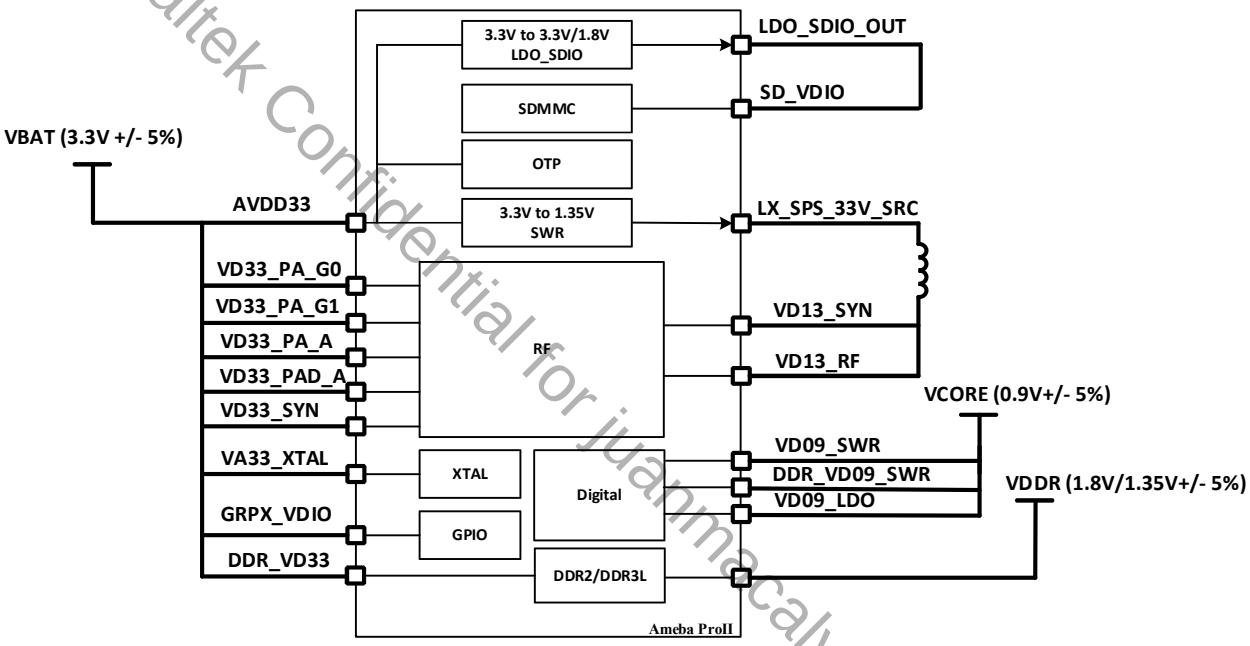


Figure 2. AmebaPro-II Regulator Architecture

Note: The Internal SWR does not support LDO Mode.

3.1.2. Shutdown Mode

CHIP_EN de-asserts to shut down the whole chip, without external power cut components required.

CHIP_EN pull-high-triggers the system back to active mode.

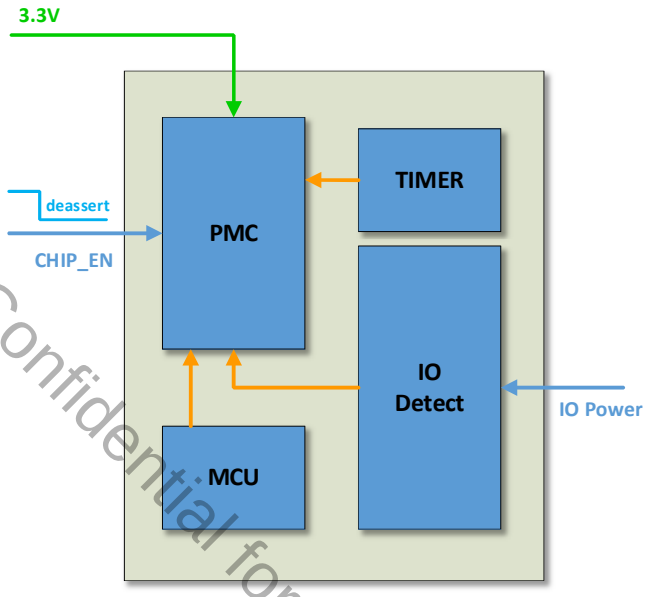


Figure 3. Power Diagram of Shutdown Mode

3.1.3. Deep Sleep Mode

CHIP_EN remains high. Users can invoke Deep Sleep API to enter deep sleep mode.

Specified interrupts can wake up the system.

The wake flow is:

1. Wake up ISR is high
2. PMC
3. Enable CPU
4. Reboot flow

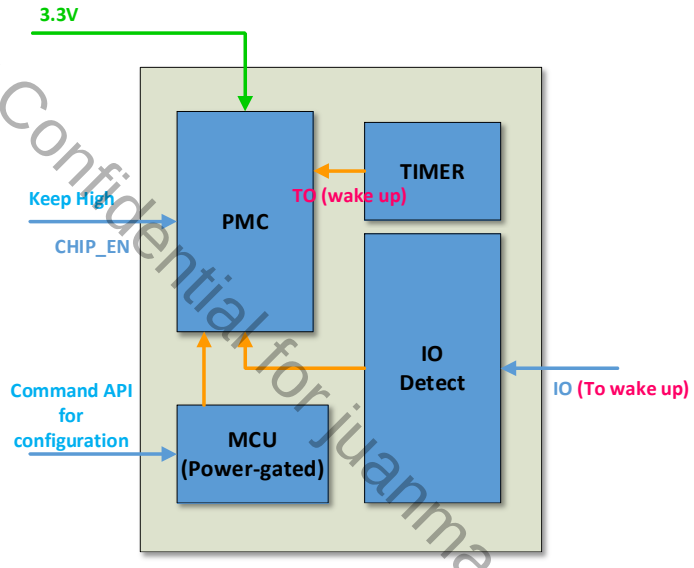


Figure 4. Diagram of Deep Sleep Mode

Table 1. Deep Sleep Mode Wakeup Source

Available Wakeup Source	Related Pins
AON Timer	N/A
Wake pin	GPIOA0~GPIOA3
RTC	N/A
Comparator	GPIOA0~GPIOA3

3.1.4. Standby Mode

CHIP_EN remains high. Users can invoke Standby API to enter standby mode.

Specified interrupts can wake up the system.

The wake flow is:

1. Wake up ISR is high
2. PMC
3. Enable CPU
4. Reboot flow

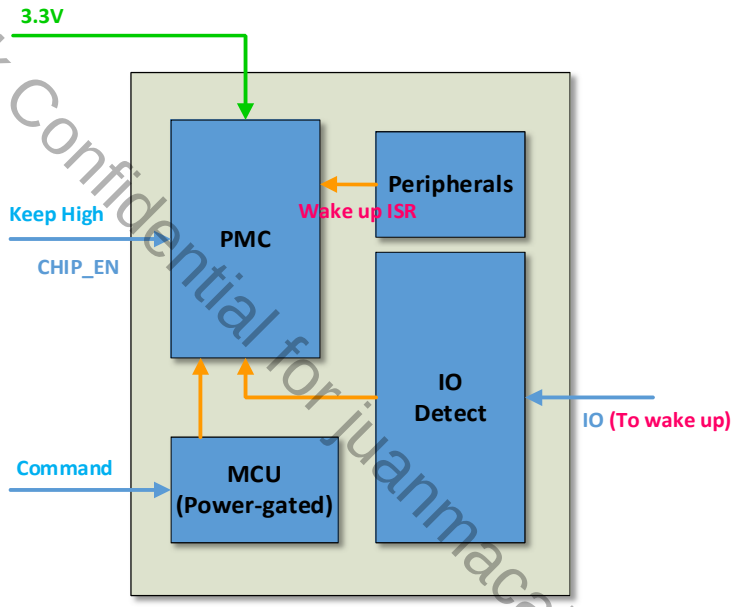


Figure 5. Power Diagram of Standby Mode

Table 2. Standby Mode Wakeup Source

Available Wakeup Source	Related Pins
AON Timer	N/A
Wake pin	GPIOA0~GPIOA3 and GPIOF0~GPIOF17
RTC	N/A
Comparator	GPIOA0~GPIOA3
UART0	GPIOA2~GPIOA3
WLAN	N/A
Timer Group0	N/A

3.1.5. Sleep Mode

CHIP_EN remains high. Users can invoke Sleep API to enter sleep mode.

Specified interrupts can wake up the system.

The wake flow is:

1. Wake up ISR is high
2. PMC
3. Enable CPU
4. Execution of instructions continues

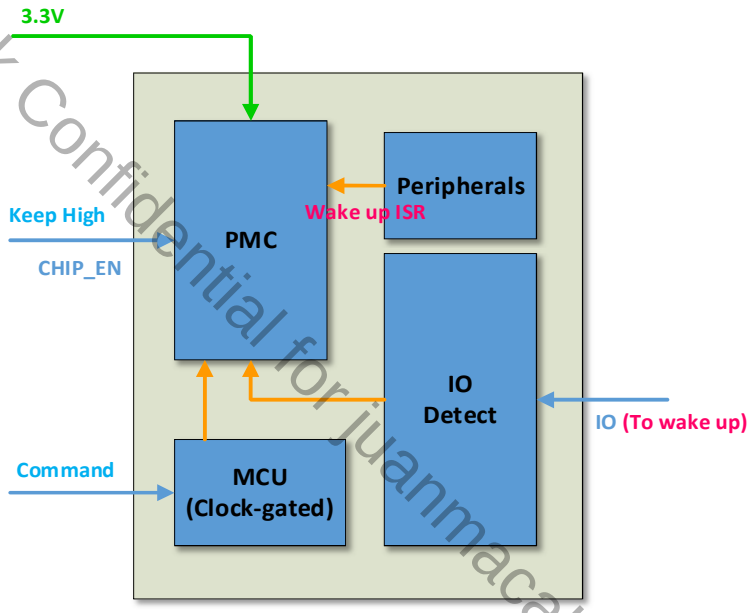


Figure 6. Power Diagram of Sleep Mode

Table 3. Sleep Mode Wakeup Source

Available Wakeup Source	Related Pins
AON Timer	N/A
Wake pin	GPIOA0~GPIOA3 and GPIOF0~GPIOF17
RTC	N/A
Comparator	GPIOA0~GPIOA3
UART0	GPIOA2~GPIOA3
WLAN	N/A
Timer Group0	N/A

3.1.6. Snooze Mode

CHIP_EN remains high. Specified interrupts can wake up the system.

The wake flow is:

1. WLAN power on request
2. Receive particular beacon
3. Wake up ISR is high
4. PMC
5. Enable CPU
6. Execution of instructions continues or Reboot occurs

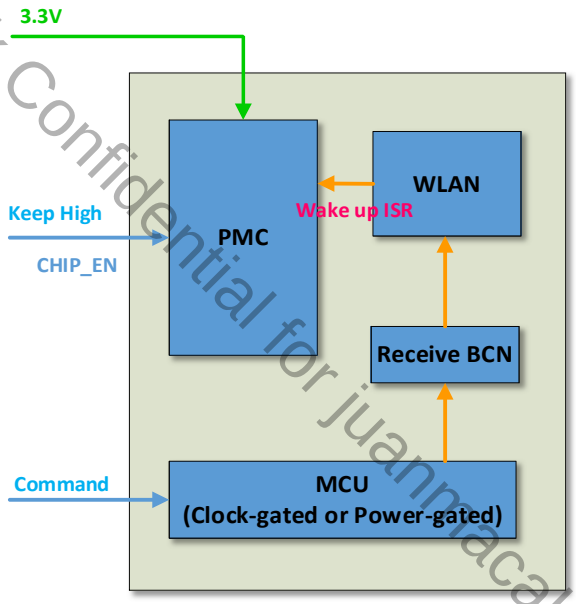


Figure 7. Power Diagram of Snooze Mode

4. Pin Assignments

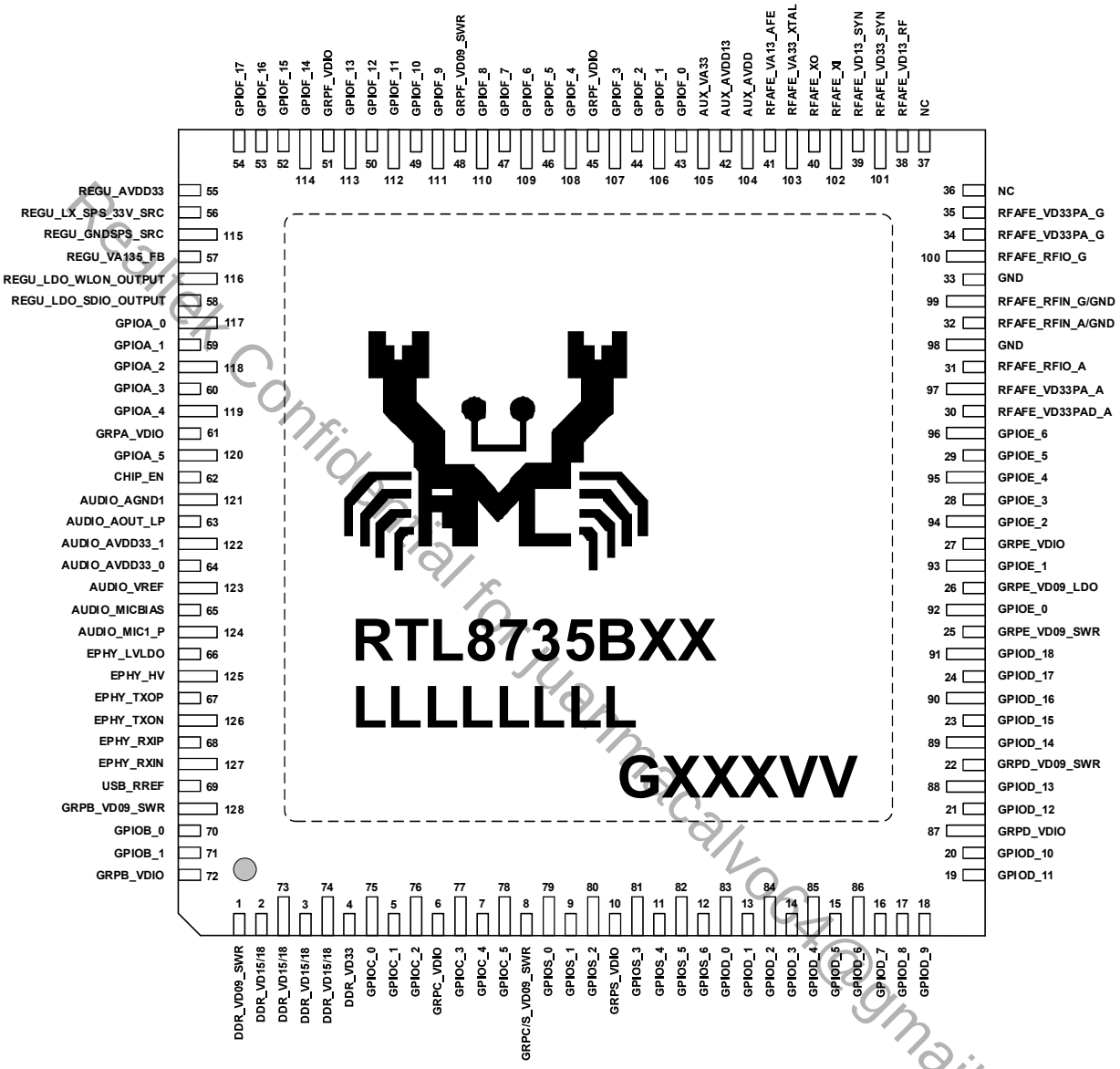


Figure 8. Pin Assignments

4.1. Package Identification

XX in the model number in Figure 8 indicates the IC model (BM or DM). The version (A3, L3, A4, L4) is indicated in the VV location in GXXXVV. Green package is indicated by the 'G' in GXXXVV. For a full list of packages see section 9 Ordering Information, page 33.

5. Pin Descriptions

The signal type codes below are used in the following tables:

I: Input

O: Output

PI: Power Input

PO: Power Output

G: Ground

5.1. Power On Trap Pins

Table 4. Power On Trap Pins

Symbol	Type	Pin No.	Description
DOWNLOAD_EN	I	120	Shared with GPIOA_5. 1: Flash download mode 0: Normal operation mode
RESERVED	I	119	Shared with GPIOA_4. MUST keep low during power-on sequence.

5.2. Analog to Digital Converter

Table 5. ADC Pins

Symbol	Type	Pin No.	Description
ADC0	I	43	Shared with GPIOF_0. AD converter input channel 0.
ADC1	I	106	Shared with GPIOF_1. AD converter input channel 1.
ADC2	I	44	Shared with GPIOF_2. AD converter input channel 2.
ADC3	I	107	Shared with GPIOF_3. AD converter input channel 3.
ADC4	I	117	Shared with GPIOA_0. AD converter input channel 4.
ADC5	I	59	Shared with GPIOA_1. AD converter input channel 5.
ADC6	I	118	Shared with GPIOA_2. AD converter input channel 6.
ADC7	I	60	Shared with GPIOA_3. AD converter input channel 7.

5.3. RF Pin

Table 6. RF Pins

Symbol	Type	Pin No.	Description
RFAFE_RFIO_A	IO	31	WL RF 5G signal.
RFAFE_RFIN_A	I	32	WL RF 5G signal.
RFAFE_RFIO_G	IO	100	WL RF 2.4G signal.
RFAFE_RFIN_G	I	99	WL RF 2.4G signal.

5.4. Power Pins

Table 7. Power Pins

Symbol	Type	Pin No.	Description
DDR_VD09_SWR	PI	1	0.9V power for DDR.
DDR_VD15/18	PI	2 3 73 74	1.8V/1.35V power for DDR.
DDR_VD33	PI	4	3.3V power for DDR.
GRPC_VDIO	PI	6	3.3V power for GPIOC.
GRPC/S_VD09_SWR	PI	8	0.9V power for GPIOC/S.
GRPS_VDIO	PI	10	3.3V/1.8V power (from PIN58) for GPIOS.
GRPD_VDIO	PI	87	3.3V power for GPIOD.
GRPD_VD09_SWR	PI	22	0.9V power for GPIOD.
GRPE_VD09_SWR	PI	25	0.9V power for GPIOE.
GRPE_VD09_LDO	PI	26	0.9V power for PON and WLON power.
GRPE_VDIO	PI	27	3.3V power for GPIOE.
RFAFE_VD33PAD_A RFAFE_VD33PA_A RFAFE_VD33PA_G RFAFE_VD33_SYN RFAFE_VA33_XTAL AUX_VA33 AUDIO_AVDD33_1	PI	30 97 34 35 101 103 105 122	3.3V power source for analog blocks.
RFAFE_VD13_RF RFAFE_VD13_SYN RFAFE_VA13_AFE AUX_AVDD13	PI	38 39 41 42	1.35V power source for analog blocks.
AUX_AVDD	PI	104	0.9V power source for analog blocks.
GRPF_VDIO	PI	45 51	3.3V power for GPIOF.
GRPF_VD09_SWR	PI	48	0.9V power for GPIOF.
REGU_AVDD33	PI	55	3.3V power source for switching regulator blocks.
REGU_LX_SPS_33V_SRC	PO	56	Switching regulator output, 1.35V±5%.
REGU_VA135_FB	PI	57	Switching regulator feedback.
REGU_LDO_WLON_OUTPUT	PO	116	Linear regulator output, 0.9V±5%.
REGU_LDO_SDIO_OUTPUT	PO	58	Linear regulator output, 3.3V±5% or 1.8V±5%.

Symbol	Type	Pin No.	Description
GRPA_VDIO	PI	61	3.3V power for GPIOA.
EPHY_LVLDO	PI	66	0.9V power for Ethernet PHY.
EPHY_HV	PI	125	3.3V power for Ethernet PHY.
GRPB_VD09_SWR	PI	128	0.9V power for GPIOB.
GRPB_VDIO	PI	72	3.3V power for GPIOB.

5.5. Clock Pins

Table 8. Clock and Other Pins

Symbol	Type	Pin No.	Description
RFAFE_XI	I	102	Input of 40MHz Crystal Clock Reference.
RFAFE_XO	O	40	Output of 40MHz Crystal Clock Reference.
XTAL_XI_32	I	59	Shared with GPIOA_1. Input of 32KHz Crystal Clock Reference.
XTAL_XO_32	O	117	Shared with GPIOA_0. Output of 32KHz Crystal Clock Reference.

5.6. Chip Enable Pin

Table 9. Chip Enable Pin

Symbol	Type	Pin No.	Description
CHIP_EN	I	62	Whole chip enable control. When asserted, chip function is enabled; when de-asserted, whole chip is shutdown.

5.7. NOR/NAND Flash Interface

Table 10. Chip Enable Pin

Symbol	Type	Pin No.	Description
SPI_CLK	IO	75	NOR/NAND Flash CLK signal. Multiplexed with GPIOC_0.
SPI_DATA0	IO	76	NOR/NAND Flash DAT0 signal. Multiplexed with GPIOC_2.
SPI_CS	IO	78	NOR/NAND Flash CS signal. Multiplexed with GPIOC_5.
SPI_DAT1	IO	7	NOR/NAND Flash DAT1 signal. Multiplexed with GPIOC_4.
SPI_DAT2	IO	77	NOR/NAND Flash DAT2 signal. Multiplexed with GPIOC_3.
SPI_DAT3	IO	5	NOR/NAND Flash DAT3 signal. Multiplexed with GPIOC_1.

5.8. USB Transceiver Interface

Table 11. USB Transceiver Interface

Symbol	Type	Pin No.	Description
HSDP	IO	70	Shared with GPIOB_0. High-Speed USB D+ signal.
HSDM	IO	71	Shared with GPIOB_1. High-Speed USB D- signal.
RREF	P	69	Precision Resistor 12K ohm for Bandgap for USB interface.

5.9. Audio Interface

Table 12. Audio Interface

Symbol	Type	Pin No.	Description
AUDIO_AGND1	G	121	Ground signal for Audio block.
AUDIO_AOUT_LP	O	63	Speaker output positive signal.
AUDIO_AVDD33_1	PI	122	The input power source 3.3V for Audio block.
AUDIO_AVDD33_0	PO	64	The output power source 2.8V for Audio block.
AUDIO_VREF	PO	123	Capacitor for Codec bandgap reference.
AUDIO_MICBIAS	PO	65	Microphone bias output.
AUDIO_MIC1_P	I	124	MIC input positive signal.

5.10. MIPI Interface

Table 13. MIPI Interface

Symbol	Type	Pin No.	Description
MIPI_CKI_P	I	85	MIPI sensor differential clock positive input.
MIPI_CKI_N	I	15	MIPI sensor differential clock negative input.
MIPI_DATA0_P	I	83	MIPI sensor lane0 differential data positive input.
MIPI_DATA0_N	I	13	MIPI sensor lane0 differential data negative input.
MIPI_DATA1_P	I	84	MIPI sensor lane1 differential data positive input.
MIPI_DATA1_N	I	14	MIPI sensor lane1 differential data negative input.
MIPI_DATA2_P	I	86	MIPI sensor lane2 differential data positive input.
MIPI_DATA2_N	I	16	MIPI sensor lane2 differential data negative input.
MIPI_DATA3_P	I	17	MIPI sensor lane3 differential data positive input.
MIPI_DATA3_N	I	18	MIPI sensor lane3 differential data negative input.

5.11. SD Card Interface

Table 14. SD Card Interface

Symbol	Type	Pin No.	Description
SD_D0	IO	80	SD Data 0. Multiplexed with GPIOS_2.
SD_D1	IO	9	SD Data 1. Multiplexed with GPIOS_1.
SD_D2	IO	12	SD Data 2. Multiplexed with GPIOS_6.
SD_D3	IO	82	SD Data 3. Multiplexed with GPIOS_5.
SD_CMD	IO	81	SD Command. Multiplexed with GPIOS_3.
SD_CLK	O	79	SD Bus clock. Multiplexed with GPIOS_0.
SD_CD	I	11	SD Card Detection. Multiplexed with GPIOS_4.

5.12. Digital IO Pins

AmebaPro-II supports a maximum of 59 GPIO pins and all of them are configurable. Refer to Table 15 for detailed information and pin mux rules.

Table 15. GPIO Pins

Symbol	Type	Pin No.	Description
GPIOA_0	IO	117	GPIO pin. The MUX function can be referred to in section 5.12.1 GPIO Pin Functions, page 18.
GPIOA_1	IO	59	
GPIOA_2	IO	118	
GPIOA_3	IO	60	
GPIOA_4	IO	119	
GPIOA_5	IO	120	
GPIOB_0	IO	70	
GPIOB_1	IO	71	
GPIOD_0	IO	83	
GPIOD_1	IO	13	
GPIOD_2	IO	84	
GPIOD_3	IO	14	
GPIOD_4	IO	85	
GPIOD_5	IO	15	
GPIOD_6	IO	86	
GPIOD_7	IO	16	
GPIOD_8	IO	17	
GPIOD_9	IO	18	
GPIOD_10	IO	20	
GPIOD_11	IO	19	
GPIOD_12	IO	21	
GPIOD_13	IO	88	
GPIOD_14	IO	89	
GPIOD_15	IO	23	
GPIOD_16	IO	90	

Symbol	Type	Pin No.	Description
GPIOD_17	IO	24	
GPIOD_18	IO	91	
GPIOE_0	IO	92	
GPIOE_1	IO	93	
GPIOE_2	IO	94	
GPIOE_3	IO	28	
GPIOE_4	IO	95	
GPIOE_5	IO	29	
GPIOE_6	IO	96	
GPIOF_0	IO	43	
GPIOF_1	IO	106	
GPIOF_2	IO	44	
GPIOF_3	IO	107	
GPIOF_4	IO	108	
GPIOF_5	IO	46	
GPIOF_6	IO	109	
GPIOF_7	IO	47	
GPIOF_8	IO	110	
GPIOF_9	IO	111	
GPIOF_10	IO	49	
GPIOF_11	IO	112	
GPIOF_12	IO	50	
GPIOF_13	IO	113	
GPIOF_14	IO	114	
GPIOF_15	IO	52	
GPIOF_16	IO	53	
GPIOF_17	IO	54	
GPIOS_0	IO	79	
GPIOS_1	IO	9	
GPIOS_2	IO	80	
GPIOS_3	IO	81	
GPIOS_4	IO	11	
GPIOS_5	IO	82	
GPIOS_6	IO	12	

Note: Default states of all pins are High-impedance; Unused pins should be kept floating.

5.12.1. GPIO Pin Functions

Table 16. GPIO Pin Function Table-1

Pin Name	Comparator/ADC	Flash	ISP-I2C	ISP Control	MIPI	I2C
GPIOA_0	Comparator/ADC4	-	-	-	-	I2C0_SCL
GPIOA_1	Comparator/ADC5	-	-	-	-	I2C0_SDA
GPIOA_2	Comparator/ADC6	-	-	-	-	-
GPIOA_3	Comparator/ADC7	-	-	-	-	-
GPIOA_4	-	-	-	-	-	-
GPIOA_5	-	-	-	-	-	-
GPIOB_0	-	-	-	-	-	I2C0_SCL
GPIOB_1	-	-	-	-	-	I2C0_SDA
GPIOC_0	-	SPI_CLK	-	-	-	-
GPIOC_1	-	SPI_DAT3	-	-	-	-
GPIOC_2	-	SPI_DAT0	-	-	-	-
GPIOC_3	-	SPI_DAT2	-	-	-	-
GPIOC_4	-	SPI_DAT1	-	-	-	-
GPIOC_5	-	SPI_CS	-	-	-	-
GPIOD_0	-	-	-	-	MIPI_DATA0_P	-
GPIOD_1	-	-	-	-	MIPI_DATA0_N	-
GPIOD_2	-	-	-	-	MIPI_DATA1_P	-
GPIOD_3	-	-	-	-	MIPI_DATA1_N	-
GPIOD_4	-	-	-	-	MIPI_CKI_P	-
GPIOD_5	-	-	-	-	MIPI_CKI_N	-
GPIOD_6	-	-	-	-	MIPI_DATA2_P	-
GPIOD_7	-	-	-	-	MIPI_DATA2_N	-
GPIOD_8	-	-	-	-	MIPI_DATA3_P	-
GPIOD_9	-	-	-	-	MIPI_DATA3_N	-
GPIOD_10	-	-	I2C3_SDA	-	-	-
GPIOD_11	-	-	-	SSOR_PDN	-	-
GPIOD_12	-	-	I2C3_SCL	-	-	-
GPIOD_13	-	-	-	SSOR_SYSCLK	-	-
GPIOD_14	-	-	-	-	-	-
GPIOD_15	-	-	-	-	-	-
GPIOD_16	-	-	-	-	-	-
GPIOD_17	-	-	-	-	-	-
GPIOD_18	-	-	-	-	-	-
GPIOE_0	-	-	-	SSOR_RST	-	-
GPIOE_1	-	-	-	-	-	-
GPIOE_2	-	-	-	-	-	-
GPIOE_3	-	-	-	-	-	I2C2_SCL
GPIOE_4	-	-	-	-	-	I2C2_SDA
GPIOE_5	-	-	-	-	-	I2C2_SCL
GPIOE_6	-	-	-	-	-	I2C2_SDA

Pin Name	Comparator/ADC	Flash	ISP-I2C	ISP Control	MIPI	I2C
GPIOF_0	ADC0	-	-	-	-	-
GPIOF_1	ADC1	-	-	-	-	I2C1_SCL
GPIOF_2	ADC2	-	-	-	-	I2C1_SDA
GPIOF_3	ADC3	-	-	-	-	-
GPIOF_4	-	-	-	-	-	-
GPIOF_5	-	-	-	-	-	-
GPIOF_6	-	-	-	-	-	-
GPIOF_7	-	-	-	-	-	-
GPIOF_8	-	-	-	-	-	-
GPIOF_9	-	-	-	-	-	-
GPIOF_10	-	-	-	-	-	-
GPIOF_11	-	-	-	-	-	-
GPIOF_12	-	-	-	-	-	-
GPIOF_13	-	-	-	-	-	-
GPIOF_14	-	-	-	-	-	-
GPIOF_15	-	-	-	-	-	-
GPIOF_16	-	-	-	-	-	-
GPIOF_17	-	-	-	-	-	-
GPIOS_0	-	-	-	-	-	-
GPIOS_1	-	-	-	-	-	-
GPIOS_2	-	-	-	-	-	-
GPIOS_3	-	-	-	-	-	-
GPIOS_4	-	-	-	-	-	-
GPIOS_5	-	-	-	-	-	-
GPIOS_6	-	-	-	-	-	-

Table 17. GPIO Pin Function Table-2

Pin Name	DMIC	SGPIO	PWM	LED	SD Card	RFE_CTRL
GPIOA_0	-	-	-	-	-	-
GPIOA_1	-	-	-	-	-	-
GPIOA_2	-	-	-	-	-	-
GPIOA_3	-	-	-	-	-	-
GPIOA_4	-	-	-	-	-	-
GPIOA_5	-	-	-	-	-	-
GPIOB_0	-	-	-	-	-	-
GPIOB_1	-	-	-	-	-	-
GPIOC_0	-	-	-	-	-	-
GPIOC_1	-	-	-	-	-	-
GPIOC_2	-	-	-	-	-	-
GPIOC_3	-	-	-	-	-	-
GPIOC_4	-	-	-	-	-	-
GPIOC_5	-	-	-	-	-	-
GPIOD_0	-	-	-	-	-	-
GPIOD_1	-	-	-	-	-	-
GPIOD_2	-	-	-	-	-	-
GPIOD_3	-	-	-	-	-	-
GPIOD_4	-	-	-	-	-	-
GPIOD_5	-	-	-	-	-	-
GPIOD_6	-	-	-	-	-	-
GPIOD_7	-	-	-	-	-	-
GPIOD_8	-	-	-	-	-	-
GPIOD_9	-	-	-	-	-	-
GPIOD_10	-	-	-	-	-	-
GPIOD_11	-	-	-	-	-	-
GPIOD_12	-	-	-	-	-	-
GPIOD_13	-	-	-	-	-	-
GPIOD_14	DMIC_CLK	-	-	WIFI_LED	-	-
GPIOD_15	-	-	-	-	-	-
GPIOD_16	DMIC_CLK	-	-	-	-	-
GPIOD_17	-	-	-	-	-	RFE_CTRL_4
GPIOD_18	DMIC_DATA	-	-	-	-	RFE_CTRL_5
GPIOE_0	-	-	-	WIFI_LED	-	RFE_CTRL_3
GPIOE_1	-	-	-	-	-	-
GPIOE_2	-	-	-	-	-	-
GPIOE_3	-	-	-	-	-	RFE_CTRL_4
GPIOE_4	-	-	-	-	-	RFE_CTRL_5
GPIOE_5	-	-	-	-	-	-
GPIOE_6	-	-	-	-	-	-
GPIOF_0	-	-	-	-	-	-
GPIOF_1	-	-	-	-	-	RFE_CTRL_0

Pin Name	DMIC	SGPIO	PWM	LED	SD Card	RFE_CTRL
GPIOF_2	-	-	-	-	-	RFE_CTRL_1
GPIOF_3	-	-	-	-	-	RFE_CTRL_2
GPIOF_4	-	-	-	-	-	-
GPIOF_5	-	-	-	-	-	-
GPIOF_6	-	-	PWM0	-	-	-
GPIOF_7	-	-	PWM1	-	-	-
GPIOF_8	-	-	PWM2	-	-	-
GPIOF_9	-	SGPIO_RX	PWM3	-	-	-
GPIOF_10	-	-	PWM4	-	-	-
GPIOF_11	-	-	PWM5	-	-	-
GPIOF_12	-	-	PWM6	-	-	-
GPIOF_13	-	-	PWM7	-	-	-
GPIOF_14	-	SGPIO_RX	PWM8	-	-	-
GPIOF_15	-	SGPIO_TX	PWM9	-	-	-
GPIOF_16	-	-	PWM10	-	-	-
GPIOF_17	-	-	PWM11	-	-	-
GPIOS_0	-	-	-	-	SD_CLK	-
GPIOS_1	-	-	PWM8	-	SD_D1	-
GPIOS_2	-	-	-	-	SD_D0	-
GPIOS_3	-	-	-	-	SD_CMD	-
GPIOS_4	-	-	PWM9	-	SD_CD	-
GPIOS_5	-	-	PWM10	-	SD_D3	-
GPIOS_6	-	-	PWM11	-	SD_D2	-

Table 18. GPIO Pin Function Table-3

Pin Name	I2S	SPI Master	SPI Slave	UART	BT Coexist
GPIOA_0	-	-	-	-	-
GPIOA_1	-	-	-	-	-
GPIOA_2	-	-	-	UART0_OUT	-
GPIOA_3	-	-	-	UART0_IN	-
GPIOA_4	-	-	-	-	-
GPIOA_5	-	-	-	-	-
GPIOB_0	-	-	-	-	-
GPIOB_1	-	-	-	-	-
GPIOC_0	-	-	-	-	-
GPIOC_1	-	-	-	-	-
GPIOC_2	-	-	-	-	-
GPIOC_3	-	-	-	-	-
GPIOC_4	-	-	-	-	-
GPIOC_5	-	-	-	-	-
GPIOD_0	-	-	-	-	-
GPIOD_1	-	-	-	-	-
GPIOD_2	-	-	-	-	-

Pin Name	I2S	SPI Master	SPI Slave	UART	BT Coexist
GPIOD_3	-	-	-	-	-
GPIOD_4	-	-	-	-	-
GPIOD_5	-	-	-	-	-
GPIOD_6	-	-	-	-	-
GPIOD_7	-	-	-	-	-
GPIOD_8	-	-	-	-	-
GPIOD_9	-	-	-	-	-
GPIOD_10	-	-	-	-	-
GPIOD_11	-	-	-	-	-
GPIOD_12	-	-	-	-	-
GPIOD_13	-	-	-	-	-
GPIOD_14	I2S1_CLK	-	-	-	BT_PRI
GPIOD_15	I2S1_SD_TX0	-	-	UART2_OUT	BT_STA
GPIOD_16	I2S1_MCK	-	-	UART2_IN	BT_CK
GPIOD_17	I2S1_WS	-	-	UART2_CTS	WL_ACT
GPIOD_18	I2S1_SD_RX	-	-	UART2_RTS	BTCMD_IRQ
GPIOE_0	-	-	-	UART2_OUT	-
GPIOE_1	-	SPI_0_SCL	SPI_2_SCL	UART3_OUT	-
GPIOE_2	-	SPI_0_MISO	SPI_2_MISO	UART3_IN	-
GPIOE_3	-	SPI_0_MOSI	SPI_2_MOSI	UART3_RTS	-
GPIOE_4	-	SPI_0_CS0	SPI_2_CS	UART3_CTS	-
GPIOE_5	-	SPI_0_CS1	-	-	-
GPIOE_6	-	SPI_0_CS2	-	-	-
GPIOF_0	-	-	-	-	-
GPIOF_1	-	-	-	UART1_CTS	-
GPIOF_2	-	-	-	UART1_RTS	-
GPIOF_3	-	-	-	UART1_IN	-
GPIOF_4	-	-	-	UART1_OUT	-
GPIOF_5	-	SPI_1_MISO	SPI_3_MISO	-	-
GPIOF_6	-	SPI_1_SCL	SPI_3_SCL	-	-
GPIOF_7	-	SPI_1_MOSI	SPI_3_MOSI	-	-
GPIOF_8	-	SPI_1_CS0	SPI_3_CS	-	-
GPIOF_9	-	SPI_1_CS1	-	-	-
GPIOF_10	-	SPI_1_CS2	-	-	-
GPIOF_11	I2S0_MCK	-	-	-	-
GPIOF_12	I2S0_SD_RX	-	-	UART1_IN	-
GPIOF_13	I2S0_CLK	-	-	UART1_OUT	-
GPIOF_14	I2S0_SD_TX0	-	-	-	-
GPIOF_15	I2S0_WS	-	-	-	-
GPIOF_16	-	SPI_1_CS3	-	-	-
GPIOF_17	-	-	-	-	-
GPIOS_0	-	-	-	-	-
GPIOS_1	-	-	-	-	-

Pin Name	I2S	SPI Master	SPI Slave	UART	BT Coexist
GPIOS_2	-	-	-	-	-
GPIOS_3	-	-	-	-	-
GPIOS_4	-	-	-	-	-
GPIOS_5	-	-	-	-	-
GPIOS_6	-	-	-	-	-

6. RF Characteristics

AmebaPro-II includes integrated WLAN RF transceiver architecture and operates in 2.4GHz/5GHz WLAN and Bluetooth systems.

6.1. RF Block Diagram

This section describes the AmebaPro-II RF block diagram. AmebaPro-II includes a Wi-Fi/BT subsystem that integrates a Wi-Fi/BT modem sharing a front-end RF (ADC, TRSW, LPF, PA, LNA, etc.), and this chip is compatible with IEEE 802.11a/b/g/n protocol.

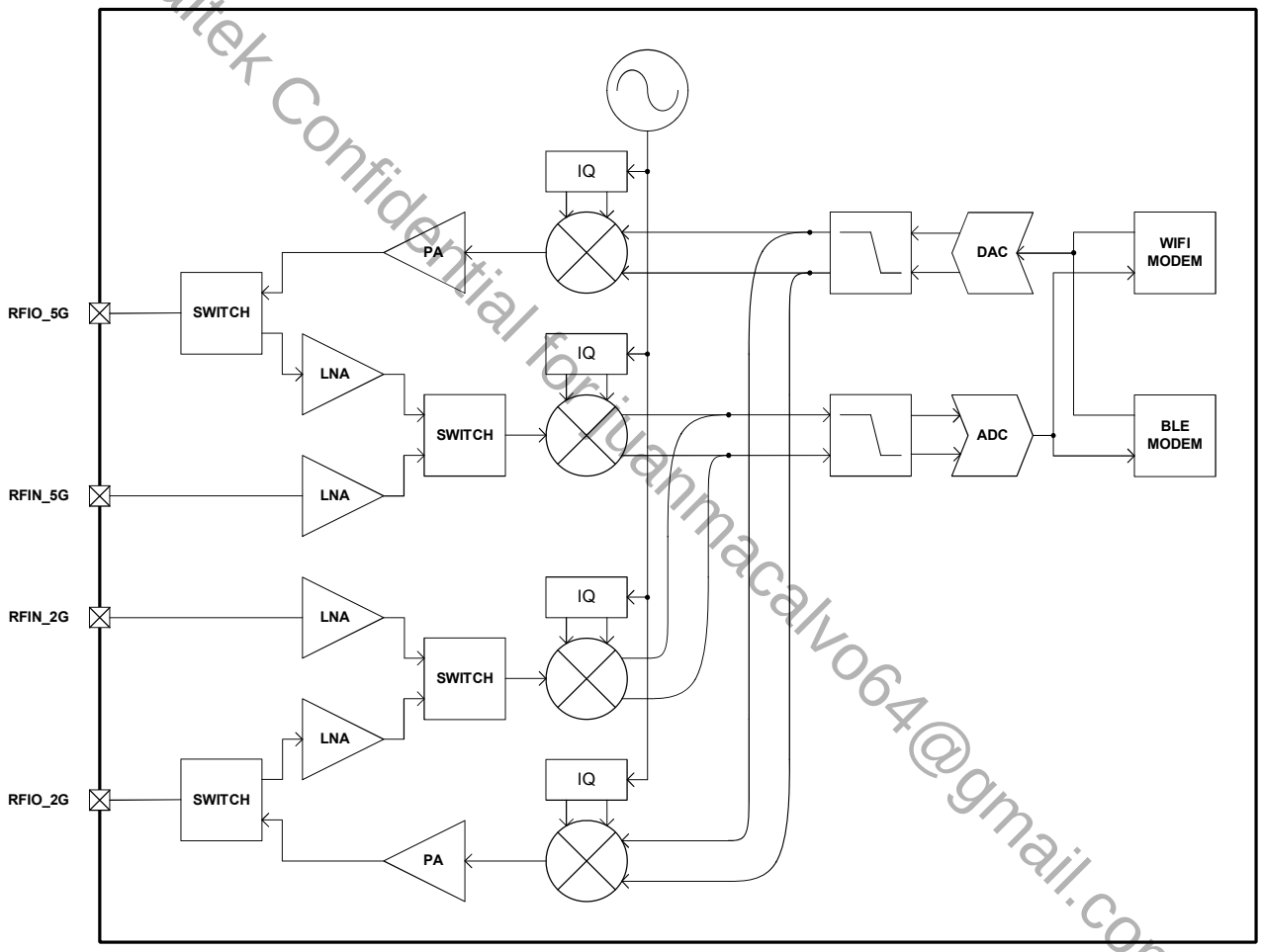


Figure 9. RF Block Diagram

6.2. Wi-Fi Radio Characteristics

Please refer to WLAN RF DVT report.

6.3. Bluetooth Radio Characteristic

Values in Table 19 and Table 20 are typical values, and the reference point is the antenna port including front-end loss. These values may change slightly depending on different RF front-end designs or PCB designs. Both the transmitter specifications and the receiver specifications follow Bluetooth SIG specifications.

6.3.1. BT RF Transmitter Specifications

Table 19. Bluetooth Transmitter Performance Table-BLE

Parameter	Description	Min	Typ.	Max	Units
Frequency Range	-	2402	-	2480	MHz
Tx Output Power	-	6	8	10	dBm
Adjacent Channel Transmit Power	F = F0 ± 1MHz	-	-50	-	dB
	F = F0 ± 2MHz	-	-50	-	dB
	F = F0 ± 3MHz	-	-50	-	dB
	F = F0 ± > 3MHz	-	-50	-	dB
Δ f1avg	-	-	250	-	kHz
Δ f2max	-	-	220	-	kHz
Δ f2avg/Δ f1avg	-	-	0.9	-	-
ICFT	-	-	0	-	KHz
Drift Rate	-	-	10	-	kHz/50μs
Initial Drift Rate	-	-	0	-	kHz

Note: The above Tx performance values are based on 25 degree, 3.3V, 50ohm @LAB environment & Realtek EVB.

6.3.2. BT RF Receiver Specifications

Table 20. Bluetooth Receiver Performance Table-BLE

Parameter	Description	Min	Typ.	Max	Units
Frequency Range	-	2402	-	2480	MHz
Rx Sensitivity @30.8% PER	Without spur channel	-	-90	-	dBm
Maximum Received Signal @30.8% PER	-	-10	-	-	dBm
Co-Channel C/I Adjacent Channel Selectivity C/I	-	-	5	-	dB
	F = F0 + 1MHz	-	-7	-	dB
	F = F0 - 1MHz	-	-7	-	dB
	F = F0 + 2MHz	-	-40	-	dB
	F = F0 - 2MHz	-	-25	-	dB
	F = F0 + 3MHz	-	-50	-	dB
	F = F0 - 3MHz	-	-25	-	dB
Out-of-Band Blocking Performance	30MHz ~ 2000MHz	-30	-	-	dBm
	2000MHz ~ 2400MHz	-35	-	-	dBm
	2500MHz ~ 3000MHz	-35	-	-	dBm

Parameter	Description	Min	Typ.	Max	Units
	3000MHz ~ 12.5 GHz	-30	-	-	dBm
Intermodulation			-36		dBm

Note: The above Rx performance values are based on 25 degree, 3.3V, 50ohm @LAB environment & Realtek EVB.

7. Electrical Characteristics

7.1. Temperature Limit Ratings

Table 21. Temperature Limit Ratings

Parameter	Min	Max	Units
Storage Temperature	-55	+150	°C
Ambient Operating Temperature	-20	+85	°C
Junction Temperature	-40	+125	°C

7.2. Temperature Characteristics

Table 22. Thermal Properties

PCB (layer)	$T_{ambient}$(°C)	θ_{JA}(°C/W)	Ψ_{JT} (°C/W)	Ψ_{JB}(°C/W)	θ_{JC}(°C/W)	θ_{JB}(°C/W)
4 (JEDEC 2s2P)	70	23.38	0.68	9.59	10.13	9.63

7.3. Power Supply DC Characteristics

Table 23. Power Supply DC Characteristics

Parameter	Symbol	Min	Typ.	Max	Units
DC Supply Voltage for 3.3V Power Rail	-	3.135	3.3	3.465	V
DC Supply Voltage for 0.9V Power Rail	-	0.855	0.9	0.945	V
DC Supply Voltage for GPIO/Embedded Flash	-	3.135	3.3	3.465	V
DC Supply Voltage for DDR2	-	1.71	1.8	1.89	V
DC Supply Voltage for DDR3L	-	1.2825	1.35	1.4175	V

7.4. Digital IO Pin DC Characteristics

Table 24. Typical Digital IO DC Parameters

Symbol	Parameter	Conditions	Min	Typ.	Max	Units
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V
V_{OH}	Output-High Voltage	LVTTL	2.4	-	-	V
V_{OL}	Output-Low Voltage	LVTTL	-	-	0.4	V
V_{T+}	Schmitt-trigger High Level	-	-	-	2.1	V
V_{T-}	Schmitt-trigger Low Level	-	0.7	-	-	V
I_{IL}	Input-Leakage Current	VIN=3.3V or 0	-10	±1	10	µA
-	Driving for Normal Pins	-	4	-	16	mA

Symbol	Parameter	Conditions	Min	Typ.	Max	Units
-	Loading for Normal Pins	-	-	15	-	pF
-	Pull Resistance for Normal Pins	3.3V	-	75	-	KΩ

Note: The pull resistance values are typical values checked in the manufacturing process and are not tested.

7.5. Power State and Power Sequence

7.5.1. Power On or Resuming from Deep Sleep Sequence

The timing sequence of Power On or Resuming from Deep Sleep is given in Figure 10.

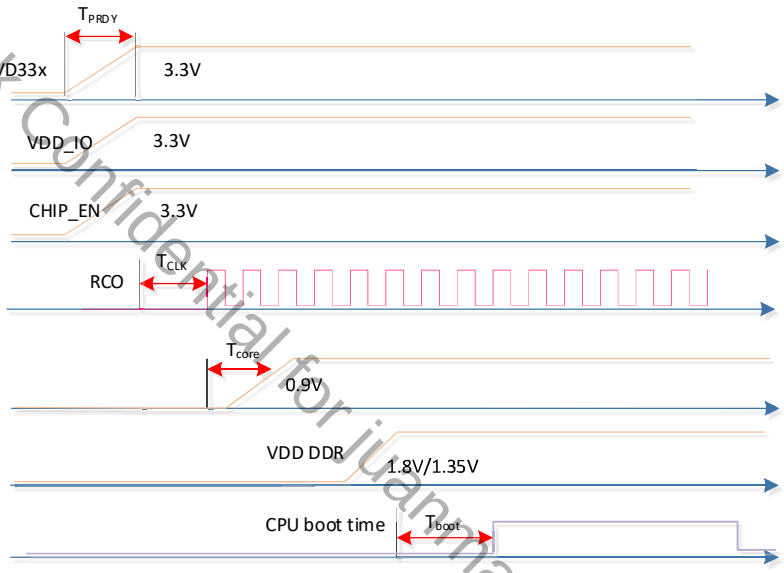


Figure 10. Power On Sequence or Resume from Deep Sleep

Table 25. Timing Specification for Power On Sequence

Symbol	Parameter	Min	Typ.	Max	Units
T_{PRDY}	VD33x Ready Time	0.6	-	5	ms
T_{CLK}	Internal ring clock stable time after VD33 ready	1	-	-	ms
T_{core}	Core Power Ready Time	-	1.5	-	ms
T_{boot}	CPU Boot Time	200	-	-	ms

7.5.2. Resume from Standby Mode Sequence

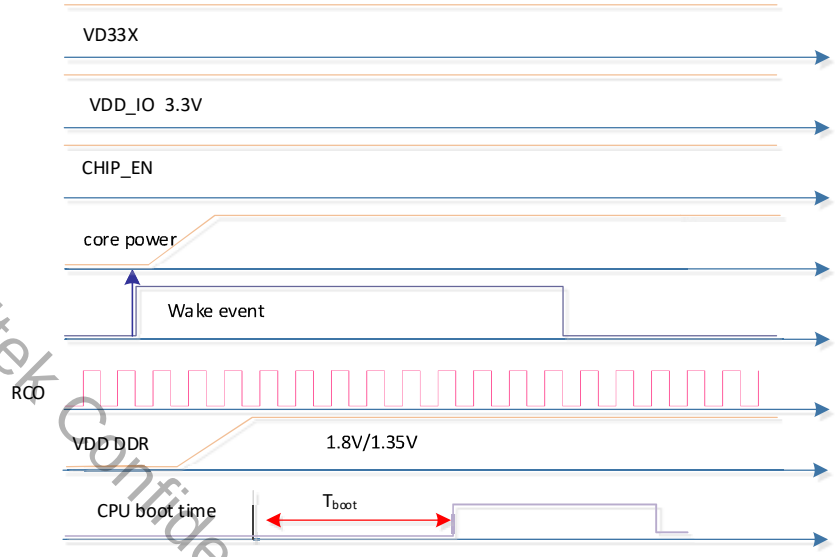


Figure 11. Timing Sequence Resume from Standby

Table 26. Timing Specification for Resume from Standby Mode Sequence

Symbol	Parameter	Min	Typ.	Max	Units
T_{boot}	CPU Boot Time	200	-	-	ms

7.5.3. Reset Sequence

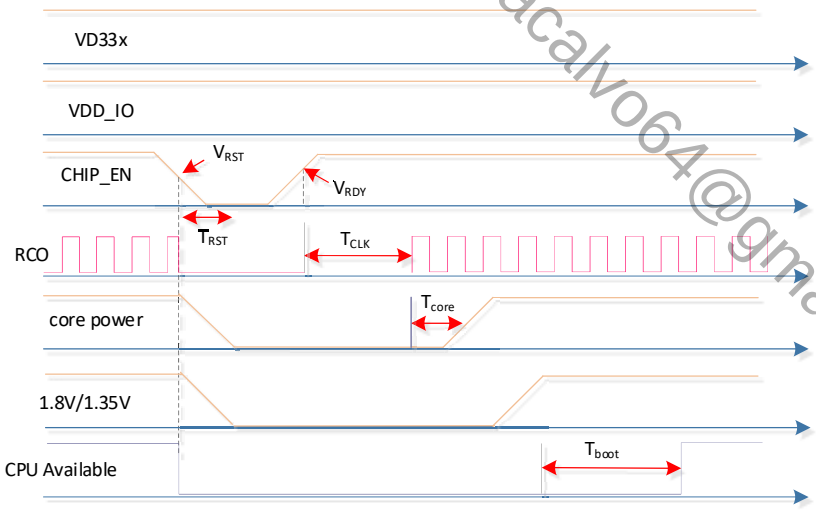


Figure 12. Timing Sequence of Reset

Table 27. Timing Specification for Reset Sequence

Symbol	Parameter	Min	Typ.	Max	Units
V_{RST}	Shutdown occurs after CHIP_EN lower than this voltage	-	0.8	-	V
T_{RST}	The require time that CHIP_EN lower than V_{RST}	1	-	-	ms
V_{RDY}	Enable PMC after CHIP_EN higher than this voltage	2	-	-	V
T_{CLK}	Internal ring clock stable time after 3.3V ready	1	-	-	ms
T_{core}	Core Power Ready Time	-	1.5	-	ms
T_{boot}	CPU Boot Time	200	-	-	ms

7.5.4. Power Off Sequence

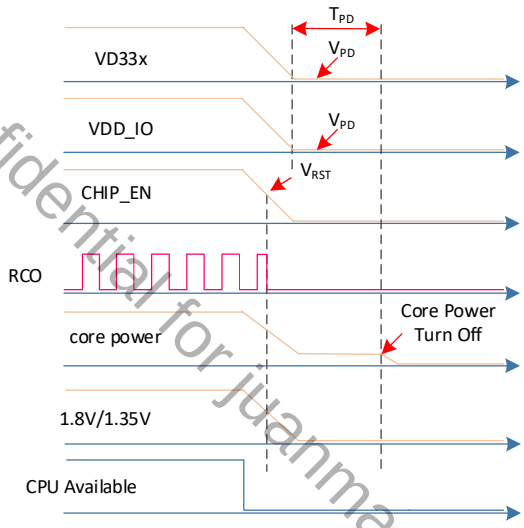


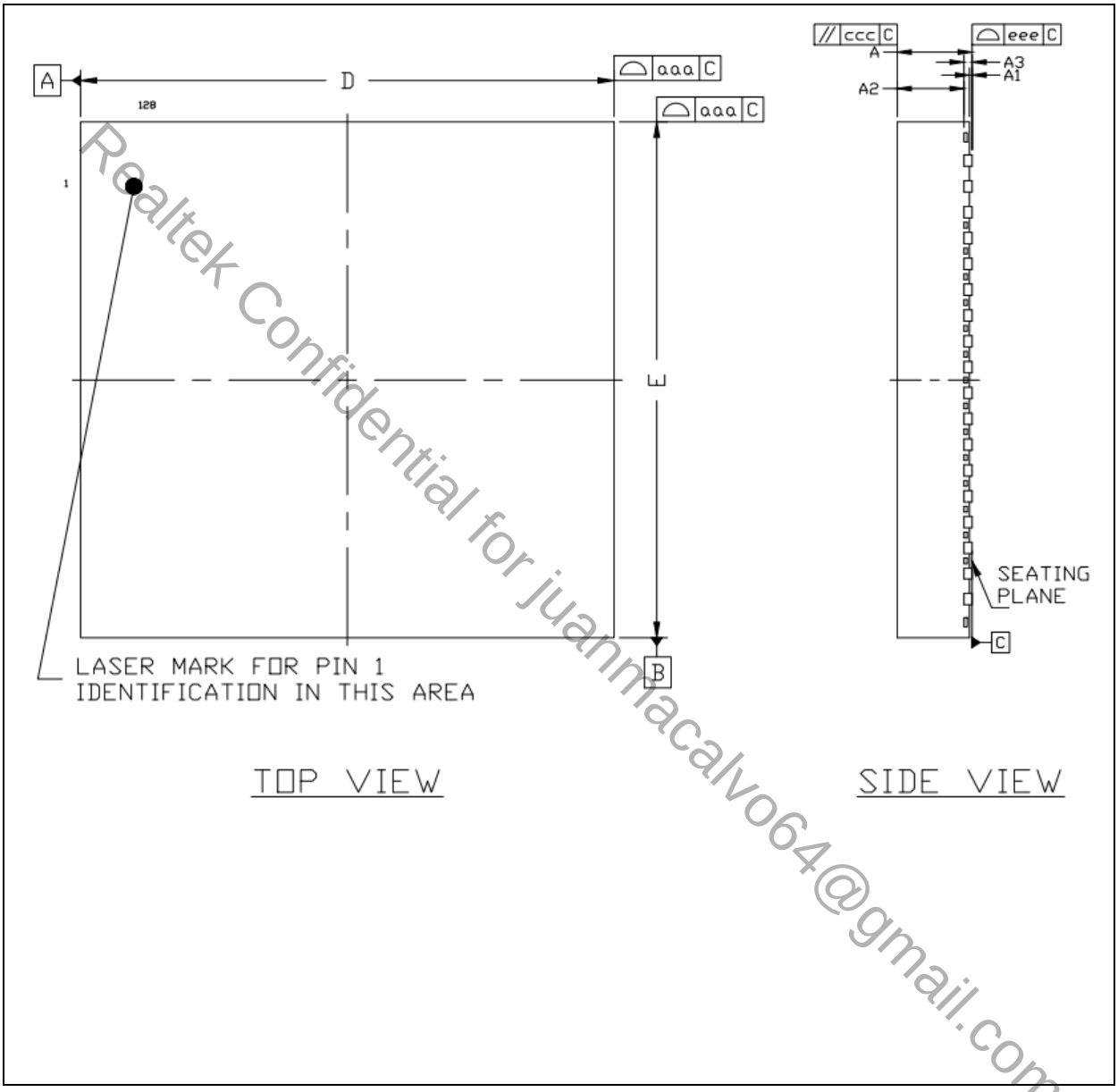
Figure 13. Timing Sequence of Power Off

Table 28. Timing Specification for Power Off Sequence

Symbol	Parameter	Min	Typ.	Max	Units
V_{RST}	Shutdown occurs after CHIP_EN is lower than this voltage	-	0.8	-	V
V_{PD}	The required voltage of CHIP_EN/VDD33x/ VDD_IO for power down state	0	0	0.08	V
T_{PD}	The required time that CHIP_EN/VDD33x/ VDD_IO is lower than V_{PD}	1	-	-	ms

8. Mechanical Dimensions

8.1. Package Specification



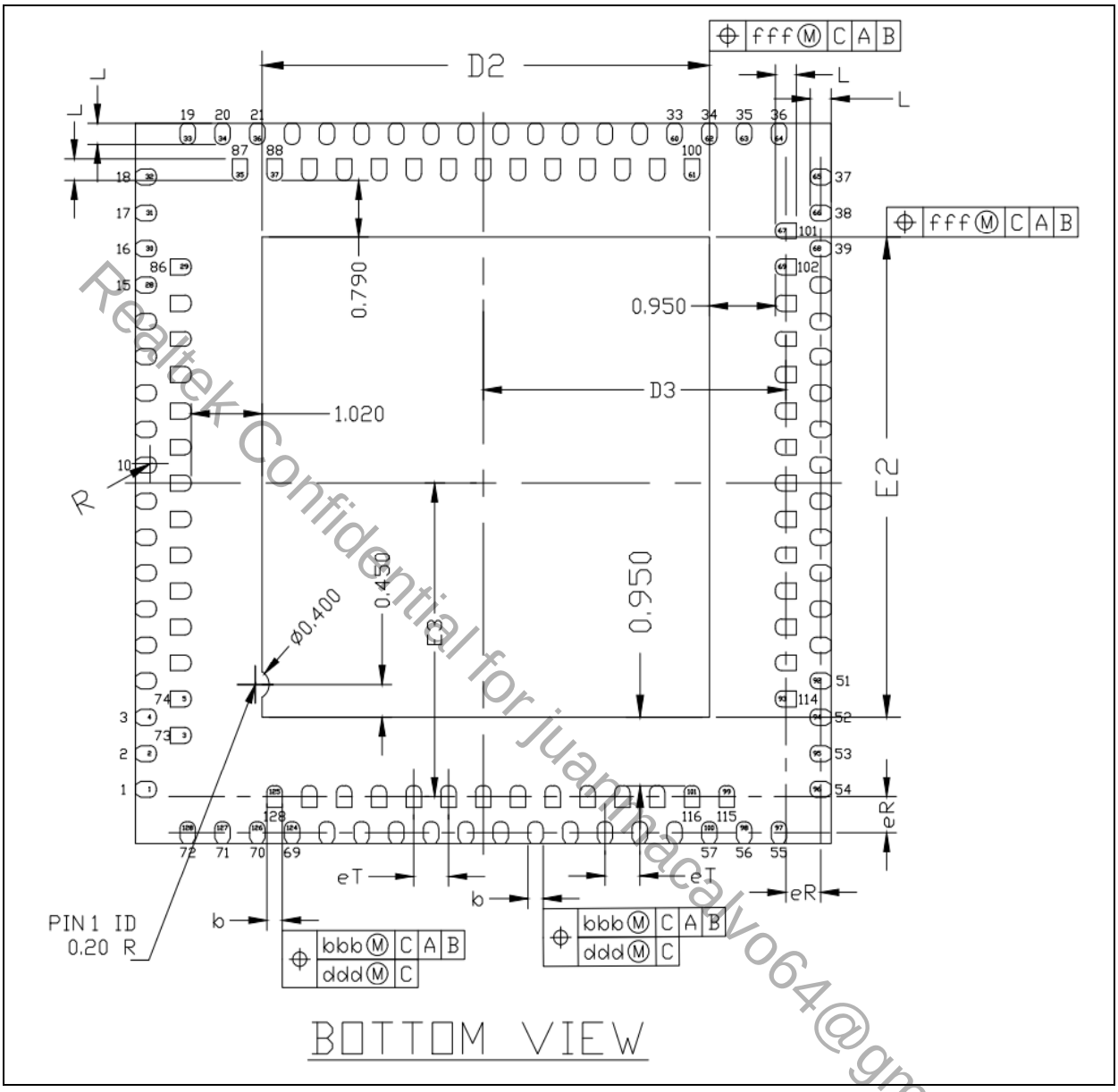


Figure 14. Package Information

Note: For detailed pin assignments, please refer to section 4 Pin Assignments.

8.2. Mechanical Dimensions Notes

Table 29. Mechanical Dimensions Notes

Symbol	Dimension in mm		
	Min	Nom.	Max
A	-	-	1.500
A_1	0.000	-	0.050
A_2	-	1.250	1.300
A_3	0.152 REF.		
b	0.180	0.220	0.300
D	10 BSC		
D_2	6.330	6.430	6.530
D_3	4.250	4.350	4.450
E	10 BSC		
E_2	6.560	6.660	6.760
E_3	4.250	4.350	4.450
L	0.200	0.300	0.400
eT	0.500 BSC		
eR	0.500 BSC		
R	0.090	-	-
TOLERANCES OF FORM AND POSITION			
aaa	0.150		
bbb	0.100		
ccc	0.100		
ddd	0.050		
eee	0.080		
fff	0.100		

Notes:

1. *CONTROLLING DIMENSION: MILLIMETER (mm).*
2. *REFERENCE DOCUMENT: JEDEC MO-220.*

9. Ordering Information

Table 30. Ordering Information

Part Number	Package
RTL8735BDM-VA3-CG	QFN128
RTL8735BM-VA3-CG	QFN128
RTL8735BDM-VL3-CG	QFN128
RTL8735BM-VL3-CG	QFN128
RTL8735BDM-VA4-CG	QFN128
RTL8735BM-VA4-CG	QFN128
RTL8735BDM-VL4-CG	QFN128
RTL8735BM-VL4-CG	QFN128

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