

# Tracking Progress

## Week-by-week Schedule

Week	Dates	Phase	Task
1	1/8 - 1/14	Design	<input checked="" type="checkbox"/> Filter
2	1/15 - 1/21	Design	<input checked="" type="checkbox"/> Comparator
3	1/22 - 1/28	Design	<input checked="" type="checkbox"/> Comparator <input checked="" type="checkbox"/> 3-feature AFC at LF (functionality)
4	1/29 - 2/4	Design	<input checked="" type="checkbox"/> Filter
5	2/5 - 2/11	Design	<input checked="" type="checkbox"/> Filter <input checked="" type="checkbox"/> Bias current divider
6	2/12 - 2/18	Design	<input checked="" type="checkbox"/> Filter <input checked="" type="checkbox"/> Comparator
7	2/19 - 2/25	Design	<input checked="" type="checkbox"/> Comparator
8	2/26 - 3/4	Design	<input checked="" type="checkbox"/> Filter <input checked="" type="checkbox"/> Comparator <input checked="" type="checkbox"/> Calibration circuitry
9	3/5 - 3/11	Design	<input checked="" type="checkbox"/> Time-domain envelope detector
10	3/12 - 3/18	Design	<input checked="" type="checkbox"/> Integrate-and-fire
11	3/19 - 3/25	Design	<input checked="" type="checkbox"/> All analog blocks
12	3/26 - 4/1	Design	<input checked="" type="checkbox"/> 1-feature AFC
13	4/2 - 4/8	Design	<input checked="" type="checkbox"/> Calibration
14	4/9 - 4/15	Design	<input checked="" type="checkbox"/> cmp_grid
15	4/16 - 4/22	Design	<input type="checkbox"/> chip_minus_pads_minus_digital <input type="checkbox"/> 3-feature AFC
16	4/23 - 4/29	Design Layout	<input type="checkbox"/> Pad frame, serializer, scan chain <input type="checkbox"/> Blocks
17	4/30 - 5/6	Design Layout	<input type="checkbox"/> Pad frame, serializer, scan chain <input type="checkbox"/> Blocks
18	5/7 - 5/13	Design Layout	<input type="checkbox"/> Pad frame, serializer, scan chain <input type="checkbox"/> System
19	5/14 - 5/20	Design Layout	<input type="checkbox"/> Pad frame, serializer, scan chain <input type="checkbox"/> System
20	5/21 - 5/27 trial: 26th	Verification	<input type="checkbox"/> Full-chip simulation <input type="checkbox"/> Work through tapeout checklist
21	5/28 - 6/3 final: 2nd	Verification	<input type="checkbox"/> Full-chip simulation <input type="checkbox"/> Work through tapeout checklist
22	6/4 - 6/10 tapeout: 9th	Margin	<input type="checkbox"/> Margin

## Progress Summary

Hierarchy level	Cell	Schematic-level design+sims	Layout	Post-layout sims
1	Filter	100%	0%	0%
1	Current divider	100%	0%	0%
1	Comparator	95%	0%	0%
1	Trianglewave generator	85%	0%	0%
1	Integrate-and-fire	90%	0%	0%
1	Counter	0%	0%	0%
1	Serializer	0%	0%	0%
1	Scan chain	0%	0%	0%
2	Filter bank	100%	0%	0%
2	Comparator grid	100%	0%	0%
2	XOR array	0%	0%	0%
2	Integrate-and-fire array	0%	0%	0%
2	Counter array	0%	0%	0%
3+	chip_minus_pads_minus_digital	40%	0%	0%
3+	chip_minus_pads	0%	0%	0%
3+	chip	0%	0%	0%
flat	1-feature AFC	80%	n/a	0%
flat	3-feature AFC	10%	n/a	0%

S. Ray and P. R. Kinget, "Ultra-Low-Power and Compact-Area Analog Audio Feature Extraction Based on Time-Mode Analog Filterbank Interpolation and Time-Mode Analog Rectification," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 4, pp. 1025–1036, Apr. 2023, doi: [10.1109/JSSC.2022.3227246](https://doi.org/10.1109/JSSC.2022.3227246).

Review and update at least once a week