

LAYOUT ERRORS RESULTS: ERRORS

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# # # # #  
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Library name:

/evprj182/projects/TEAM_Chipathon2025/DRC/synopsys_custom/trackA.icv.drc/trackA.custom_compiler.gds

Structure name: trackA

Generated by: IC Validator RHEL64 X-2025.06.11869009 2025/05/28

Runset name:

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180mcu_drc.rs

User name: trng6tusr263

Time started: 2025/09/23 04:19:38PM

Time ended: 2025/09/23 04:20:45PM

Called as: icv -f gdsii -i

/evprj182/projects/TEAM_Chipathon2025/DRC/synopsys_custom/trackA.icv.drc/trackA.custom_compiler.gds -c trackA -l

/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/ -oa_dm6 -vue

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180mcu_drc.rs

ERROR SUMMARY

CO.10 Contact on Poly2 gate over COMP is forbidden
and 78 violations found.

CO.1: Min/max contact size : 0.22
not_length_edge 102 violations found.
Error limit exceeded. Details only available for first 100.
Check was stopped early because error limit was reached.

CO.3 Poly2 overlap of contact : 0.07
enclose 16 violations found.

CO.4 COMP overlap of contact : 0.07

enclose 4 violations found.

CO.7 Space from COMP contact to Poly2 on COMP : 0.15
external2 18 violations found.

CO.9 Contact on NCOMP to PCOMP butting edge is
forbidden
and_edge 4 violations found.

COHVNESD.7_COHVPESD.7 : Recommended/max. salicided
block edge to at least one or nearest contact (CA)
<= 0.22
not_interacting 6 violations found.

CUP.3_Metal2 : Min space of Metal2 line used for
bond pads = 1.0
external1 28 violations found.

CUP.3_Metal3 : Min space of Metal3 line used for
bond pads = 1.0
external1 28 violations found.

CUP.3_Metal4 : Min space of Metal4 line used for
bond pads = 1.0
external1 28 violations found.

CUP.5 : Top via (Via4) not allowed directly under
pad opening
and 101 violations found.
Error limit exceeded. Details only available for first 100.
Check was stopped early because error limit was reached.

CUP.7_Via2 : CUP.7c Vias shall be in the form of
cluster or arrays (<=3x3). Sea of via (> 3x3 array)
is not allowed.
CUP.7d Min Via2 space in via arrays = 0.3
CUP.7e Min space between via arrays = 0.36
not_rectangle_spacing1 280 violations found.
Error limit exceeded. Details only available for first 100.

CUP.7_Via3 : CUP.7c Vias shall be in the form of
cluster or arrays (<=3x3). Sea of via (> 3x3 array)
is not allowed.
CUP.7d Min Via3 space in via arrays = 0.3

CUP.7e Min space between via arrays = 0.36
not_rectangle_spacing1 168 violations found.
Error limit exceeded. Details only available for first 100.

CUP.7_Via4 : CUP.7c Vias shall be in the form of
cluster or arrays ($\leq 3 \times 3$). Sea of via ($> 3 \times 3$ array)
is not allowed.

CUP.7d Min Via4 space in via arrays = 0.3

CUP.7e Min space between via arrays = 0.36
not_rectangle_spacing1 168 violations found.
Error limit exceeded. Details only available for first 100.

CUP.8 : Top_Via-1 directly underneath the Pad mask
is not Allowed
and 101 violations found.
Error limit exceeded. Details only available for first 100.
Check was stopped early because error limit was reached.

CUP.9 : 1LM, 2LM and 3LM process not allowed to have
CUP for wire bond case

CUP.1a CUP is not allowed for Wedge-type Wire bond
case
and 58 violations found.
and 213 violations found.
Error limit exceeded. Details only available for first 100.
Check was stopped early because error limit was reached.

CUP.9_Wedge_4LM : 9.3 Wedge type wire-bond not
allowed to have CUP
and 31 violations found.
and 101 violations found.
Error limit exceeded. Details only available for first 100.
Check was stopped early because error limit was reached.

CUP.9_Wedge_5LM : 9.3 Wedge type wire-bond not
allowed to have CUP
and 3 violations found.
and 101 violations found.
Error limit exceeded. Details only available for first 100.
Check was stopped early because error limit was reached.

DCF.1a : All area between active polygons (COMP)
(with spacing greater than equal to this rule) \geq
20.0

must be filled with 'Dummy COMP' except area marked by NDMY, RES_MK, Pad and IND_MK as well as the region define by DCF.6a, 6b, 6c, 6d, 6e, 6f, 6g.

or 102 violations found.
Error limit exceeded. Details only available for first 100.

DCF.1b_DCF.1d : Minimum global density for active layers (COMP+ Dummy COMP) = 25.0%
Maximum global density for active layers (COMP+ Dummy COMP) = 70.0%
density 1 violation found.

DF.11 : Min. Length of butting COMP edge : 0.30
length_edge 102 violations found.
Error limit exceeded. Details only available for first 100.
Check was stopped early because error limit was reached.

DF.12 : Max distance of Nwell tap (NCOMP inside Nwell) from (PCOMP inside Nwell) : 20
and 110 violations found.
Error limit exceeded. Details only available for first 100.
Check was stopped early because error limit was reached.

DF.13 : Max distance of substrate tap (PCOMP outside Nwell) from (NCOMP outside Nwell) : 20
and 102 violations found.
Error limit exceeded. Details only available for first 100.
Check was stopped early because error limit was reached.

DF.18_LV : Min DNWELL space to (PCOMP outside Nwell and DNWELL) = 2.5
external2 24 violations found.

DF.1a : Min. COMP Width : 0.22
internal1 4 violations found.

DF.3a_LV : Minimum COMP space. P-substrate tap (PCOMP outside DNWELL and Nwell) can be butted for different voltage device like Low voltage, Medium voltage and High voltage as the potential is same
outside 2 violations found.

DF.3a_MV : Minimum COMP space. P-substrate tap (PCOMP

outside DNWELL and NWELL) can be butted for different voltage device like Low voltage, Medium voltage and High voltage as the potential is same

external1 9 violations found.

DF.3b : Min/Max space from NCOMP to PCOMP in the same well for butted COMP = 0.0

and 51 violations found.

DN.2 : Min. DNWELL Space : 5.42

external1 4 violations found.

DN.3 : Each DNWELL shall be directly surrounded by PCOMP guard ring tied to the P-substrate potential

and 84 violations found.

and 102 violations found.

Error limit exceeded. Details only available for first 100.

Check was stopped early because error limit was reached.

and 3 violations found.

not_outside 11 violations found.

DV.1 : Min. Dualgate enclose DNWELL = 0.5

enclose 24 violations found.

HRES.10 : Minimum/Maximum Pplus overlap of SAB = 0.1

interacting 100 violations found.

HRES.12 : P type Poly2 resistor (high sheet rho)

shall be covered by RES_MK marking.

RES_MK length shall be coincide with resistor length

(Defined by Pplus space)

and width covering the width of Poly2.

If the size of single RES_MK mark layer is greater than 15000 um² and both sides (X and Y) are greater than 80 um, then the minimum spacing to adjacent

RES_MK layer >= 20

Checked in PRES.9

xor 26 violations found.

HRES.2 : Min width of Poly2 resistor = 1.0

internal1 72 violations found.

HRES.4 : Minimum RESISTOR overlap of Poly2 resistor = 0.4

enclose 36 violations found.

HRES.7 : Minimum Pplus overlap of contact on Poly2
resistor = 0.2

enclose 48 violations found.

HVNESD.13(b) : Max. at least one or nearest source
contact to gate edge space (SCGS) <= 1
not_interacting 2 violations found.

HVNESD.8(c) : Max. at least one or nearest drain
contact to gate edge space (DCGS) <= 4
not_interacting 5 violations found.

HVPESD.11 : Source COMP must enclose by LVS_Source
not 1 violation found.

IO.0 : Guidelines : To flag I/O latch-up related
violation:

(a) Non well tap COMP directly connected to PAD is
recommended to be marked by 'Latchup_MK' layer

(b) Min/max Latchup_MK layer overlap of COMP
(directly connected to Pad) = 0.0

xor 28 violations found.

IO.1_a2 : For LV and MV

It should also be directly surrounded by an Nwell
guard ring

(Non broken NCOMP ring inside Nwell).

Nwell guard ring shall be connected to the most
positive supply.

Max space of Nwell guard ring to the NCOMP in Psub
directly

connected to I/O pad = 15

edge_size 16 violations found.

IO.1_b : Within 15um from the edge of the NCOMP
connected to I/O pad (marked by Latchup_MK):

Max Nwell tap distance to PCOMP inside Nwell <= 2
(irrespective of its direct connection to Pad)

wide 25 violations found.

IO.3_a2 : For LV and MV

It should also be directly surrounded by PCOMP guard

ring outside Nwell.

PCOMP guardring shall be connected to the lowest potential.

Max space of guard ring PCOMP to the PCOMP in Nwell directly connected to the I/O pad = 15

edge_size 12 violations found.

IO.3_b : For LV and MV

Within 10um from the edge of the PCOMP connected to I/O Pad (marked by Latchup_MK):

Max P substrate tap distance to NCOMP outside Nwell <= 5.0 (irrespective of its direct connection to Pad)

wide 14 violations found.

LPW.12 : LVPWELL cannot overlap with Nwell

and 2 violations found.

LU.3a_MV_LU.3b_MV_LU.3c_MV : Max. Psub tap outside (DNWELL and YMTP_MK) space to any point in the boundary of Ncomp outside Nwell/DNWELL = 15 (MV)

coincident_edge 48 violations found.

LU.4a_LV : Max. Nwell tap outside DNWELL space to any point in the boundary of Pcomp inside Nwell = 50 (LV)

For Nwell to Ncomp space outside DNWELL >= 2.0um

coincident_edge 48 violations found.

LU.4a_MV_LU.4b_MV_LU.4c_MV : Max. Nwell tap outside DNWELL space to any point in the boundary of Pcomp inside Nwell = 15 (MV)

coincident_edge 80 violations found.

M1.1 : Metal1 minimum width : 0.23

internal1 128 violations found.

Error limit exceeded. Details only available for first 100.

M1.2a : Metal1 minimum space : 0.23

external1 301 violations found.

Error limit exceeded. Details only available for first 100.

Check was stopped early because error limit was reached.

M2.1 : Metal2 minimum width : 0.28

internal1 12 violations found.

M2.2a : Metal2 minimum space : 0.28

external1 301 violations found.

Error limit exceeded. Details only available for first 100.

Check was stopped early because error limit was reached.

MIMTM.10 : (a) There cannot be any Via3 touching

MIM bottom plate Metal4

(b) MIM bottom plate Metal4 can only be connected
through the higher Via (Via4)

and 40 violations found.

MSLOT.1_Metal1 : Maximum Metal1 width without
slotting = 30.0

or 3 violations found.

MSLOT.1_Metal2 : Maximum Metal2 width without
slotting = 30.0

or 2 violations found.

MSLOT.1_Metal3 : Maximum Metal3 width without
slotting = 30.0

or 2 violations found.

Mn.4_Metal1 : Metal1 coverage over the entire die
shall be > 30%

density 1 violation found.

Mn.4_Metal2 : Metal2 coverage over the entire die
shall be > 30%

density 1 violation found.

NP.11 : Butting Nplus and PCOMP is forbidden within
0.43 of well (Nwell and LVPWELL) edge (for inside
DNWELL case)

and 5 violations found.

NP.3a : Nplus space to PCOMP (1) inside Nwell (2)
outside LVPWELL but inside DNWELL : 0.16

external2 12 violations found.

NP.4a : Nplus space to related P-channel gate at
a butting edge parallel to gate : 0.32

external2 24 violations found.

NP.5a : Nplus overlap of N-channel gate : 0.23
enclose 24 violations found.

NP.5d(i) : Nplus extension beyond COMP inside DNWELL
for Nwell overlap of Nplus < 0.43 : 0.16
enclose 302 violations found.
Error limit exceeded. Details only available for first 100.
Check was stopped early because error limit was reached.

NP.6 : Nplus overlap with NCOMP butted to PCOMP :
0.22
internal1 19 violations found.

NW.2 : Min. Nwell Space : 1.4
external1 5 violations found.

NW.3 : Min. Nwell to DNWELL space : 3.1
external2 32 violations found.

PAD.16 : Max pad opening space to nearest S/L guard
ring (Inner edge of GUARD_RING_MK marking) = 200.0
not_interacting 1 violation found.

PAD.17 : Pad opening space to active circuit COMP
= 15.0
external2 301 violations found.
Error limit exceeded. Details only available for first 100.
Check was stopped early because error limit was reached.

PAD.18 : Pad opening space to active circuit Poly2
= 15.0
external2 301 violations found.
Error limit exceeded. Details only available for first 100.
Check was stopped early because error limit was reached.

PAD.19a_M1 : Pad opening to non-pad circuit Metal1,
2, 3, 4,5 up to Top Metal-1 = 6.0
external2 16 violations found.

PAD.19a_M2 : Pad opening to non-pad circuit Metal1,
2, 3, 4,5 up to Top Metal-1 = 6.0
external2 227 violations found.
Error limit exceeded. Details only available for first 100.

PL.12 : V5_Xtor enclose 5V COMP
not 34 violations found.

PL.3 : Min. Poly2 Spacing : 0.24
external1 3 violations found.

PL.3b_MV : Min Poly2 space on COMP for low active
sheet resistivity (guideline)
outside 3 violations found.

PL.4 : Min. Poly2 Extension beyond COMP to form end
cap : 0.22
internal1 24 violations found.

PL.6 : (Poly2 gate not touching YMTP_MK) with 90
degree bends are not allowed.
external1_error 8 violations found.
internal1_error 16 violations found.

PL.8 : Poly2 coverage over the entire die shall be
>= 14%
density 1 violation found.

PP.11 : Butting Pplus and NCOMP is forbidden within
0.43um of Nwell edge (for outside DNWELL) and of
LVPWELL edge (for inside DNWELL case)
and 5 violations found.

PP.12 : Pplus overlap with N-channel Poly2 gate
extension is forbidden within 0.32um of N-channel
gate
and 42 violations found.

PP.2 : Min. Pplus Space : 0.4
external1 132 violations found.
Error limit exceeded. Details only available for first 100.

PP.3c(ii) : Pplus space to NCOMP outside DNWELL for
NCOMP space to Nwell < 0.43 : 0.16
external2 108 violations found.
Error limit exceeded. Details only available for first 100.

PP.4a : Pplus space to related N-channel gate at

a butting edge parallel to gate : 0.32
external2 12 violations found.

PP.5a : Pplus overlap of P-channel gate : 0.23
enclose 30 violations found.

PP.5b : Pplus extension beyond COMP for the COMP
(1) inside NWELL (2) outside LVPWELL but inside
DNWELL : 0.16
enclose 12 violations found.

PP.5c(ii) : Pplus extension beyond COMP inside DNWELL
for LVPWELL overlap of Pplus < 0.43 : 0.16
enclose 16 violations found.

PP.5d(ii) : Pplus extension beyond COMP outside
DNWELL for Pplus space to Nwell < 0.43 : 0.16
enclose 176 violations found.
Error limit exceeded. Details only available for first 100.

PP.6 : Pplus overlap with PCOMP butted to NCOMP :
0.22
internal1 16 violations found.

V1.1: Min/max Via1 size : 0.26
not_length_edge 102 violations found.
Error limit exceeded. Details only available for first 100.
Check was stopped early because error limit was reached.

V2.1: Min/max Via2 size : 0.26
not_length_edge 102 violations found.
Error limit exceeded. Details only available for first 100.
Check was stopped early because error limit was reached.

ERROR DETAILS

CO.10 Contact on Poly2 gate over COMP is forbidden

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2751:and

Structure (lower left x, y) (upper right x, y)

trackA (1349.3300, 2367.1500) (1349.5500, 2367.3700)
trackA (1356.7300, 2367.1600) (1356.9500, 2367.3800)
trackA (1358.4100, 2367.1850) (1358.6300, 2367.4050)
trackA (1367.7200, 2367.1850) (1367.9400, 2367.4050)
trackA (1377.0300, 2367.1850) (1377.2500, 2367.4050)
trackA (1386.3400, 2367.1850) (1386.5600, 2367.4050)
trackA (1349.3300, 2372.9750) (1349.5500, 2372.9800)
trackA (1349.3300, 2373.2700) (1349.5500, 2373.4750)
trackA (1356.7300, 2372.9750) (1356.9500, 2372.9900)
trackA (1356.7300, 2373.2800) (1356.9500, 2373.4750)
trackA (1349.3300, 2378.8800) (1349.5500, 2379.1000)
trackA (1356.7300, 2378.8900) (1356.9500, 2379.1100)
trackA (1349.3300, 2384.6750) (1349.5500, 2384.7100)
trackA (1349.3300, 2385.0000) (1349.5500, 2385.1750)
trackA (1356.7300, 2384.6750) (1356.9500, 2384.7200)
trackA (1356.7300, 2385.0100) (1356.9500, 2385.1750)
trackA (1349.3300, 2390.6100) (1349.5500, 2390.8300)
trackA (1356.7300, 2390.6200) (1356.9500, 2390.8400)
trackA (1359.1000, 2390.4650) (1359.3200, 2390.6850)
trackA (1368.4100, 2390.4650) (1368.6300, 2390.6850)
trackA (1377.7200, 2390.4650) (1377.9400, 2390.6850)
trackA (1387.0300, 2390.4650) (1387.2500, 2390.6850)
trackA (1454.8300, 2418.5650) (1455.0500, 2418.7050)
trackA (1454.8300, 2418.9950) (1455.0500, 2419.0650)
trackA (1462.9250, 2418.5850) (1463.1450, 2418.8050)
trackA (1468.0700, 2418.7050) (1468.2900, 2418.9250)
trackA (1487.7500, 2418.7050) (1487.9700, 2418.9250)
trackA (1477.9100, 2418.7050) (1478.1300, 2418.9250)
trackA (1454.8300, 2410.9550) (1455.0500, 2411.0550)
trackA (1454.8300, 2411.3450) (1455.0500, 2411.4550)
trackA (1462.9250, 2410.9550) (1463.1450, 2411.1550)
trackA (1462.9250, 2411.4450) (1463.1450, 2411.4550)
trackA (1496.6100, 2411.3700) (1496.8300, 2411.4550)
trackA (1468.0700, 2411.0950) (1468.2900, 2411.3150)
trackA (1477.9100, 2411.0950) (1478.1300, 2411.3150)
trackA (1487.7500, 2411.0950) (1487.9700, 2411.3150)
trackA (1454.8300, 2403.3450) (1455.0500, 2403.4050)
trackA (1454.8300, 2403.6950) (1455.0500, 2403.8450)
trackA (1462.9250, 2403.3450) (1463.1450, 2403.5050)

trackA (1462.9250, 2403.7950) (1463.1450, 2403.8450)
trackA (1496.6100, 2403.3700) (1496.8300, 2403.5900)
trackA (1468.0700, 2403.4850) (1468.2900, 2403.7050)
trackA (1477.9100, 2403.4850) (1478.1300, 2403.7050)
trackA (1487.7500, 2403.4850) (1487.9700, 2403.7050)
trackA (1454.8300, 2395.7350) (1455.0500, 2395.7550)
trackA (1454.8300, 2396.0450) (1455.0500, 2396.2350)
trackA (1462.9250, 2395.7350) (1463.1450, 2395.8550)
trackA (1462.9250, 2396.1450) (1463.1450, 2396.2350)
trackA (1496.6100, 2396.1700) (1496.8300, 2396.2350)
trackA (1468.0700, 2395.8750) (1468.2900, 2396.0950)
trackA (1477.9100, 2395.8750) (1478.1300, 2396.0950)
trackA (1487.7500, 2395.8750) (1487.9700, 2396.0950)
trackA (1454.8300, 2388.3950) (1455.0500, 2388.6150)
trackA (1462.9250, 2388.1250) (1463.1450, 2388.2050)
trackA (1462.9250, 2388.4950) (1463.1450, 2388.6250)
trackA (1496.6100, 2388.1700) (1496.8300, 2388.3900)
trackA (1468.0700, 2388.2650) (1468.2900, 2388.4850)
trackA (1477.9100, 2388.2650) (1478.1300, 2388.4850)
trackA (1487.7500, 2388.2650) (1487.9700, 2388.4850)
trackA (1454.8300, 2380.7450) (1455.0500, 2380.9650)
trackA (1462.9250, 2380.5150) (1463.1450, 2380.5550)
trackA (1462.9250, 2380.8450) (1463.1450, 2381.0150)
trackA (1496.6100, 2380.9700) (1496.8300, 2381.0150)
trackA (1468.0700, 2380.6550) (1468.2900, 2380.8750)
trackA (1477.9100, 2380.6550) (1478.1300, 2380.8750)
trackA (1487.7500, 2380.6550) (1487.9700, 2380.8750)
trackA (1454.8300, 2373.0950) (1455.0500, 2373.3150)
trackA (1462.9250, 2373.1950) (1463.1450, 2373.4050)
trackA (1496.6100, 2372.9700) (1496.8300, 2373.1900)
trackA (1468.0700, 2373.0450) (1468.2900, 2373.2650)
trackA (1477.9100, 2373.0450) (1478.1300, 2373.2650)
trackA (1487.7500, 2373.0450) (1487.9700, 2373.2650)
trackA (1454.8300, 2365.4450) (1455.0500, 2365.6650)
trackA (1462.9250, 2365.5450) (1463.1450, 2365.7650)
trackA (1496.6100, 2365.7700) (1496.8300, 2365.7950)
trackA (1468.0700, 2365.4350) (1468.2900, 2365.6550)
trackA (1477.9100, 2365.4350) (1478.1300, 2365.6550)
trackA (1487.7500, 2365.4350) (1487.9700, 2365.6550)

CO.1: Min/max contact size : 0.22

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2661:not_length_edge

WARNING: The error count of 102 for this check exceeds the limit set in
the runset. Details only available for the first 100.

Check was stopped early because error limit was reached.

```
-----  
Structure      ( lower left x, y ) ( upper right x, y ) Distance  
-----  
Unnamed_02d9ae27 (-10.5300, 10.8950) (-10.5300, 11.1200) 0.2250  
Unnamed_02d9ae27 (-10.3100, 10.8950) (-10.3100, 11.1200) 0.2250  
Unnamed_02d9ae27 (-10.5300, 11.3950) (-10.5300, 11.6200) 0.2250  
Unnamed_02d9ae27 (-10.3100, 11.3950) (-10.3100, 11.6200) 0.2250  
Unnamed_02d9ae27 (-10.5300, 11.8950) (-10.5300, 12.1200) 0.2250  
Unnamed_02d9ae27 (-10.3100, 11.8950) (-10.3100, 12.1200) 0.2250  
Unnamed_02d9ae27 (-10.5300, 12.3950) (-10.5300, 12.6200) 0.2250  
Unnamed_02d9ae27 (-10.3100, 12.3950) (-10.3100, 12.6200) 0.2250  
Unnamed_02d9ae27 (10.3100, 10.8950) (10.3100, 11.1200) 0.2250  
Unnamed_02d9ae27 (10.5300, 10.8950) (10.5300, 11.1200) 0.2250  
Unnamed_02d9ae27 (10.3100, 11.3950) (10.3100, 11.6200) 0.2250  
Unnamed_02d9ae27 (10.5300, 11.3950) (10.5300, 11.6200) 0.2250  
Unnamed_02d9ae27 (10.3100, 11.8950) (10.3100, 12.1200) 0.2250  
Unnamed_02d9ae27 (10.5300, 11.8950) (10.5300, 12.1200) 0.2250  
Unnamed_02d9ae27 (10.3100, 12.3950) (10.3100, 12.6200) 0.2250  
Unnamed_02d9ae27 (10.5300, 12.3950) (10.5300, 12.6200) 0.2250  
Unnamed_02d9ae27 (-10.5300, 12.8950) (-10.5300, 13.1200) 0.2250  
Unnamed_02d9ae27 (-10.3100, 12.8950) (-10.3100, 13.1200) 0.2250  
Unnamed_02d9ae27 (-10.5300, 13.3950) (-10.5300, 13.6200) 0.2250  
Unnamed_02d9ae27 (-10.3100, 13.3950) (-10.3100, 13.6200) 0.2250  
Unnamed_02d9ae27 (-9.3100, 14.1450) (-9.3100, 14.3700) 0.2250  
Unnamed_02d9ae27 (-9.0900, 14.1450) (-9.0900, 14.3700) 0.2250  
Unnamed_02d9ae27 (-8.5100, 14.1450) (-8.5100, 14.3700) 0.2250  
Unnamed_02d9ae27 (-8.2900, 14.1450) (-8.2900, 14.3700) 0.2250  
Unnamed_02d9ae27 (-7.7100, 14.1450) (-7.7100, 14.3700) 0.2250  
Unnamed_02d9ae27 (-7.4900, 14.1450) (-7.4900, 14.3700) 0.2250  
Unnamed_02d9ae27 (-6.9100, 14.1450) (-6.9100, 14.3700) 0.2250  
Unnamed_02d9ae27 (-6.6900, 14.1450) (-6.6900, 14.3700) 0.2250  
Unnamed_02d9ae27 (-6.1100, 14.1450) (-6.1100, 14.3700) 0.2250  
Unnamed_02d9ae27 (-5.8900, 14.1450) (-5.8900, 14.3700) 0.2250  
Unnamed_02d9ae27 (-5.3100, 14.1450) (-5.3100, 14.3700) 0.2250  
Unnamed_02d9ae27 (-5.0900, 14.1450) (-5.0900, 14.3700) 0.2250  
Unnamed_02d9ae27 (-4.5100, 14.1450) (-4.5100, 14.3700) 0.2250
```

Unnamed_02d9ae27 (-4.2900, 14.1450) (-4.2900, 14.3700) 0.2250
Unnamed_02d9ae27 (-3.7100, 14.1450) (-3.7100, 14.3700) 0.2250
Unnamed_02d9ae27 (-3.4900, 14.1450) (-3.4900, 14.3700) 0.2250
Unnamed_02d9ae27 (-2.9100, 14.1450) (-2.9100, 14.3700) 0.2250
Unnamed_02d9ae27 (-2.6900, 14.1450) (-2.6900, 14.3700) 0.2250
Unnamed_02d9ae27 (-2.1100, 14.1450) (-2.1100, 14.3700) 0.2250
Unnamed_02d9ae27 (-1.8900, 14.1450) (-1.8900, 14.3700) 0.2250
Unnamed_02d9ae27 (-1.3100, 14.1450) (-1.3100, 14.3700) 0.2250
Unnamed_02d9ae27 (-1.0900, 14.1450) (-1.0900, 14.3700) 0.2250
Unnamed_02d9ae27 (-0.5100, 14.1450) (-0.5100, 14.3700) 0.2250
Unnamed_02d9ae27 (-0.2900, 14.1450) (-0.2900, 14.3700) 0.2250
Unnamed_02d9ae27 (0.2900, 14.1450) (0.2900, 14.3700) 0.2250
Unnamed_02d9ae27 (0.5100, 14.1450) (0.5100, 14.3700) 0.2250
Unnamed_02d9ae27 (1.0900, 14.1450) (1.0900, 14.3700) 0.2250
Unnamed_02d9ae27 (1.3100, 14.1450) (1.3100, 14.3700) 0.2250
Unnamed_02d9ae27 (1.8900, 14.1450) (1.8900, 14.3700) 0.2250
Unnamed_02d9ae27 (2.1100, 14.1450) (2.1100, 14.3700) 0.2250
Unnamed_02d9ae27 (2.6900, 14.1450) (2.6900, 14.3700) 0.2250
Unnamed_02d9ae27 (2.9100, 14.1450) (2.9100, 14.3700) 0.2250
Unnamed_02d9ae27 (3.4900, 14.1450) (3.4900, 14.3700) 0.2250
Unnamed_02d9ae27 (3.7100, 14.1450) (3.7100, 14.3700) 0.2250
Unnamed_02d9ae27 (4.2900, 14.1450) (4.2900, 14.3700) 0.2250
Unnamed_02d9ae27 (4.5100, 14.1450) (4.5100, 14.3700) 0.2250
Unnamed_02d9ae27 (5.0900, 14.1450) (5.0900, 14.3700) 0.2250
Unnamed_02d9ae27 (5.3100, 14.1450) (5.3100, 14.3700) 0.2250
Unnamed_02d9ae27 (5.8900, 14.1450) (5.8900, 14.3700) 0.2250
Unnamed_02d9ae27 (6.1100, 14.1450) (6.1100, 14.3700) 0.2250
Unnamed_02d9ae27 (6.6900, 14.1450) (6.6900, 14.3700) 0.2250
Unnamed_02d9ae27 (6.9100, 14.1450) (6.9100, 14.3700) 0.2250
Unnamed_02d9ae27 (7.4900, 14.1450) (7.4900, 14.3700) 0.2250
Unnamed_02d9ae27 (7.7100, 14.1450) (7.7100, 14.3700) 0.2250
Unnamed_02d9ae27 (8.2900, 14.1450) (8.2900, 14.3700) 0.2250
Unnamed_02d9ae27 (8.5100, 14.1450) (8.5100, 14.3700) 0.2250
Unnamed_02d9ae27 (9.0900, 14.1450) (9.0900, 14.3700) 0.2250
Unnamed_02d9ae27 (9.3100, 14.1450) (9.3100, 14.3700) 0.2250
Unnamed_02d9ae27 (10.3100, 12.8950) (10.3100, 13.1200) 0.2250
Unnamed_02d9ae27 (10.5300, 12.8950) (10.5300, 13.1200) 0.2250
Unnamed_02d9ae27 (10.3100, 13.3950) (10.3100, 13.6200) 0.2250
Unnamed_02d9ae27 (10.5300, 13.3950) (10.5300, 13.6200) 0.2250
Unnamed_02d9ae27 (-9.3600, 19.0900) (-9.3600, 19.3150) 0.2250
Unnamed_02d9ae27 (-9.1400, 19.0900) (-9.1400, 19.3150) 0.2250
Unnamed_02d9ae27 (-8.2200, 19.0900) (-8.2200, 19.3150) 0.2250
Unnamed_02d9ae27 (-8.0000, 19.0900) (-8.0000, 19.3150) 0.2250
Unnamed_02d9ae27 (-6.7400, 19.0900) (-6.7400, 19.3150) 0.2250

Unnamed_02d9ae27	(-6.5200, 19.0900)	(-6.5200, 19.3150)	0.2250
Unnamed_02d9ae27	(-5.6000, 19.0900)	(-5.6000, 19.3150)	0.2250
Unnamed_02d9ae27	(-5.3800, 19.0900)	(-5.3800, 19.3150)	0.2250
Unnamed_02d9ae27	(-4.4600, 19.0900)	(-4.4600, 19.3150)	0.2250
Unnamed_02d9ae27	(-4.2400, 19.0900)	(-4.2400, 19.3150)	0.2250
Unnamed_02d9ae27	(-3.0800, 19.0900)	(-3.0800, 19.3150)	0.2250
Unnamed_02d9ae27	(-2.8600, 19.0900)	(-2.8600, 19.3150)	0.2250
Unnamed_02d9ae27	(-1.9400, 19.0900)	(-1.9400, 19.3150)	0.2250
Unnamed_02d9ae27	(-1.7200, 19.0900)	(-1.7200, 19.3150)	0.2250
Unnamed_02d9ae27	(-0.8000, 19.0900)	(-0.8000, 19.3150)	0.2250
Unnamed_02d9ae27	(-0.5800, 19.0900)	(-0.5800, 19.3150)	0.2250
Unnamed_02d9ae27	(0.5800, 19.0900)	(0.5800, 19.3150)	0.2250
Unnamed_02d9ae27	(0.8000, 19.0900)	(0.8000, 19.3150)	0.2250
Unnamed_02d9ae27	(1.7200, 19.0900)	(1.7200, 19.3150)	0.2250
Unnamed_02d9ae27	(1.9400, 19.0900)	(1.9400, 19.3150)	0.2250
Unnamed_02d9ae27	(2.8600, 19.0900)	(2.8600, 19.3150)	0.2250
Unnamed_02d9ae27	(3.0800, 19.0900)	(3.0800, 19.3150)	0.2250
Unnamed_02d9ae27	(4.2400, 19.0900)	(4.2400, 19.3150)	0.2250
Unnamed_02d9ae27	(4.4600, 19.0900)	(4.4600, 19.3150)	0.2250
Unnamed_02d9ae27	(5.3800, 19.0900)	(5.3800, 19.3150)	0.2250
Unnamed_02d9ae27	(5.6000, 19.0900)	(5.6000, 19.3150)	0.2250
Unnamed_02d9ae27	(6.5200, 19.0900)	(6.5200, 19.3150)	0.2250
Unnamed_02d9ae27	(6.7400, 19.0900)	(6.7400, 19.3150)	0.2250

CO.3 Poly2 overlap of contact : 0.07

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2681:enclose

Structure (lower left x, y) (upper right x, y) Distance

trackA	(1462.9250, 2365.7650)	(1463.1450, 2365.7950)	0.0300
trackA	(1349.3300, 2367.1250)	(1349.5500, 2367.1500)	0.0250
trackA	(1356.7300, 2367.1250)	(1356.9500, 2367.1600)	0.0350
trackA	(1358.4100, 2367.1250)	(1358.6300, 2367.1850)	0.0600
trackA	(1367.7200, 2367.1250)	(1367.9400, 2367.1850)	0.0600
trackA	(1377.0300, 2367.1250)	(1377.2500, 2367.1850)	0.0600
trackA	(1386.3400, 2367.1250)	(1386.5600, 2367.1850)	0.0600
trackA	(1349.3300, 2378.8250)	(1349.5500, 2378.8800)	0.0550
trackA	(1356.7300, 2378.8250)	(1356.9500, 2378.8900)	0.0650
trackA	(1454.8300, 2380.9650)	(1455.0500, 2381.0150)	0.0500

trackA	(1496.6100, 2372.9050)	(1496.8300, 2372.9700)	0.0650
trackA	(1376.6300, 2383.2950)	(1376.6550, 2383.5150)	0.0250
trackA	(1454.8300, 2388.6150)	(1455.0500, 2388.6250)	0.0100
trackA	(1496.6100, 2388.1250)	(1496.8300, 2388.1700)	0.0450
trackA	(1462.9250, 2418.5650)	(1463.1450, 2418.5850)	0.0200
trackA	(1496.6100, 2403.3450)	(1496.8300, 2403.3700)	0.0250

CO.4 COMP overlap of contact : 0.07

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2686:enclose

Structure (lower left x, y) (upper right x, y) Distance

trackA	(1359.1000, 2383.1750)	(1359.3200, 2383.2150)	0.0400
trackA	(1368.4100, 2383.1750)	(1368.6300, 2383.2150)	0.0400
trackA	(1377.7200, 2383.1750)	(1377.9400, 2383.2150)	0.0400
trackA	(1387.0300, 2383.1750)	(1387.2500, 2383.2150)	0.0400

CO.7 Space from COMP contact to Poly2 on COMP : 0.15

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2733:external2

Structure (lower left x, y) (upper right x, y) Distance

trackA	(1349.3300, 2367.6250)	(1349.5500, 2367.6600)	0.0350
trackA	(1356.7300, 2367.6250)	(1356.9500, 2367.6700)	0.0450
trackA	(1349.3300, 2379.3250)	(1349.5500, 2379.3900)	0.0650
trackA	(1356.7300, 2379.3250)	(1356.9500, 2379.4000)	0.0750
trackA	(1349.3300, 2391.0250)	(1349.5500, 2391.1200)	0.0950
trackA	(1356.7300, 2391.0250)	(1356.9500, 2391.1300)	0.1050
trackA	(1462.9250, 2419.0650)	(1463.1450, 2419.0950)	0.0300
trackA	(1496.6100, 2395.5900)	(1496.8300, 2395.7350)	0.1450
trackA	(1454.8300, 2388.1050)	(1455.0500, 2388.1250)	0.0200
trackA	(1454.8300, 2380.4550)	(1455.0500, 2380.5150)	0.0600
trackA	(1496.6100, 2380.3900)	(1496.8300, 2380.5150)	0.1250
trackA	(1454.8300, 2372.8050)	(1455.0500, 2372.9050)	0.1000

trackA (1454.8300, 2365.1550) (1455.0500, 2365.2950) 0.1400
trackA (1462.9250, 2365.2550) (1463.1450, 2365.2950) 0.0400
trackA (1496.6100, 2365.1900) (1496.8300, 2365.2950) 0.1050
trackA (1358.0050, 2383.2950) (1358.0100, 2383.5150) 0.0050
trackA (1367.1850, 2383.2950) (1367.3200, 2383.5150) 0.1350
trackA (1387.3200, 2383.2950) (1387.3650, 2383.5150) 0.0450

CO.9 Contact on NCOMP to PCOMP butting edge is forbidden

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2745:and_edge

Structure (lower left x, y) (upper right x, y)

trackA (1356.7300, 2366.3550) (1356.9500, 2366.3550)
trackA (1356.7300, 2378.0550) (1356.9500, 2378.0550)
trackA (1356.7300, 2389.7550) (1356.9500, 2389.7550)
trackA (1496.6100, 2402.5750) (1496.8300, 2402.5750)

COHVNESD.7_COHVPESD.7 : Recommended/max. salicided block edge to at
least one or nearest contact (CA) <= 0.22

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:7062:not_interacting

Structure (lower left x, y) (upper right x, y)

comp018green_out_drv_nleg_4T\$1 (6.6200, 40.8800) (11.8300, 41.1000)
comp018green_out_drv_nleg_4T\$1 (6.6200, 2.2200) (11.8300, 2.4400)
comp018green_out_drv_nleg_4T\$1 (0.7500, 40.8800) (5.9600, 41.1000)
comp018green_out_drv_nleg_4T\$1 (0.7500, 2.2200) (5.9600, 2.4400)
pmos_6p0_esd_40\$1 (1.1100, 40.8800) (4.8700, 41.1000)
pmos_6p0_esd_40\$1 (1.1100, 0.2200) (4.8700, 0.4400)

CUP.3_Metal2 : Min space of Metal2 line used for bond pads = 1.0

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:3001:external1

Structure (lower left x, y) (upper right x, y) Distance

Bondpad_5LM\$1	(5.0400, 2.0000)	(5.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(7.0400, 2.0000)	(7.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(9.0400, 2.0000)	(9.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(11.0400, 2.0000)	(11.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(13.0400, 2.0000)	(13.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(15.0400, 2.0000)	(15.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(17.0400, 2.0000)	(17.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(19.0400, 2.0000)	(19.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(21.0400, 2.0000)	(21.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(23.0400, 2.0000)	(23.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(25.0400, 2.0000)	(25.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(27.0400, 2.0000)	(27.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(29.0400, 2.0000)	(29.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(31.0400, 2.0000)	(31.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(33.0400, 2.0000)	(33.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(35.0400, 2.0000)	(35.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(37.0400, 2.0000)	(37.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(39.0400, 2.0000)	(39.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(41.0400, 2.0000)	(41.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(43.0400, 2.0000)	(43.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(45.0400, 2.0000)	(45.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(47.0400, 2.0000)	(47.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(49.0400, 2.0000)	(49.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(51.0400, 2.0000)	(51.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(53.0400, 2.0000)	(53.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(55.0400, 2.0000)	(55.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(57.0400, 2.0000)	(57.3400, 62.0000)	0.3000
Bondpad_5LM\$1	(59.0400, 2.0000)	(59.3400, 62.0000)	0.3000

CUP.3_Metal3 : Min space of Metal3 line used for bond pads = 1.0

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2998:external1

Structure (lower left x, y) (upper right x, y) Distance

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-----
Bondpad_5LM$1 (5.0400, 2.2900) (5.3400, 61.6000) 0.3000
Bondpad_5LM$1 (7.0400, 2.2900) (7.3400, 61.6000) 0.3000
Bondpad_5LM$1 (9.0400, 2.2900) (9.3400, 61.6000) 0.3000
Bondpad_5LM$1 (11.0400, 2.2900) (11.3400, 61.6000) 0.3000
Bondpad_5LM$1 (13.0400, 2.2900) (13.3400, 61.6000) 0.3000
Bondpad_5LM$1 (15.0400, 2.2900) (15.3400, 61.6000) 0.3000
Bondpad_5LM$1 (17.0400, 2.2900) (17.3400, 61.6000) 0.3000
Bondpad_5LM$1 (19.0400, 2.2900) (19.3400, 61.6000) 0.3000
Bondpad_5LM$1 (21.0400, 2.2900) (21.3400, 61.6000) 0.3000
Bondpad_5LM$1 (23.0400, 2.2900) (23.3400, 61.6000) 0.3000
Bondpad_5LM$1 (25.0400, 2.2900) (25.3400, 61.6000) 0.3000
Bondpad_5LM$1 (27.0400, 2.2900) (27.3400, 61.6000) 0.3000
Bondpad_5LM$1 (29.0400, 2.2900) (29.3400, 61.6000) 0.3000
Bondpad_5LM$1 (31.0400, 2.2900) (31.3400, 61.6000) 0.3000
Bondpad_5LM$1 (33.0400, 2.2900) (33.3400, 61.6000) 0.3000
Bondpad_5LM$1 (35.0400, 2.2900) (35.3400, 61.6000) 0.3000
Bondpad_5LM$1 (37.0400, 2.2900) (37.3400, 61.6000) 0.3000
Bondpad_5LM$1 (39.0400, 2.2900) (39.3400, 61.6000) 0.3000
Bondpad_5LM$1 (41.0400, 2.2900) (41.3400, 61.6000) 0.3000
Bondpad_5LM$1 (43.0400, 2.2900) (43.3400, 61.6000) 0.3000
Bondpad_5LM$1 (45.0400, 2.2900) (45.3400, 61.6000) 0.3000
Bondpad_5LM$1 (47.0400, 2.2900) (47.3400, 61.6000) 0.3000
Bondpad_5LM$1 (49.0400, 2.2900) (49.3400, 61.6000) 0.3000
Bondpad_5LM$1 (51.0400, 2.2900) (51.3400, 61.6000) 0.3000
Bondpad_5LM$1 (53.0400, 2.2900) (53.3400, 61.6000) 0.3000
Bondpad_5LM$1 (55.0400, 2.2900) (55.3400, 61.6000) 0.3000
Bondpad_5LM$1 (57.0400, 2.2900) (57.3400, 61.6000) 0.3000
Bondpad_5LM$1 (59.0400, 2.2900) (59.3400, 61.6000) 0.3000

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CUP.3_Metal4 : Min space of Metal4 line used for bond pads = 1.0
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/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2995:external1

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Structure    ( lower left x, y ) ( upper right x, y ) Distance
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Bondpad_5LM$1 (5.0400, 2.2900) (5.3400, 61.6000) 0.3000
Bondpad_5LM$1 (7.0400, 2.2900) (7.3400, 61.6000) 0.3000
Bondpad_5LM$1 (9.0400, 2.2900) (9.3400, 61.6000) 0.3000
Bondpad_5LM$1 (11.0400, 2.2900) (11.3400, 61.6000) 0.3000

```

Bondpad_5LM\$1	(13.0400, 2.2900)	(13.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(15.0400, 2.2900)	(15.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(17.0400, 2.2900)	(17.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(19.0400, 2.2900)	(19.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(21.0400, 2.2900)	(21.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(23.0400, 2.2900)	(23.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(25.0400, 2.2900)	(25.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(27.0400, 2.2900)	(27.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(29.0400, 2.2900)	(29.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(31.0400, 2.2900)	(31.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(33.0400, 2.2900)	(33.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(35.0400, 2.2900)	(35.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(37.0400, 2.2900)	(37.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(39.0400, 2.2900)	(39.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(41.0400, 2.2900)	(41.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(43.0400, 2.2900)	(43.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(45.0400, 2.2900)	(45.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(47.0400, 2.2900)	(47.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(49.0400, 2.2900)	(49.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(51.0400, 2.2900)	(51.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(53.0400, 2.2900)	(53.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(55.0400, 2.2900)	(55.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(57.0400, 2.2900)	(57.3400, 61.6000)	0.3000
Bondpad_5LM\$1	(59.0400, 2.2900)	(59.3400, 61.6000)	0.3000

CUP.5 : Top via (Via4) not allowed directly under pad opening

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:3016:and

WARNING: The error count of 101 for this check exceeds the limit set in
the runset. Details only available for the first 100.

Check was stopped early because error limit was reached.

Structure (lower left x, y) (upper right x, y)

M5_M4_CDNS_4066195314556\$1	(-29.5950, -0.4850)	(-29.3350, -0.2250)
M5_M4_CDNS_4066195314556\$1	(-29.5950, 0.2250)	(-29.3350, 0.4850)
M5_M4_CDNS_4066195314556\$1	(-28.8850, -0.4850)	(-28.6250, -0.2250)
M5_M4_CDNS_4066195314556\$1	(-28.8850, 0.2250)	(-28.6250, 0.4850)

M5_M4_CDNS_4066195314556\$1 (-28.1750, -0.4850) (-27.9150, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-28.1750, 0.2250) (-27.9150, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-27.4650, -0.4850) (-27.2050, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-27.4650, 0.2250) (-27.2050, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-26.7550, -0.4850) (-26.4950, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-26.7550, 0.2250) (-26.4950, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-26.0450, -0.4850) (-25.7850, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-26.0450, 0.2250) (-25.7850, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-25.3350, -0.4850) (-25.0750, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-25.3350, 0.2250) (-25.0750, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-24.6250, -0.4850) (-24.3650, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-24.6250, 0.2250) (-24.3650, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-23.9150, -0.4850) (-23.6550, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-23.9150, 0.2250) (-23.6550, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-23.2050, -0.4850) (-22.9450, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-23.2050, 0.2250) (-22.9450, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-22.4950, -0.4850) (-22.2350, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-22.4950, 0.2250) (-22.2350, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-21.7850, -0.4850) (-21.5250, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-21.7850, 0.2250) (-21.5250, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-21.0750, -0.4850) (-20.8150, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-21.0750, 0.2250) (-20.8150, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-20.3650, -0.4850) (-20.1050, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-20.3650, 0.2250) (-20.1050, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-19.6550, -0.4850) (-19.3950, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-19.6550, 0.2250) (-19.3950, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-18.9450, -0.4850) (-18.6850, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-18.9450, 0.2250) (-18.6850, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-18.2350, -0.4850) (-17.9750, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-18.2350, 0.2250) (-17.9750, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-17.5250, -0.4850) (-17.2650, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-17.5250, 0.2250) (-17.2650, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-16.8150, -0.4850) (-16.5550, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-16.8150, 0.2250) (-16.5550, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-16.1050, -0.4850) (-15.8450, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-16.1050, 0.2250) (-15.8450, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-15.3950, -0.4850) (-15.1350, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-15.3950, 0.2250) (-15.1350, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-14.6850, -0.4850) (-14.4250, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-14.6850, 0.2250) (-14.4250, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-13.9750, -0.4850) (-13.7150, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-13.9750, 0.2250) (-13.7150, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-13.2650, -0.4850) (-13.0050, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-13.2650, 0.2250) (-13.0050, 0.4850)

M5_M4_CDNS_4066195314556\$1 (-12.5550, -0.4850) (-12.2950, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-12.5550, 0.2250) (-12.2950, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-11.8450, -0.4850) (-11.5850, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-11.8450, 0.2250) (-11.5850, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-11.1350, -0.4850) (-10.8750, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-11.1350, 0.2250) (-10.8750, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-10.4250, -0.4850) (-10.1650, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-10.4250, 0.2250) (-10.1650, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-9.7150, -0.4850) (-9.4550, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-9.7150, 0.2250) (-9.4550, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-9.0050, -0.4850) (-8.7450, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-9.0050, 0.2250) (-8.7450, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-8.2950, -0.4850) (-8.0350, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-8.2950, 0.2250) (-8.0350, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-7.5850, -0.4850) (-7.3250, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-7.5850, 0.2250) (-7.3250, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-6.8750, -0.4850) (-6.6150, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-6.8750, 0.2250) (-6.6150, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-6.1650, -0.4850) (-5.9050, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-6.1650, 0.2250) (-5.9050, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-5.4550, -0.4850) (-5.1950, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-5.4550, 0.2250) (-5.1950, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-4.7450, -0.4850) (-4.4850, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-4.7450, 0.2250) (-4.4850, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-4.0350, -0.4850) (-3.7750, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-4.0350, 0.2250) (-3.7750, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-3.3250, -0.4850) (-3.0650, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-3.3250, 0.2250) (-3.0650, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-2.6150, -0.4850) (-2.3550, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-2.6150, 0.2250) (-2.3550, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-1.9050, -0.4850) (-1.6450, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-1.9050, 0.2250) (-1.6450, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-1.1950, -0.4850) (-0.9350, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-1.1950, 0.2250) (-0.9350, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-0.4850, -0.4850) (-0.2250, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-0.4850, 0.2250) (-0.2250, 0.4850)
M5_M4_CDNS_4066195314556\$1 (0.2250, -0.4850) (0.4850, -0.2250)
M5_M4_CDNS_4066195314556\$1 (0.2250, 0.2250) (0.4850, 0.4850)
M5_M4_CDNS_4066195314556\$1 (0.9350, -0.4850) (1.1950, -0.2250)
M5_M4_CDNS_4066195314556\$1 (0.9350, 0.2250) (1.1950, 0.4850)
M5_M4_CDNS_4066195314556\$1 (1.6450, -0.4850) (1.9050, -0.2250)
M5_M4_CDNS_4066195314556\$1 (1.6450, 0.2250) (1.9050, 0.4850)
M5_M4_CDNS_4066195314556\$1 (2.3550, -0.4850) (2.6150, -0.2250)
M5_M4_CDNS_4066195314556\$1 (2.3550, 0.2250) (2.6150, 0.4850)

M5_M4_CDNS_4066195314556\$1 (3.0650, -0.4850) (3.3250, -0.2250)
M5_M4_CDNS_4066195314556\$1 (3.0650, 0.2250) (3.3250, 0.4850)
M5_M4_CDNS_4066195314556\$1 (3.7750, -0.4850) (4.0350, -0.2250)
M5_M4_CDNS_4066195314556\$1 (3.7750, 0.2250) (4.0350, 0.4850)
M5_M4_CDNS_4066195314556\$1 (4.4850, -0.4850) (4.7450, -0.2250)
M5_M4_CDNS_4066195314556\$1 (4.4850, 0.2250) (4.7450, 0.4850)
M5_M4_CDNS_4066195314556\$1 (5.1950, -0.4850) (5.4550, -0.2250)
M5_M4_CDNS_4066195314556\$1 (5.1950, 0.2250) (5.4550, 0.4850)

CUP.7_Via2 : CUP.7c Vias shall be in the form of cluster or arrays
(<=3x3). Sea of via (> 3x3 array) is not allowed.
CUP.7d Min Via2 space in via arrays = 0.3
CUP.7e Min space between via arrays = 0.36

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:3095:not_rectangle_spacing1

WARNING: The error count of 280 for this check exceeds the limit set in
the runset. Details only available for the first 100.

Structure (lower left x, y) (upper right x, y)

Bondpad_5LM\$1 (44.4050, 2.3500) (44.6650, 2.6100)
Bondpad_5LM\$1 (8.4300, 2.3500) (8.6900, 2.6100)
Bondpad_5LM\$1 (4.4250, 2.3500) (4.6850, 2.6100)
Bondpad_5LM\$1 (6.4300, 2.3500) (6.6900, 2.6100)
Bondpad_5LM\$1 (10.4150, 2.3500) (10.6750, 2.6100)
Bondpad_5LM\$1 (12.4000, 2.3500) (12.6600, 2.6100)
Bondpad_5LM\$1 (14.4200, 2.3500) (14.6800, 2.6100)
Bondpad_5LM\$1 (24.4100, 2.3500) (24.6700, 2.6100)
Bondpad_5LM\$1 (22.4100, 2.3500) (22.6700, 2.6100)
Bondpad_5LM\$1 (20.3850, 2.3500) (20.6450, 2.6100)
Bondpad_5LM\$1 (18.4000, 2.3500) (18.6600, 2.6100)
Bondpad_5LM\$1 (26.4350, 2.3500) (26.6950, 2.6100)
Bondpad_5LM\$1 (16.4000, 2.3500) (16.6600, 2.6100)
Bondpad_5LM\$1 (60.4250, 2.3500) (60.6850, 2.6100)
Bondpad_5LM\$1 (58.4000, 2.3500) (58.6600, 2.6100)
Bondpad_5LM\$1 (56.4000, 2.3500) (56.6600, 2.6100)
Bondpad_5LM\$1 (54.3750, 2.3500) (54.6350, 2.6100)
Bondpad_5LM\$1 (52.3900, 2.3500) (52.6500, 2.6100)
Bondpad_5LM\$1 (50.3900, 2.3500) (50.6500, 2.6100)

Bondpad_5LM\$1 (48.4100, 2.3500) (48.6700, 2.6100)
Bondpad_5LM\$1 (28.4200, 2.3500) (28.6800, 2.6100)
Bondpad_5LM\$1 (42.4200, 2.3500) (42.6800, 2.6100)
Bondpad_5LM\$1 (40.4200, 2.3500) (40.6800, 2.6100)
Bondpad_5LM\$1 (38.4150, 2.3500) (38.6750, 2.6100)
Bondpad_5LM\$1 (36.4450, 2.3500) (36.7050, 2.6100)
Bondpad_5LM\$1 (34.4300, 2.3500) (34.6900, 2.6100)
Bondpad_5LM\$1 (32.4200, 2.3500) (32.6800, 2.6100)
Bondpad_5LM\$1 (30.4050, 2.3500) (30.6650, 2.6100)
Bondpad_5LM\$1 (46.3900, 2.3500) (46.6500, 2.6100)
Bondpad_5LM\$1 (43.6950, 2.3500) (43.9550, 2.6100)
Bondpad_5LM\$1 (7.7200, 2.3500) (7.9800, 2.6100)
Bondpad_5LM\$1 (3.7150, 2.3500) (3.9750, 2.6100)
Bondpad_5LM\$1 (5.7200, 2.3500) (5.9800, 2.6100)
Bondpad_5LM\$1 (9.7050, 2.3500) (9.9650, 2.6100)
Bondpad_5LM\$1 (11.6900, 2.3500) (11.9500, 2.6100)
Bondpad_5LM\$1 (13.7100, 2.3500) (13.9700, 2.6100)
Bondpad_5LM\$1 (23.7000, 2.3500) (23.9600, 2.6100)
Bondpad_5LM\$1 (21.7000, 2.3500) (21.9600, 2.6100)
Bondpad_5LM\$1 (19.6750, 2.3500) (19.9350, 2.6100)
Bondpad_5LM\$1 (17.6900, 2.3500) (17.9500, 2.6100)
Bondpad_5LM\$1 (25.7250, 2.3500) (25.9850, 2.6100)
Bondpad_5LM\$1 (15.6900, 2.3500) (15.9500, 2.6100)
Bondpad_5LM\$1 (59.7150, 2.3500) (59.9750, 2.6100)
Bondpad_5LM\$1 (57.6900, 2.3500) (57.9500, 2.6100)
Bondpad_5LM\$1 (55.6900, 2.3500) (55.9500, 2.6100)
Bondpad_5LM\$1 (53.6650, 2.3500) (53.9250, 2.6100)
Bondpad_5LM\$1 (51.6800, 2.3500) (51.9400, 2.6100)
Bondpad_5LM\$1 (49.6800, 2.3500) (49.9400, 2.6100)
Bondpad_5LM\$1 (47.7000, 2.3500) (47.9600, 2.6100)
Bondpad_5LM\$1 (27.7100, 2.3500) (27.9700, 2.6100)
Bondpad_5LM\$1 (41.7100, 2.3500) (41.9700, 2.6100)
Bondpad_5LM\$1 (39.7100, 2.3500) (39.9700, 2.6100)
Bondpad_5LM\$1 (37.7050, 2.3500) (37.9650, 2.6100)
Bondpad_5LM\$1 (35.7350, 2.3500) (35.9950, 2.6100)
Bondpad_5LM\$1 (33.7200, 2.3500) (33.9800, 2.6100)
Bondpad_5LM\$1 (31.7100, 2.3500) (31.9700, 2.6100)
Bondpad_5LM\$1 (29.6950, 2.3500) (29.9550, 2.6100)
Bondpad_5LM\$1 (45.6800, 2.3500) (45.9400, 2.6100)
Bondpad_5LM\$1 (44.4050, 3.0600) (44.6650, 3.3200)
Bondpad_5LM\$1 (8.4300, 3.0600) (8.6900, 3.3200)
Bondpad_5LM\$1 (4.4250, 3.0600) (4.6850, 3.3200)
Bondpad_5LM\$1 (6.4300, 3.0600) (6.6900, 3.3200)
Bondpad_5LM\$1 (10.4150, 3.0600) (10.6750, 3.3200)

Bondpad_5LM\$1	(12.4000, 3.0600)	(12.6600, 3.3200)
Bondpad_5LM\$1	(14.4200, 3.0600)	(14.6800, 3.3200)
Bondpad_5LM\$1	(24.4100, 3.0600)	(24.6700, 3.3200)
Bondpad_5LM\$1	(22.4100, 3.0600)	(22.6700, 3.3200)
Bondpad_5LM\$1	(20.3850, 3.0600)	(20.6450, 3.3200)
Bondpad_5LM\$1	(18.4000, 3.0600)	(18.6600, 3.3200)
Bondpad_5LM\$1	(26.4350, 3.0600)	(26.6950, 3.3200)
Bondpad_5LM\$1	(16.4000, 3.0600)	(16.6600, 3.3200)
Bondpad_5LM\$1	(60.4250, 3.0600)	(60.6850, 3.3200)
Bondpad_5LM\$1	(58.4000, 3.0600)	(58.6600, 3.3200)
Bondpad_5LM\$1	(56.4000, 3.0600)	(56.6600, 3.3200)
Bondpad_5LM\$1	(54.3750, 3.0600)	(54.6350, 3.3200)
Bondpad_5LM\$1	(52.3900, 3.0600)	(52.6500, 3.3200)
Bondpad_5LM\$1	(50.3900, 3.0600)	(50.6500, 3.3200)
Bondpad_5LM\$1	(48.4100, 3.0600)	(48.6700, 3.3200)
Bondpad_5LM\$1	(28.4200, 3.0600)	(28.6800, 3.3200)
Bondpad_5LM\$1	(42.4200, 3.0600)	(42.6800, 3.3200)
Bondpad_5LM\$1	(40.4200, 3.0600)	(40.6800, 3.3200)
Bondpad_5LM\$1	(38.4150, 3.0600)	(38.6750, 3.3200)
Bondpad_5LM\$1	(36.4450, 3.0600)	(36.7050, 3.3200)
Bondpad_5LM\$1	(34.4300, 3.0600)	(34.6900, 3.3200)
Bondpad_5LM\$1	(32.4200, 3.0600)	(32.6800, 3.3200)
Bondpad_5LM\$1	(30.4050, 3.0600)	(30.6650, 3.3200)
Bondpad_5LM\$1	(46.3900, 3.0600)	(46.6500, 3.3200)
Bondpad_5LM\$1	(43.6950, 3.0600)	(43.9550, 3.3200)
Bondpad_5LM\$1	(7.7200, 3.0600)	(7.9800, 3.3200)
Bondpad_5LM\$1	(3.7150, 3.0600)	(3.9750, 3.3200)
Bondpad_5LM\$1	(5.7200, 3.0600)	(5.9800, 3.3200)
Bondpad_5LM\$1	(9.7050, 3.0600)	(9.9650, 3.3200)
Bondpad_5LM\$1	(11.6900, 3.0600)	(11.9500, 3.3200)
Bondpad_5LM\$1	(13.7100, 3.0600)	(13.9700, 3.3200)
Bondpad_5LM\$1	(23.7000, 3.0600)	(23.9600, 3.3200)
Bondpad_5LM\$1	(21.7000, 3.0600)	(21.9600, 3.3200)
Bondpad_5LM\$1	(19.6750, 3.0600)	(19.9350, 3.3200)
Bondpad_5LM\$1	(17.6900, 3.0600)	(17.9500, 3.3200)
Bondpad_5LM\$1	(25.7250, 3.0600)	(25.9850, 3.3200)
Bondpad_5LM\$1	(15.6900, 3.0600)	(15.9500, 3.3200)

CUP.7_Via3 : CUP.7c Vias shall be in the form of cluster or arrays
(<=3x3). Sea of via (> 3x3 array) is not allowed.

CUP.7d Min Via3 space in via arrays = 0.3

CUP.7e Min space between via arrays = 0.36

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:3080:not_rectangle_spacing1

WARNING: The error count of 168 for this check exceeds the limit set in
the runset. Details only available for the first 100.

Structure (lower left x, y) (upper right x, y)

M4_M3_CDNS_4066195314551\$1 (-29.5950, -0.4850) (-29.3350, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-29.5950, 0.2250) (-29.3350, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-28.8850, -0.4850) (-28.6250, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-28.8850, 0.2250) (-28.6250, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-28.1750, -0.4850) (-27.9150, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-28.1750, 0.2250) (-27.9150, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-27.4650, -0.4850) (-27.2050, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-27.4650, 0.2250) (-27.2050, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-26.7550, -0.4850) (-26.4950, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-26.7550, 0.2250) (-26.4950, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-26.0450, -0.4850) (-25.7850, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-26.0450, 0.2250) (-25.7850, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-25.3350, -0.4850) (-25.0750, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-25.3350, 0.2250) (-25.0750, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-24.6250, -0.4850) (-24.3650, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-24.6250, 0.2250) (-24.3650, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-23.9150, -0.4850) (-23.6550, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-23.9150, 0.2250) (-23.6550, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-23.2050, -0.4850) (-22.9450, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-23.2050, 0.2250) (-22.9450, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-22.4950, -0.4850) (-22.2350, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-22.4950, 0.2250) (-22.2350, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-21.7850, -0.4850) (-21.5250, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-21.7850, 0.2250) (-21.5250, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-21.0750, -0.4850) (-20.8150, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-21.0750, 0.2250) (-20.8150, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-20.3650, -0.4850) (-20.1050, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-20.3650, 0.2250) (-20.1050, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-19.6550, -0.4850) (-19.3950, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-19.6550, 0.2250) (-19.3950, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-18.9450, -0.4850) (-18.6850, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-18.9450, 0.2250) (-18.6850, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-18.2350, -0.4850) (-17.9750, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-18.2350, 0.2250) (-17.9750, 0.4850)

M4_M3_CDNS_4066195314551\$1 (-17.5250, -0.4850) (-17.2650, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-17.5250, 0.2250) (-17.2650, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-16.8150, -0.4850) (-16.5550, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-16.8150, 0.2250) (-16.5550, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-16.1050, -0.4850) (-15.8450, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-16.1050, 0.2250) (-15.8450, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-15.3950, -0.4850) (-15.1350, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-15.3950, 0.2250) (-15.1350, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-14.6850, -0.4850) (-14.4250, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-14.6850, 0.2250) (-14.4250, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-13.9750, -0.4850) (-13.7150, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-13.9750, 0.2250) (-13.7150, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-13.2650, -0.4850) (-13.0050, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-13.2650, 0.2250) (-13.0050, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-12.5550, -0.4850) (-12.2950, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-12.5550, 0.2250) (-12.2950, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-11.8450, -0.4850) (-11.5850, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-11.8450, 0.2250) (-11.5850, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-11.1350, -0.4850) (-10.8750, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-11.1350, 0.2250) (-10.8750, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-10.4250, -0.4850) (-10.1650, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-10.4250, 0.2250) (-10.1650, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-9.7150, -0.4850) (-9.4550, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-9.7150, 0.2250) (-9.4550, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-9.0050, -0.4850) (-8.7450, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-9.0050, 0.2250) (-8.7450, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-8.2950, -0.4850) (-8.0350, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-8.2950, 0.2250) (-8.0350, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-7.5850, -0.4850) (-7.3250, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-7.5850, 0.2250) (-7.3250, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-6.8750, -0.4850) (-6.6150, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-6.8750, 0.2250) (-6.6150, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-6.1650, -0.4850) (-5.9050, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-6.1650, 0.2250) (-5.9050, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-5.4550, -0.4850) (-5.1950, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-5.4550, 0.2250) (-5.1950, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-4.7450, -0.4850) (-4.4850, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-4.7450, 0.2250) (-4.4850, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-4.0350, -0.4850) (-3.7750, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-4.0350, 0.2250) (-3.7750, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-3.3250, -0.4850) (-3.0650, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-3.3250, 0.2250) (-3.0650, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-2.6150, -0.4850) (-2.3550, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-2.6150, 0.2250) (-2.3550, 0.4850)

M4_M3_CDNS_4066195314551\$1 (-1.9050, -0.4850) (-1.6450, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-1.9050, 0.2250) (-1.6450, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-1.1950, -0.4850) (-0.9350, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-1.1950, 0.2250) (-0.9350, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-0.4850, -0.4850) (-0.2250, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-0.4850, 0.2250) (-0.2250, 0.4850)
M4_M3_CDNS_4066195314551\$1 (0.2250, -0.4850) (0.4850, -0.2250)
M4_M3_CDNS_4066195314551\$1 (0.2250, 0.2250) (0.4850, 0.4850)
M4_M3_CDNS_4066195314551\$1 (0.9350, -0.4850) (1.1950, -0.2250)
M4_M3_CDNS_4066195314551\$1 (0.9350, 0.2250) (1.1950, 0.4850)
M4_M3_CDNS_4066195314551\$1 (1.6450, -0.4850) (1.9050, -0.2250)
M4_M3_CDNS_4066195314551\$1 (1.6450, 0.2250) (1.9050, 0.4850)
M4_M3_CDNS_4066195314551\$1 (2.3550, -0.4850) (2.6150, -0.2250)
M4_M3_CDNS_4066195314551\$1 (2.3550, 0.2250) (2.6150, 0.4850)
M4_M3_CDNS_4066195314551\$1 (3.0650, -0.4850) (3.3250, -0.2250)
M4_M3_CDNS_4066195314551\$1 (3.0650, 0.2250) (3.3250, 0.4850)
M4_M3_CDNS_4066195314551\$1 (3.7750, -0.4850) (4.0350, -0.2250)
M4_M3_CDNS_4066195314551\$1 (3.7750, 0.2250) (4.0350, 0.4850)
M4_M3_CDNS_4066195314551\$1 (4.4850, -0.4850) (4.7450, -0.2250)
M4_M3_CDNS_4066195314551\$1 (4.4850, 0.2250) (4.7450, 0.4850)
M4_M3_CDNS_4066195314551\$1 (5.1950, -0.4850) (5.4550, -0.2250)
M4_M3_CDNS_4066195314551\$1 (5.1950, 0.2250) (5.4550, 0.4850)

CUP.7_Via4 : CUP.7c Vias shall be in the form of cluster or arrays
(<=3x3). Sea of via (> 3x3 array) is not allowed.
CUP.7d Min Via4 space in via arrays = 0.3
CUP.7e Min space between via arrays = 0.36

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:3065:not_rectangle_spacing1

WARNING: The error count of 168 for this check exceeds the limit set in
the runset. Details only available for the first 100.

Structure (lower left x, y) (upper right x, y)

M5_M4_CDNS_4066195314556\$1 (-29.5950, -0.4850) (-29.3350, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-29.5950, 0.2250) (-29.3350, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-28.8850, -0.4850) (-28.6250, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-28.8850, 0.2250) (-28.6250, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-28.1750, -0.4850) (-27.9150, -0.2250)

M5_M4_CDNS_4066195314556\$1 (-28.1750, 0.2250) (-27.9150, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-27.4650, -0.4850) (-27.2050, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-27.4650, 0.2250) (-27.2050, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-26.7550, -0.4850) (-26.4950, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-26.7550, 0.2250) (-26.4950, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-26.0450, -0.4850) (-25.7850, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-26.0450, 0.2250) (-25.7850, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-25.3350, -0.4850) (-25.0750, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-25.3350, 0.2250) (-25.0750, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-24.6250, -0.4850) (-24.3650, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-24.6250, 0.2250) (-24.3650, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-23.9150, -0.4850) (-23.6550, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-23.9150, 0.2250) (-23.6550, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-23.2050, -0.4850) (-22.9450, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-23.2050, 0.2250) (-22.9450, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-22.4950, -0.4850) (-22.2350, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-22.4950, 0.2250) (-22.2350, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-21.7850, -0.4850) (-21.5250, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-21.7850, 0.2250) (-21.5250, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-21.0750, -0.4850) (-20.8150, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-21.0750, 0.2250) (-20.8150, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-20.3650, -0.4850) (-20.1050, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-20.3650, 0.2250) (-20.1050, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-19.6550, -0.4850) (-19.3950, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-19.6550, 0.2250) (-19.3950, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-18.9450, -0.4850) (-18.6850, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-18.9450, 0.2250) (-18.6850, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-18.2350, -0.4850) (-17.9750, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-18.2350, 0.2250) (-17.9750, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-17.5250, -0.4850) (-17.2650, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-17.5250, 0.2250) (-17.2650, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-16.8150, -0.4850) (-16.5550, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-16.8150, 0.2250) (-16.5550, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-16.1050, -0.4850) (-15.8450, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-16.1050, 0.2250) (-15.8450, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-15.3950, -0.4850) (-15.1350, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-15.3950, 0.2250) (-15.1350, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-14.6850, -0.4850) (-14.4250, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-14.6850, 0.2250) (-14.4250, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-13.9750, -0.4850) (-13.7150, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-13.9750, 0.2250) (-13.7150, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-13.2650, -0.4850) (-13.0050, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-13.2650, 0.2250) (-13.0050, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-12.5550, -0.4850) (-12.2950, -0.2250)

M5_M4_CDNS_4066195314556\$1 (-12.5550, 0.2250) (-12.2950, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-11.8450, -0.4850) (-11.5850, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-11.8450, 0.2250) (-11.5850, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-11.1350, -0.4850) (-10.8750, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-11.1350, 0.2250) (-10.8750, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-10.4250, -0.4850) (-10.1650, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-10.4250, 0.2250) (-10.1650, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-9.7150, -0.4850) (-9.4550, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-9.7150, 0.2250) (-9.4550, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-9.0050, -0.4850) (-8.7450, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-9.0050, 0.2250) (-8.7450, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-8.2950, -0.4850) (-8.0350, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-8.2950, 0.2250) (-8.0350, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-7.5850, -0.4850) (-7.3250, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-7.5850, 0.2250) (-7.3250, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-6.8750, -0.4850) (-6.6150, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-6.8750, 0.2250) (-6.6150, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-6.1650, -0.4850) (-5.9050, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-6.1650, 0.2250) (-5.9050, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-5.4550, -0.4850) (-5.1950, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-5.4550, 0.2250) (-5.1950, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-4.7450, -0.4850) (-4.4850, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-4.7450, 0.2250) (-4.4850, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-4.0350, -0.4850) (-3.7750, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-4.0350, 0.2250) (-3.7750, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-3.3250, -0.4850) (-3.0650, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-3.3250, 0.2250) (-3.0650, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-2.6150, -0.4850) (-2.3550, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-2.6150, 0.2250) (-2.3550, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-1.9050, -0.4850) (-1.6450, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-1.9050, 0.2250) (-1.6450, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-1.1950, -0.4850) (-0.9350, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-1.1950, 0.2250) (-0.9350, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-0.4850, -0.4850) (-0.2250, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-0.4850, 0.2250) (-0.2250, 0.4850)
M5_M4_CDNS_4066195314556\$1 (0.2250, -0.4850) (0.4850, -0.2250)
M5_M4_CDNS_4066195314556\$1 (0.2250, 0.2250) (0.4850, 0.4850)
M5_M4_CDNS_4066195314556\$1 (0.9350, -0.4850) (1.1950, -0.2250)
M5_M4_CDNS_4066195314556\$1 (0.9350, 0.2250) (1.1950, 0.4850)
M5_M4_CDNS_4066195314556\$1 (1.6450, -0.4850) (1.9050, -0.2250)
M5_M4_CDNS_4066195314556\$1 (1.6450, 0.2250) (1.9050, 0.4850)
M5_M4_CDNS_4066195314556\$1 (2.3550, -0.4850) (2.6150, -0.2250)
M5_M4_CDNS_4066195314556\$1 (2.3550, 0.2250) (2.6150, 0.4850)
M5_M4_CDNS_4066195314556\$1 (3.0650, -0.4850) (3.3250, -0.2250)

M5_M4_CDNS_4066195314556\$1 (3.0650, 0.2250) (3.3250, 0.4850)
M5_M4_CDNS_4066195314556\$1 (3.7750, -0.4850) (4.0350, -0.2250)
M5_M4_CDNS_4066195314556\$1 (3.7750, 0.2250) (4.0350, 0.4850)
M5_M4_CDNS_4066195314556\$1 (4.4850, -0.4850) (4.7450, -0.2250)
M5_M4_CDNS_4066195314556\$1 (4.4850, 0.2250) (4.7450, 0.4850)
M5_M4_CDNS_4066195314556\$1 (5.1950, -0.4850) (5.4550, -0.2250)
M5_M4_CDNS_4066195314556\$1 (5.1950, 0.2250) (5.4550, 0.4850)

CUP.8 : Top_Via-1 directly underneath the Pad mask is not Allowed

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:3121:and

WARNING: The error count of 101 for this check exceeds the limit set in
the runset. Details only available for the first 100.

Check was stopped early because error limit was reached.

Structure (lower left x, y) (upper right x, y)

M4_M3_CDNS_4066195314551\$1 (-29.5950, -0.4850) (-29.3350, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-29.5950, 0.2250) (-29.3350, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-28.8850, -0.4850) (-28.6250, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-28.8850, 0.2250) (-28.6250, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-28.1750, -0.4850) (-27.9150, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-28.1750, 0.2250) (-27.9150, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-27.4650, -0.4850) (-27.2050, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-27.4650, 0.2250) (-27.2050, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-26.7550, -0.4850) (-26.4950, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-26.7550, 0.2250) (-26.4950, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-26.0450, -0.4850) (-25.7850, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-26.0450, 0.2250) (-25.7850, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-25.3350, -0.4850) (-25.0750, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-25.3350, 0.2250) (-25.0750, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-24.6250, -0.4850) (-24.3650, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-24.6250, 0.2250) (-24.3650, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-23.9150, -0.4850) (-23.6550, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-23.9150, 0.2250) (-23.6550, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-23.2050, -0.4850) (-22.9450, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-23.2050, 0.2250) (-22.9450, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-22.4950, -0.4850) (-22.2350, -0.2250)

M4_M3_CDNS_4066195314551\$1 (-22.4950, 0.2250) (-22.2350, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-21.7850, -0.4850) (-21.5250, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-21.7850, 0.2250) (-21.5250, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-21.0750, -0.4850) (-20.8150, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-21.0750, 0.2250) (-20.8150, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-20.3650, -0.4850) (-20.1050, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-20.3650, 0.2250) (-20.1050, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-19.6550, -0.4850) (-19.3950, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-19.6550, 0.2250) (-19.3950, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-18.9450, -0.4850) (-18.6850, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-18.9450, 0.2250) (-18.6850, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-18.2350, -0.4850) (-17.9750, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-18.2350, 0.2250) (-17.9750, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-17.5250, -0.4850) (-17.2650, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-17.5250, 0.2250) (-17.2650, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-16.8150, -0.4850) (-16.5550, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-16.8150, 0.2250) (-16.5550, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-16.1050, -0.4850) (-15.8450, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-16.1050, 0.2250) (-15.8450, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-15.3950, -0.4850) (-15.1350, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-15.3950, 0.2250) (-15.1350, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-14.6850, -0.4850) (-14.4250, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-14.6850, 0.2250) (-14.4250, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-13.9750, -0.4850) (-13.7150, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-13.9750, 0.2250) (-13.7150, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-13.2650, -0.4850) (-13.0050, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-13.2650, 0.2250) (-13.0050, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-12.5550, -0.4850) (-12.2950, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-12.5550, 0.2250) (-12.2950, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-11.8450, -0.4850) (-11.5850, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-11.8450, 0.2250) (-11.5850, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-11.1350, -0.4850) (-10.8750, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-11.1350, 0.2250) (-10.8750, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-10.4250, -0.4850) (-10.1650, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-10.4250, 0.2250) (-10.1650, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-9.7150, -0.4850) (-9.4550, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-9.7150, 0.2250) (-9.4550, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-9.0050, -0.4850) (-8.7450, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-9.0050, 0.2250) (-8.7450, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-8.2950, -0.4850) (-8.0350, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-8.2950, 0.2250) (-8.0350, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-7.5850, -0.4850) (-7.3250, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-7.5850, 0.2250) (-7.3250, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-6.8750, -0.4850) (-6.6150, -0.2250)

M4_M3_CDNS_4066195314551\$1 (-6.8750, 0.2250) (-6.6150, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-6.1650, -0.4850) (-5.9050, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-6.1650, 0.2250) (-5.9050, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-5.4550, -0.4850) (-5.1950, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-5.4550, 0.2250) (-5.1950, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-4.7450, -0.4850) (-4.4850, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-4.7450, 0.2250) (-4.4850, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-4.0350, -0.4850) (-3.7750, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-4.0350, 0.2250) (-3.7750, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-3.3250, -0.4850) (-3.0650, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-3.3250, 0.2250) (-3.0650, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-2.6150, -0.4850) (-2.3550, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-2.6150, 0.2250) (-2.3550, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-1.9050, -0.4850) (-1.6450, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-1.9050, 0.2250) (-1.6450, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-1.1950, -0.4850) (-0.9350, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-1.1950, 0.2250) (-0.9350, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-0.4850, -0.4850) (-0.2250, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-0.4850, 0.2250) (-0.2250, 0.4850)
M4_M3_CDNS_4066195314551\$1 (0.2250, -0.4850) (0.4850, -0.2250)
M4_M3_CDNS_4066195314551\$1 (0.2250, 0.2250) (0.4850, 0.4850)
M4_M3_CDNS_4066195314551\$1 (0.9350, -0.4850) (1.1950, -0.2250)
M4_M3_CDNS_4066195314551\$1 (0.9350, 0.2250) (1.1950, 0.4850)
M4_M3_CDNS_4066195314551\$1 (1.6450, -0.4850) (1.9050, -0.2250)
M4_M3_CDNS_4066195314551\$1 (1.6450, 0.2250) (1.9050, 0.4850)
M4_M3_CDNS_4066195314551\$1 (2.3550, -0.4850) (2.6150, -0.2250)
M4_M3_CDNS_4066195314551\$1 (2.3550, 0.2250) (2.6150, 0.4850)
M4_M3_CDNS_4066195314551\$1 (3.0650, -0.4850) (3.3250, -0.2250)
M4_M3_CDNS_4066195314551\$1 (3.0650, 0.2250) (3.3250, 0.4850)
M4_M3_CDNS_4066195314551\$1 (3.7750, -0.4850) (4.0350, -0.2250)
M4_M3_CDNS_4066195314551\$1 (3.7750, 0.2250) (4.0350, 0.4850)
M4_M3_CDNS_4066195314551\$1 (4.4850, -0.4850) (4.7450, -0.2250)
M4_M3_CDNS_4066195314551\$1 (4.4850, 0.2250) (4.7450, 0.4850)
M4_M3_CDNS_4066195314551\$1 (5.1950, -0.4850) (5.4550, -0.2250)
M4_M3_CDNS_4066195314551\$1 (5.1950, 0.2250) (5.4550, 0.4850)

CUP.9 : 1LM, 2LM and 3LM process not allowed to have CUP for wire
bond case
CUP.1a CUP is not allowed for Wedge-type Wire bond case

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:3140:and

Structure (lower left x, y) (upper right x, y)

Bondpad_5LM\$1 (43.6350, 2.2900) (44.7250, 61.6000)
Bondpad_5LM\$1 (7.6600, 2.2900) (8.7500, 61.6000)
Bondpad_5LM\$1 (3.6550, 2.2900) (4.7450, 61.6000)
Bondpad_5LM\$1 (5.6600, 2.2900) (6.7500, 61.6000)
Bondpad_5LM\$1 (9.6450, 2.2900) (10.7350, 61.6000)
Bondpad_5LM\$1 (11.6300, 2.2900) (12.7200, 61.6000)
Bondpad_5LM\$1 (13.6500, 2.2900) (14.7400, 61.6000)
Bondpad_5LM\$1 (23.6400, 2.2900) (24.7300, 61.6000)
Bondpad_5LM\$1 (21.6400, 2.2900) (22.7300, 61.6000)
Bondpad_5LM\$1 (19.6150, 2.2900) (20.7050, 61.6000)
Bondpad_5LM\$1 (17.6300, 2.2900) (18.7200, 61.6000)
Bondpad_5LM\$1 (25.6650, 2.2900) (26.7550, 61.6000)
Bondpad_5LM\$1 (15.6300, 2.2900) (16.7200, 61.6000)
Bondpad_5LM\$1 (59.6550, 2.2900) (60.7450, 61.6000)
Bondpad_5LM\$1 (57.6300, 2.2900) (58.7200, 61.6000)
Bondpad_5LM\$1 (55.6300, 2.2900) (56.7200, 61.6000)
Bondpad_5LM\$1 (53.6050, 2.2900) (54.6950, 61.6000)
Bondpad_5LM\$1 (51.6200, 2.2900) (52.7100, 61.6000)
Bondpad_5LM\$1 (49.6200, 2.2900) (50.7100, 61.6000)
Bondpad_5LM\$1 (47.6400, 2.2900) (48.7300, 61.6000)
Bondpad_5LM\$1 (27.6500, 2.2900) (28.7400, 61.6000)
Bondpad_5LM\$1 (41.6500, 2.2900) (42.7400, 61.6000)
Bondpad_5LM\$1 (39.6500, 2.2900) (40.7400, 61.6000)
Bondpad_5LM\$1 (37.6450, 2.2900) (38.7350, 61.6000)
Bondpad_5LM\$1 (35.6750, 2.2900) (36.7650, 61.6000)
Bondpad_5LM\$1 (33.6600, 2.2900) (34.7500, 61.6000)
Bondpad_5LM\$1 (31.6500, 2.2900) (32.7400, 61.6000)
Bondpad_5LM\$1 (29.6350, 2.2900) (30.7250, 61.6000)
Bondpad_5LM\$1 (45.6200, 2.2900) (46.7100, 61.6000)
Bondpad_5LM\$1 (31.3400, 2.0000) (33.0400, 62.0000)
Bondpad_5LM\$1 (33.3400, 2.0000) (35.0400, 62.0000)
Bondpad_5LM\$1 (35.3400, 2.0000) (37.0400, 62.0000)
Bondpad_5LM\$1 (37.3400, 2.0000) (39.0400, 62.0000)
Bondpad_5LM\$1 (39.3400, 2.0000) (41.0400, 62.0000)
Bondpad_5LM\$1 (41.3400, 2.0000) (43.0400, 62.0000)
Bondpad_5LM\$1 (43.3400, 2.0000) (45.0400, 62.0000)
Bondpad_5LM\$1 (45.3400, 2.0000) (47.0400, 62.0000)
Bondpad_5LM\$1 (47.3400, 2.0000) (49.0400, 62.0000)
Bondpad_5LM\$1 (49.3400, 2.0000) (51.0400, 62.0000)

Bondpad_5LM\$1 (51.3400, 2.0000) (53.0400, 62.0000)
Bondpad_5LM\$1 (53.3400, 2.0000) (55.0400, 62.0000)
Bondpad_5LM\$1 (55.3400, 2.0000) (57.0400, 62.0000)
Bondpad_5LM\$1 (57.3400, 2.0000) (59.0400, 62.0000)
Bondpad_5LM\$1 (59.3400, 2.0000) (61.0400, 62.0000)
Bondpad_5LM\$1 (3.3400, 2.0000) (5.0400, 62.0000)
Bondpad_5LM\$1 (5.3400, 2.0000) (7.0400, 62.0000)
Bondpad_5LM\$1 (7.3400, 2.0000) (9.0400, 62.0000)
Bondpad_5LM\$1 (9.3400, 2.0000) (11.0400, 62.0000)
Bondpad_5LM\$1 (11.3400, 2.0000) (13.0400, 62.0000)
Bondpad_5LM\$1 (13.3400, 2.0000) (15.0400, 62.0000)
Bondpad_5LM\$1 (15.3400, 2.0000) (17.0400, 62.0000)
Bondpad_5LM\$1 (17.3400, 2.0000) (19.0400, 62.0000)
Bondpad_5LM\$1 (19.3400, 2.0000) (21.0400, 62.0000)
Bondpad_5LM\$1 (21.3400, 2.0000) (23.0400, 62.0000)
Bondpad_5LM\$1 (23.3400, 2.0000) (25.0400, 62.0000)
Bondpad_5LM\$1 (25.3400, 2.0000) (27.0400, 62.0000)
Bondpad_5LM\$1 (27.3400, 2.0000) (29.0400, 62.0000)
Bondpad_5LM\$1 (29.3400, 2.0000) (31.0400, 62.0000)

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:3141:and

WARNING: The error count of 213 for this check exceeds the limit set in
the runset. Details only available for the first 100.

Check was stopped early because error limit was reached.

Structure (lower left x, y) (upper right x, y)

Bondpad_5LM\$1 (44.4050, 2.3500) (44.6650, 2.6100)
Bondpad_5LM\$1 (8.4300, 2.3500) (8.6900, 2.6100)
Bondpad_5LM\$1 (4.4250, 2.3500) (4.6850, 2.6100)
Bondpad_5LM\$1 (6.4300, 2.3500) (6.6900, 2.6100)
Bondpad_5LM\$1 (10.4150, 2.3500) (10.6750, 2.6100)
Bondpad_5LM\$1 (12.4000, 2.3500) (12.6600, 2.6100)
Bondpad_5LM\$1 (14.4200, 2.3500) (14.6800, 2.6100)
Bondpad_5LM\$1 (24.4100, 2.3500) (24.6700, 2.6100)
Bondpad_5LM\$1 (22.4100, 2.3500) (22.6700, 2.6100)
Bondpad_5LM\$1 (20.3850, 2.3500) (20.6450, 2.6100)
Bondpad_5LM\$1 (18.4000, 2.3500) (18.6600, 2.6100)
Bondpad_5LM\$1 (26.4350, 2.3500) (26.6950, 2.6100)
Bondpad_5LM\$1 (16.4000, 2.3500) (16.6600, 2.6100)
Bondpad_5LM\$1 (60.4250, 2.3500) (60.6850, 2.6100)

Bondpad_5LM\$1 (58.4000, 2.3500) (58.6600, 2.6100)
Bondpad_5LM\$1 (56.4000, 2.3500) (56.6600, 2.6100)
Bondpad_5LM\$1 (54.3750, 2.3500) (54.6350, 2.6100)
Bondpad_5LM\$1 (52.3900, 2.3500) (52.6500, 2.6100)
Bondpad_5LM\$1 (50.3900, 2.3500) (50.6500, 2.6100)
Bondpad_5LM\$1 (48.4100, 2.3500) (48.6700, 2.6100)
Bondpad_5LM\$1 (28.4200, 2.3500) (28.6800, 2.6100)
Bondpad_5LM\$1 (42.4200, 2.3500) (42.6800, 2.6100)
Bondpad_5LM\$1 (40.4200, 2.3500) (40.6800, 2.6100)
Bondpad_5LM\$1 (38.4150, 2.3500) (38.6750, 2.6100)
Bondpad_5LM\$1 (36.4450, 2.3500) (36.7050, 2.6100)
Bondpad_5LM\$1 (34.4300, 2.3500) (34.6900, 2.6100)
Bondpad_5LM\$1 (32.4200, 2.3500) (32.6800, 2.6100)
Bondpad_5LM\$1 (30.4050, 2.3500) (30.6650, 2.6100)
Bondpad_5LM\$1 (46.3900, 2.3500) (46.6500, 2.6100)
Bondpad_5LM\$1 (43.6950, 2.3500) (43.9550, 2.6100)
Bondpad_5LM\$1 (7.7200, 2.3500) (7.9800, 2.6100)
Bondpad_5LM\$1 (3.7150, 2.3500) (3.9750, 2.6100)
Bondpad_5LM\$1 (5.7200, 2.3500) (5.9800, 2.6100)
Bondpad_5LM\$1 (9.7050, 2.3500) (9.9650, 2.6100)
Bondpad_5LM\$1 (11.6900, 2.3500) (11.9500, 2.6100)
Bondpad_5LM\$1 (13.7100, 2.3500) (13.9700, 2.6100)
Bondpad_5LM\$1 (23.7000, 2.3500) (23.9600, 2.6100)
Bondpad_5LM\$1 (21.7000, 2.3500) (21.9600, 2.6100)
Bondpad_5LM\$1 (19.6750, 2.3500) (19.9350, 2.6100)
Bondpad_5LM\$1 (17.6900, 2.3500) (17.9500, 2.6100)
Bondpad_5LM\$1 (25.7250, 2.3500) (25.9850, 2.6100)
Bondpad_5LM\$1 (15.6900, 2.3500) (15.9500, 2.6100)
Bondpad_5LM\$1 (59.7150, 2.3500) (59.9750, 2.6100)
Bondpad_5LM\$1 (57.6900, 2.3500) (57.9500, 2.6100)
Bondpad_5LM\$1 (55.6900, 2.3500) (55.9500, 2.6100)
Bondpad_5LM\$1 (53.6650, 2.3500) (53.9250, 2.6100)
Bondpad_5LM\$1 (51.6800, 2.3500) (51.9400, 2.6100)
Bondpad_5LM\$1 (49.6800, 2.3500) (49.9400, 2.6100)
Bondpad_5LM\$1 (47.7000, 2.3500) (47.9600, 2.6100)
Bondpad_5LM\$1 (27.7100, 2.3500) (27.9700, 2.6100)
Bondpad_5LM\$1 (41.7100, 2.3500) (41.9700, 2.6100)
Bondpad_5LM\$1 (39.7100, 2.3500) (39.9700, 2.6100)
Bondpad_5LM\$1 (37.7050, 2.3500) (37.9650, 2.6100)
Bondpad_5LM\$1 (35.7350, 2.3500) (35.9950, 2.6100)
Bondpad_5LM\$1 (33.7200, 2.3500) (33.9800, 2.6100)
Bondpad_5LM\$1 (31.7100, 2.3500) (31.9700, 2.6100)
Bondpad_5LM\$1 (29.6950, 2.3500) (29.9550, 2.6100)
Bondpad_5LM\$1 (45.6800, 2.3500) (45.9400, 2.6100)

Bondpad_5LM\$1 (44.4050, 3.0600) (44.6650, 3.3200)
Bondpad_5LM\$1 (8.4300, 3.0600) (8.6900, 3.3200)
Bondpad_5LM\$1 (4.4250, 3.0600) (4.6850, 3.3200)
Bondpad_5LM\$1 (6.4300, 3.0600) (6.6900, 3.3200)
Bondpad_5LM\$1 (10.4150, 3.0600) (10.6750, 3.3200)
Bondpad_5LM\$1 (12.4000, 3.0600) (12.6600, 3.3200)
Bondpad_5LM\$1 (14.4200, 3.0600) (14.6800, 3.3200)
Bondpad_5LM\$1 (24.4100, 3.0600) (24.6700, 3.3200)
Bondpad_5LM\$1 (22.4100, 3.0600) (22.6700, 3.3200)
Bondpad_5LM\$1 (20.3850, 3.0600) (20.6450, 3.3200)
Bondpad_5LM\$1 (18.4000, 3.0600) (18.6600, 3.3200)
Bondpad_5LM\$1 (26.4350, 3.0600) (26.6950, 3.3200)
Bondpad_5LM\$1 (16.4000, 3.0600) (16.6600, 3.3200)
Bondpad_5LM\$1 (60.4250, 3.0600) (60.6850, 3.3200)
Bondpad_5LM\$1 (58.4000, 3.0600) (58.6600, 3.3200)
Bondpad_5LM\$1 (56.4000, 3.0600) (56.6600, 3.3200)
Bondpad_5LM\$1 (54.3750, 3.0600) (54.6350, 3.3200)
Bondpad_5LM\$1 (52.3900, 3.0600) (52.6500, 3.3200)
Bondpad_5LM\$1 (50.3900, 3.0600) (50.6500, 3.3200)
Bondpad_5LM\$1 (48.4100, 3.0600) (48.6700, 3.3200)
Bondpad_5LM\$1 (28.4200, 3.0600) (28.6800, 3.3200)
Bondpad_5LM\$1 (42.4200, 3.0600) (42.6800, 3.3200)
Bondpad_5LM\$1 (40.4200, 3.0600) (40.6800, 3.3200)
Bondpad_5LM\$1 (38.4150, 3.0600) (38.6750, 3.3200)
Bondpad_5LM\$1 (36.4450, 3.0600) (36.7050, 3.3200)
Bondpad_5LM\$1 (34.4300, 3.0600) (34.6900, 3.3200)
Bondpad_5LM\$1 (32.4200, 3.0600) (32.6800, 3.3200)
Bondpad_5LM\$1 (30.4050, 3.0600) (30.6650, 3.3200)
Bondpad_5LM\$1 (46.3900, 3.0600) (46.6500, 3.3200)
Bondpad_5LM\$1 (43.6950, 3.0600) (43.9550, 3.3200)
Bondpad_5LM\$1 (7.7200, 3.0600) (7.9800, 3.3200)
Bondpad_5LM\$1 (3.7150, 3.0600) (3.9750, 3.3200)
Bondpad_5LM\$1 (5.7200, 3.0600) (5.9800, 3.3200)
Bondpad_5LM\$1 (9.7050, 3.0600) (9.9650, 3.3200)
Bondpad_5LM\$1 (11.6900, 3.0600) (11.9500, 3.3200)
Bondpad_5LM\$1 (13.7100, 3.0600) (13.9700, 3.3200)
Bondpad_5LM\$1 (23.7000, 3.0600) (23.9600, 3.3200)
Bondpad_5LM\$1 (21.7000, 3.0600) (21.9600, 3.3200)
Bondpad_5LM\$1 (19.6750, 3.0600) (19.9350, 3.3200)
Bondpad_5LM\$1 (17.6900, 3.0600) (17.9500, 3.3200)
Bondpad_5LM\$1 (25.7250, 3.0600) (25.9850, 3.3200)
Bondpad_5LM\$1 (15.6900, 3.0600) (15.9500, 3.3200)

CUP.9_Wedge_4LM : 9.3 Wedge type wire-bond not allowed to have CUP

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:3146:and

Structure (lower left x, y) (upper right x, y)

Bondpad_5LM\$1 (43.6350, 2.2900) (44.7250, 61.6000)
Bondpad_5LM\$1 (7.6600, 2.2900) (8.7500, 61.6000)
Bondpad_5LM\$1 (3.6550, 2.2900) (4.7450, 61.6000)
Bondpad_5LM\$1 (5.6600, 2.2900) (6.7500, 61.6000)
Bondpad_5LM\$1 (9.6450, 2.2900) (10.7350, 61.6000)
Bondpad_5LM\$1 (11.6300, 2.2900) (12.7200, 61.6000)
Bondpad_5LM\$1 (13.6500, 2.2900) (14.7400, 61.6000)
Bondpad_5LM\$1 (23.6400, 2.2900) (24.7300, 61.6000)
Bondpad_5LM\$1 (21.6400, 2.2900) (22.7300, 61.6000)
Bondpad_5LM\$1 (19.6150, 2.2900) (20.7050, 61.6000)
Bondpad_5LM\$1 (17.6300, 2.2900) (18.7200, 61.6000)
Bondpad_5LM\$1 (25.6650, 2.2900) (26.7550, 61.6000)
Bondpad_5LM\$1 (15.6300, 2.2900) (16.7200, 61.6000)
Bondpad_5LM\$1 (59.6550, 2.2900) (60.7450, 61.6000)
Bondpad_5LM\$1 (57.6300, 2.2900) (58.7200, 61.6000)
Bondpad_5LM\$1 (55.6300, 2.2900) (56.7200, 61.6000)
Bondpad_5LM\$1 (53.6050, 2.2900) (54.6950, 61.6000)
Bondpad_5LM\$1 (51.6200, 2.2900) (52.7100, 61.6000)
Bondpad_5LM\$1 (49.6200, 2.2900) (50.7100, 61.6000)
Bondpad_5LM\$1 (47.6400, 2.2900) (48.7300, 61.6000)
Bondpad_5LM\$1 (27.6500, 2.2900) (28.7400, 61.6000)
Bondpad_5LM\$1 (41.6500, 2.2900) (42.7400, 61.6000)
Bondpad_5LM\$1 (39.6500, 2.2900) (40.7400, 61.6000)
Bondpad_5LM\$1 (37.6450, 2.2900) (38.7350, 61.6000)
Bondpad_5LM\$1 (35.6750, 2.2900) (36.7650, 61.6000)
Bondpad_5LM\$1 (33.6600, 2.2900) (34.7500, 61.6000)
Bondpad_5LM\$1 (31.6500, 2.2900) (32.7400, 61.6000)
Bondpad_5LM\$1 (29.6350, 2.2900) (30.7250, 61.6000)
Bondpad_5LM\$1 (45.6200, 2.2900) (46.7100, 61.6000)
Bondpad_5LM\$1 (2.0000, 2.0000) (62.0000, 62.0000)
M4_M3_CDNS_4066195314551\$1 (-29.6550, -0.5450) (29.6550, 0.5450)

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:3147:and

WARNING: The error count of 101 for this check exceeds the limit set in the runset. Details only available for the first 100.

Check was stopped early because error limit was reached.

```
-----  
Structure          ( lower left x, y ) ( upper right x, y )  
-----  
M4_M3_CDNS_4066195314551$1 (-29.5950, -0.4850) (-29.3350, -0.2250)  
M4_M3_CDNS_4066195314551$1 (-29.5950, 0.2250) (-29.3350, 0.4850)  
M4_M3_CDNS_4066195314551$1 (-28.8850, -0.4850) (-28.6250, -0.2250)  
M4_M3_CDNS_4066195314551$1 (-28.8850, 0.2250) (-28.6250, 0.4850)  
M4_M3_CDNS_4066195314551$1 (-28.1750, -0.4850) (-27.9150, -0.2250)  
M4_M3_CDNS_4066195314551$1 (-28.1750, 0.2250) (-27.9150, 0.4850)  
M4_M3_CDNS_4066195314551$1 (-27.4650, -0.4850) (-27.2050, -0.2250)  
M4_M3_CDNS_4066195314551$1 (-27.4650, 0.2250) (-27.2050, 0.4850)  
M4_M3_CDNS_4066195314551$1 (-26.7550, -0.4850) (-26.4950, -0.2250)  
M4_M3_CDNS_4066195314551$1 (-26.7550, 0.2250) (-26.4950, 0.4850)  
M4_M3_CDNS_4066195314551$1 (-26.0450, -0.4850) (-25.7850, -0.2250)  
M4_M3_CDNS_4066195314551$1 (-26.0450, 0.2250) (-25.7850, 0.4850)  
M4_M3_CDNS_4066195314551$1 (-25.3350, -0.4850) (-25.0750, -0.2250)  
M4_M3_CDNS_4066195314551$1 (-25.3350, 0.2250) (-25.0750, 0.4850)  
M4_M3_CDNS_4066195314551$1 (-24.6250, -0.4850) (-24.3650, -0.2250)  
M4_M3_CDNS_4066195314551$1 (-24.6250, 0.2250) (-24.3650, 0.4850)  
M4_M3_CDNS_4066195314551$1 (-23.9150, -0.4850) (-23.6550, -0.2250)  
M4_M3_CDNS_4066195314551$1 (-23.9150, 0.2250) (-23.6550, 0.4850)  
M4_M3_CDNS_4066195314551$1 (-23.2050, -0.4850) (-22.9450, -0.2250)  
M4_M3_CDNS_4066195314551$1 (-23.2050, 0.2250) (-22.9450, 0.4850)  
M4_M3_CDNS_4066195314551$1 (-22.4950, -0.4850) (-22.2350, -0.2250)  
M4_M3_CDNS_4066195314551$1 (-22.4950, 0.2250) (-22.2350, 0.4850)  
M4_M3_CDNS_4066195314551$1 (-21.7850, -0.4850) (-21.5250, -0.2250)  
M4_M3_CDNS_4066195314551$1 (-21.7850, 0.2250) (-21.5250, 0.4850)  
M4_M3_CDNS_4066195314551$1 (-21.0750, -0.4850) (-20.8150, -0.2250)  
M4_M3_CDNS_4066195314551$1 (-21.0750, 0.2250) (-20.8150, 0.4850)  
M4_M3_CDNS_4066195314551$1 (-20.3650, -0.4850) (-20.1050, -0.2250)  
M4_M3_CDNS_4066195314551$1 (-20.3650, 0.2250) (-20.1050, 0.4850)  
M4_M3_CDNS_4066195314551$1 (-19.6550, -0.4850) (-19.3950, -0.2250)  
M4_M3_CDNS_4066195314551$1 (-19.6550, 0.2250) (-19.3950, 0.4850)  
M4_M3_CDNS_4066195314551$1 (-18.9450, -0.4850) (-18.6850, -0.2250)  
M4_M3_CDNS_4066195314551$1 (-18.9450, 0.2250) (-18.6850, 0.4850)  
M4_M3_CDNS_4066195314551$1 (-18.2350, -0.4850) (-17.9750, -0.2250)  
M4_M3_CDNS_4066195314551$1 (-18.2350, 0.2250) (-17.9750, 0.4850)  
M4_M3_CDNS_4066195314551$1 (-17.5250, -0.4850) (-17.2650, -0.2250)  
M4_M3_CDNS_4066195314551$1 (-17.5250, 0.2250) (-17.2650, 0.4850)  
M4_M3_CDNS_4066195314551$1 (-16.8150, -0.4850) (-16.5550, -0.2250)
```


M4_M3_CDNS_4066195314551\$1 (-16.8150, 0.2250) (-16.5550, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-16.1050, -0.4850) (-15.8450, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-16.1050, 0.2250) (-15.8450, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-15.3950, -0.4850) (-15.1350, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-15.3950, 0.2250) (-15.1350, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-14.6850, -0.4850) (-14.4250, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-14.6850, 0.2250) (-14.4250, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-13.9750, -0.4850) (-13.7150, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-13.9750, 0.2250) (-13.7150, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-13.2650, -0.4850) (-13.0050, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-13.2650, 0.2250) (-13.0050, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-12.5550, -0.4850) (-12.2950, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-12.5550, 0.2250) (-12.2950, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-11.8450, -0.4850) (-11.5850, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-11.8450, 0.2250) (-11.5850, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-11.1350, -0.4850) (-10.8750, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-11.1350, 0.2250) (-10.8750, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-10.4250, -0.4850) (-10.1650, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-10.4250, 0.2250) (-10.1650, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-9.7150, -0.4850) (-9.4550, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-9.7150, 0.2250) (-9.4550, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-9.0050, -0.4850) (-8.7450, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-9.0050, 0.2250) (-8.7450, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-8.2950, -0.4850) (-8.0350, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-8.2950, 0.2250) (-8.0350, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-7.5850, -0.4850) (-7.3250, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-7.5850, 0.2250) (-7.3250, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-6.8750, -0.4850) (-6.6150, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-6.8750, 0.2250) (-6.6150, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-6.1650, -0.4850) (-5.9050, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-6.1650, 0.2250) (-5.9050, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-5.4550, -0.4850) (-5.1950, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-5.4550, 0.2250) (-5.1950, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-4.7450, -0.4850) (-4.4850, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-4.7450, 0.2250) (-4.4850, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-4.0350, -0.4850) (-3.7750, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-4.0350, 0.2250) (-3.7750, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-3.3250, -0.4850) (-3.0650, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-3.3250, 0.2250) (-3.0650, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-2.6150, -0.4850) (-2.3550, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-2.6150, 0.2250) (-2.3550, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-1.9050, -0.4850) (-1.6450, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-1.9050, 0.2250) (-1.6450, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-1.1950, -0.4850) (-0.9350, -0.2250)

M4_M3_CDNS_4066195314551\$1 (-1.1950, 0.2250) (-0.9350, 0.4850)
M4_M3_CDNS_4066195314551\$1 (-0.4850, -0.4850) (-0.2250, -0.2250)
M4_M3_CDNS_4066195314551\$1 (-0.4850, 0.2250) (-0.2250, 0.4850)
M4_M3_CDNS_4066195314551\$1 (0.2250, -0.4850) (0.4850, -0.2250)
M4_M3_CDNS_4066195314551\$1 (0.2250, 0.2250) (0.4850, 0.4850)
M4_M3_CDNS_4066195314551\$1 (0.9350, -0.4850) (1.1950, -0.2250)
M4_M3_CDNS_4066195314551\$1 (0.9350, 0.2250) (1.1950, 0.4850)
M4_M3_CDNS_4066195314551\$1 (1.6450, -0.4850) (1.9050, -0.2250)
M4_M3_CDNS_4066195314551\$1 (1.6450, 0.2250) (1.9050, 0.4850)
M4_M3_CDNS_4066195314551\$1 (2.3550, -0.4850) (2.6150, -0.2250)
M4_M3_CDNS_4066195314551\$1 (2.3550, 0.2250) (2.6150, 0.4850)
M4_M3_CDNS_4066195314551\$1 (3.0650, -0.4850) (3.3250, -0.2250)
M4_M3_CDNS_4066195314551\$1 (3.0650, 0.2250) (3.3250, 0.4850)
M4_M3_CDNS_4066195314551\$1 (3.7750, -0.4850) (4.0350, -0.2250)
M4_M3_CDNS_4066195314551\$1 (3.7750, 0.2250) (4.0350, 0.4850)
M4_M3_CDNS_4066195314551\$1 (4.4850, -0.4850) (4.7450, -0.2250)
M4_M3_CDNS_4066195314551\$1 (4.4850, 0.2250) (4.7450, 0.4850)
M4_M3_CDNS_4066195314551\$1 (5.1950, -0.4850) (5.4550, -0.2250)
M4_M3_CDNS_4066195314551\$1 (5.1950, 0.2250) (5.4550, 0.4850)

CUP.9_Wedge_5LM : 9.3 Wedge type wire-bond not allowed to have CUP

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:3152:and

Structure (lower left x, y) (upper right x, y)

Bondpad_5LM\$1 (2.0000, 2.0000) (62.0000, 62.0000)
M5_M4_CDNS_4066195314556\$1 (-29.6550, -0.5450) (29.6550, 0.5450)
M4_M3_CDNS_4066195314551\$1 (-29.6550, -0.5450) (29.6550, 0.5450)

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:3153:and

WARNING: The error count of 101 for this check exceeds the limit set in
the runset. Details only available for the first 100.

Check was stopped early because error limit was reached.

Structure (lower left x, y) (upper right x, y)

M5_M4_CDNS_4066195314556\$1 (-29.5950, -0.4850) (-29.3350, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-29.5950, 0.2250) (-29.3350, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-28.8850, -0.4850) (-28.6250, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-28.8850, 0.2250) (-28.6250, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-28.1750, -0.4850) (-27.9150, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-28.1750, 0.2250) (-27.9150, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-27.4650, -0.4850) (-27.2050, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-27.4650, 0.2250) (-27.2050, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-26.7550, -0.4850) (-26.4950, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-26.7550, 0.2250) (-26.4950, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-26.0450, -0.4850) (-25.7850, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-26.0450, 0.2250) (-25.7850, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-25.3350, -0.4850) (-25.0750, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-25.3350, 0.2250) (-25.0750, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-24.6250, -0.4850) (-24.3650, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-24.6250, 0.2250) (-24.3650, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-23.9150, -0.4850) (-23.6550, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-23.9150, 0.2250) (-23.6550, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-23.2050, -0.4850) (-22.9450, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-23.2050, 0.2250) (-22.9450, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-22.4950, -0.4850) (-22.2350, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-22.4950, 0.2250) (-22.2350, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-21.7850, -0.4850) (-21.5250, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-21.7850, 0.2250) (-21.5250, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-21.0750, -0.4850) (-20.8150, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-21.0750, 0.2250) (-20.8150, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-20.3650, -0.4850) (-20.1050, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-20.3650, 0.2250) (-20.1050, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-19.6550, -0.4850) (-19.3950, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-19.6550, 0.2250) (-19.3950, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-18.9450, -0.4850) (-18.6850, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-18.9450, 0.2250) (-18.6850, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-18.2350, -0.4850) (-17.9750, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-18.2350, 0.2250) (-17.9750, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-17.5250, -0.4850) (-17.2650, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-17.5250, 0.2250) (-17.2650, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-16.8150, -0.4850) (-16.5550, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-16.8150, 0.2250) (-16.5550, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-16.1050, -0.4850) (-15.8450, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-16.1050, 0.2250) (-15.8450, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-15.3950, -0.4850) (-15.1350, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-15.3950, 0.2250) (-15.1350, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-14.6850, -0.4850) (-14.4250, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-14.6850, 0.2250) (-14.4250, 0.4850)

M5_M4_CDNS_4066195314556\$1 (-13.9750, -0.4850) (-13.7150, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-13.9750, 0.2250) (-13.7150, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-13.2650, -0.4850) (-13.0050, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-13.2650, 0.2250) (-13.0050, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-12.5550, -0.4850) (-12.2950, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-12.5550, 0.2250) (-12.2950, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-11.8450, -0.4850) (-11.5850, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-11.8450, 0.2250) (-11.5850, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-11.1350, -0.4850) (-10.8750, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-11.1350, 0.2250) (-10.8750, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-10.4250, -0.4850) (-10.1650, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-10.4250, 0.2250) (-10.1650, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-9.7150, -0.4850) (-9.4550, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-9.7150, 0.2250) (-9.4550, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-9.0050, -0.4850) (-8.7450, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-9.0050, 0.2250) (-8.7450, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-8.2950, -0.4850) (-8.0350, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-8.2950, 0.2250) (-8.0350, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-7.5850, -0.4850) (-7.3250, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-7.5850, 0.2250) (-7.3250, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-6.8750, -0.4850) (-6.6150, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-6.8750, 0.2250) (-6.6150, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-6.1650, -0.4850) (-5.9050, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-6.1650, 0.2250) (-5.9050, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-5.4550, -0.4850) (-5.1950, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-5.4550, 0.2250) (-5.1950, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-4.7450, -0.4850) (-4.4850, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-4.7450, 0.2250) (-4.4850, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-4.0350, -0.4850) (-3.7750, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-4.0350, 0.2250) (-3.7750, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-3.3250, -0.4850) (-3.0650, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-3.3250, 0.2250) (-3.0650, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-2.6150, -0.4850) (-2.3550, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-2.6150, 0.2250) (-2.3550, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-1.9050, -0.4850) (-1.6450, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-1.9050, 0.2250) (-1.6450, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-1.1950, -0.4850) (-0.9350, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-1.1950, 0.2250) (-0.9350, 0.4850)
M5_M4_CDNS_4066195314556\$1 (-0.4850, -0.4850) (-0.2250, -0.2250)
M5_M4_CDNS_4066195314556\$1 (-0.4850, 0.2250) (-0.2250, 0.4850)
M5_M4_CDNS_4066195314556\$1 (0.2250, -0.4850) (0.4850, -0.2250)
M5_M4_CDNS_4066195314556\$1 (0.2250, 0.2250) (0.4850, 0.4850)
M5_M4_CDNS_4066195314556\$1 (0.9350, -0.4850) (1.1950, -0.2250)
M5_M4_CDNS_4066195314556\$1 (0.9350, 0.2250) (1.1950, 0.4850)

M5_M4_CDNS_4066195314556\$1 (1.6450, -0.4850) (1.9050, -0.2250)
M5_M4_CDNS_4066195314556\$1 (1.6450, 0.2250) (1.9050, 0.4850)
M5_M4_CDNS_4066195314556\$1 (2.3550, -0.4850) (2.6150, -0.2250)
M5_M4_CDNS_4066195314556\$1 (2.3550, 0.2250) (2.6150, 0.4850)
M5_M4_CDNS_4066195314556\$1 (3.0650, -0.4850) (3.3250, -0.2250)
M5_M4_CDNS_4066195314556\$1 (3.0650, 0.2250) (3.3250, 0.4850)
M5_M4_CDNS_4066195314556\$1 (3.7750, -0.4850) (4.0350, -0.2250)
M5_M4_CDNS_4066195314556\$1 (3.7750, 0.2250) (4.0350, 0.4850)
M5_M4_CDNS_4066195314556\$1 (4.4850, -0.4850) (4.7450, -0.2250)
M5_M4_CDNS_4066195314556\$1 (4.4850, 0.2250) (4.7450, 0.4850)
M5_M4_CDNS_4066195314556\$1 (5.1950, -0.4850) (5.4550, -0.2250)
M5_M4_CDNS_4066195314556\$1 (5.1950, 0.2250) (5.4550, 0.4850)

DCF.1a : All area between active polygons (COMP) (with spacing greater
than equal to this rule) >= 20.0
must be filled with 'Dummy COMP' except area marked by NDMY, RES_MK,
Pad and IND_MK
as well as the region define by DCF.6a, 6b, 6c, 6d, 6e, 6f, 6g.

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:3218:or

WARNING: The error count of 102 for this check exceeds the limit set in
the runset. Details only available for the first 100.

Structure (lower left x, y) (upper right x, y)

trackA (447.5000, 2869.5150) (487.5000, 2925.0000)
trackA (547.5000, 2869.5150) (587.5000, 2925.0000)
trackA (647.5000, 2869.5150) (687.5000, 2925.0000)
trackA (747.5000, 2869.5150) (787.5000, 2925.0000)
trackA (847.5000, 2869.5150) (887.5000, 2925.0000)
trackA (947.5000, 2869.5150) (987.5000, 2925.0000)
trackA (1047.5000, 2869.5150) (1087.5000, 2925.0000)
trackA (1147.5000, 2869.5150) (1187.5000, 2925.0000)
trackA (1247.5000, 2869.5150) (1287.5000, 2925.0000)
trackA (1347.5000, 2869.5150) (1387.5000, 2925.0000)
trackA (1447.5000, 2869.5150) (1487.5000, 2925.0000)
trackA (1547.5000, 2869.5150) (1587.5000, 2925.0000)
trackA (1647.5000, 2869.5150) (1687.5000, 2925.0000)
trackA (1747.5000, 2869.5150) (1787.5000, 2925.0000)

trackA	(1847.5000, 2869.5150) (1887.5000, 2925.0000)
trackA	(1947.5000, 2869.5150) (1987.5000, 2925.0000)
trackA	(2047.5000, 2869.5150) (2087.5000, 2925.0000)
trackA	(2147.5000, 2869.5150) (2187.5000, 2925.0000)
trackA	(2247.5000, 2869.5150) (2287.5000, 2925.0000)
trackA	(2347.5000, 2869.5150) (2387.5000, 2925.0000)
trackA	(2447.5000, 2869.5150) (2487.5000, 2925.0000)
trackA	(10.0000, 2447.5000) (65.4850, 2487.5000)
trackA	(2869.5150, 2447.5000) (2925.0000, 2487.5000)
trackA	(10.0000, 2247.5000) (65.4850, 2287.5000)
trackA	(10.0000, 2347.5000) (65.4850, 2387.5000)
trackA	(1338.2950, 2288.1050) (1392.9150, 2348.2350)
trackA	(2869.5150, 2247.5000) (2925.0000, 2287.5000)
trackA	(2869.5150, 2347.5000) (2925.0000, 2387.5000)
trackA	(10.0000, 2047.5000) (65.4850, 2087.5000)
trackA	(10.0000, 2147.5000) (65.4850, 2187.5000)
trackA	(2869.5150, 2047.5000) (2925.0000, 2087.5000)
trackA	(2869.5150, 2147.5000) (2925.0000, 2187.5000)
trackA	(10.0000, 1747.5000) (65.4850, 1787.5000)
trackA	(10.0000, 1847.5000) (65.4850, 1887.5000)
trackA	(2869.5150, 1747.5000) (2925.0000, 1787.5000)
trackA	(2869.5150, 1847.5000) (2925.0000, 1887.5000)
trackA	(10.0000, 1547.5000) (65.4850, 1587.5000)
trackA	(10.0000, 1647.5000) (65.4850, 1687.5000)
trackA	(2869.5150, 1547.5000) (2925.0000, 1587.5000)
trackA	(2869.5150, 1647.5000) (2925.0000, 1687.5000)
trackA	(10.0000, 1247.5000) (65.4850, 1287.5000)
trackA	(10.0000, 1347.5000) (65.4850, 1387.5000)
trackA	(2869.5150, 1247.5000) (2925.0000, 1287.5000)
trackA	(2869.5150, 1347.5000) (2925.0000, 1387.5000)
trackA	(10.0000, 1047.5000) (65.4850, 1087.5000)
trackA	(10.0000, 1147.5000) (65.4850, 1187.5000)
trackA	(496.4250, 1065.5850) (560.8450, 1090.5150)
trackA	(567.9550, 1065.5850) (632.3750, 1090.5150)
trackA	(639.4850, 1065.5850) (703.9050, 1090.5150)
trackA	(711.0150, 1064.5850) (775.4350, 1089.5150)
trackA	(2869.5150, 1047.5000) (2925.0000, 1087.5000)
trackA	(2869.5150, 1147.5000) (2925.0000, 1187.5000)
trackA	(10.0000, 747.5000) (65.4850, 787.5000)
trackA	(10.0000, 847.5000) (65.4850, 887.5000)
trackA	(2869.5150, 747.5000) (2925.0000, 787.5000)
trackA	(2869.5150, 847.5000) (2925.0000, 887.5000)
trackA	(10.0000, 547.5000) (65.4850, 587.5000)
trackA	(10.0000, 647.5000) (65.4850, 687.5000)

trackA	(2869.5150, 547.5000)	(2925.0000, 587.5000)
trackA	(2869.5150, 647.5000)	(2925.0000, 687.5000)
trackA	(10.0000, 447.5000)	(65.4850, 487.5000)
trackA	(2045.5150, 349.8400)	(2090.7550, 373.4300)
trackA	(2869.5150, 447.5000)	(2925.0000, 487.5000)
trackA	(447.5000, 10.0000)	(487.5000, 65.4850)
trackA	(547.5000, 10.0000)	(587.5000, 65.4850)
trackA	(647.5000, 10.0000)	(687.5000, 65.4850)
trackA	(747.5000, 10.0000)	(787.5000, 65.4850)
trackA	(847.5000, 10.0000)	(887.5000, 65.4850)
trackA	(947.5000, 10.0000)	(987.5000, 65.4850)
trackA	(1047.5000, 10.0000)	(1087.5000, 65.4850)
trackA	(1147.5000, 10.0000)	(1187.5000, 65.4850)
trackA	(1247.5000, 10.0000)	(1287.5000, 65.4850)
trackA	(1347.5000, 10.0000)	(1387.5000, 65.4850)
trackA	(1447.5000, 10.0000)	(1487.5000, 65.4850)
trackA	(1547.5000, 10.0000)	(1587.5000, 65.4850)
trackA	(1647.5000, 10.0000)	(1687.5000, 65.4850)
trackA	(1747.5000, 10.0000)	(1787.5000, 65.4850)
trackA	(1847.5000, 10.0000)	(1887.5000, 65.4850)
trackA	(1947.5000, 10.0000)	(1987.5000, 65.4850)
trackA	(2047.5000, 10.0000)	(2087.5000, 65.4850)
trackA	(2147.5000, 10.0000)	(2187.5000, 65.4850)
trackA	(2247.5000, 10.0000)	(2287.5000, 65.4850)
trackA	(2347.5000, 10.0000)	(2387.5000, 65.4850)
trackA	(2447.5000, 10.0000)	(2487.5000, 65.4850)
trackA	(10.0000, 2547.5000)	(387.5000, 2925.0000)
trackA	(2547.5000, 2547.5000)	(2925.0000, 2925.0000)
trackA	(349.8400, 349.8400)	(2585.1600, 2585.1600)
trackA	(10.0000, 1947.5000)	(65.4850, 1987.5000)
trackA	(2869.5150, 1947.5000)	(2925.0000, 1987.5000)
trackA	(10.0000, 1447.5000)	(65.4850, 1487.5000)
trackA	(2869.5150, 1447.5000)	(2925.0000, 1487.5000)
trackA	(10.0000, 947.5000)	(65.4850, 987.5000)
trackA	(2869.5150, 947.5000)	(2925.0000, 987.5000)
op_buffer	(-42.5450, -63.9200)	(-7.7200, -41.3250)
op_buffer	(-22.7450, -63.9200)	(14.5750, 6.1600)
io_secondary_5p0	(14.4600, -14.1500)	(32.6500, -8.5500)
io_secondary_5p0	(-37.3500, -14.1500)	(21.3500, 51.2000)
io_secondary_5p0	(14.3200, 36.2100)	(32.6500, 51.2000)
cap_mim	(9.4000, 9.4000)	(15.6000, 15.6000)
gf180mcu_fd_io__cor\$2	(75.3250, 75.3250)	(214.3750, 214.3750)

DCF.1b_DCF.1d : Minimum global density for active layers (COMP+ Dummy
COMP) = 25.0%
Maximum global density for active layers (COMP+ Dummy COMP) = 70.0%

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:3236:density

Structure Window (x1,y1) (x2,y2)

Report = Value

trackA (0.0000, 0.0000) (2935.0000, 2935.0000)

Min ratio = 0.1966

Max ratio = 0.1966

Avg ratio = 0.1966

Min areaL1 = 1693142.3202

Max areaL1 = 1693142.3202

Avg areaL1 = 1693142.3202

Min areaW = 8614225.0000

Max areaW = 8614225.0000

Avg areaW = 8614225.0000

DF.11 : Min. Length of butting COMP edge : 0.30

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2209:length_edge

WARNING: The error count of 102 for this check exceeds the limit set in
the runset. Details only available for the first 100.

Check was stopped early because error limit was reached.

Structure (lower left x, y) (upper right x, y) Distance

trackA (1349.0800, 2368.3950) (1349.2500, 2368.3950) 0.1700

trackA (1349.2500, 2368.3950) (1349.2500, 2368.5650) 0.1700

trackA (1349.0800, 2374.2450) (1349.2500, 2374.2450) 0.1700

trackA (1349.2500, 2374.2450) (1349.2500, 2374.4150) 0.1700

trackA (1349.6300, 2368.3950) (1349.6300, 2368.5650) 0.1700

trackA (1349.6300, 2368.3950) (1349.8000, 2368.3950) 0.1700

trackA (1349.6300, 2374.2450) (1349.6300, 2374.4150) 0.1700
trackA (1349.6300, 2374.2450) (1349.8000, 2374.2450) 0.1700
trackA (1356.4800, 2365.6250) (1356.6500, 2365.6250) 0.1700
trackA (1356.6500, 2365.4550) (1356.6500, 2365.6250) 0.1700
trackA (1356.4800, 2371.4750) (1356.6500, 2371.4750) 0.1700
trackA (1356.6500, 2371.3050) (1356.6500, 2371.4750) 0.1700
trackA (1356.4800, 2377.3250) (1356.6500, 2377.3250) 0.1700
trackA (1356.6500, 2377.1550) (1356.6500, 2377.3250) 0.1700
trackA (1357.0300, 2365.4550) (1357.0300, 2365.6250) 0.1700
trackA (1357.0300, 2365.6250) (1357.2000, 2365.6250) 0.1700
trackA (1357.0300, 2371.3050) (1357.0300, 2371.4750) 0.1700
trackA (1357.0300, 2371.4750) (1357.2000, 2371.4750) 0.1700
trackA (1357.0300, 2377.1550) (1357.0300, 2377.3250) 0.1700
trackA (1357.0300, 2377.3250) (1357.2000, 2377.3250) 0.1700
trackA (1358.0600, 2368.3950) (1358.3100, 2368.3950) 0.2500
trackA (1358.3100, 2368.3950) (1358.3100, 2368.5650) 0.1700
trackA (1358.7300, 2368.3950) (1358.7300, 2368.5650) 0.1700
trackA (1358.7300, 2368.3950) (1358.9800, 2368.3950) 0.2500
trackA (1367.3700, 2368.3950) (1367.6200, 2368.3950) 0.2500
trackA (1367.6200, 2368.3950) (1367.6200, 2368.5650) 0.1700
trackA (1368.0400, 2368.3950) (1368.0400, 2368.5650) 0.1700
trackA (1368.0400, 2368.3950) (1368.2900, 2368.3950) 0.2500
trackA (1376.6800, 2368.3950) (1376.9300, 2368.3950) 0.2500
trackA (1376.9300, 2368.3950) (1376.9300, 2368.5650) 0.1700
trackA (1377.3500, 2368.3950) (1377.3500, 2368.5650) 0.1700
trackA (1377.3500, 2368.3950) (1377.6000, 2368.3950) 0.2500
trackA (1385.9900, 2368.3950) (1386.2400, 2368.3950) 0.2500
trackA (1386.2400, 2368.3950) (1386.2400, 2368.5650) 0.1700
trackA (1386.6600, 2368.3950) (1386.6600, 2368.5650) 0.1700
trackA (1386.6600, 2368.3950) (1386.9100, 2368.3950) 0.2500
trackA (1454.5800, 2366.5650) (1454.7500, 2366.5650) 0.1700
trackA (1454.7500, 2366.5650) (1454.7500, 2366.7350) 0.1700
trackA (1454.5800, 2374.1750) (1454.7500, 2374.1750) 0.1700
trackA (1454.7500, 2374.1750) (1454.7500, 2374.3450) 0.1700
trackA (1455.1300, 2366.5650) (1455.1300, 2366.7350) 0.1700
trackA (1455.1300, 2366.5650) (1455.3000, 2366.5650) 0.1700
trackA (1455.1300, 2374.1750) (1455.1300, 2374.3450) 0.1700
trackA (1455.1300, 2374.1750) (1455.3000, 2374.1750) 0.1700
trackA (1462.6750, 2363.7950) (1462.8450, 2363.7950) 0.1700
trackA (1462.8450, 2363.6250) (1462.8450, 2363.7950) 0.1700
trackA (1462.6750, 2371.4050) (1462.8450, 2371.4050) 0.1700
trackA (1462.8450, 2371.2350) (1462.8450, 2371.4050) 0.1700
trackA (1463.2250, 2363.6250) (1463.2250, 2363.7950) 0.1700
trackA (1463.2250, 2363.7950) (1463.3950, 2363.7950) 0.1700

trackA (1463.2250, 2371.2350) (1463.2250, 2371.4050) 0.1700
trackA (1463.2250, 2371.4050) (1463.3950, 2371.4050) 0.1700
trackA (1496.3800, 2363.7950) (1496.5400, 2363.7950) 0.1600
trackA (1496.5400, 2363.6250) (1496.5400, 2363.7950) 0.1700
trackA (1496.3800, 2371.4050) (1496.5400, 2371.4050) 0.1600
trackA (1496.5400, 2371.2350) (1496.5400, 2371.4050) 0.1700
trackA (1496.9000, 2363.6250) (1496.9000, 2363.7950) 0.1700
trackA (1496.9000, 2363.7950) (1497.0600, 2363.7950) 0.1600
trackA (1496.9000, 2371.2350) (1496.9000, 2371.4050) 0.1700
trackA (1496.9000, 2371.4050) (1497.0600, 2371.4050) 0.1600
trackA (1497.0600, 2364.5250) (1497.2100, 2364.5250) 0.1500
trackA (1497.0600, 2372.1350) (1497.2100, 2372.1350) 0.1500
trackA (1349.0800, 2380.0950) (1349.2500, 2380.0950) 0.1700
trackA (1349.2500, 2380.0950) (1349.2500, 2380.2650) 0.1700
trackA (1349.0800, 2385.9450) (1349.2500, 2385.9450) 0.1700
trackA (1349.2500, 2385.9450) (1349.2500, 2386.1150) 0.1700
trackA (1349.6300, 2380.0950) (1349.6300, 2380.2650) 0.1700
trackA (1349.6300, 2380.0950) (1349.8000, 2380.0950) 0.1700
trackA (1349.6300, 2385.9450) (1349.6300, 2386.1150) 0.1700
trackA (1349.6300, 2385.9450) (1349.8000, 2385.9450) 0.1700
trackA (1356.4800, 2383.1750) (1356.6500, 2383.1750) 0.1700
trackA (1356.6500, 2383.0050) (1356.6500, 2383.1750) 0.1700
trackA (1356.4800, 2389.0250) (1356.6500, 2389.0250) 0.1700
trackA (1356.6500, 2388.8550) (1356.6500, 2389.0250) 0.1700
trackA (1357.0300, 2383.0050) (1357.0300, 2383.1750) 0.1700
trackA (1357.0300, 2383.1750) (1357.2000, 2383.1750) 0.1700
trackA (1357.0300, 2388.8550) (1357.0300, 2389.0250) 0.1700
trackA (1357.0300, 2389.0250) (1357.2000, 2389.0250) 0.1700
trackA (1358.1400, 2389.0250) (1358.3000, 2389.0250) 0.1600
trackA (1358.3000, 2388.8550) (1358.3000, 2389.0250) 0.1700
trackA (1358.7400, 2388.8550) (1358.7400, 2389.0250) 0.1700
trackA (1358.7400, 2389.0250) (1358.9000, 2389.0250) 0.1600
trackA (1367.4500, 2389.0250) (1367.6100, 2389.0250) 0.1600
trackA (1367.6100, 2388.8550) (1367.6100, 2389.0250) 0.1700
trackA (1368.0500, 2388.8550) (1368.0500, 2389.0250) 0.1700
trackA (1368.0500, 2389.0250) (1368.2100, 2389.0250) 0.1600
trackA (1376.7600, 2389.0250) (1376.9200, 2389.0250) 0.1600
trackA (1376.9200, 2388.8550) (1376.9200, 2389.0250) 0.1700
trackA (1377.3600, 2388.8550) (1377.3600, 2389.0250) 0.1700
trackA (1377.3600, 2389.0250) (1377.5200, 2389.0250) 0.1600
trackA (1386.0700, 2389.0250) (1386.2300, 2389.0250) 0.1600
trackA (1386.2300, 2388.8550) (1386.2300, 2389.0250) 0.1700
trackA (1386.6700, 2388.8550) (1386.6700, 2389.0250) 0.1700
trackA (1386.6700, 2389.0250) (1386.8300, 2389.0250) 0.1600

```

trackA (1454.5800, 2381.7850) (1454.7500, 2381.7850) 0.1700
trackA (1454.7500, 2381.7850) (1454.7500, 2381.9550) 0.1700
trackA (1454.5800, 2389.3950) (1454.7500, 2389.3950) 0.1700
trackA (1454.7500, 2389.3950) (1454.7500, 2389.5650) 0.1700
trackA (1455.1300, 2381.7850) (1455.1300, 2381.9550) 0.1700
trackA (1455.1300, 2381.7850) (1455.3000, 2381.7850) 0.1700

```

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-----
DF.12 : Max distance of Nwell tap (NCOMP inside Nwell) from (PCOMP
inside Nwell) : 20
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/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2218:and

```

WARNING: The error count of 110 for this check exceeds the limit set in the runset. Details only available for the first 100.

Check was stopped early because error limit was reached.

```

-----
Structure          ( lower left x, y ) ( upper right x, y )
-----
op_buffer          (-40.2550, -22.5200) (-38.5150, -10.5200)
op_buffer          (-40.2550, 9.6200) (-38.5150, 10.7500)
op_buffer          (-37.6550, -22.5200) (-35.8750, -10.5200)
op_buffer          (-37.6550, 9.6200) (-35.8750, 10.7500)
op_buffer          (-35.1250, -22.5200) (-33.3450, -10.5200)
op_buffer          (-35.1250, 9.6200) (-33.3450, 10.7500)
op_buffer          (-32.5950, -22.5200) (-30.8150, -10.5200)
op_buffer          (-32.5950, 9.6200) (-30.8150, 10.7500)
op_buffer          (-30.0650, -22.5200) (-28.2850, -10.5200)
op_buffer          (-30.0650, 9.6200) (-28.2850, 10.7500)
op_buffer          (-27.5350, -22.5200) (-25.7550, -10.5200)
op_buffer          (-27.4250, 9.6200) (-25.6850, 10.7500)
op_buffer          (-25.0050, -22.5200) (-23.2250, -10.5200)
op_buffer          (-22.4750, -22.5200) (-20.6950, -10.5200)
op_buffer          (-19.9450, -22.5200) (-18.1650, -10.5200)
op_buffer          (-17.3050, -22.5200) (-15.5650, -10.5200)
op_buffer          (-7.2850, -12.7150) (-5.5450, -10.5150)
op_buffer          (-4.6850, -12.7150) (-2.9050, -10.5150)
op_buffer          (-2.1550, -12.7150) (-0.3750, -10.5150)
op_buffer          (0.3750, -12.7150) (2.1550, -10.5150)
op_buffer          (2.9050, -12.7150) (4.6850, -10.5150)

```

op_buffer	(5.5450, -12.7150)	(7.2850, -10.5150)
Unnamed_02d9ae27	(-9.5500, -12.8700)	(-7.8100, -10.7100)
Unnamed_02d9ae27	(-9.5500, 18.5800)	(-7.8100, 21.8250)
Unnamed_02d9ae27	(-6.9500, -12.8700)	(-4.0300, -10.7100)
Unnamed_02d9ae27	(-6.9500, 18.5800)	(-4.0300, 21.8250)
Unnamed_02d9ae27	(-3.2900, -12.8700)	(-0.3700, -10.7100)
Unnamed_02d9ae27	(-3.2900, 18.5800)	(-0.3700, 21.8250)
Unnamed_02d9ae27	(0.3700, -12.8700)	(3.2900, -10.7100)
Unnamed_02d9ae27	(0.3700, 18.5800)	(3.2900, 21.8250)
Unnamed_02d9ae27	(4.0300, -12.8700)	(6.9500, -10.7100)
Unnamed_02d9ae27	(4.0300, 18.5800)	(6.9500, 21.8250)
Unnamed_02d9ae27	(7.8100, -12.8700)	(9.5500, -10.7100)
Unnamed_02d9ae27	(7.8100, 18.5800)	(9.5500, 21.8250)
transformed_9f8db47f	(-16.3900, -4.4250)	(-14.6500, 0.5750)
transformed_9f8db47f	(-13.7900, -4.4250)	(-7.4500, 0.5750)
transformed_9f8db47f	(-6.7100, -4.4250)	(-0.3700, 0.5750)
transformed_9f8db47f	(0.3700, -4.4250)	(6.7100, 0.5750)
transformed_9f8db47f	(7.4500, -4.4250)	(13.7900, 0.5750)
transformed_9f8db47f	(14.6500, -4.4250)	(16.3900, 0.5750)
transformed_729ded33	(-16.3900, -4.4250)	(-14.6500, 0.5750)
transformed_729ded33	(-13.7900, -4.4250)	(-7.4500, 0.5750)
transformed_729ded33	(-6.7100, -4.4250)	(-0.3700, 0.5750)
transformed_729ded33	(0.3700, -4.4250)	(6.7100, 0.5750)
transformed_729ded33	(7.4500, -4.4250)	(13.7900, 0.5750)
transformed_729ded33	(14.6500, -4.4250)	(16.3900, 0.5750)
gf180mcu_fd_sc_mcu7t5v0__buf_1	(0.2800, 2.3600)	(2.9000, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__buf_4	(0.1800, 2.3600)	(7.1600, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__antenna	(0.1800, 2.3600)	(0.5400, 2.9300)
gf180mcu_fd_sc_mcu7t5v0__buf_3	(0.1800, 2.3600)	(5.1100, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_16	(6.9000, 2.3600)	(8.7800, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_16	(4.6600, 2.3600)	(6.5400, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_16	(2.4200, 2.3600)	(4.3000, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_16	(0.1800, 2.3600)	(2.0600, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__clkbuf_1	(0.2800, 2.3600)	(2.8600, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__dffrnq_1	(17.4050, 2.3600)	(18.7850, 3.5750)
gf180mcu_fd_sc_mcu7t5v0__dffrnq_1	(3.0400, 2.3600)	(9.0600, 3.3000)
gf180mcu_fd_sc_mcu7t5v0__dffrnq_1	(0.2800, 2.3600)	(2.6800, 3.2250)
gf180mcu_fd_sc_mcu7t5v0__dffrnq_1	(9.4200, 2.5800)	(17.0450, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__dffrnq_1	(8.5200, 4.2600)	(9.9000, 4.3500)
gf180mcu_fd_sc_mcu7t5v0__fillcap_4	(0.1800, 2.3600)	(2.0600, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_8	(2.4200, 2.3600)	(4.3000, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_8	(0.1800, 2.3600)	(2.0600, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(33.7800, 2.3600)	(35.6600, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(31.5400, 2.3600)	(33.4200, 3.5800)

gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(29.3000, 2.3600)	(31.1800, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(27.0600, 2.3600)	(28.9400, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(24.8200, 2.3600)	(26.7000, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(22.5800, 2.3600)	(24.4600, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(20.3400, 2.3600)	(22.2200, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(18.1000, 2.3600)	(19.9800, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(15.8600, 2.3600)	(17.7400, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(13.6200, 2.3600)	(15.5000, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(11.3800, 2.3600)	(13.2600, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(9.1400, 2.3600)	(11.0200, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(6.9000, 2.3600)	(8.7800, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(4.6600, 2.3600)	(6.5400, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(2.4200, 2.3600)	(4.3000, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(0.1800, 2.3600)	(2.0600, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_32	(15.8600, 2.3600)	(17.7400, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_32	(13.6200, 2.3600)	(15.5000, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_32	(11.3800, 2.3600)	(13.2600, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_32	(9.1400, 2.3600)	(11.0200, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_32	(6.9000, 2.3600)	(8.7800, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_32	(4.6600, 2.3600)	(6.5400, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_32	(2.4200, 2.3600)	(4.3000, 3.5800)
gf180mcu_fd_sc_mcu7t5v0__fillcap_32	(0.1800, 2.3600)	(2.0600, 3.5800)
io_secondary_5p0	(1.9000, 37.7100)	(11.9000, 47.7100)
io_secondary_5p0	(-9.1800, 37.7100)	(0.8200, 47.7100)
pfet\$6	(-0.4600, 0.0000)	(1.5800, 0.5000)
pfet\$5	(-0.4600, 0.0000)	(1.5800, 1.5000)
pfet\$4	(-0.4600, 0.0000)	(1.5800, 1.5000)
pfet\$3	(-0.4600, 0.0000)	(1.5800, 50.0000)
pfet\$2	(-0.4600, 0.0000)	(1.5800, 50.0000)
pfet\$1	(-0.4600, 0.0000)	(1.5800, 50.0000)
pfet	(-0.4600, 0.0000)	(1.5800, 50.0000)
pn_6p0_CDNS_4066195314528\$1	(0.0000, 0.0000)	(1.0000, 1.0000)
pmos_6p0_CDNS_4066195314515\$1	(-0.4400, 0.0000)	(1.1400, 12.0000)
pmos_6p0_CDNS_4066195314516\$1	(-0.4400, 0.0000)	(2.3600, 12.0000)
pn_6p0_CDNS_4066195314510\$1	(0.0000, 0.0000)	(0.4800, 0.4800)

DF.13 : Max distance of substrate tap (PCOMP outside Nwell) from
(NCOMP outside Nwell) : 20

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2227:and

WARNING: The error count of 102 for this check exceeds the limit set in the runset. Details only available for the first 100.

Check was stopped early because error limit was reached.

```
-----  
Structure          ( lower left x, y )  ( upper right x, y )  
-----  
op_buffer          (-41.3050, -39.7450) (-14.5150, -26.6650)  
op_buffer          (-41.3050, -2.8300)  (-24.6350, 5.4600)  
op_buffer          (-8.3350, -25.6400)   (8.3350, -16.8600)  
op_buffer          (-7.7200, -56.7850)   (7.7200, -40.1800)  
Unnamed_02d9ae27   (-10.6000, -25.5000) (10.6000, -17.0000)  
Unnamed_02d9ae27   (-10.6000, 5.5750)  (10.6000, 14.4400)  
gf180mcu_fd_sc_mcu7t5v0__filltie (0.2800, 0.2800)  (0.8400, 1.2800)  
gf180mcu_fd_sc_mcu7t5v0__endcap (0.2800, 0.2800)  (0.8000, 1.2800)  
cmirror_interdigitized$2 (-13.1000, -4.0450) (13.1000, 4.0450)  
cmirror_interdigitized$1 (-13.1000, -4.0450) (13.1000, 4.0450)  
io_secondary_5p0    (-32.0800, -19.3300) (12.9200, -7.8100)  
nfet$17            (1.6400, 0.0000)    (2.3500, 0.5000)  
nfet$16            (1.6400, -0.0100)    (2.3500, 0.4300)  
nfet$15            (1.6400, -0.0100)    (2.3500, 0.4300)  
nfet$13            (1.6400, -0.0100)    (2.3500, 0.4300)  
nfet$12            (1.6400, -0.0100)    (2.3500, 0.4300)  
nfet$11            (1.6400, -0.0100)    (2.3500, 0.4300)  
nfet$10            (1.6400, -0.0100)    (2.3500, 0.4300)  
gf180mcu_fd_io__dvss$1 (0.0000, 65.4850)  (75.0000, 349.8400)  
gf180mcu_fd_io__dvss$1 (1.7250, 327.9150) (2.4950, 347.6350)  
gf180mcu_fd_io__dvss$1 (72.5050, 327.9150) (73.2750, 347.6350)  
gf180mcu_fd_io__dvss$1 (15.5250, 303.1250) (59.4750, 322.2550)  
gf180mcu_fd_io__dvss$1 (65.0600, 197.8950) (70.0100, 275.3450)  
gf180mcu_fd_io__dvss$1 (16.3600, 196.0100) (58.6400, 204.9850)  
gf180mcu_fd_io__dvss$1 (9.9550, 189.1100) (10.2750, 191.0600)  
gf180mcu_fd_io__dvss$1 (64.7250, 189.1100) (65.0450, 191.0600)  
gf180mcu_fd_io__dvss$1 (9.9550, 159.7200) (10.2750, 160.6700)  
gf180mcu_fd_io__dvss$1 (64.7250, 159.7200) (65.0450, 160.6700)  
gf180mcu_fd_io__dvss$1 (9.9550, 130.3600) (10.2750, 131.3100)  
gf180mcu_fd_io__dvss$1 (64.7250, 130.3600) (65.0450, 131.3100)  
gf180mcu_fd_io__dvss$1 (9.9550, 101.0000) (10.2750, 101.9500)  
gf180mcu_fd_io__dvss$1 (64.7250, 101.0000) (65.0450, 101.9500)  
gf180mcu_fd_io__dvss$1 (9.9550, 70.6100)  (10.2750, 72.5600)  
gf180mcu_fd_io__dvss$1 (64.7250, 70.6100)  (65.0450, 72.5600)  
M1_PSUB_CDNS_40661953145101$1 (-4.9750, -12.4750) (4.9750, 12.4750)  
M1_PSUB_CDNS_40661953145130$1 (-27.2250, -0.4750) (27.2250, 0.4750)
```

M1_PSUB_CDNS_40661953145133\$1	(-0.9750, -60.2250)	(0.9750, 60.2250)
M1_PSUB_CDNS_40661953145134\$1	(-27.2250, -0.9750)	(27.2250, 0.9750)
comp018green_esd_rc_v5p0\$2	(7.8250, 23.7500)	(9.1650, 85.1900)
comp018green_esd_rc_v5p0\$2	(59.2050, 23.7500)	(59.5250, 24.7700)
comp018green_esd_rc_v5p0\$2	(59.2050, 53.7150)	(59.5250, 54.7350)
comp018green_esd_rc_v5p0\$2	(59.2050, 84.1700)	(59.5250, 85.1900)
M1_PSUB_CDNS_40661953145129\$1	(-0.5100, -25.0200)	(0.5100, 25.0200)
M1_PSUB_CDNS_40661953145126\$1	(-0.5100, -30.7200)	(0.5100, 30.7200)
M1_PSUB_CDNS_40661953145100\$1	(-1.2250, -103.7250)	(1.2250, 103.7250)
M1_PSUB_CDNS_4066195314565\$1	(-35.0050, -0.2250)	(35.0050, 0.2250)
M1_PSUB_CDNS_4066195314567\$1	(-20.5950, -0.2250)	(20.5950, 0.2250)
M1_PSUB_CDNS_406619531455\$1	(-0.2250, -141.9750)	(0.2250, 141.9750)
gf180mcu_fd_io__dvdd\$1	(0.0000, 65.4850)	(75.0000, 349.8400)
gf180mcu_fd_io__dvdd\$1	(1.7250, 327.9150)	(2.4950, 347.6350)
gf180mcu_fd_io__dvdd\$1	(72.5050, 327.9150)	(73.2750, 347.6350)
gf180mcu_fd_io__dvdd\$1	(15.5250, 303.1250)	(59.4750, 322.2550)
gf180mcu_fd_io__dvdd\$1	(65.0600, 197.8950)	(70.0100, 275.3450)
gf180mcu_fd_io__dvdd\$1	(16.3600, 196.2950)	(58.6400, 205.2700)
gf180mcu_fd_io__dvdd\$1	(9.9550, 189.3950)	(10.2750, 191.3450)
gf180mcu_fd_io__dvdd\$1	(64.7250, 189.3950)	(65.0450, 191.3450)
gf180mcu_fd_io__dvdd\$1	(9.9550, 160.0050)	(10.2750, 160.9550)
gf180mcu_fd_io__dvdd\$1	(64.7250, 160.0050)	(65.0450, 160.9550)
gf180mcu_fd_io__dvdd\$1	(9.9550, 130.6450)	(10.2750, 131.5950)
gf180mcu_fd_io__dvdd\$1	(64.7250, 130.6450)	(65.0450, 131.5950)
gf180mcu_fd_io__dvdd\$1	(9.9550, 101.2850)	(10.2750, 102.2350)
gf180mcu_fd_io__dvdd\$1	(64.7250, 101.2850)	(65.0450, 102.2350)
gf180mcu_fd_io__dvdd\$1	(9.9550, 70.8950)	(10.2750, 72.8450)
gf180mcu_fd_io__dvdd\$1	(64.7250, 70.8950)	(65.0450, 72.8450)
gf180mcu_fd_io__cor\$2	(65.4850, 65.4850)	(355.0000, 355.0000)
gf180mcu_fd_io__cor\$2	(109.3450, 126.6200)	(164.4600, 181.7350)
gf180mcu_fd_io__cor\$2	(171.8850, 94.9200)	(196.1600, 119.1950)
gf180mcu_fd_io__cor\$2	(67.7300, 173.6400)	(262.3900, 284.2350)
gf180mcu_fd_io__cor\$2	(88.0250, 198.7700)	(99.2250, 205.1150)
gf180mcu_fd_io__cor\$2	(120.2750, 143.6750)	(178.4100, 173.6400)
nmos_clamp_20_50_4\$2	(4.8600, 3.1600)	(5.1800, 5.1100)
nmos_clamp_20_50_4\$2	(4.8600, 33.5500)	(5.1800, 34.5000)
nmos_clamp_20_50_4\$2	(4.8600, 62.9100)	(5.1800, 63.8600)
nmos_clamp_20_50_4\$2	(4.8600, 92.2700)	(5.1800, 93.2200)
nmos_clamp_20_50_4\$2	(4.8600, 121.6600)	(5.1800, 123.6100)
nmos_clamp_20_50_4\$2	(59.6300, 3.1600)	(59.9500, 5.1100)
nmos_clamp_20_50_4\$2	(59.6300, 33.5500)	(59.9500, 34.5000)
nmos_clamp_20_50_4\$2	(59.6300, 62.9100)	(59.9500, 63.8600)
nmos_clamp_20_50_4\$2	(59.6300, 92.2700)	(59.9500, 93.2200)
nmos_clamp_20_50_4\$2	(59.6300, 121.6600)	(59.9500, 123.6100)

moscap_corner\$2	(0.1600, 0.1600)	(1.5000, 61.6000)
moscap_corner\$2	(51.5400, 0.1600)	(51.8600, 1.1800)
moscap_corner\$2	(51.5400, 30.1250)	(51.8600, 31.1450)
moscap_corner\$2	(51.5400, 60.5800)	(51.8600, 61.6000)
M1_PSUB_CDNS_40661953145283\$1	(-1.0050, -38.6350)	(1.0050, 38.6350)
comp018green_out_predrv\$1	(0.0000, 0.0000)	(17.9700, 13.6000)
comp018green_sigbuf\$1	(6.4000, 0.0000)	(13.5600, 5.1500)
comp018green_sigbuf\$1	(0.0000, 0.0000)	(3.8700, 5.1500)
comp018green_std_nand2\$1	(0.0000, 0.0550)	(5.2800, 5.2050)
comp018green_out_sigbuf_oe\$1	(7.8100, 0.0000)	(13.5600, 5.1500)
comp018green_out_sigbuf_oe\$1	(0.0000, 0.0000)	(5.2800, 5.1500)
gf180mcu_fd_io__asig_5p0\$1	(0.0000, 65.4850)	(75.0000, 349.8400)
gf180mcu_fd_io__asig_5p0\$1	(1.2850, 67.9600)	(5.2350, 165.4100)
gf180mcu_fd_io__asig_5p0\$1	(1.7250, 169.2400)	(2.4950, 347.3500)
gf180mcu_fd_io__asig_5p0\$1	(7.0050, 67.9600)	(67.9950, 102.9100)
gf180mcu_fd_io__asig_5p0\$1	(10.2650, 108.2050)	(64.7350, 136.7350)
gf180mcu_fd_io__asig_5p0\$1	(15.4200, 145.5100)	(59.5800, 163.4800)
gf180mcu_fd_io__asig_5p0\$1	(69.7650, 67.9600)	(73.7150, 165.4100)
gf180mcu_fd_io__asig_5p0\$1	(72.5050, 169.2400)	(73.2750, 347.3500)
gf180mcu_fd_io__fill5\$1	(0.0000, 65.4850)	(5.0000, 349.8400)

DF.18_LV : Min DNWELL space to (PCOMP outside Nwell and DNWELL) = 2.5

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2260:external2

Structure (lower left x, y) (upper right x, y) Distance

trackA	(521.9600, 1232.2650)	(536.9100, 1233.1950)	0.9300
trackA	(535.9800, 1232.2650)	(536.9100, 1257.4160)	0.9300
trackA	(521.9600, 1232.2650)	(522.8900, 1257.4160)	0.9300
trackA	(521.9600, 1282.2950)	(536.9100, 1283.2250)	0.9300
trackA	(535.9800, 1258.0740)	(536.9100, 1283.2250)	0.9300
trackA	(521.9600, 1258.0740)	(522.8900, 1283.2250)	0.9300
trackA	(592.4600, 1232.2650)	(607.4100, 1233.1950)	0.9300
trackA	(606.4800, 1232.2650)	(607.4100, 1257.4160)	0.9300
trackA	(592.4600, 1232.2650)	(593.3900, 1257.4160)	0.9300
trackA	(592.4600, 1282.2950)	(607.4100, 1283.2250)	0.9300
trackA	(606.4800, 1258.0740)	(607.4100, 1283.2250)	0.9300
trackA	(592.4600, 1258.0740)	(593.3900, 1283.2250)	0.9300
trackA	(662.9600, 1232.2650)	(677.9100, 1233.1950)	0.9300


```

trackA (676.9800, 1232.2650) (677.9100, 1257.4160) 0.9300
trackA (662.9600, 1232.2650) (663.8900, 1257.4160) 0.9300
trackA (662.9600, 1282.2950) (677.9100, 1283.2250) 0.9300
trackA (676.9800, 1258.0740) (677.9100, 1283.2250) 0.9300
trackA (662.9600, 1258.0740) (663.8900, 1283.2250) 0.9300
trackA (733.4600, 1232.2650) (748.4100, 1233.1950) 0.9300
trackA (747.4800, 1232.2650) (748.4100, 1257.4160) 0.9300
trackA (733.4600, 1232.2650) (734.3900, 1257.4160) 0.9300
trackA (733.4600, 1282.2950) (748.4100, 1283.2250) 0.9300
trackA (747.4800, 1258.0740) (748.4100, 1283.2250) 0.9300
trackA (733.4600, 1258.0740) (734.3900, 1283.2250) 0.9300

```

DF.1a : Min. COMP Width : 0.22

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2092:internal1

Structure (lower left x, y) (upper right x, y) Distance

```

trackA (1642.4950, 2408.6150) (1642.6250, 2408.6200) 0.0050
trackA (1642.2750, 2408.6150) (1642.4950, 2408.6200) 0.0050
trackA (1642.4950, 2409.0350) (1642.6250, 2409.0400) 0.0050
trackA (1642.2750, 2409.0350) (1642.4950, 2409.0400) 0.0050

```

DF.3a_LV : Minimum COMP space. P-substrate tap (PCOMP outside DNWELL
and NWELL) can be butted for different voltage device like Low voltage,
Medium voltage and High voltage as the potential is same

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2130:outside

Structure (lower left x, y) (upper right x, y)

```

trackA (1642.4950, 2408.6200) (1642.6250, 2409.0350)
trackA (1642.6250, 2409.0350) (1642.9050, 2409.0400)

```

DF.3a_MV : Minimum COMP space. P-substrate tap (PCOMP outside DNWELL and NWELL) can be butted for different voltage device like Low voltage, Medium voltage and High voltage as the potential is same

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2136:external1

Structure (lower left x, y) (upper right x, y) Distance

trackA	(1358.0150, 2377.1050)	(1359.0250, 2377.3250)	0.2200
trackA	(1357.9510, 2374.2450)	(1359.0890, 2374.3350)	0.0900
trackA	(1367.3250, 2377.1050)	(1368.3350, 2377.3250)	0.2200
trackA	(1367.2610, 2374.2450)	(1368.3990, 2374.3350)	0.0900
trackA	(1376.6350, 2377.1050)	(1377.6450, 2377.3250)	0.2200
trackA	(1376.5710, 2374.2450)	(1377.7090, 2374.3350)	0.0900
trackA	(1385.9450, 2377.1050)	(1386.9550, 2377.3250)	0.2200
trackA	(1385.8810, 2374.2450)	(1387.0190, 2374.3350)	0.0900
trackA	(1496.1810, 2417.0350)	(1497.5690, 2417.0650)	0.0300

DF.3b : Min/Max space from NCOMP to PCOMP in the same well for butted
COMP = 0.0

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2146:and

Structure (lower left x, y) (upper right x, y)

trackA	(1349.0800, 2389.7550)	(1349.8000, 2391.9650)
trackA	(1358.0600, 2389.7550)	(1358.9800, 2391.7750)
trackA	(1367.3700, 2389.7550)	(1368.2900, 2391.7750)
trackA	(1376.6800, 2389.7550)	(1377.6000, 2391.7750)
trackA	(1385.9900, 2389.7550)	(1386.9100, 2391.7750)
trackA	(1356.4800, 2388.8550)	(1357.2000, 2389.7550)
trackA	(1349.0800, 2383.9050)	(1349.8000, 2386.1150)
trackA	(1358.0600, 2383.9050)	(1358.9800, 2384.5250)
trackA	(1367.3700, 2383.9050)	(1368.2900, 2384.5250)
trackA	(1376.6800, 2383.9050)	(1377.6000, 2384.5250)
trackA	(1385.9900, 2383.9050)	(1386.9100, 2384.5250)
trackA	(1356.4800, 2383.0050)	(1357.2000, 2383.9050)
trackA	(1349.0800, 2378.0550)	(1349.8000, 2380.2650)

trackA (1356.4800, 2377.1550) (1357.2000, 2378.0550)
trackA (1349.0800, 2372.2050) (1349.8000, 2374.4150)
trackA (1356.4800, 2371.3050) (1357.2000, 2372.2050)
trackA (1349.0800, 2366.3550) (1349.8000, 2368.5650)
trackA (1356.4800, 2365.4550) (1357.2000, 2366.3550)
trackA (1358.1400, 2388.8550) (1358.9000, 2389.5450)
trackA (1367.4500, 2388.8550) (1368.2100, 2389.5450)
trackA (1376.7600, 2388.8550) (1377.5200, 2389.5450)
trackA (1386.0700, 2388.8550) (1386.8300, 2389.5450)
trackA (1454.5800, 2417.7950) (1455.3000, 2420.0050)
trackA (1462.6750, 2416.8950) (1463.3950, 2417.7950)
trackA (1454.5800, 2410.1850) (1455.3000, 2412.3950)
trackA (1462.6750, 2409.2850) (1463.3950, 2410.1850)
trackA (1496.3800, 2409.2850) (1497.0600, 2410.1850)
trackA (1454.5800, 2402.5750) (1455.3000, 2404.7850)
trackA (1462.6750, 2401.6750) (1463.3950, 2402.5750)
trackA (1496.3800, 2401.6750) (1497.0600, 2402.5750)
trackA (1454.5800, 2394.9650) (1455.3000, 2397.1750)
trackA (1462.6750, 2394.0650) (1463.3950, 2394.9650)
trackA (1496.3800, 2394.0650) (1497.0600, 2394.9650)
trackA (1454.5800, 2387.3550) (1455.3000, 2389.5650)
trackA (1462.6750, 2386.4550) (1463.3950, 2387.3550)
trackA (1496.3800, 2386.4550) (1497.0600, 2387.3550)
trackA (1454.5800, 2379.7450) (1455.3000, 2381.9550)
trackA (1462.6750, 2378.8450) (1463.3950, 2379.7450)
trackA (1496.3800, 2378.8450) (1497.0600, 2379.7450)
trackA (1454.5800, 2372.1350) (1455.3000, 2374.3450)
trackA (1462.6750, 2371.2350) (1463.3950, 2372.1350)
trackA (1496.3800, 2371.2350) (1497.0600, 2372.1350)
trackA (1454.5800, 2364.5250) (1455.3000, 2366.7350)
trackA (1462.6750, 2363.6250) (1463.3950, 2364.5250)
trackA (1496.3800, 2363.6250) (1497.0600, 2364.5250)
trackA (1496.3800, 2417.0650) (1497.2100, 2417.1950)
trackA (1358.0600, 2367.7950) (1358.9800, 2368.5650)
trackA (1367.3700, 2367.7950) (1368.2900, 2368.5650)
trackA (1376.6800, 2367.7950) (1377.6000, 2368.5650)
trackA (1385.9900, 2367.7950) (1386.9100, 2368.5650)
trackA (1496.5400, 2416.8950) (1497.3800, 2417.0350)

DN.2 : Min. DNWELL Space : 5.42

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:1961:external1

Structure (lower left x, y) (upper right x, y) Distance

trackA (522.8900, 1255.0950) (535.9800, 1260.3950) 5.3000
trackA (593.3900, 1255.0950) (606.4800, 1260.3950) 5.3000
trackA (663.8900, 1255.0950) (676.9800, 1260.3950) 5.3000
trackA (734.3900, 1255.0950) (747.4800, 1260.3950) 5.3000

DN.3 : Each DNWELL shall be directly surrounded by PCOMP guard ring
tied to the P-substrate potential

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:1971:and

Structure (lower left x, y) (upper right x, y)

trackA	(1787.0200, 2579.7850) (1790.1200, 2582.9900)
trackA	(1796.1500, 2579.8050) (1799.2500, 2583.0100)
trackA	(1217.6150, 2298.7250) (1227.2750, 2315.0450)
trackA	(1218.3450, 2319.6150) (1227.2050, 2339.7150)
trackA	(1236.6400, 2352.4200) (1262.6100, 2423.1100)
trackA	(1248.3400, 2330.7200) (1262.3000, 2347.4000)
trackA	(1287.7150, 2294.2350) (1310.8350, 2358.2150)
trackA	(1312.7550, 2294.2350) (1336.9950, 2365.3350)
trackA	(1620.3500, 2313.1050) (1682.4800, 2332.9850)
trackA	(1620.3500, 2334.9850) (1682.4800, 2354.8650)
trackA	(1639.8300, 2285.7550) (1659.7300, 2305.2850)
trackA	(1649.5100, 2356.8650) (1682.4800, 2376.7450)
trackA	(1459.5750, 2416.3750) (1497.9000, 2420.5250)
trackA	(1459.5750, 2408.7650) (1497.9000, 2412.9150)
trackA	(1459.5750, 2401.1550) (1497.9000, 2405.3050)
trackA	(1459.5750, 2393.5450) (1497.9000, 2397.6950)
trackA	(1459.5750, 2385.9350) (1497.9000, 2390.0850)
trackA	(1459.5750, 2378.3250) (1497.9000, 2382.4750)
trackA	(1459.5750, 2370.7150) (1497.9000, 2374.8650)
trackA	(1459.5750, 2363.1050) (1497.9000, 2367.2550)
trackA	(1615.0600, 2118.4350) (1659.8600, 2188.2750)
trackA	(1661.5650, 2118.4350) (1682.0050, 2188.2750)
trackA	(458.0100, 1161.2550) (462.3300, 1164.9150)

trackA	(458.0100, 1182.5350)	(460.6000, 1185.0750)
trackA	(465.8500, 1157.8950)	(470.1700, 1159.8750)
trackA	(465.8500, 1182.5350)	(468.4400, 1183.9550)
trackA	(467.5800, 1162.3750)	(470.1700, 1163.7950)
trackA	(473.6900, 1157.8950)	(478.0100, 1159.8750)
trackA	(473.6900, 1182.5350)	(476.2800, 1183.9550)
trackA	(475.4200, 1162.3750)	(478.0100, 1163.7950)
trackA	(481.5300, 1171.3350)	(484.1200, 1175.5550)
trackA	(481.5300, 1195.9750)	(484.1200, 1197.3950)
trackA	(483.2600, 1157.8950)	(485.8500, 1159.8750)
trackA	(483.2600, 1190.3750)	(485.8500, 1192.9150)
trackA	(489.3700, 1157.8950)	(493.6900, 1160.4350)
trackA	(489.3700, 1180.2950)	(493.6900, 1182.2750)
trackA	(489.3700, 1182.5350)	(491.9600, 1183.9550)
trackA	(491.1000, 1170.2150)	(493.6900, 1177.7950)
trackA	(497.2100, 1157.8950)	(499.8000, 1160.4350)
trackA	(497.2100, 1162.9350)	(499.8000, 1164.3550)
trackA	(497.2100, 1175.8150)	(499.8000, 1177.7950)
trackA	(497.2100, 1182.5350)	(499.8000, 1183.9550)
trackA	(2120.8250, 934.9300)	(2176.7350, 965.7100)
trackA	(2227.2450, 934.9300)	(2283.1550, 965.7100)
trackA	(2285.1650, 874.3400)	(2312.0750, 945.6800)
trackA	(865.7850, 510.8700)	(887.9250, 521.3100)
trackA	(916.0650, 510.8700)	(934.1250, 521.3100)
trackA	(936.4350, 510.0200)	(954.4950, 521.5600)
trackA	(1151.9100, 545.9050)	(1165.9800, 573.2150)
trackA	(1151.9100, 577.8300)	(1165.9800, 595.4700)
trackA	(1185.6000, 538.6550)	(1203.6700, 565.9650)
trackA	(1215.6900, 538.6550)	(1233.7600, 565.9650)
trackA	(1245.7700, 538.6550)	(1263.8400, 565.9650)
trackA	(1275.8500, 538.6550)	(1367.1800, 565.9650)
trackA	(1379.1900, 538.6550)	(1592.6200, 565.9650)
trackA	(797.0200, 358.6400)	(839.1800, 371.8200)
trackA	(897.0100, 358.6400)	(939.1700, 371.8200)
trackA	(2499.4500, 448.3150)	(2524.3000, 460.7150)
trackA	(1605.4750, 2193.2750)	(1640.7750, 2283.2250)
trackA	(1642.4750, 2193.2750)	(1659.7300, 2283.2250)
trackA	(2121.4050, 968.5250)	(2135.3050, 983.6150)
trackA	(2227.8250, 968.5250)	(2241.7250, 983.6150)
trackA	(1182.8000, 475.2700)	(1396.6900, 495.4900)
op_buffer	(-41.8950, -26.0800)	(-13.9250, -5.1100)
op_buffer	(-41.8950, 6.0500)	(-24.0450, 16.1600)
op_buffer	(-8.9250, -16.2750)	(8.9250, -5.1050)
Unnamed_02d9ae27	(-11.1900, -16.4200)	(11.1900, -5.3000)

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Unnamed_02d9ae27      (-11.1900, 15.0200) (11.1900, 27.2300)
transformed_9f8db47f   (-18.0350, -7.9850) (18.0350, 7.9850)
transformed_729ded33   (-18.0350, -7.9850) (18.0350, 7.9850)
gf180mcu_fd_sc_mcu7t5v0__buf_1   (-0.4300, 1.7600) (3.7900, 4.3500)
gf180mcu_fd_sc_mcu7t5v0__buf_4   (-0.4300, 1.7600) (8.2700, 4.3500)
gf180mcu_fd_sc_mcu7t5v0__antenna (-0.4300, 1.7600) (1.5500, 4.3500)
gf180mcu_fd_sc_mcu7t5v0__buf_3   (-0.4300, 1.7600) (6.0300, 4.3500)
gf180mcu_fd_sc_mcu7t5v0__fillcap_16 (-0.4300, 1.7600) (9.3900, 4.3500)
gf180mcu_fd_sc_mcu7t5v0__clkbuf_1 (-0.4300, 1.7600) (3.7900, 4.3500)
gf180mcu_fd_sc_mcu7t5v0__dffrnq_1 (-0.4300, 1.7600) (19.4700, 4.3500)
gf180mcu_fd_sc_mcu7t5v0__filltie (-0.4300, 1.7600) (1.5500, 4.3500)
gf180mcu_fd_sc_mcu7t5v0__fillcap_4 (-0.4300, 1.7600) (2.6700, 4.3500)
gf180mcu_fd_sc_mcu7t5v0__fillcap_8 (-0.4300, 1.7600) (4.9100, 4.3500)
gf180mcu_fd_sc_mcu7t5v0__endcap   (-0.4300, 1.7600) (1.5500, 4.3500)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64 (-0.4300, 1.7600) (36.2700, 4.3500)
gf180mcu_fd_sc_mcu7t5v0__fillcap_32 (-0.4300, 1.7600) (18.3500, 4.3500)
io_secondary_5p0       (22.6500, -7.2500) (35.8300, 34.9100)

```

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180mcu_drc.rs:1974:and

WARNING: The error count of 102 for this check exceeds the limit set in the runset. Details only available for the first 100.

Check was stopped early because error limit was reached.

```

-----
Structure      ( lower left x, y ) ( upper right x, y )
-----
trackA         (1787.6300, 2578.5250) (1789.1100, 2579.1850)
trackA         (1796.7650, 2578.5450) (1798.2450, 2579.2050)
trackA         (1459.5750, 2416.8950) (1497.2100, 2417.7950)
trackA         (1459.5750, 2409.2850) (1497.2100, 2410.1850)
trackA         (1459.5750, 2401.6750) (1497.2100, 2402.5750)
trackA         (1459.5750, 2394.0650) (1497.2100, 2394.9650)
trackA         (1459.5750, 2386.4550) (1497.2100, 2387.3550)
trackA         (1459.5750, 2378.8450) (1497.2100, 2379.7450)
trackA         (1459.5750, 2371.2350) (1497.2100, 2372.1350)
trackA         (1459.5750, 2363.6250) (1497.2100, 2364.5250)
trackA         (1219.6750, 2300.7850) (1225.2150, 2305.8050)
trackA         (1219.6750, 2307.9650) (1225.2150, 2312.9850)
trackA         (1220.0050, 2321.2750) (1225.5450, 2326.2950)
trackA         (1220.0050, 2327.1550) (1225.5450, 2332.1750)
trackA         (1220.0050, 2333.0350) (1225.5450, 2338.0550)
trackA         (1240.5700, 2354.7800) (1258.6800, 2371.2400)

```

trackA	(1240.5700, 2372.8750)	(1258.6800, 2387.1850)
trackA	(1240.5700, 2388.3450)	(1258.6800, 2402.6550)
trackA	(1240.5700, 2404.2900)	(1258.6800, 2420.7500)
trackA	(1250.0000, 2332.3800)	(1255.0400, 2336.2600)
trackA	(1250.0000, 2337.1200)	(1255.0400, 2341.0000)
trackA	(1250.0000, 2341.8600)	(1255.0400, 2345.7400)
trackA	(1256.9800, 2343.2400)	(1262.0200, 2347.1200)
trackA	(1288.0250, 2294.5450)	(1310.5250, 2357.9050)
trackA	(1313.0650, 2294.5450)	(1336.6850, 2365.0250)
trackA	(1496.5400, 2416.8950)	(1497.3800, 2417.0350)
trackA	(1620.6700, 2313.4250)	(1682.1600, 2332.0750)
trackA	(1620.6700, 2335.3050)	(1682.1600, 2353.9550)
trackA	(1640.1500, 2286.0750)	(1659.4100, 2304.9650)
trackA	(1649.8300, 2357.1850)	(1682.1600, 2375.8350)
trackA	(1615.3800, 2118.7550)	(1659.5400, 2187.9550)
trackA	(1665.5350, 2118.7550)	(1681.6850, 2187.9550)
trackA	(480.4500, 1171.9450)	(480.9300, 1173.4250)
trackA	(494.2900, 1170.8250)	(495.1100, 1176.7650)
trackA	(2121.1050, 935.2100)	(2176.4550, 965.4300)
trackA	(2227.5250, 935.2100)	(2282.8750, 965.4300)
trackA	(2285.4450, 874.6200)	(2311.7950, 945.4000)
trackA	(1276.1300, 538.9350)	(1366.9000, 565.6850)
trackA	(1379.4700, 538.9350)	(1592.3400, 565.6850)
trackA	(866.0650, 511.1500)	(887.6450, 521.0300)
trackA	(916.3450, 511.1500)	(933.8450, 521.0300)
trackA	(936.7150, 510.3000)	(954.2150, 521.2800)
trackA	(1152.1900, 546.1850)	(1165.7000, 572.9350)
trackA	(1152.1900, 578.1100)	(1165.7000, 595.1900)
trackA	(1185.8800, 538.9350)	(1203.3900, 565.6850)
trackA	(1215.9700, 538.9350)	(1233.4800, 565.6850)
trackA	(1246.0500, 538.9350)	(1263.5600, 565.6850)
trackA	(1466.0450, 2200.6850)	(1511.8050, 2277.2650)
trackA	(1605.7950, 2193.5950)	(1640.4550, 2282.9050)
trackA	(1649.7400, 2193.5950)	(1659.4100, 2282.9050)
trackA	(2121.6850, 968.8050)	(2135.0250, 983.3350)
op_buffer	(-41.3050, -25.4900)	(-14.5150, -5.7000)
op_buffer	(-41.3050, 6.6400)	(-24.6350, 15.5700)
op_buffer	(-8.3350, -15.6850)	(8.3350, -5.6950)
Unnamed_02d9ae27	(-10.6000, 15.6100)	(10.6000, 26.6450)
Unnamed_02d9ae27	(-10.6000, -15.8300)	(10.6000, -5.8900)
transformed_9f8db47f	(-17.4450, -7.3950)	(17.4450, 7.3950)
transformed_729ded33	(-17.4450, -7.3950)	(17.4450, 7.3950)
gf180mcu_fd_sc_mcu7t5v0__buf_1	(0.1800, 0.3400)	(3.0000, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__buf_4	(0.1800, 0.3400)	(7.2600, 1.1600)

gf180mcu_fd_sc_mcu7t5v0__antenna	(0.1800, 0.5900)	(0.5400, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__buf_3	(0.1800, 0.3400)	(5.2100, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_16	(6.9000, 0.3400)	(8.7800, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_16	(4.6600, 0.3400)	(6.5400, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_16	(2.4200, 0.3400)	(4.3000, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_16	(0.1800, 0.3400)	(2.0600, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__clkbuf_1	(0.1800, 0.5650)	(2.9600, 1.0600)
gf180mcu_fd_sc_mcu7t5v0__dffrnq_1	(17.3050, 0.3450)	(18.7850, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__dffrnq_1	(3.1600, 0.6200)	(16.9450, 1.2950)
gf180mcu_fd_sc_mcu7t5v0__dffrnq_1	(0.1800, 0.7550)	(2.7800, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__filltie	(0.3600, 1.9200)	(0.7600, 3.5600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_4	(0.1800, 0.3400)	(2.0600, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_8	(2.4200, 0.3400)	(4.3000, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_8	(0.1800, 0.3400)	(2.0600, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__endcap	(0.3600, 1.9200)	(0.7200, 3.5600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(33.7800, 0.3400)	(35.6600, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(31.5400, 0.3400)	(33.4200, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(29.3000, 0.3400)	(31.1800, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(27.0600, 0.3400)	(28.9400, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(24.8200, 0.3400)	(26.7000, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(22.5800, 0.3400)	(24.4600, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(20.3400, 0.3400)	(22.2200, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(18.1000, 0.3400)	(19.9800, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(15.8600, 0.3400)	(17.7400, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(13.6200, 0.3400)	(15.5000, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(11.3800, 0.3400)	(13.2600, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(9.1400, 0.3400)	(11.0200, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(6.9000, 0.3400)	(8.7800, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(4.6600, 0.3400)	(6.5400, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(2.4200, 0.3400)	(4.3000, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_64	(0.1800, 0.3400)	(2.0600, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_32	(15.8600, 0.3400)	(17.7400, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_32	(13.6200, 0.3400)	(15.5000, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_32	(11.3800, 0.3400)	(13.2600, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_32	(9.1400, 0.3400)	(11.0200, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_32	(6.9000, 0.3400)	(8.7800, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_32	(4.6600, 0.3400)	(6.5400, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_32	(2.4200, 0.3400)	(4.3000, 1.1600)
gf180mcu_fd_sc_mcu7t5v0__fillcap_32	(0.1800, 0.3400)	(2.0600, 1.1600)
io_secondary_5p0	(22.7700, -7.1300)	(35.7100, 34.7900)

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:1981:and

Structure (lower left x, y) (upper right x, y)

trackA (2076.8300, 2011.2600) (2117.2800, 2027.8700)

trackA (1284.1750, 2291.3750) (1459.5750, 2425.1450)

trackA (1499.4000, 2331.9850) (1545.9700, 2414.1750)

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:1984:not_outside

Structure (lower left x, y) (upper right x, y)

trackA (1284.1750, 2291.3750) (1459.5750, 2425.1450)

trackA (1499.4000, 2331.9850) (1545.9700, 2414.1750)

trackA (2076.8300, 2011.2600) (2117.2800, 2027.8700)

trackA (522.8900, 1233.1950) (535.9800, 1255.0950)

trackA (522.8900, 1260.3950) (535.9800, 1282.2950)

trackA (593.3900, 1233.1950) (606.4800, 1255.0950)

trackA (593.3900, 1260.3950) (606.4800, 1282.2950)

trackA (663.8900, 1233.1950) (676.9800, 1255.0950)

trackA (663.8900, 1260.3950) (676.9800, 1282.2950)

trackA (734.3900, 1233.1950) (747.4800, 1255.0950)

trackA (734.3900, 1260.3950) (747.4800, 1282.2950)

DV.1 : Min. Dualgate enclose DNWELL = 0.5

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:6130:enclose

Structure (lower left x, y) (upper right x, y) Distance

trackA (1132.2950, 2367.5050) (1179.8850, 2367.5060) 0.0000

trackA (1132.2950, 2415.4940) (1179.8850, 2415.4950) 0.0000

trackA (1179.8840, 2367.5050) (1179.8850, 2415.4950) 0.0000

trackA (1132.2950, 2367.5050) (1132.2960, 2415.4950) 0.0000

trackA (1280.2000, 2222.7790) (1390.1800, 2222.7800) 0.0000

trackA (1284.1750, 2380.5400) (1340.0950, 2380.5410) 0.0000

trackA (1340.0950, 2352.2350) (1396.9150, 2352.2360) 0.0000

trackA (1396.9150, 2291.3750) (1459.5750, 2291.3760) 0.0000

trackA (1284.1750, 2425.1440) (1459.5750, 2425.1450) 0.0000

trackA (1459.5740, 2291.3750) (1459.5750, 2362.6050) 0.0000

trackA (1459.5740, 2367.7550) (1459.5750, 2370.2150) 0.0000

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trackA (1459.5740, 2375.3650) (1459.5750, 2377.8250) 0.0000
trackA (1459.5740, 2382.9750) (1459.5750, 2385.4350) 0.0000
trackA (1459.5740, 2390.5850) (1459.5750, 2393.0450) 0.0000
trackA (1459.5740, 2398.1950) (1459.5750, 2400.6550) 0.0000
trackA (1459.5740, 2405.8050) (1459.5750, 2408.2650) 0.0000
trackA (1459.5740, 2413.4150) (1459.5750, 2415.8750) 0.0000
trackA (1459.5740, 2421.0250) (1459.5750, 2425.1450) 0.0000
trackA (1284.1750, 2380.5400) (1284.1760, 2425.1450) 0.0000
trackA (1340.0950, 2352.2350) (1340.0960, 2380.5400) 0.0000
trackA (1396.9150, 2291.3750) (1396.9160, 2352.2350) 0.0000
trackA (1280.2000, 2117.6200) (1390.1800, 2117.6210) 0.0000
trackA (1390.1790, 2117.6200) (1390.1800, 2222.7800) 0.0000
trackA (1280.2000, 2117.6200) (1280.2010, 2222.7800) 0.0000

```

HRES.10 : Minimum/Maximum Pplus overlap of SAB = 0.1

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:3917:interacting

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-----
Structure      ( lower left x, y ) ( upper right x, y )
-----
trackA          (1289.3750, 2297.0950) (1290.3750, 2302.0950)
trackA          (1289.3750, 2305.7550) (1290.3750, 2310.7550)
trackA          (1289.3750, 2314.4150) (1290.3750, 2319.4150)
trackA          (1289.3750, 2323.0750) (1290.3750, 2328.0750)
trackA          (1289.3750, 2331.7350) (1290.3750, 2336.7350)
trackA          (1289.3750, 2340.3950) (1290.3750, 2345.3950)
trackA          (1289.3750, 2349.0550) (1290.3750, 2354.0550)
trackA          (1293.1350, 2297.0950) (1294.1350, 2302.0950)
trackA          (1293.1350, 2305.7550) (1294.1350, 2310.7550)
trackA          (1293.1350, 2314.4150) (1294.1350, 2319.4150)
trackA          (1293.1350, 2323.0750) (1294.1350, 2328.0750)
trackA          (1293.1350, 2331.7350) (1294.1350, 2336.7350)
trackA          (1293.1350, 2340.3950) (1294.1350, 2345.3950)
trackA          (1293.1350, 2349.0550) (1294.1350, 2354.0550)
trackA          (1296.8950, 2297.0950) (1297.8950, 2302.0950)
trackA          (1296.8950, 2305.7550) (1297.8950, 2310.7550)
trackA          (1296.8950, 2314.4150) (1297.8950, 2319.4150)
trackA          (1296.8950, 2323.0750) (1297.8950, 2328.0750)
trackA          (1296.8950, 2331.7350) (1297.8950, 2336.7350)
trackA          (1296.8950, 2340.3950) (1297.8950, 2345.3950)

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trackA	(1296.8950, 2349.0550) (1297.8950, 2354.0550)
trackA	(1300.6550, 2297.0950) (1301.6550, 2302.0950)
trackA	(1300.6550, 2305.7550) (1301.6550, 2310.7550)
trackA	(1300.6550, 2314.4150) (1301.6550, 2319.4150)
trackA	(1300.6550, 2323.0750) (1301.6550, 2328.0750)
trackA	(1300.6550, 2331.7350) (1301.6550, 2336.7350)
trackA	(1300.6550, 2340.3950) (1301.6550, 2345.3950)
trackA	(1300.6550, 2349.0550) (1301.6550, 2354.0550)
trackA	(1304.4150, 2297.0950) (1305.4150, 2302.0950)
trackA	(1304.4150, 2305.7550) (1305.4150, 2310.7550)
trackA	(1304.4150, 2314.4150) (1305.4150, 2319.4150)
trackA	(1304.4150, 2323.0750) (1305.4150, 2328.0750)
trackA	(1304.4150, 2331.7350) (1305.4150, 2336.7350)
trackA	(1304.4150, 2340.3950) (1305.4150, 2345.3950)
trackA	(1304.4150, 2349.0550) (1305.4150, 2354.0550)
trackA	(1308.1750, 2297.0950) (1309.1750, 2302.0950)
trackA	(1308.1750, 2305.7550) (1309.1750, 2310.7550)
trackA	(1308.1750, 2314.4150) (1309.1750, 2319.4150)
trackA	(1308.1750, 2323.0750) (1309.1750, 2328.0750)
trackA	(1308.1750, 2331.7350) (1309.1750, 2336.7350)
trackA	(1308.1750, 2340.3950) (1309.1750, 2345.3950)
trackA	(1308.1750, 2349.0550) (1309.1750, 2354.0550)
trackA	(1314.4150, 2297.0950) (1315.4150, 2307.0950)
trackA	(1314.4150, 2310.7550) (1315.4150, 2320.7550)
trackA	(1314.4150, 2324.4150) (1315.4150, 2334.4150)
trackA	(1314.4150, 2338.0750) (1315.4150, 2348.0750)
trackA	(1314.4150, 2351.7350) (1315.4150, 2361.7350)
trackA	(1318.1750, 2297.0950) (1319.1750, 2307.0950)
trackA	(1318.1750, 2310.7550) (1319.1750, 2320.7550)
trackA	(1318.1750, 2324.4150) (1319.1750, 2334.4150)
trackA	(1318.1750, 2338.0750) (1319.1750, 2348.0750)
trackA	(1318.1750, 2351.7350) (1319.1750, 2361.7350)
trackA	(1321.9350, 2297.0950) (1322.9350, 2307.0950)
trackA	(1321.9350, 2310.7550) (1322.9350, 2320.7550)
trackA	(1321.9350, 2324.4150) (1322.9350, 2334.4150)
trackA	(1321.9350, 2338.0750) (1322.9350, 2348.0750)
trackA	(1321.9350, 2351.7350) (1322.9350, 2361.7350)
trackA	(1325.6950, 2297.0950) (1326.6950, 2307.0950)
trackA	(1325.6950, 2310.7550) (1326.6950, 2320.7550)
trackA	(1325.6950, 2324.4150) (1326.6950, 2334.4150)
trackA	(1325.6950, 2338.0750) (1326.6950, 2348.0750)
trackA	(1325.6950, 2351.7350) (1326.6950, 2361.7350)
trackA	(1329.4550, 2297.0950) (1330.4550, 2307.0950)
trackA	(1329.4550, 2310.7550) (1330.4550, 2320.7550)

trackA	(1329.4550, 2324.4150)	(1330.4550, 2334.4150)
trackA	(1329.4550, 2338.0750)	(1330.4550, 2348.0750)
trackA	(1329.4550, 2351.7350)	(1330.4550, 2361.7350)
trackA	(1333.2150, 2297.0950)	(1334.2150, 2307.0950)
trackA	(1333.2150, 2310.7550)	(1334.2150, 2320.7550)
trackA	(1333.2150, 2324.4150)	(1334.2150, 2334.4150)
trackA	(1333.2150, 2338.0750)	(1334.2150, 2348.0750)
trackA	(1333.2150, 2351.7350)	(1334.2150, 2361.7350)
op_buffer	(-4.0000, -72.3300)	(-3.0000, -72.2200)
op_buffer	(-4.0000, -59.6900)	(-3.0000, -59.5800)
op_buffer	(-4.0000, -54.3600)	(-3.0000, -54.2500)
op_buffer	(-4.0000, -41.7200)	(-3.0000, -41.6100)
op_buffer	(-2.6000, -72.3300)	(-1.6000, -72.2200)
op_buffer	(-2.6000, -59.6900)	(-1.6000, -59.5800)
op_buffer	(-2.6000, -54.3600)	(-1.6000, -54.2500)
op_buffer	(-2.6000, -41.7200)	(-1.6000, -41.6100)
op_buffer	(-1.2000, -72.3300)	(-0.2000, -72.2200)
op_buffer	(-1.2000, -59.6900)	(-0.2000, -59.5800)
op_buffer	(-1.2000, -54.3600)	(-0.2000, -54.2500)
op_buffer	(-1.2000, -41.7200)	(-0.2000, -41.6100)
op_buffer	(0.2000, -72.3300)	(1.2000, -72.2200)
op_buffer	(0.2000, -59.6900)	(1.2000, -59.5800)
op_buffer	(0.2000, -54.3600)	(1.2000, -54.2500)
op_buffer	(0.2000, -41.7200)	(1.2000, -41.6100)
op_buffer	(1.6000, -72.3300)	(2.6000, -72.2200)
op_buffer	(1.6000, -59.6900)	(2.6000, -59.5800)
op_buffer	(1.6000, -54.3600)	(2.6000, -54.2500)
op_buffer	(1.6000, -41.7200)	(2.6000, -41.6100)
op_buffer	(3.0000, -72.3300)	(4.0000, -72.2200)
op_buffer	(3.0000, -59.6900)	(4.0000, -59.5800)
op_buffer	(3.0000, -54.3600)	(4.0000, -54.2500)
op_buffer	(3.0000, -41.7200)	(4.0000, -41.6100)
ppolyf_u_high_Rs_resistor\$1	(10.0000, 0.0000)	(10.1000, 1.0000)
ppolyf_u_high_Rs_resistor\$1	(-0.1000, 0.0000)	(0.0000, 1.0000)
ppolyf_u_high_Rs_resistor	(5.0000, 0.0000)	(5.1000, 1.0000)
ppolyf_u_high_Rs_resistor	(-0.1000, 0.0000)	(0.0000, 1.0000)

HRES.12 : P type Poly2 resistor (high sheet rho) shall be covered by RES_MK marking.
RES_MK length shall be coincide with resistor length (Defined by Pplus space)
and width covering the width of Poly2.

If the size of single RES_MK mark layer is greater than 15000 um2
and both sides (X and Y) are greater than 80 um, then the minimum
spacing to adjacent RES_MK layer >= 20
Checked in PRES.9

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:3928:xor

Structure (lower left x, y) (upper right x, y)

op_buffer (3.0000, -41.7350) (4.0000, -41.7200)
op_buffer (3.0000, -54.2500) (4.0000, -54.2350)
op_buffer (3.0000, -59.7050) (4.0000, -59.6900)
op_buffer (3.0000, -72.2200) (4.0000, -72.2050)
op_buffer (1.6000, -41.7350) (2.6000, -41.7200)
op_buffer (1.6000, -54.2500) (2.6000, -54.2350)
op_buffer (1.6000, -59.7050) (2.6000, -59.6900)
op_buffer (1.6000, -72.2200) (2.6000, -72.2050)
op_buffer (0.2000, -41.7350) (1.2000, -41.7200)
op_buffer (0.2000, -54.2500) (1.2000, -54.2350)
op_buffer (0.2000, -59.7050) (1.2000, -59.6900)
op_buffer (0.2000, -72.2200) (1.2000, -72.2050)
op_buffer (-1.2000, -41.7350) (-0.2000, -41.7200)
op_buffer (-1.2000, -54.2500) (-0.2000, -54.2350)
op_buffer (-1.2000, -59.7050) (-0.2000, -59.6900)
op_buffer (-1.2000, -72.2200) (-0.2000, -72.2050)
op_buffer (-2.6000, -41.7350) (-1.6000, -41.7200)
op_buffer (-2.6000, -54.2500) (-1.6000, -54.2350)
op_buffer (-2.6000, -59.7050) (-1.6000, -59.6900)
op_buffer (-2.6000, -72.2200) (-1.6000, -72.2050)
op_buffer (-4.0000, -41.7350) (-3.0000, -41.7200)
op_buffer (-4.0000, -54.2500) (-3.0000, -54.2350)
op_buffer (-4.0000, -59.7050) (-3.0000, -59.6900)
op_buffer (-4.0000, -72.2200) (-3.0000, -72.2050)
ppolyf_u_high_Rs_resistor\$1 (-0.6400, 0.0000) (10.6400, 1.0000)
ppolyf_u_high_Rs_resistor (-0.6400, 0.0000) (5.6400, 1.0000)

HRES.2 : Min width of Poly2 resistor = 1.0

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mcu_drc.rs:3880:internal1

Structure (lower left x, y) (upper right x, y) Distance

op_buffer (-4.0000, -72.8600) (-3.0700, -72.3470) 0.9300
op_buffer (-3.9300, -72.8600) (-3.0000, -72.3470) 0.9300
op_buffer (-3.9300, -72.8600) (-3.0700, -72.7150) 0.8600
op_buffer (-2.6000, -72.8600) (-1.6700, -72.3470) 0.9300
op_buffer (-2.5300, -72.8600) (-1.6000, -72.3470) 0.9300
op_buffer (-2.5300, -72.8600) (-1.6700, -72.7150) 0.8600
op_buffer (-1.2000, -72.8600) (-0.2700, -72.3470) 0.9300
op_buffer (-1.1300, -72.8600) (-0.2000, -72.3470) 0.9300
op_buffer (-1.1300, -72.8600) (-0.2700, -72.7150) 0.8600
op_buffer (0.2000, -72.8600) (1.1300, -72.3470) 0.9300
op_buffer (0.2700, -72.8600) (1.2000, -72.3470) 0.9300
op_buffer (0.2700, -72.8600) (1.1300, -72.7150) 0.8600
op_buffer (1.6000, -72.8600) (2.5300, -72.3470) 0.9300
op_buffer (1.6700, -72.8600) (2.6000, -72.3470) 0.9300
op_buffer (1.6700, -72.8600) (2.5300, -72.7150) 0.8600
op_buffer (3.0000, -72.8600) (3.9300, -72.3470) 0.9300
op_buffer (3.0700, -72.8600) (4.0000, -72.3470) 0.9300
op_buffer (3.0700, -72.8600) (3.9300, -72.7150) 0.8600
op_buffer (-3.9300, -59.5630) (-3.0000, -59.0500) 0.9300
op_buffer (-4.0000, -59.5630) (-3.0700, -59.0500) 0.9300
op_buffer (-3.9300, -59.1950) (-3.0700, -59.0500) 0.8600
op_buffer (-2.5300, -59.5630) (-1.6000, -59.0500) 0.9300
op_buffer (-2.6000, -59.5630) (-1.6700, -59.0500) 0.9300
op_buffer (-2.5300, -59.1950) (-1.6700, -59.0500) 0.8600
op_buffer (-1.1300, -59.5630) (-0.2000, -59.0500) 0.9300
op_buffer (-1.2000, -59.5630) (-0.2700, -59.0500) 0.9300
op_buffer (-1.1300, -59.1950) (-0.2700, -59.0500) 0.8600
op_buffer (0.2700, -59.5630) (1.2000, -59.0500) 0.9300
op_buffer (0.2000, -59.5630) (1.1300, -59.0500) 0.9300
op_buffer (0.2700, -59.1950) (1.1300, -59.0500) 0.8600
op_buffer (1.6700, -59.5630) (2.6000, -59.0500) 0.9300
op_buffer (1.6000, -59.5630) (2.5300, -59.0500) 0.9300
op_buffer (1.6700, -59.1950) (2.5300, -59.0500) 0.8600
op_buffer (3.0700, -59.5630) (4.0000, -59.0500) 0.9300
op_buffer (3.0000, -59.5630) (3.9300, -59.0500) 0.9300
op_buffer (3.0700, -59.1950) (3.9300, -59.0500) 0.8600
op_buffer (-4.0000, -54.8900) (-3.0700, -54.3770) 0.9300
op_buffer (-3.9300, -54.8900) (-3.0000, -54.3770) 0.9300
op_buffer (-3.9300, -54.8900) (-3.0700, -54.7450) 0.8600

```

op_buffer (-2.6000, -54.8900) (-1.6700, -54.3770) 0.9300
op_buffer (-2.5300, -54.8900) (-1.6000, -54.3770) 0.9300
op_buffer (-2.5300, -54.8900) (-1.6700, -54.7450) 0.8600
op_buffer (-1.2000, -54.8900) (-0.2700, -54.3770) 0.9300
op_buffer (-1.1300, -54.8900) (-0.2000, -54.3770) 0.9300
op_buffer (-1.1300, -54.8900) (-0.2700, -54.7450) 0.8600
op_buffer (0.2000, -54.8900) (1.1300, -54.3770) 0.9300
op_buffer (0.2700, -54.8900) (1.2000, -54.3770) 0.9300
op_buffer (0.2700, -54.8900) (1.1300, -54.7450) 0.8600
op_buffer (1.6000, -54.8900) (2.5300, -54.3770) 0.9300
op_buffer (1.6700, -54.8900) (2.6000, -54.3770) 0.9300
op_buffer (1.6700, -54.8900) (2.5300, -54.7450) 0.8600
op_buffer (3.0000, -54.8900) (3.9300, -54.3770) 0.9300
op_buffer (3.0700, -54.8900) (4.0000, -54.3770) 0.9300
op_buffer (3.0700, -54.8900) (3.9300, -54.7450) 0.8600
op_buffer (-3.9300, -41.5930) (-3.0000, -41.0800) 0.9300
op_buffer (-4.0000, -41.5930) (-3.0700, -41.0800) 0.9300
op_buffer (-3.9300, -41.2250) (-3.0700, -41.0800) 0.8600
op_buffer (-2.5300, -41.5930) (-1.6000, -41.0800) 0.9300
op_buffer (-2.6000, -41.5930) (-1.6700, -41.0800) 0.9300
op_buffer (-2.5300, -41.2250) (-1.6700, -41.0800) 0.8600
op_buffer (-1.1300, -41.5930) (-0.2000, -41.0800) 0.9300
op_buffer (-1.2000, -41.5930) (-0.2700, -41.0800) 0.9300
op_buffer (-1.1300, -41.2250) (-0.2700, -41.0800) 0.8600
op_buffer (0.2700, -41.5930) (1.2000, -41.0800) 0.9300
op_buffer (0.2000, -41.5930) (1.1300, -41.0800) 0.9300
op_buffer (0.2700, -41.2250) (1.1300, -41.0800) 0.8600
op_buffer (1.6700, -41.5930) (2.6000, -41.0800) 0.9300
op_buffer (1.6000, -41.5930) (2.5300, -41.0800) 0.9300
op_buffer (1.6700, -41.2250) (2.5300, -41.0800) 0.8600
op_buffer (3.0700, -41.5930) (4.0000, -41.0800) 0.9300
op_buffer (3.0000, -41.5930) (3.9300, -41.0800) 0.9300
op_buffer (3.0700, -41.2250) (3.9300, -41.0800) 0.8600

```

HRES.4 : Minimum RESISTOR overlap of Poly2 resistor = 0.4

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:3887:enclose

Structure (lower left x, y) (upper right x, y)

op_buffer (-4.3310, -72.9400) (-3.5990, -72.7150)
op_buffer (-4.3310, -41.2250) (-3.5990, -41.0000)
op_buffer (-4.3220, -72.9400) (-2.6780, -72.8600)
op_buffer (-4.3220, -41.0800) (-2.6780, -41.0000)
op_buffer (-3.4010, -72.9400) (-2.6690, -72.7150)
op_buffer (-3.4010, -41.2250) (-2.6690, -41.0000)
op_buffer (-2.9310, -72.9400) (-2.1990, -72.7150)
op_buffer (-2.9310, -41.2250) (-2.1990, -41.0000)
op_buffer (-2.9220, -72.9400) (-1.2780, -72.8600)
op_buffer (-2.9220, -41.0800) (-1.2780, -41.0000)
op_buffer (-2.0010, -72.9400) (-1.2690, -72.7150)
op_buffer (-2.0010, -41.2250) (-1.2690, -41.0000)
op_buffer (-1.5310, -72.9400) (-0.7990, -72.7150)
op_buffer (-1.5310, -41.2250) (-0.7990, -41.0000)
op_buffer (-1.5220, -72.9400) (0.1220, -72.8600)
op_buffer (-1.5220, -41.0800) (0.1220, -41.0000)
op_buffer (-0.6010, -72.9400) (0.1310, -72.7150)
op_buffer (-0.6010, -41.2250) (0.1310, -41.0000)
op_buffer (-0.1310, -72.9400) (0.6010, -72.7150)
op_buffer (-0.1310, -41.2250) (0.6010, -41.0000)
op_buffer (-0.1220, -72.9400) (1.5220, -72.8600)
op_buffer (-0.1220, -41.0800) (1.5220, -41.0000)
op_buffer (0.7990, -72.9400) (1.5310, -72.7150)
op_buffer (0.7990, -41.2250) (1.5310, -41.0000)
op_buffer (1.2690, -72.9400) (2.0010, -72.7150)
op_buffer (1.2690, -41.2250) (2.0010, -41.0000)
op_buffer (1.2780, -72.9400) (2.9220, -72.8600)
op_buffer (1.2780, -41.0800) (2.9220, -41.0000)
op_buffer (2.1990, -72.9400) (2.9310, -72.7150)
op_buffer (2.1990, -41.2250) (2.9310, -41.0000)
op_buffer (2.6690, -72.9400) (3.4010, -72.7150)
op_buffer (2.6690, -41.2250) (3.4010, -41.0000)
op_buffer (2.6780, -72.9400) (4.3220, -72.8600)
op_buffer (2.6780, -41.0800) (4.3220, -41.0000)
op_buffer (3.5990, -72.9400) (4.3310, -72.7150)
op_buffer (3.5990, -41.2250) (4.3310, -41.0000)

HRES.7 : Minimum Pplus overlap of contact on Poly2 resistor = 0.2

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:3897:enclose

Structure (lower left x, y) (upper right x, y)

op_buffer (-3.9920, -72.9400) (-3.5080, -72.7900)
op_buffer (-3.9920, -59.1200) (-3.5080, -58.9700)
op_buffer (-3.9920, -54.9700) (-3.5080, -54.8200)
op_buffer (-3.9920, -41.1500) (-3.5080, -41.0000)
op_buffer (-3.4920, -72.9400) (-3.0080, -72.7900)
op_buffer (-3.4920, -59.1200) (-3.0080, -58.9700)
op_buffer (-3.4920, -54.9700) (-3.0080, -54.8200)
op_buffer (-3.4920, -41.1500) (-3.0080, -41.0000)
op_buffer (-2.5920, -72.9400) (-2.1080, -72.7900)
op_buffer (-2.5920, -59.1200) (-2.1080, -58.9700)
op_buffer (-2.5920, -54.9700) (-2.1080, -54.8200)
op_buffer (-2.5920, -41.1500) (-2.1080, -41.0000)
op_buffer (-2.0920, -72.9400) (-1.6080, -72.7900)
op_buffer (-2.0920, -59.1200) (-1.6080, -58.9700)
op_buffer (-2.0920, -54.9700) (-1.6080, -54.8200)
op_buffer (-2.0920, -41.1500) (-1.6080, -41.0000)
op_buffer (-1.1920, -72.9400) (-0.7080, -72.7900)
op_buffer (-1.1920, -59.1200) (-0.7080, -58.9700)
op_buffer (-1.1920, -54.9700) (-0.7080, -54.8200)
op_buffer (-1.1920, -41.1500) (-0.7080, -41.0000)
op_buffer (-0.6920, -72.9400) (-0.2080, -72.7900)
op_buffer (-0.6920, -59.1200) (-0.2080, -58.9700)
op_buffer (-0.6920, -54.9700) (-0.2080, -54.8200)
op_buffer (-0.6920, -41.1500) (-0.2080, -41.0000)
op_buffer (0.2080, -72.9400) (0.6920, -72.7900)
op_buffer (0.2080, -59.1200) (0.6920, -58.9700)
op_buffer (0.2080, -54.9700) (0.6920, -54.8200)
op_buffer (0.2080, -41.1500) (0.6920, -41.0000)
op_buffer (0.7080, -72.9400) (1.1920, -72.7900)
op_buffer (0.7080, -59.1200) (1.1920, -58.9700)
op_buffer (0.7080, -54.9700) (1.1920, -54.8200)
op_buffer (0.7080, -41.1500) (1.1920, -41.0000)
op_buffer (1.6080, -72.9400) (2.0920, -72.7900)
op_buffer (1.6080, -59.1200) (2.0920, -58.9700)
op_buffer (1.6080, -54.9700) (2.0920, -54.8200)
op_buffer (1.6080, -41.1500) (2.0920, -41.0000)
op_buffer (2.1080, -72.9400) (2.5920, -72.7900)
op_buffer (2.1080, -59.1200) (2.5920, -58.9700)
op_buffer (2.1080, -54.9700) (2.5920, -54.8200)
op_buffer (2.1080, -41.1500) (2.5920, -41.0000)
op_buffer (3.0080, -72.9400) (3.4920, -72.7900)

op_buffer (3.0080, -59.1200) (3.4920, -58.9700)
op_buffer (3.0080, -54.9700) (3.4920, -54.8200)
op_buffer (3.0080, -41.1500) (3.4920, -41.0000)
op_buffer (3.5080, -72.9400) (3.9920, -72.7900)
op_buffer (3.5080, -59.1200) (3.9920, -58.9700)
op_buffer (3.5080, -54.9700) (3.9920, -54.8200)
op_buffer (3.5080, -41.1500) (3.9920, -41.0000)

HVNESD.13(b) : Max. at least one or nearest source contact to gate
edge space (SCGS) <= 1

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mcu_drc.rs:7058:not_interacting

Structure (lower left x, y) (upper right x, y)

comp018green_out_drv_nleg_4T\$1 (10.5500, 2.6600) (11.5500, 40.6600)
comp018green_out_drv_nleg_4T\$1 (1.0300, 2.6600) (2.0300, 40.6600)

HVNESD.8(c) : Max. at least one or nearest drain contact to gate edge
space (DCGS) <= 4

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mcu_drc.rs:7038:not_interacting

Structure (lower left x, y) (upper right x, y)

gf180mcu_fd_io__bi_t\$1 (59.1100, 75.6900) (63.1100, 113.6900)
gf180mcu_fd_io__bi_t\$1 (46.8900, 75.6900) (51.3700, 113.6900)
gf180mcu_fd_io__bi_t\$1 (35.1500, 75.6900) (39.6300, 113.6900)
gf180mcu_fd_io__bi_t\$1 (23.4100, 75.6900) (27.8900, 113.6900)
gf180mcu_fd_io__bi_t\$1 (11.6700, 75.6900) (15.6700, 113.6900)

HVPESD.11 : Source COMP must enclose by LVS_Source

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mcu_drc.rs:7139:not

Structure (lower left x, y) (upper right x, y)

comp018green_out_drv_nleg_4T\$1 (1.0300, 2.6600) (11.5500, 40.6600)

IO.0 : Guidelines : To flag I/O latch-up related violation:

(a) Non well tap COMP directly connected to PAD is recommended to
be marked by 'Latchup_MK' layer

(b) Min/max Latchup_MK layer overlap of COMP (directly connected to
Pad) = 0.0

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mcu_drc.rs:5629:xor

Structure (lower left x, y) (upper right x, y)

trackA (2049.9500, 2003.8300) (2054.0100, 2006.8300)

trackA (2054.7500, 2003.8300) (2058.8100, 2006.8300)

trackA (2059.5500, 2003.8300) (2063.6100, 2006.8300)

trackA (2064.3500, 2003.8300) (2068.4100, 2006.8300)

op_buffer (-37.6550, -36.7850) (-35.8750, -31.4850)

op_buffer (-37.6550, -22.5200) (-35.8750, -10.5200)

op_buffer (-37.6550, 0.1400) (-35.8750, 0.6400)

op_buffer (-37.6550, 9.6200) (-35.8750, 10.7500)

op_buffer (-35.1250, -36.7850) (-33.3450, -31.4850)

op_buffer (-35.1250, -22.5200) (-33.3450, -10.5200)

op_buffer (-35.1250, 0.1400) (-33.3450, 0.6400)

op_buffer (-35.1250, 9.6200) (-33.3450, 10.7500)

op_buffer (-32.5950, -36.7850) (-30.8150, -31.4850)

op_buffer (-32.5950, -22.5200) (-30.8150, -10.5200)

op_buffer (-32.5950, 0.1400) (-30.8150, 0.6400)

op_buffer (-32.5950, 9.6200) (-30.8150, 10.7500)

op_buffer (-30.0650, -36.7850) (-28.2850, -31.4850)

op_buffer (-30.0650, -22.5200) (-28.2850, -10.5200)

op_buffer (-30.0650, 0.1400) (-28.2850, 0.6400)

op_buffer (-30.0650, 9.6200) (-28.2850, 10.7500)

op_buffer (-27.5350, -36.7850) (-25.7550, -31.4850)

op_buffer (-27.5350, -22.5200) (-25.7550, -10.5200)

op_buffer (-25.0050, -36.7850) (-23.2250, -31.4850)

op_buffer (-25.0050, -22.5200) (-23.2250, -10.5200)
op_buffer (-22.4750, -36.7850) (-20.6950, -31.4850)
op_buffer (-22.4750, -22.5200) (-20.6950, -10.5200)
op_buffer (-19.9450, -36.7850) (-18.1650, -31.4850)
op_buffer (-19.9450, -22.5200) (-18.1650, -10.5200)

IO.1_a2 : For LV and MV

It should also be directly surrounded by an Nwell guard ring
(Non broken NCOMP ring inside Nwell).

Nwell guard ring shall be connected to the most positive supply.

Max space of Nwell guard ring to the NCOMP in Psub directly
connected to I/O pad = 15

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:5670:edge_size

Structure (lower left x, y) (upper right x, y)

trackA (2049.9450, 2003.8250) (2054.0150, 2006.8350)
trackA (2054.7450, 2003.8250) (2058.8150, 2006.8350)
trackA (2059.5450, 2003.8250) (2063.6150, 2006.8350)
trackA (2064.3450, 2003.8250) (2068.4150, 2006.8350)
op_buffer (-37.6600, -36.7900) (-35.8700, -31.4800)
op_buffer (-37.6600, 0.1350) (-35.8700, 0.6450)
op_buffer (-35.1300, -36.7900) (-33.3400, -31.4800)
op_buffer (-35.1300, 0.1350) (-33.3400, 0.6450)
op_buffer (-32.6000, -36.7900) (-30.8100, -31.4800)
op_buffer (-32.6000, 0.1350) (-30.8100, 0.6450)
op_buffer (-30.0700, -36.7900) (-28.2800, -31.4800)
op_buffer (-30.0700, 0.1350) (-28.2800, 0.6450)
op_buffer (-27.5400, -36.7900) (-25.7500, -31.4800)
op_buffer (-25.0100, -36.7900) (-23.2200, -31.4800)
op_buffer (-22.4800, -36.7900) (-20.6900, -31.4800)
op_buffer (-19.9500, -36.7900) (-18.1600, -31.4800)

IO.1_b : Within 15um from the edge of the NCOMP connected to I/O pad
(marked by Latchup_MK):

Max Nwell tap distance to PCOMP inside Nwell <= 2 (irrespective of
its direct connection to Pad)

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:5684:wide

Structure (lower left x, y) (upper right x, y)

op_buffer (-38.9450, -22.5250) (-38.5100, -16.5695)
op_buffer (-38.9450, -14.7755) (-38.5100, -10.5150)
op_buffer (-38.9450, 9.6150) (-38.5100, 10.7550)
op_buffer (-37.6600, -22.5250) (-35.8700, -16.4850)
op_buffer (-37.6600, -14.8600) (-35.8700, -10.5150)
op_buffer (-37.6600, 9.6150) (-35.8700, 10.7550)
op_buffer (-35.1300, -22.5250) (-33.3400, -16.4850)
op_buffer (-35.1300, -14.8600) (-33.3400, -10.5150)
op_buffer (-35.1300, 9.6150) (-33.3400, 10.7550)
op_buffer (-32.6000, -22.5250) (-30.8100, -16.4850)
op_buffer (-32.6000, -14.8600) (-30.8100, -10.5150)
op_buffer (-32.6000, 9.6150) (-30.8100, 10.7550)
op_buffer (-30.0700, -22.5250) (-28.2800, -16.4850)
op_buffer (-30.0700, -14.8600) (-28.2800, -10.5150)
op_buffer (-30.0700, 9.6150) (-28.2800, 10.7550)
op_buffer (-27.5400, -22.5250) (-25.7500, -16.4850)
op_buffer (-27.5400, -14.7860) (-25.7500, -10.5150)
op_buffer (-27.4300, 9.6150) (-26.9950, 10.7550)
op_buffer (-25.0100, -22.5250) (-23.2200, -16.4850)
op_buffer (-25.0100, -14.4645) (-23.2200, -10.5150)
op_buffer (-22.4800, -22.5250) (-20.6900, -16.4850)
op_buffer (-22.4800, -13.6810) (-20.6900, -10.5150)
op_buffer (-19.9500, -22.5250) (-18.1600, -16.4850)
op_buffer (-19.9500, -12.3265) (-18.1600, -10.5150)
op_buffer (-17.3100, -22.5250) (-16.8750, -16.5695)

IO.3_a2 : For LV and MV

It should also be directly surrounded by PCOMP guard ring outside Nwell.

PCOMP guardring shall be connected to the lowest potential.

Max space of guard ring PCOMP to the PCOMP in Nwell directly connected
to the I/O pad = 15

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:5734:edge_size

Structure (lower left x, y) (upper right x, y)

op_buffer (-37.6600, -22.5250) (-35.8700, -10.5150)
op_buffer (-37.6600, 9.6150) (-35.8700, 10.7550)
op_buffer (-35.1300, -22.5250) (-33.3400, -10.5150)
op_buffer (-35.1300, 9.6150) (-33.3400, 10.7550)
op_buffer (-32.6000, -22.5250) (-30.8100, -10.5150)
op_buffer (-32.6000, 9.6150) (-30.8100, 10.7550)
op_buffer (-30.0700, -22.5250) (-28.2800, -10.5150)
op_buffer (-30.0700, 9.6150) (-28.2800, 10.7550)
op_buffer (-27.5400, -22.5250) (-25.7500, -10.5150)
op_buffer (-25.0100, -22.5250) (-23.2200, -10.5150)
op_buffer (-22.4800, -22.5250) (-20.6900, -10.5150)
op_buffer (-19.9500, -22.5250) (-18.1600, -10.5150)

IO.3_b : For LV and MV

Within 10um from the edge of the PCOMP connected to I/O Pad (marked
by Latchup_MK):

Max P substrate tap distance to NCOMP outside Nwell <= 5.0 (irrespective
of its direct connection to Pad)

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:5746:wide

Structure (lower left x, y) (upper right x, y)

op_buffer (-35.8800, -32.5200) (-35.8700, -32.0250)
op_buffer (-35.1300, -32.5200) (-35.1200, -32.0250)
op_buffer (-33.3500, -32.5200) (-33.3400, -32.0250)
op_buffer (-32.6000, -32.5200) (-32.5900, -32.0250)
op_buffer (-30.8200, -32.5200) (-30.8100, -32.0250)
op_buffer (-30.0700, -32.5200) (-30.0600, -32.0250)
op_buffer (-28.2900, -32.5200) (-28.2800, -32.0250)
op_buffer (-27.5400, -32.5200) (-27.5300, -32.0250)
op_buffer (-25.7600, -32.5200) (-25.7500, -32.0250)
op_buffer (-25.0100, -32.5200) (-25.0000, -32.0250)
op_buffer (-23.2300, -32.5200) (-23.2200, -32.0250)
op_buffer (-22.4800, -32.5200) (-22.4700, -32.0250)
op_buffer (-20.7000, -32.5200) (-20.6900, -32.0250)
op_buffer (-19.9500, -32.5200) (-19.9400, -32.0250)

LPW.12 : LVPWELL cannot overlap with Nwell

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2021:and

Structure (lower left x, y) (upper right x, y)

transformed_9f8db47f (-18.0350, -7.9850) (18.0350, 7.9850)
transformed_729ded33 (-18.0350, -7.9850) (18.0350, 7.9850)

LU.3a_MV_LU.3b_MV_LU.3c_MV : Max. Psub tap outside (DNWELL and YMTP_MK)
space to any point in the boundary of Ncomp outside Nwell/DNWELL =
15 (MV)

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:5418:coincident_edge

Structure (lower left x, y) (upper right x, y)

trackA (1598.8600, 2332.4700) (1599.1200, 2332.4700)
trackA (1599.1200, 2330.2700) (1599.1200, 2332.4700)
trackA (1598.8600, 2330.2700) (1599.1200, 2330.2700)
trackA (1598.8600, 2337.7000) (1599.1200, 2337.7000)
trackA (1599.1200, 2335.5000) (1599.1200, 2337.7000)
trackA (1598.8600, 2335.5000) (1599.1200, 2335.5000)
trackA (1602.4100, 2330.2700) (1602.6700, 2330.2700)
trackA (1602.4100, 2330.2700) (1602.4100, 2332.4700)
trackA (1602.4100, 2332.4700) (1602.6700, 2332.4700)
trackA (1602.4100, 2335.5000) (1602.6700, 2335.5000)
trackA (1602.4100, 2335.5000) (1602.4100, 2337.7000)
trackA (1602.4100, 2337.7000) (1602.6700, 2337.7000)
trackA (1588.3700, 2147.0100) (1589.7300, 2147.0100)
trackA (1589.7300, 2145.2100) (1589.7300, 2147.0100)
trackA (1588.3700, 2145.2100) (1589.7300, 2145.2100)
trackA (1588.3700, 2151.8400) (1589.7300, 2151.8400)
trackA (1589.7300, 2150.0400) (1589.7300, 2151.8400)
trackA (1588.3700, 2150.0400) (1589.7300, 2150.0400)

trackA (1588.3700, 2156.6700) (1589.7300, 2156.6700)
 trackA (1589.7300, 2154.8700) (1589.7300, 2156.6700)
 trackA (1588.3700, 2154.8700) (1589.7300, 2154.8700)
 trackA (1588.3700, 2161.5000) (1589.7300, 2161.5000)
 trackA (1589.7300, 2159.7000) (1589.7300, 2161.5000)
 trackA (1588.3700, 2159.7000) (1589.7300, 2159.7000)
 trackA (1588.8100, 2092.2900) (1589.0700, 2092.2900)
 trackA (1589.0700, 2090.0900) (1589.0700, 2092.2900)
 trackA (1588.8100, 2090.0900) (1589.0700, 2090.0900)
 trackA (1588.8100, 2097.5200) (1589.0700, 2097.5200)
 trackA (1589.0700, 2095.3200) (1589.0700, 2097.5200)
 trackA (1588.8100, 2095.3200) (1589.0700, 2095.3200)
 trackA (1592.3600, 2090.0900) (1592.6200, 2090.0900)
 trackA (1592.3600, 2090.0900) (1592.3600, 2092.2900)
 trackA (1592.3600, 2092.2900) (1592.6200, 2092.2900)
 trackA (1592.3600, 2095.3200) (1592.6200, 2095.3200)
 trackA (1592.3600, 2095.3200) (1592.3600, 2097.5200)
 trackA (1592.3600, 2097.5200) (1592.6200, 2097.5200)
 trackA (1593.0200, 2145.2100) (1594.3800, 2145.2100)
 trackA (1593.0200, 2145.2100) (1593.0200, 2147.0100)
 trackA (1593.0200, 2147.0100) (1594.3800, 2147.0100)
 trackA (1593.0200, 2150.0400) (1594.3800, 2150.0400)
 trackA (1593.0200, 2150.0400) (1593.0200, 2151.8400)
 trackA (1593.0200, 2151.8400) (1594.3800, 2151.8400)
 trackA (1593.0200, 2154.8700) (1594.3800, 2154.8700)
 trackA (1593.0200, 2154.8700) (1593.0200, 2156.6700)
 trackA (1593.0200, 2156.6700) (1594.3800, 2156.6700)
 trackA (1593.0200, 2159.7000) (1594.3800, 2159.7000)
 trackA (1593.0200, 2159.7000) (1593.0200, 2161.5000)
 trackA (1593.0200, 2161.5000) (1594.3800, 2161.5000)

 LU.4a_LV : Max. Nwell tap outside DNWELL space to any point in the
 boundary of Pcomp inside Nwell = 50 (LV)
 For Nwell to Ncomp space outside DNWELL >= 2.0um

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
 mcu_drc.rs:5443:coincident_edge

 Structure (lower left x, y) (upper right x, y)

transformed_9f8db47f (-16.3900, 0.5750) (-14.6500, 0.5750)

transformed_9f8db47f (-14.6500, -4.4250) (-14.6500, 0.5750)
transformed_9f8db47f (-16.3900, -4.4250) (-14.6500, -4.4250)
transformed_9f8db47f (-16.3900, -4.4250) (-16.3900, 0.5750)
transformed_9f8db47f (-13.7900, 0.5750) (-7.4500, 0.5750)
transformed_9f8db47f (-7.4500, -4.4250) (-7.4500, 0.5750)
transformed_9f8db47f (-13.7900, -4.4250) (-7.4500, -4.4250)
transformed_9f8db47f (-13.7900, -4.4250) (-13.7900, 0.5750)
transformed_9f8db47f (-6.7100, 0.5750) (-0.3700, 0.5750)
transformed_9f8db47f (-0.3700, -4.4250) (-0.3700, 0.5750)
transformed_9f8db47f (-6.7100, -4.4250) (-0.3700, -4.4250)
transformed_9f8db47f (-6.7100, -4.4250) (-6.7100, 0.5750)
transformed_9f8db47f (0.3700, 0.5750) (6.7100, 0.5750)
transformed_9f8db47f (6.7100, -4.4250) (6.7100, 0.5750)
transformed_9f8db47f (0.3700, -4.4250) (6.7100, -4.4250)
transformed_9f8db47f (0.3700, -4.4250) (0.3700, 0.5750)
transformed_9f8db47f (7.4500, 0.5750) (13.7900, 0.5750)
transformed_9f8db47f (13.7900, -4.4250) (13.7900, 0.5750)
transformed_9f8db47f (7.4500, -4.4250) (13.7900, -4.4250)
transformed_9f8db47f (7.4500, -4.4250) (7.4500, 0.5750)
transformed_9f8db47f (14.6500, 0.5750) (16.3900, 0.5750)
transformed_9f8db47f (16.3900, -4.4250) (16.3900, 0.5750)
transformed_9f8db47f (14.6500, -4.4250) (16.3900, -4.4250)
transformed_9f8db47f (14.6500, -4.4250) (14.6500, 0.5750)
transformed_729ded33 (-16.3900, 0.5750) (-14.6500, 0.5750)
transformed_729ded33 (-14.6500, -4.4250) (-14.6500, 0.5750)
transformed_729ded33 (-16.3900, -4.4250) (-14.6500, -4.4250)
transformed_729ded33 (-16.3900, -4.4250) (-16.3900, 0.5750)
transformed_729ded33 (-13.7900, 0.5750) (-7.4500, 0.5750)
transformed_729ded33 (-7.4500, -4.4250) (-7.4500, 0.5750)
transformed_729ded33 (-13.7900, -4.4250) (-7.4500, -4.4250)
transformed_729ded33 (-13.7900, -4.4250) (-13.7900, 0.5750)
transformed_729ded33 (-6.7100, 0.5750) (-0.3700, 0.5750)
transformed_729ded33 (-0.3700, -4.4250) (-0.3700, 0.5750)
transformed_729ded33 (-6.7100, -4.4250) (-0.3700, -4.4250)
transformed_729ded33 (-6.7100, -4.4250) (-6.7100, 0.5750)
transformed_729ded33 (0.3700, 0.5750) (6.7100, 0.5750)
transformed_729ded33 (6.7100, -4.4250) (6.7100, 0.5750)
transformed_729ded33 (0.3700, -4.4250) (6.7100, -4.4250)
transformed_729ded33 (0.3700, -4.4250) (0.3700, 0.5750)
transformed_729ded33 (7.4500, 0.5750) (13.7900, 0.5750)
transformed_729ded33 (13.7900, -4.4250) (13.7900, 0.5750)
transformed_729ded33 (7.4500, -4.4250) (13.7900, -4.4250)
transformed_729ded33 (7.4500, -4.4250) (7.4500, 0.5750)
transformed_729ded33 (14.6500, 0.5750) (16.3900, 0.5750)

transformed_729ded33 (16.3900, -4.4250) (16.3900, 0.5750)
transformed_729ded33 (14.6500, -4.4250) (16.3900, -4.4250)
transformed_729ded33 (14.6500, -4.4250) (14.6500, 0.5750)

LU.4a_MV_LU.4b_MV_LU.4c_MV : Max. Nwell tap outside DNWELL space to
any point in the boundary of Pcomp inside Nwell = 15 (MV)

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:5481:coincident_edge

Structure (lower left x, y) (upper right x, y)

trackA (1787.7300, 2581.2850) (1789.1100, 2581.2850)
trackA (1789.1100, 2580.3850) (1789.1100, 2581.2850)
trackA (1787.7300, 2580.3850) (1789.1100, 2580.3850)
trackA (1787.7300, 2580.3850) (1787.7300, 2581.2850)
trackA (1796.7650, 2581.3050) (1798.1450, 2581.3050)
trackA (1798.1450, 2580.4050) (1798.1450, 2581.3050)
trackA (1796.7650, 2580.4050) (1798.1450, 2580.4050)
trackA (1796.7650, 2580.4050) (1796.7650, 2581.3050)
trackA (1621.1550, 2209.5850) (1625.0950, 2209.5850)
trackA (1621.1550, 2211.5850) (1625.0950, 2211.5850)
trackA (1621.1550, 2214.6150) (1625.0950, 2214.6150)
trackA (1621.1550, 2216.6150) (1625.0950, 2216.6150)
trackA (1621.1550, 2219.6450) (1625.0950, 2219.6450)
trackA (1621.1550, 2221.6450) (1625.0950, 2221.6450)
trackA (1621.1550, 2224.6750) (1625.0950, 2224.6750)
trackA (1621.1550, 2226.6750) (1625.0950, 2226.6750)
trackA (1621.1550, 2229.7050) (1625.0950, 2229.7050)
trackA (1621.1550, 2231.7050) (1625.0950, 2231.7050)
trackA (1621.1550, 2234.7350) (1625.0950, 2234.7350)
trackA (1621.1550, 2236.7350) (1625.0950, 2236.7350)
trackA (1621.1550, 2239.7650) (1625.0950, 2239.7650)
trackA (1621.1550, 2241.7650) (1625.0950, 2241.7650)
trackA (1621.1550, 2244.7950) (1625.0950, 2244.7950)
trackA (1621.1550, 2246.7950) (1625.0950, 2246.7950)
trackA (1621.1550, 2249.8250) (1625.0950, 2249.8250)
trackA (1621.1550, 2251.8250) (1625.0950, 2251.8250)
trackA (1621.1550, 2254.8550) (1625.0950, 2254.8550)
trackA (1621.1550, 2256.8550) (1625.0950, 2256.8550)
trackA (1621.1550, 2259.8850) (1625.0950, 2259.8850)

trackA (1621.1550, 2261.8850) (1625.0950, 2261.8850)
trackA (1621.1550, 2264.9150) (1625.0950, 2264.9150)
trackA (1621.1550, 2266.9150) (1625.0950, 2266.9150)
trackA (1630.7400, 2136.7500) (1635.8100, 2136.7500)
trackA (1635.8100, 2134.7500) (1635.8100, 2136.7500)
trackA (1630.7400, 2134.7500) (1635.8100, 2134.7500)
trackA (1630.7400, 2141.7800) (1635.8100, 2141.7800)
trackA (1635.8100, 2139.7800) (1635.8100, 2141.7800)
trackA (1630.7400, 2139.7800) (1635.8100, 2139.7800)
trackA (1630.7400, 2146.8100) (1635.8100, 2146.8100)
trackA (1635.8100, 2144.8100) (1635.8100, 2146.8100)
trackA (1630.7400, 2144.8100) (1635.8100, 2144.8100)
trackA (1630.7400, 2151.8400) (1635.8100, 2151.8400)
trackA (1635.8100, 2149.8400) (1635.8100, 2151.8400)
trackA (1630.7400, 2149.8400) (1635.8100, 2149.8400)
trackA (1630.7400, 2156.8700) (1635.8100, 2156.8700)
trackA (1635.8100, 2154.8700) (1635.8100, 2156.8700)
trackA (1630.7400, 2154.8700) (1635.8100, 2154.8700)
trackA (1630.7400, 2161.9000) (1635.8100, 2161.9000)
trackA (1635.8100, 2159.9000) (1635.8100, 2161.9000)
trackA (1630.7400, 2159.9000) (1635.8100, 2159.9000)
trackA (1630.7400, 2166.9300) (1635.8100, 2166.9300)
trackA (1635.8100, 2164.9300) (1635.8100, 2166.9300)
trackA (1630.7400, 2164.9300) (1635.8100, 2164.9300)
trackA (1630.7400, 2171.9600) (1635.8100, 2171.9600)
trackA (1635.8100, 2169.9600) (1635.8100, 2171.9600)
trackA (1630.7400, 2169.9600) (1635.8100, 2169.9600)
trackA (1639.1100, 2134.7500) (1644.1800, 2134.7500)
trackA (1639.1100, 2134.7500) (1639.1100, 2136.7500)
trackA (1639.1100, 2136.7500) (1644.1800, 2136.7500)
trackA (1639.1100, 2139.7800) (1644.1800, 2139.7800)
trackA (1639.1100, 2139.7800) (1639.1100, 2141.7800)
trackA (1639.1100, 2141.7800) (1644.1800, 2141.7800)
trackA (1639.1100, 2144.8100) (1644.1800, 2144.8100)
trackA (1639.1100, 2144.8100) (1639.1100, 2146.8100)
trackA (1639.1100, 2146.8100) (1644.1800, 2146.8100)
trackA (1639.1100, 2149.8400) (1644.1800, 2149.8400)
trackA (1639.1100, 2149.8400) (1639.1100, 2151.8400)
trackA (1639.1100, 2151.8400) (1644.1800, 2151.8400)
trackA (1639.1100, 2154.8700) (1644.1800, 2154.8700)
trackA (1639.1100, 2154.8700) (1639.1100, 2156.8700)
trackA (1639.1100, 2156.8700) (1644.1800, 2156.8700)
trackA (1639.1100, 2159.9000) (1644.1800, 2159.9000)
trackA (1639.1100, 2159.9000) (1639.1100, 2161.9000)

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trackA (1639.1100, 2161.9000) (1644.1800, 2161.9000)
trackA (1639.1100, 2164.9300) (1644.1800, 2164.9300)
trackA (1639.1100, 2164.9300) (1639.1100, 2166.9300)
trackA (1639.1100, 2166.9300) (1644.1800, 2166.9300)
trackA (1639.1100, 2169.9600) (1644.1800, 2169.9600)
trackA (1639.1100, 2169.9600) (1639.1100, 2171.9600)
trackA (1639.1100, 2171.9600) (1644.1800, 2171.9600)

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M1.1 : Metal1 minimum width : 0.23
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/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:1808:internal1

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WARNING: The error count of 128 for this check exceeds the limit set in
the runset. Details only available for the first 100.

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Structure ( lower left x, y ) ( upper right x, y ) Distance
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trackA (1394.2300, 2367.9750) (1394.3950, 2368.1350) 0.1725
trackA (1394.2300, 2367.9750) (1394.2950, 2368.1960) 0.1725
trackA (1394.1300, 2367.9750) (1394.2950, 2368.1350) 0.1725
trackA (1394.2300, 2367.9140) (1394.2950, 2368.1350) 0.1725
trackA (1290.5200, 2388.3750) (1290.6800, 2388.5400) 0.1605
trackA (1290.4500, 2388.3750) (1290.6800, 2388.3850) 0.1605
trackA (1290.5200, 2388.2200) (1290.6800, 2388.3850) 0.1605
trackA (1290.5200, 2388.3750) (1290.7500, 2388.3850) 0.1605
trackA (1295.5200, 2388.3750) (1295.6800, 2388.5400) 0.1605
trackA (1295.4500, 2388.3750) (1295.6800, 2388.3850) 0.1605
trackA (1295.5200, 2388.2200) (1295.6800, 2388.3850) 0.1605
trackA (1295.5200, 2388.3750) (1295.7500, 2388.3850) 0.1605
trackA (1300.5200, 2388.3750) (1300.6800, 2388.5400) 0.1605
trackA (1300.4500, 2388.3750) (1300.6800, 2388.3850) 0.1605
trackA (1300.5200, 2388.2200) (1300.6800, 2388.3850) 0.1605
trackA (1300.5200, 2388.3750) (1300.7500, 2388.3850) 0.1605
trackA (1394.2300, 2389.7950) (1394.4420, 2389.8850) 0.1110
trackA (1394.2300, 2389.7950) (1394.2950, 2390.0160) 0.1110
trackA (1394.0830, 2389.7950) (1394.2950, 2389.8850) 0.1110
trackA (1394.2300, 2389.6640) (1394.2950, 2389.8850) 0.1110
trackA (1290.5200, 2394.3450) (1290.6800, 2394.5100) 0.1605
trackA (1290.4500, 2394.3450) (1290.6800, 2394.3550) 0.1605
trackA (1290.5200, 2394.1900) (1290.6800, 2394.3550) 0.1605

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trackA (1290.5200, 2394.3450) (1290.7500, 2394.3550) 0.1605
trackA (1290.5200, 2400.3150) (1290.6800, 2400.4800) 0.1605
trackA (1290.4500, 2400.3150) (1290.6800, 2400.3250) 0.1605
trackA (1290.5200, 2400.1600) (1290.6800, 2400.3250) 0.1605
trackA (1290.5200, 2400.3150) (1290.7500, 2400.3250) 0.1605
trackA (1295.5200, 2394.3450) (1295.6800, 2394.5100) 0.1605
trackA (1295.4500, 2394.3450) (1295.6800, 2394.3550) 0.1605
trackA (1295.5200, 2394.1900) (1295.6800, 2394.3550) 0.1605
trackA (1295.5200, 2394.3450) (1295.7500, 2394.3550) 0.1605
trackA (1300.5200, 2394.3450) (1300.6800, 2394.5100) 0.1605
trackA (1300.4500, 2394.3450) (1300.6800, 2394.3550) 0.1605
trackA (1300.5200, 2394.1900) (1300.6800, 2394.3550) 0.1605
trackA (1300.5200, 2394.3450) (1300.7500, 2394.3550) 0.1605
trackA (1295.5200, 2400.3150) (1295.6800, 2400.4800) 0.1605
trackA (1295.4500, 2400.3150) (1295.6800, 2400.3250) 0.1605
trackA (1295.5200, 2400.1600) (1295.6800, 2400.3250) 0.1605
trackA (1295.5200, 2400.3150) (1295.7500, 2400.3250) 0.1605
trackA (1300.5200, 2400.3150) (1300.6800, 2400.4800) 0.1605
trackA (1300.4500, 2400.3150) (1300.6800, 2400.3250) 0.1605
trackA (1300.5200, 2400.1600) (1300.6800, 2400.3250) 0.1605
trackA (1300.5200, 2400.3150) (1300.7500, 2400.3250) 0.1605
trackA (1313.1100, 2400.3150) (1313.1600, 2400.5390) 0.0510
trackA (1312.9300, 2400.3150) (1313.1600, 2400.3250) 0.0510
trackA (1313.1100, 2400.1010) (1313.1600, 2400.3250) 0.0510
trackA (1313.1100, 2400.3150) (1313.3400, 2400.3250) 0.0510
trackA (1319.8600, 2400.3150) (1319.9100, 2400.5390) 0.0510
trackA (1319.6800, 2400.3150) (1319.9100, 2400.3250) 0.0510
trackA (1319.8600, 2400.1010) (1319.9100, 2400.3250) 0.0510
trackA (1319.8600, 2400.3150) (1320.0900, 2400.3250) 0.0510
trackA (1326.6100, 2400.3150) (1326.6600, 2400.5390) 0.0510
trackA (1326.4300, 2400.3150) (1326.6600, 2400.3250) 0.0510
trackA (1326.6100, 2400.1010) (1326.6600, 2400.3250) 0.0510
trackA (1326.6100, 2400.3150) (1326.8400, 2400.3250) 0.0510
trackA (1290.5200, 2406.2850) (1290.6800, 2406.4500) 0.1605
trackA (1290.4500, 2406.2850) (1290.6800, 2406.2950) 0.1605
trackA (1290.5200, 2406.1300) (1290.6800, 2406.2950) 0.1605
trackA (1290.5200, 2406.2850) (1290.7500, 2406.2950) 0.1605
trackA (1290.5200, 2412.2550) (1290.6800, 2412.4200) 0.1605
trackA (1290.4500, 2412.2550) (1290.6800, 2412.2650) 0.1605
trackA (1290.5200, 2412.1000) (1290.6800, 2412.2650) 0.1605
trackA (1290.5200, 2412.2550) (1290.7500, 2412.2650) 0.1605
trackA (1295.5200, 2406.2850) (1295.6800, 2406.4500) 0.1605
trackA (1295.4500, 2406.2850) (1295.6800, 2406.2950) 0.1605
trackA (1295.5200, 2406.1300) (1295.6800, 2406.2950) 0.1605

trackA (1295.5200, 2406.2850) (1295.7500, 2406.2950) 0.1605
trackA (1300.5200, 2406.2850) (1300.6800, 2406.4500) 0.1605
trackA (1300.4500, 2406.2850) (1300.6800, 2406.2950) 0.1605
trackA (1300.5200, 2406.1300) (1300.6800, 2406.2950) 0.1605
trackA (1300.5200, 2406.2850) (1300.7500, 2406.2950) 0.1605
trackA (1295.5200, 2412.2550) (1295.6800, 2412.4200) 0.1605
trackA (1295.4500, 2412.2550) (1295.6800, 2412.2650) 0.1605
trackA (1295.5200, 2412.1000) (1295.6800, 2412.2650) 0.1605
trackA (1295.5200, 2412.2550) (1295.7500, 2412.2650) 0.1605
trackA (1300.5200, 2412.2550) (1300.6800, 2412.4200) 0.1605
trackA (1300.4500, 2412.2550) (1300.6800, 2412.2650) 0.1605
trackA (1300.5200, 2412.1000) (1300.6800, 2412.2650) 0.1605
trackA (1300.5200, 2412.2550) (1300.7500, 2412.2650) 0.1605
trackA (1290.5200, 2418.2250) (1290.6800, 2418.3900) 0.1605
trackA (1290.4500, 2418.2250) (1290.6800, 2418.2350) 0.1605
trackA (1290.5200, 2418.0700) (1290.6800, 2418.2350) 0.1605
trackA (1290.5200, 2418.2250) (1290.7500, 2418.2350) 0.1605
trackA (1295.5200, 2418.2250) (1295.6800, 2418.3900) 0.1605
trackA (1295.4500, 2418.2250) (1295.6800, 2418.2350) 0.1605
trackA (1295.5200, 2418.0700) (1295.6800, 2418.2350) 0.1605
trackA (1295.5200, 2418.2250) (1295.7500, 2418.2350) 0.1605
trackA (1300.5200, 2418.2250) (1300.6800, 2418.3900) 0.1605
trackA (1300.4500, 2418.2250) (1300.6800, 2418.2350) 0.1605
trackA (1300.5200, 2418.0700) (1300.6800, 2418.2350) 0.1605
trackA (1300.5200, 2418.2250) (1300.7500, 2418.2350) 0.1605
trackA (1313.1100, 2406.2850) (1313.1600, 2406.5090) 0.0510
trackA (1312.9300, 2406.2850) (1313.1600, 2406.2950) 0.0510
trackA (1313.1100, 2406.0710) (1313.1600, 2406.2950) 0.0510
trackA (1313.1100, 2406.2850) (1313.3400, 2406.2950) 0.0510
trackA (1319.8600, 2406.2850) (1319.9100, 2406.5090) 0.0510
trackA (1319.6800, 2406.2850) (1319.9100, 2406.2950) 0.0510
trackA (1319.8600, 2406.0710) (1319.9100, 2406.2950) 0.0510
trackA (1319.8600, 2406.2850) (1320.0900, 2406.2950) 0.0510

M1.2a : Metal1 minimum space : 0.23

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:1818:external1

WARNING: The error count of 301 for this check exceeds the limit set in
the runset. Details only available for the first 100.

Check was stopped early because error limit was reached.

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-----  
Structure ( lower left x, y ) ( upper right x, y) Distance  
-----  
trackA (1417.8720, 2363.6550) (1418.0150, 2363.8350) 0.1800  
trackA (1417.8720, 2364.3850) (1418.0150, 2364.5650) 0.1800  
trackA (1425.1750, 2363.6550) (1425.3180, 2363.8350) 0.1800  
trackA (1427.7120, 2363.6550) (1427.8550, 2363.8350) 0.1800  
trackA (1425.1750, 2364.3850) (1425.3180, 2364.5650) 0.1800  
trackA (1427.7120, 2364.3850) (1427.8550, 2364.5650) 0.1800  
trackA (1425.1750, 2364.9450) (1425.2420, 2365.1650) 0.2200  
trackA (1423.4830, 2364.9450) (1423.5500, 2365.1650) 0.2200  
trackA (1433.3230, 2364.9450) (1433.3900, 2365.1650) 0.2200  
trackA (1417.8720, 2371.2650) (1418.0150, 2371.4450) 0.1800  
trackA (1417.8720, 2371.9950) (1418.0150, 2372.1750) 0.1800  
trackA (1425.1750, 2371.2650) (1425.3180, 2371.4450) 0.1800  
trackA (1427.7120, 2371.2650) (1427.8550, 2371.4450) 0.1800  
trackA (1425.1750, 2371.9950) (1425.3180, 2372.1750) 0.1800  
trackA (1427.7120, 2371.9950) (1427.8550, 2372.1750) 0.1800  
trackA (1425.1750, 2372.5550) (1425.2420, 2372.7750) 0.2200  
trackA (1423.4830, 2372.5550) (1423.5500, 2372.7750) 0.2200  
trackA (1433.3230, 2372.5550) (1433.3900, 2372.7750) 0.2200  
trackA (1434.8300, 2363.6550) (1434.9730, 2363.8350) 0.1800  
trackA (1434.8300, 2364.3850) (1434.9730, 2364.5650) 0.1800  
trackA (1434.8300, 2364.9450) (1434.8970, 2365.1650) 0.2200  
trackA (1437.5520, 2363.6550) (1437.6950, 2363.8350) 0.1800  
trackA (1437.5520, 2364.3850) (1437.6950, 2364.5650) 0.1800  
trackA (1444.6700, 2363.6550) (1444.8130, 2363.8350) 0.1800  
trackA (1445.2670, 2363.6550) (1445.4100, 2363.8350) 0.1800  
trackA (1444.6700, 2364.3850) (1444.8130, 2364.5650) 0.1800  
trackA (1445.2670, 2364.3850) (1445.4100, 2364.5650) 0.1800  
trackA (1444.6700, 2364.9450) (1444.7370, 2365.1650) 0.2200  
trackA (1443.1630, 2364.9450) (1443.2300, 2365.1650) 0.2200  
trackA (1452.3850, 2363.6550) (1452.5280, 2363.8350) 0.1800  
trackA (1452.3850, 2364.3850) (1452.5280, 2364.5650) 0.1800  
trackA (1454.2300, 2364.9450) (1454.2970, 2365.1650) 0.2200  
trackA (1453.0030, 2364.9450) (1453.0700, 2365.1650) 0.2200  
trackA (1434.8300, 2371.2650) (1434.9730, 2371.4450) 0.1800  
trackA (1434.8300, 2371.9950) (1434.9730, 2372.1750) 0.1800  
trackA (1437.5520, 2371.2650) (1437.6950, 2371.4450) 0.1800  
trackA (1437.5520, 2371.9950) (1437.6950, 2372.1750) 0.1800  
trackA (1435.3900, 2372.5550) (1435.4570, 2372.7750) 0.2200  
trackA (1444.6700, 2371.2650) (1444.8130, 2371.4450) 0.1800
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trackA (1445.2670, 2371.2650) (1445.4100, 2371.4450) 0.1800
trackA (1444.6700, 2371.9950) (1444.8130, 2372.1750) 0.1800
trackA (1445.2670, 2371.9950) (1445.4100, 2372.1750) 0.1800
trackA (1445.2300, 2372.5550) (1445.2970, 2372.7750) 0.2200
trackA (1443.1630, 2372.5550) (1443.2300, 2372.7750) 0.2200
trackA (1452.3850, 2371.2650) (1452.5280, 2371.4450) 0.1800
trackA (1452.3850, 2371.9950) (1452.5280, 2372.1750) 0.1800
trackA (1454.2300, 2372.5550) (1454.2970, 2372.7750) 0.2200
trackA (1453.0030, 2372.5550) (1453.0700, 2372.7750) 0.2200
trackA (1290.3040, 2387.9250) (1290.5200, 2388.0050) 0.0800
trackA (1290.6800, 2387.9250) (1290.8960, 2388.0050) 0.0800
trackA (1290.3040, 2388.6350) (1290.5200, 2388.7150) 0.0800
trackA (1290.6800, 2388.6350) (1290.8960, 2388.7150) 0.0800
trackA (1295.3040, 2387.9250) (1295.5200, 2388.0050) 0.0800
trackA (1295.6800, 2387.9250) (1295.8960, 2388.0050) 0.0800
trackA (1295.3040, 2388.6350) (1295.5200, 2388.7150) 0.0800
trackA (1295.6800, 2388.6350) (1295.8960, 2388.7150) 0.0800
trackA (1300.3040, 2387.9250) (1300.5200, 2388.0050) 0.0800
trackA (1300.6800, 2387.9250) (1300.8960, 2388.0050) 0.0800
trackA (1300.3040, 2388.6350) (1300.5200, 2388.7150) 0.0800
trackA (1300.6800, 2388.6350) (1300.8960, 2388.7150) 0.0800
trackA (1305.0840, 2387.9250) (1305.3000, 2388.0050) 0.0800
trackA (1305.0840, 2388.6350) (1305.3000, 2388.7150) 0.0800
trackA (1305.6800, 2387.9250) (1305.8960, 2388.0050) 0.0800
trackA (1305.6800, 2388.6350) (1305.8960, 2388.7150) 0.0800
trackA (1358.7100, 2374.2050) (1358.8840, 2374.3550) 0.1500
trackA (1358.1560, 2374.2050) (1358.3300, 2374.3550) 0.1500
trackA (1365.1400, 2374.2050) (1365.2340, 2374.4150) 0.2100
trackA (1368.0200, 2374.2050) (1368.1940, 2374.3550) 0.1500
trackA (1367.4660, 2374.2050) (1367.6400, 2374.3550) 0.1500
trackA (1358.7100, 2389.4450) (1358.9060, 2389.5650) 0.1200
trackA (1358.1340, 2389.4450) (1358.3300, 2389.5650) 0.1200
trackA (1358.9260, 2390.1750) (1359.0200, 2390.3850) 0.2100
trackA (1359.4000, 2390.1750) (1359.4940, 2390.3850) 0.2100
trackA (1366.0170, 2389.4450) (1366.1600, 2389.6250) 0.1800
trackA (1365.1400, 2389.4450) (1365.2830, 2389.6250) 0.1800
trackA (1368.0200, 2389.4450) (1368.2160, 2389.5650) 0.1200
trackA (1367.4440, 2389.4450) (1367.6400, 2389.5650) 0.1200
trackA (1368.7100, 2390.1750) (1368.8040, 2390.3850) 0.2100
trackA (1368.2360, 2390.1750) (1368.3300, 2390.3850) 0.2100
trackA (1372.2900, 2389.4450) (1372.4330, 2389.6250) 0.1800
trackA (1377.3300, 2374.2050) (1377.5040, 2374.3550) 0.1500
trackA (1376.7760, 2374.2050) (1376.9500, 2374.3550) 0.1500
trackA (1374.3100, 2374.2050) (1374.4040, 2374.4150) 0.2100

trackA	(1383.6200, 2374.2050)	(1383.7140, 2374.4150)	0.2100
trackA	(1386.6400, 2374.2050)	(1386.8140, 2374.3550)	0.1500
trackA	(1386.0860, 2374.2050)	(1386.2600, 2374.3550)	0.1500
trackA	(1392.9300, 2374.2050)	(1393.0240, 2374.4150)	0.2100
trackA	(1376.7540, 2389.4450)	(1376.9500, 2389.5650)	0.1200
trackA	(1375.4670, 2389.4450)	(1375.6100, 2389.6250)	0.1800
trackA	(1377.3300, 2389.4450)	(1377.5260, 2389.5650)	0.1200
trackA	(1378.0200, 2390.1750)	(1378.1140, 2390.3850)	0.2100
trackA	(1377.5460, 2390.1750)	(1377.6400, 2390.3850)	0.2100
trackA	(1381.6000, 2389.4450)	(1381.7430, 2389.6250)	0.1800
trackA	(1386.6400, 2389.4450)	(1386.8360, 2389.5650)	0.1200
trackA	(1386.0640, 2389.4450)	(1386.2600, 2389.5650)	0.1200
trackA	(1384.7770, 2389.4450)	(1384.9200, 2389.6250)	0.1800
trackA	(1387.3300, 2390.1750)	(1387.4240, 2390.3850)	0.2100
trackA	(1386.8560, 2390.1750)	(1386.9500, 2390.3850)	0.2100
trackA	(1390.9100, 2389.4450)	(1391.0530, 2389.6250)	0.1800
trackA	(1394.2950, 2389.4450)	(1394.4380, 2389.6250)	0.1800

M2.1 : Metal2 minimum width : 0.28

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:1813:internal1

Structure (lower left x, y)	(upper right x, y)	Distance

trackA	(1785.2200, 2585.0000)	(1785.4050, 2585.2100) 0.2510
trackA	(1785.1830, 2585.0000)	(1785.4050, 2585.1700) 0.2510
trackA	(1847.5100, 2585.0000)	(1847.7000, 2585.2060) 0.2550
trackA	(1847.4780, 2585.0000)	(1847.7000, 2585.1700) 0.2550
trackA	(1785.2200, 2584.9600)	(1785.4050, 2585.1700) 0.2510
trackA	(1785.2200, 2585.0000)	(1785.4420, 2585.1700) 0.2510
trackA	(1847.5100, 2584.9640)	(1847.7000, 2585.1700) 0.2550
trackA	(1847.5100, 2585.0000)	(1847.7320, 2585.1700) 0.2550
trackA	(1784.4900, 2585.0000)	(1784.6450, 2585.2330) 0.2300
trackA	(1784.4230, 2585.0000)	(1784.6450, 2585.1700) 0.2300
trackA	(1784.4900, 2584.9370)	(1784.6450, 2585.1700) 0.2300
trackA	(1784.4900, 2585.0000)	(1784.7120, 2585.1700) 0.2300

M2.2a : Metal2 minimum space : 0.28

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:1823:external1

WARNING: The error count of 301 for this check exceeds the limit set in
the runset. Details only available for the first 100.

Check was stopped early because error limit was reached.

Structure (lower left x, y) (upper right x, y) Distance

trackA (397.8800, 2587.9500) (398.1500, 2588.0240) 0.2700
trackA (397.8800, 2587.0860) (398.1500, 2587.1600) 0.2700
trackA (397.8800, 2587.1600) (398.1500, 2587.9500) 0.2700
trackA (597.8800, 2588.1950) (598.1400, 2588.2990) 0.2600
trackA (597.8800, 2587.3010) (598.1400, 2587.4050) 0.2600
trackA (597.8800, 2587.4050) (598.1400, 2588.1950) 0.2600
trackA (997.8800, 2588.3850) (998.1000, 2588.5580) 0.2200
trackA (997.8800, 2587.4220) (998.1000, 2587.5950) 0.2200
trackA (997.8800, 2587.5950) (998.1000, 2588.3850) 0.2200
trackA (1784.1400, 2584.7400) (1784.2450, 2585.0000) 0.1050
trackA (1784.1400, 2585.1700) (1784.2450, 2585.4300) 0.1050
trackA (1784.1400, 2585.0000) (1784.2450, 2585.1700) 0.1050
trackA (1784.8700, 2584.7550) (1785.0050, 2585.0000) 0.1350
trackA (1784.8700, 2585.1700) (1785.0050, 2585.4150) 0.1350
trackA (1784.8700, 2585.0000) (1785.0050, 2585.1700) 0.1350
trackA (1847.8900, 2584.7430) (1848.0000, 2585.0000) 0.1100
trackA (1847.8900, 2585.1700) (1848.0000, 2585.4270) 0.1100
trackA (1847.8900, 2585.0000) (1848.0000, 2585.1700) 0.1100
trackA (1786.3300, 2584.7400) (1786.4350, 2585.0000) 0.1050
trackA (1786.3300, 2585.1650) (1786.4350, 2585.4250) 0.1050
trackA (1786.3300, 2585.0000) (1786.4350, 2585.1650) 0.1050
trackA (1847.1800, 2584.7470) (1847.3000, 2585.0000) 0.1200
trackA (1847.1800, 2585.1700) (1847.3000, 2585.4230) 0.1200
trackA (1847.1800, 2585.0000) (1847.3000, 2585.1700) 0.1200
trackA (1849.0350, 2584.7450) (1849.1500, 2585.0000) 0.1150
trackA (1848.4000, 2584.8840) (1848.6550, 2585.0000) 0.2550
trackA (1848.4000, 2585.1700) (1848.6550, 2585.2860) 0.2550
trackA (1849.0350, 2585.1700) (1849.1500, 2585.4250) 0.1150
trackA (1848.4000, 2585.0000) (1848.6550, 2585.1700) 0.2550
trackA (1849.0350, 2585.0000) (1849.1500, 2585.1700) 0.1150
trackA (1851.6400, 2584.7430) (1851.7500, 2585.0000) 0.1100
trackA (1851.6400, 2585.1700) (1851.7500, 2585.4270) 0.1100

trackA (1851.6400, 2585.0000) (1851.7500, 2585.1700) 0.1100
trackA (1843.6150, 2584.7370) (1843.7100, 2585.0000) 0.0950
trackA (1843.6150, 2585.1700) (1843.7100, 2585.4330) 0.0950
trackA (1843.6150, 2585.0000) (1843.7100, 2585.1700) 0.0950
trackA (1844.6700, 2584.7600) (1844.8150, 2585.0000) 0.1450
trackA (1844.1100, 2584.7860) (1844.2900, 2585.0000) 0.1800
trackA (1844.1100, 2585.1700) (1844.2900, 2585.3840) 0.1800
trackA (1844.6700, 2585.1700) (1844.8150, 2585.4100) 0.1450
trackA (1844.1100, 2585.0000) (1844.2900, 2585.1700) 0.1800
trackA (1844.6700, 2585.0000) (1844.8150, 2585.1700) 0.1450
trackA (1844.1100, 2584.5650) (1844.2650, 2584.7980) 0.1550
trackA (1844.6650, 2584.5650) (1844.8150, 2584.8010) 0.1500
trackA (1844.1100, 2584.5550) (1844.2650, 2584.5650) 0.1550
trackA (1844.6650, 2584.5550) (1844.8150, 2584.5650) 0.1500
trackA (2130.6900, 2586.5250) (2130.9570, 2586.6100) 0.0850
trackA (2129.4230, 2586.5250) (2129.6900, 2586.6100) 0.0850
trackA (2129.6900, 2586.5250) (2130.6900, 2586.6100) 0.0850
trackA (2105.3100, 2586.5250) (2105.5770, 2586.6100) 0.0850
trackA (2104.0430, 2586.5250) (2104.3100, 2586.6100) 0.0850
trackA (2104.3100, 2586.5250) (2105.3100, 2586.6100) 0.0850
trackA (2118.8400, 2586.5250) (2119.1070, 2586.6100) 0.0850
trackA (2115.8930, 2586.5250) (2116.1600, 2586.6100) 0.0850
trackA (2116.1600, 2586.5250) (2118.8400, 2586.6100) 0.0850
trackA (343.4850, 2204.0100) (344.6550, 2204.1700) 0.1600
trackA (344.6550, 2204.0100) (350.0000, 2204.2800) 0.2700
trackA (350.0000, 2204.0100) (350.0740, 2204.2800) 0.2700
trackA (344.6550, 2204.0100) (344.8850, 2204.1700) 0.1600
trackA (343.4850, 2205.5700) (350.0000, 2205.6100) 0.0400
trackA (350.0000, 2205.5700) (350.2770, 2205.6100) 0.0400
trackA (343.1300, 2415.8600) (350.0000, 2416.0800) 0.2200
trackA (350.0000, 2415.8600) (350.1730, 2416.0800) 0.2200
trackA (340.9450, 2078.6000) (341.1150, 2078.8220) 0.1700
trackA (340.9450, 2077.9980) (341.1150, 2078.2200) 0.1700
trackA (340.9450, 2078.2200) (341.1150, 2078.6000) 0.1700
trackA (341.9050, 2076.7200) (342.0210, 2076.9750) 0.2550
trackA (340.9990, 2076.7200) (341.1150, 2076.9750) 0.2550
trackA (341.1150, 2076.7200) (341.9050, 2076.9750) 0.2550
trackA (343.4500, 1992.2000) (344.6200, 1992.3300) 0.1300
trackA (344.6200, 1992.2000) (344.8680, 1992.3300) 0.1300
trackA (341.0600, 1970.8050) (341.8500, 1970.9650) 0.1600
trackA (341.8500, 1970.8050) (342.0800, 1970.9650) 0.1600
trackA (340.8300, 1970.8050) (341.0600, 1970.9650) 0.1600
trackA (340.9450, 1978.6000) (341.0600, 1978.8550) 0.1150
trackA (340.9450, 1977.9650) (341.0600, 1978.2200) 0.1150

trackA	(340.9450, 1978.2200)	(341.0600, 1978.6000)	0.1150
trackA	(340.9450, 1973.6000)	(341.0600, 1973.8550)	0.1150
trackA	(340.9450, 1972.9650)	(341.0600, 1973.2200)	0.1150
trackA	(340.9450, 1973.2200)	(341.0600, 1973.6000)	0.1150
trackA	(341.3000, 1903.6750)	(341.7000, 1903.8600)	0.1850
trackA	(341.7000, 1903.6750)	(341.9100, 1903.8600)	0.1850
trackA	(341.7000, 1897.9950)	(342.1000, 1898.1800)	0.1850
trackA	(342.1000, 1897.9950)	(342.3100, 1898.1800)	0.1850
trackA	(342.1000, 1892.3150)	(342.5000, 1892.5000)	0.1850
trackA	(342.5000, 1892.3150)	(342.7100, 1892.5000)	0.1850
trackA	(341.3000, 1909.3550)	(341.5100, 1909.5400)	0.1850
trackA	(340.3000, 1909.3550)	(340.5100, 1909.5400)	0.1850
trackA	(340.5100, 1909.3550)	(341.3000, 1909.5400)	0.1850
trackA	(342.4800, 1775.8050)	(342.8800, 1775.9900)	0.1850
trackA	(342.8800, 1775.8050)	(343.0900, 1775.9900)	0.1850
trackA	(343.2050, 1566.7200)	(343.6050, 1566.8150)	0.0950
trackA	(343.6050, 1566.7200)	(343.8680, 1566.8150)	0.0950
trackA	(343.2050, 1572.0550)	(343.6050, 1572.2600)	0.2050
trackA	(343.6050, 1572.0550)	(343.7960, 1572.2600)	0.2050
trackA	(340.9450, 1558.6000)	(341.2150, 1558.6740)	0.2700
trackA	(340.9450, 1558.1460)	(341.2150, 1558.2200)	0.2700
trackA	(340.9450, 1558.2200)	(341.2150, 1558.6000)	0.2700
trackA	(340.9450, 1563.6000)	(341.2150, 1563.6740)	0.2700
trackA	(340.9450, 1563.1460)	(341.2150, 1563.2200)	0.2700

MIMTM.10 : (a) There cannot be any Via3 touching MIM bottom plate Metal4
(b) MIM bottom plate Metal4 can only be connected through the higher
Via (Via4)

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:4151:and

Structure	(lower left x, y)	(upper right x, y)

trackA	(1397.7050, 2297.4850)	(1397.9650, 2297.7450)
trackA	(1520.8950, 2342.0550)	(1521.1550, 2342.3150)
trackA	(1520.8950, 2348.2850)	(1521.1550, 2348.5450)
trackA	(1520.8950, 2354.5150)	(1521.1550, 2354.7750)
trackA	(1520.8950, 2360.7450)	(1521.1550, 2361.0050)
trackA	(2315.1800, 483.1000)	(2315.4400, 483.3600)
trackA	(2315.9800, 483.1000)	(2316.2400, 483.3600)

trackA	(2316.7800, 483.1000)	(2317.0400, 483.3600)
trackA	(2317.5800, 483.1000)	(2317.8400, 483.3600)
trackA	(2318.3800, 483.1000)	(2318.6400, 483.3600)
trackA	(2319.1800, 483.1000)	(2319.4400, 483.3600)
trackA	(2319.9800, 483.1000)	(2320.2400, 483.3600)
trackA	(2528.7900, 451.4350)	(2529.0500, 451.6950)
trackA	(2528.7900, 452.2350)	(2529.0500, 452.4950)
trackA	(2529.5900, 451.4350)	(2529.8500, 451.6950)
trackA	(2529.5900, 452.2350)	(2529.8500, 452.4950)
trackA	(2530.3900, 451.4350)	(2530.6500, 451.6950)
trackA	(2530.3900, 452.2350)	(2530.6500, 452.4950)
trackA	(2531.1900, 451.4350)	(2531.4500, 451.6950)
trackA	(2531.1900, 452.2350)	(2531.4500, 452.4950)
trackA	(2531.9900, 451.4350)	(2532.2500, 451.6950)
trackA	(2531.9900, 452.2350)	(2532.2500, 452.4950)
trackA	(2532.7900, 451.4350)	(2533.0500, 451.6950)
trackA	(2532.7900, 452.2350)	(2533.0500, 452.4950)
trackA	(2533.5900, 451.4350)	(2533.8500, 451.6950)
trackA	(2533.5900, 452.2350)	(2533.8500, 452.4950)
L_route_9825ad4f\$1	(-21.4300, -1.8050)	(-21.1700, -1.5450)
L_route_9825ad4f\$1	(-20.6300, -1.8050)	(-20.3700, -1.5450)
L_route_9825ad4f\$1	(-19.8300, -1.8050)	(-19.5700, -1.5450)
L_route_9825ad4f\$1	(-19.0300, -1.8050)	(-18.7700, -1.5450)
L_route_9825ad4f\$1	(-18.2300, -1.8050)	(-17.9700, -1.5450)
L_route_9825ad4f\$1	(-17.4300, -1.8050)	(-17.1700, -1.5450)
L_route_9825ad4f\$1	(-16.6300, -1.8050)	(-16.3700, -1.5450)
L_route_9825ad4f	(-21.4300, -1.8050)	(-21.1700, -1.5450)
L_route_9825ad4f	(-20.6300, -1.8050)	(-20.3700, -1.5450)
L_route_9825ad4f	(-19.8300, -1.8050)	(-19.5700, -1.5450)
L_route_9825ad4f	(-19.0300, -1.8050)	(-18.7700, -1.5450)
L_route_9825ad4f	(-18.2300, -1.8050)	(-17.9700, -1.5450)
L_route_9825ad4f	(-17.4300, -1.8050)	(-17.1700, -1.5450)
L_route_9825ad4f	(-16.6300, -1.8050)	(-16.3700, -1.5450)

MSLOT.1_Metal1 : Maximum Metal1 width without slotting = 30.0

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:5822:or

Structure (lower left x, y) (upper right x, y)

trackA (796.1650, 379.7200) (840.7200, 430.4700)
trackA (896.1550, 379.7200) (940.7100, 430.4700)
io_secondary_5p0 (-42.3000, -8.1050) (14.7500, 36.4500)

MSLOT.1_Metal2 : Maximum Metal2 width without slotting = 30.0

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:5828:or

Structure (lower left x, y) (upper right x, y)

trackA (798.0700, 370.4200) (838.0700, 430.4700)
trackA (898.0600, 370.4200) (938.0600, 430.4700)

MSLOT.1_Metal3 : Maximum Metal3 width without slotting = 30.0

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:5834:or

Structure (lower left x, y) (upper right x, y)

trackA (2195.1050, 356.9400) (2235.1550, 508.6250)
io_secondary_5p0 (-47.3500, -6.2000) (24.0500, 33.8000)

Mn.4_Metal1 : Metal1 coverage over the entire die shall be > 30%

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2832:density

Structure Window (x1,y1) (x2,y2)
Report = Value

trackA (0.0000, 0.0000) (2935.0000, 2935.0000)
Min ratio = 0.2252
Max ratio = 0.2252

Avg ratio = 0.2252
Min areaL1 = 1940121.3014
Max areaL1 = 1940121.3014
Avg areaL1 = 1940121.3014
Min areaW = 8614225.0000
Max areaW = 8614225.0000
Avg areaW = 8614225.0000

Mn.4_Metal2 : Metal2 coverage over the entire die shall be > 30%

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2849:density

Structure Window (x1,y1) (x2,y2)

Report = Value

trackA (0.0000, 0.0000) (2935.0000, 2935.0000)

Min ratio = 0.2735

Max ratio = 0.2735

Avg ratio = 0.2735

Min areaL1 = 2356217.4076

Max areaL1 = 2356217.4076

Avg areaL1 = 2356217.4076

Min areaW = 8614225.0000

Max areaW = 8614225.0000

Avg areaW = 8614225.0000

NP.11 : Butting Nplus and PCOMP is forbidden within 0.43 of well (Nwell
and LVPWELL) edge (for inside DNWELL case)

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2494:and

Structure (lower left x, y) (upper right x, y)

trackA (1351.8510, 2366.3550) (1352.7090, 2366.3560)

trackA (1351.8510, 2372.2050) (1352.7090, 2372.2060)

trackA (1351.8510, 2378.0550) (1352.7090, 2378.0560)

trackA (1351.8510, 2383.9050) (1352.7090, 2383.9060)
trackA (1351.8510, 2389.7550) (1352.7090, 2389.7560)

NP.3a : Nplus space to PCOMP (1) inside Nwell (2) outside LVPWELL
but inside DNWELL : 0.16

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2372:external2

Structure (lower left x, y) (upper right x, y) Distance

trackA (1358.7400, 2374.9350) (1358.8560, 2375.0450) 0.1100
trackA (1358.1840, 2374.9350) (1358.3000, 2375.0450) 0.1100
trackA (1358.3000, 2374.9350) (1358.7400, 2375.0450) 0.1100
trackA (1368.0500, 2374.9350) (1368.1660, 2375.0450) 0.1100
trackA (1367.4940, 2374.9350) (1367.6100, 2375.0450) 0.1100
trackA (1367.6100, 2374.9350) (1368.0500, 2375.0450) 0.1100
trackA (1377.3600, 2374.9350) (1377.4760, 2375.0450) 0.1100
trackA (1376.8040, 2374.9350) (1376.9200, 2375.0450) 0.1100
trackA (1376.9200, 2374.9350) (1377.3600, 2375.0450) 0.1100
trackA (1386.6700, 2374.9350) (1386.7860, 2375.0450) 0.1100
trackA (1386.1140, 2374.9350) (1386.2300, 2375.0450) 0.1100
trackA (1386.2300, 2374.9350) (1386.6700, 2375.0450) 0.1100

NP.4a : Nplus space to related P-channel gate at a butting edge parallel
to gate : 0.32

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2404:external2

Structure (lower left x, y) (upper right x, y) Distance

trackA (1358.9800, 2367.6250) (1359.2510, 2367.7950) 0.1700
trackA (1357.7890, 2367.6250) (1358.0600, 2367.7950) 0.1700
trackA (1358.0600, 2367.6250) (1358.9800, 2367.7950) 0.1700
trackA (1368.2900, 2367.6250) (1368.5610, 2367.7950) 0.1700
trackA (1367.0990, 2367.6250) (1367.3700, 2367.7950) 0.1700
trackA (1367.3700, 2367.6250) (1368.2900, 2367.7950) 0.1700

trackA	(1377.6000, 2367.6250)	(1377.8710, 2367.7950)	0.1700
trackA	(1376.4090, 2367.6250)	(1376.6800, 2367.7950)	0.1700
trackA	(1376.6800, 2367.6250)	(1377.6000, 2367.7950)	0.1700
trackA	(1386.9100, 2367.6250)	(1387.1810, 2367.7950)	0.1700
trackA	(1385.7190, 2367.6250)	(1385.9900, 2367.7950)	0.1700
trackA	(1385.9900, 2367.6250)	(1386.9100, 2367.7950)	0.1700
trackA	(1358.9800, 2384.5250)	(1359.2630, 2384.6750)	0.1500
trackA	(1357.7770, 2384.5250)	(1358.0600, 2384.6750)	0.1500
trackA	(1358.0600, 2384.5250)	(1358.9800, 2384.6750)	0.1500
trackA	(1368.2900, 2384.5250)	(1368.5730, 2384.6750)	0.1500
trackA	(1367.0870, 2384.5250)	(1367.3700, 2384.6750)	0.1500
trackA	(1367.3700, 2384.5250)	(1368.2900, 2384.6750)	0.1500
trackA	(1377.6000, 2384.5250)	(1377.8830, 2384.6750)	0.1500
trackA	(1376.3970, 2384.5250)	(1376.6800, 2384.6750)	0.1500
trackA	(1376.6800, 2384.5250)	(1377.6000, 2384.6750)	0.1500
trackA	(1386.9100, 2384.5250)	(1387.1930, 2384.6750)	0.1500
trackA	(1385.7070, 2384.5250)	(1385.9900, 2384.6750)	0.1500
trackA	(1385.9900, 2384.5250)	(1386.9100, 2384.6750)	0.1500

NP.5a : Nplus overlap of N-channel gate : 0.23

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2422:enclose

Structure (lower left x, y) (upper right x, y) Distance

trackA	(1358.0100, 2383.0050)	(1358.0600, 2383.1750)	0.1700
trackA	(1358.0600, 2383.0050)	(1358.2150, 2383.1750)	0.1700
trackA	(1357.8550, 2383.0050)	(1358.0100, 2383.1750)	0.1700
trackA	(1358.9800, 2383.0050)	(1359.3900, 2383.1750)	0.1700
trackA	(1358.8250, 2383.0050)	(1358.9800, 2383.1750)	0.1700
trackA	(1359.3900, 2383.0050)	(1359.5450, 2383.1750)	0.1700
trackA	(1367.3200, 2383.0050)	(1367.3700, 2383.1750)	0.1700
trackA	(1367.3700, 2383.0050)	(1367.5250, 2383.1750)	0.1700
trackA	(1367.1650, 2383.0050)	(1367.3200, 2383.1750)	0.1700
trackA	(1368.2900, 2383.0050)	(1368.7000, 2383.1750)	0.1700
trackA	(1368.1350, 2383.0050)	(1368.2900, 2383.1750)	0.1700
trackA	(1368.7000, 2383.0050)	(1368.8550, 2383.1750)	0.1700
trackA	(1376.6300, 2383.0050)	(1376.6800, 2383.1750)	0.1700
trackA	(1376.6800, 2383.0050)	(1376.8350, 2383.1750)	0.1700
trackA	(1376.4750, 2383.0050)	(1376.6300, 2383.1750)	0.1700

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trackA (1377.6000, 2383.0050) (1378.0100, 2383.1750) 0.1700
trackA (1377.4450, 2383.0050) (1377.6000, 2383.1750) 0.1700
trackA (1378.0100, 2383.0050) (1378.1650, 2383.1750) 0.1700
trackA (1385.9400, 2383.0050) (1385.9900, 2383.1750) 0.1700
trackA (1385.9900, 2383.0050) (1386.1450, 2383.1750) 0.1700
trackA (1385.7850, 2383.0050) (1385.9400, 2383.1750) 0.1700
trackA (1386.9100, 2383.0050) (1387.3200, 2383.1750) 0.1700
trackA (1386.7550, 2383.0050) (1386.9100, 2383.1750) 0.1700
trackA (1387.3200, 2383.0050) (1387.4750, 2383.1750) 0.1700

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NP.5d(i) : Nplus extension beyond COMP inside DNWELL for Nwell overlap
of Nplus < 0.43 : 0.16

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2447:enclose

WARNING: The error count of 302 for this check exceeds the limit set in
the runset. Details only available for the first 100.

Check was stopped early because error limit was reached.

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Structure          ( lower left x, y ) ( upper right x, y) Distance
-----
gf180mcu_fd_sc_mcu7t5v0__endcap (0.2000, 1.8560) (0.2595, 2.0280) 0.0000
gf180mcu_fd_sc_mcu7t5v0__endcap (0.2000, 1.8560) (0.3600, 1.9200) 0.0000
io_secondary_5p0      (35.8300, -7.2500) (35.8700, 34.9100) 0.0400
io_secondary_5p0      (35.8300, 34.9100) (35.8700, 34.9500) 0.0400
io_secondary_5p0      (35.8300, 34.9100) (35.8700, 34.9500) 0.0400
io_secondary_5p0      (35.8300, -7.2900) (35.8700, -7.2500) 0.0400
io_secondary_5p0      (35.8300, -7.2900) (35.8700, -7.2500) 0.0400
io_secondary_5p0      (22.6100, -7.2500) (22.6500, 34.9100) 0.0400
io_secondary_5p0      (22.6100, -7.2900) (22.6500, -7.2500) 0.0400
io_secondary_5p0      (22.6100, -7.2900) (22.6500, -7.2500) 0.0400
io_secondary_5p0      (22.6100, 34.9100) (22.6500, 34.9500) 0.0400
io_secondary_5p0      (22.6100, 34.9100) (22.6500, 34.9500) 0.0400
io_secondary_5p0      (22.6500, -7.2900) (35.8300, -7.2500) 0.0400
io_secondary_5p0      (22.6500, 34.9100) (35.8300, 34.9500) 0.0400
comp018green_esd_rc_v5p0$2 (0.0000, 2.7100) (0.1165, 2.8480) 0.1205
comp018green_esd_rc_v5p0$2 (0.0000, 22.0420) (0.1165, 22.1800) 0.1205
comp018green_esd_rc_v5p0$2 (0.0000, 22.0635) (0.1480, 22.1800) 0.1165
comp018green_esd_rc_v5p0$2 (0.0000, 2.7100) (0.1480, 2.8265) 0.1165

```

comp018green_esd_rc_v5p0\$2	(0.0000, 2.7100)	(0.1380, 2.8265)	0.1205
comp018green_esd_rc_v5p0\$2	(0.0000, 22.0635)	(0.1380, 22.1800)	0.1205
comp018green_esd_rc_v5p0\$2	(68.2320, 22.0635)	(68.3700, 22.1800)	0.1205
comp018green_esd_rc_v5p0\$2	(68.2320, 2.7100)	(68.3700, 2.8265)	0.1205
comp018green_esd_rc_v5p0\$2	(68.2535, 2.7100)	(68.3700, 2.8480)	0.1205
comp018green_esd_rc_v5p0\$2	(68.2535, 22.0420)	(68.3700, 22.1800)	0.1205
comp018green_esd_rc_v5p0\$2	(68.2220, 22.0635)	(68.3700, 22.1800)	0.1165
comp018green_esd_rc_v5p0\$2	(68.2220, 2.7100)	(68.3700, 2.8265)	0.1165
comp018green_esd_rc_v5p0\$2	(68.2535, 2.7100)	(68.3700, 2.8580)	0.1165
comp018green_esd_rc_v5p0\$2	(0.0000, 2.7100)	(0.1165, 2.8580)	0.1165
comp018green_esd_rc_v5p0\$2	(68.2535, 22.0320)	(68.3700, 22.1800)	0.1165
comp018green_esd_rc_v5p0\$2	(0.0000, 22.0320)	(0.1165, 22.1800)	0.1165
nmos_clamp_20_50_4\$2	(2.2295, 2.2900)	(2.2700, 2.4555)	0.0000
nmos_clamp_20_50_4\$2	(2.2295, 124.3145)	(2.2700, 124.4800)	0.0000
nmos_clamp_20_50_4\$2	(2.1100, 2.4120)	(2.2700, 2.4555)	0.0000
nmos_clamp_20_50_4\$2	(2.1100, 124.3145)	(2.2700, 124.3580)	0.0000
nmos_clamp_20_50_4\$2	(62.3545, 2.2280)	(62.5200, 2.2700)	0.0000
nmos_clamp_20_50_4\$2	(2.2900, 2.2280)	(2.4555, 2.2700)	0.0000
nmos_clamp_20_50_4\$2	(2.4120, 2.1100)	(2.4555, 2.2700)	0.0000
nmos_clamp_20_50_4\$2	(62.3545, 2.1100)	(62.3980, 2.2700)	0.0000
nmos_clamp_20_50_4\$2	(62.3545, 124.5000)	(62.5200, 124.5420)	0.0000
nmos_clamp_20_50_4\$2	(2.2900, 124.5000)	(2.4555, 124.5420)	0.0000
nmos_clamp_20_50_4\$2	(2.4120, 124.5000)	(2.4555, 124.6600)	0.0000
nmos_clamp_20_50_4\$2	(62.3545, 124.5000)	(62.3980, 124.6600)	0.0000
nmos_clamp_20_50_4\$2	(62.5400, 2.2900)	(62.5805, 2.4555)	0.0000
nmos_clamp_20_50_4\$2	(62.5400, 124.3145)	(62.5805, 124.4800)	0.0000
nmos_clamp_20_50_4\$2	(62.5400, 124.3145)	(62.7000, 124.3580)	0.0000
nmos_clamp_20_50_4\$2	(62.5400, 2.4120)	(62.7000, 2.4555)	0.0000
nmos_clamp_20_50_4\$2	(0.0000, 0.0000)	(0.1380, 0.1165)	0.1205
nmos_clamp_20_50_4\$2	(64.6720, 0.0000)	(64.8100, 0.1165)	0.1205
nmos_clamp_20_50_4\$2	(64.6935, 0.0000)	(64.8100, 0.1480)	0.1165
nmos_clamp_20_50_4\$2	(0.0000, 0.0000)	(0.1165, 0.1480)	0.1165
nmos_clamp_20_50_4\$2	(0.0000, 0.0000)	(0.1165, 0.1380)	0.1205
nmos_clamp_20_50_4\$2	(64.6935, 0.0000)	(64.8100, 0.1380)	0.1205
nmos_clamp_20_50_4\$2	(64.6935, 126.6320)	(64.8100, 126.7700)	0.1205
nmos_clamp_20_50_4\$2	(0.0000, 126.6320)	(0.1165, 126.7700)	0.1205
nmos_clamp_20_50_4\$2	(0.0000, 126.6535)	(0.1380, 126.7700)	0.1205
nmos_clamp_20_50_4\$2	(64.6720, 126.6535)	(64.8100, 126.7700)	0.1205
nmos_clamp_20_50_4\$2	(64.6935, 126.6220)	(64.8100, 126.7700)	0.1165
nmos_clamp_20_50_4\$2	(0.0000, 126.6220)	(0.1165, 126.7700)	0.1165
nmos_clamp_20_50_4\$2	(0.0000, 126.6535)	(0.1480, 126.7700)	0.1165
nmos_clamp_20_50_4\$2	(0.0000, 0.0000)	(0.1480, 0.1165)	0.1165
nmos_clamp_20_50_4\$2	(64.6620, 126.6535)	(64.8100, 126.7700)	0.1165
nmos_clamp_20_50_4\$2	(64.6620, 0.0000)	(64.8100, 0.1165)	0.1165

comp018green_sigbuf\$1	(6.2400, 7.1500)	(6.4205, 7.3040)	0.1205
comp018green_sigbuf\$1	(6.2400, 7.1500)	(6.4000, 7.3100)	0.1165
comp018green_sigbuf\$1	(3.8495, 7.1500)	(4.0300, 7.3040)	0.1205
comp018green_sigbuf\$1	(3.8700, 7.1500)	(4.0300, 7.3100)	0.1165
comp018green_sigbuf\$1	(3.8920, 12.5035)	(4.0300, 12.6200)	0.1205
comp018green_sigbuf\$1	(6.2400, 12.5035)	(6.3780, 12.6200)	0.1205
comp018green_sigbuf\$1	(3.9135, 12.4720)	(4.0300, 12.6200)	0.1165
comp018green_sigbuf\$1	(6.2400, 12.4720)	(6.3565, 12.6200)	0.1165
comp018green_sigbuf\$1	(6.2400, 12.4820)	(6.3565, 12.6200)	0.1205
comp018green_sigbuf\$1	(3.9135, 12.4820)	(4.0300, 12.6200)	0.1205
comp018green_sigbuf\$1	(6.2400, 12.5035)	(6.3880, 12.6200)	0.1165
comp018green_sigbuf\$1	(3.8820, 12.5035)	(4.0300, 12.6200)	0.1165
comp018green_out_sigbuf_oe\$1	(7.6500, 6.4800)	(7.8305, 6.6340)	0.1205
comp018green_out_sigbuf_oe\$1	(7.6500, 6.4800)	(7.8100, 6.6400)	0.1165
comp018green_out_sigbuf_oe\$1	(5.2595, 6.4800)	(5.4400, 6.6340)	0.1205
comp018green_out_sigbuf_oe\$1	(5.2800, 6.4800)	(5.4400, 6.6400)	0.1165
comp018green_out_sigbuf_oe\$1	(5.3020, 14.1835)	(5.4400, 14.3000)	0.1205
comp018green_out_sigbuf_oe\$1	(7.6500, 14.1835)	(7.7880, 14.3000)	0.1205
comp018green_out_sigbuf_oe\$1	(5.3235, 14.1520)	(5.4400, 14.3000)	0.1165
comp018green_out_sigbuf_oe\$1	(7.6500, 14.1520)	(7.7665, 14.3000)	0.1165
comp018green_out_sigbuf_oe\$1	(7.6500, 14.1620)	(7.7665, 14.3000)	0.1205
comp018green_out_sigbuf_oe\$1	(5.3235, 14.1620)	(5.4400, 14.3000)	0.1205
comp018green_out_sigbuf_oe\$1	(7.6500, 14.1835)	(7.7980, 14.3000)	0.1165
comp018green_out_sigbuf_oe\$1	(5.2920, 14.1835)	(5.4400, 14.3000)	0.1165
gf180mcu_fd_io__asig_5p0\$1	(10.1050, 71.0100)	(10.2430, 71.1265)	0.1205
gf180mcu_fd_io__asig_5p0\$1	(10.1050, 71.0100)	(10.2215, 71.1580)	0.1165
gf180mcu_fd_io__asig_5p0\$1	(10.1050, 71.0100)	(10.2215, 71.1480)	0.1205
gf180mcu_fd_io__asig_5p0\$1	(10.1050, 71.0100)	(10.2530, 71.1265)	0.1165
gf180mcu_fd_io__asig_5p0\$1	(64.7570, 71.0100)	(64.8950, 71.1265)	0.1205
gf180mcu_fd_io__asig_5p0\$1	(64.7785, 71.0100)	(64.8950, 71.1580)	0.1165
gf180mcu_fd_io__asig_5p0\$1	(64.7785, 71.0100)	(64.8950, 71.1480)	0.1205
gf180mcu_fd_io__asig_5p0\$1	(64.7470, 71.0100)	(64.8950, 71.1265)	0.1165
gf180mcu_fd_io__asig_5p0\$1	(10.1050, 99.7220)	(10.2215, 99.8600)	0.1205
gf180mcu_fd_io__asig_5p0\$1	(10.1050, 99.7435)	(10.2430, 99.8600)	0.1205
gf180mcu_fd_io__asig_5p0\$1	(10.1050, 99.7120)	(10.2215, 99.8600)	0.1165
gf180mcu_fd_io__asig_5p0\$1	(6.8450, 104.8350)	(6.9830, 104.9515)	0.1205
gf180mcu_fd_io__asig_5p0\$1	(6.8450, 104.8350)	(6.9615, 104.9830)	0.1165
gf180mcu_fd_io__asig_5p0\$1	(6.8450, 104.8350)	(6.9615, 104.9730)	0.1205

NP.6 : Nplus overlap with NCOMP butted to PCOMP : 0.22

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2459:internal1

Structure (lower left x, y) (upper right x, y) Distance

trackA	(1376.7600, 2389.5450)	(1377.5200, 2389.7550)	0.2100
trackA	(1376.6940, 2389.5450)	(1376.7600, 2389.7550)	0.2100
trackA	(1377.5200, 2389.5450)	(1377.5860, 2389.7550)	0.2100
trackA	(1358.1400, 2389.5450)	(1358.9000, 2389.7550)	0.2100
trackA	(1358.0740, 2389.5450)	(1358.1400, 2389.7550)	0.2100
trackA	(1358.9000, 2389.5450)	(1358.9660, 2389.7550)	0.2100
trackA	(1386.0700, 2389.5450)	(1386.8300, 2389.7550)	0.2100
trackA	(1386.0040, 2389.5450)	(1386.0700, 2389.7550)	0.2100
trackA	(1386.8300, 2389.5450)	(1386.8960, 2389.7550)	0.2100
trackA	(1367.4500, 2389.5450)	(1368.2100, 2389.7550)	0.2100
trackA	(1367.3840, 2389.5450)	(1367.4500, 2389.7550)	0.2100
trackA	(1368.2100, 2389.5450)	(1368.2760, 2389.7550)	0.2100
trackA	(1497.0600, 2363.7950)	(1497.2100, 2364.5250)	0.1500
trackA	(1497.0600, 2379.0150)	(1497.2100, 2379.7450)	0.1500
trackA	(1497.0600, 2371.4050)	(1497.2100, 2372.1350)	0.1500
trackA	(1497.0600, 2394.2350)	(1497.2100, 2394.9650)	0.1500
trackA	(1497.0600, 2386.6250)	(1497.2100, 2387.3550)	0.1500
trackA	(1497.0600, 2401.8450)	(1497.2100, 2402.5750)	0.1500
trackA	(1497.0600, 2409.4550)	(1497.2100, 2410.1850)	0.1500

NW.2 : Min. Nwell Space : 1.4

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2047:external1

Structure (lower left x, y) (upper right x, y) Distance

gf180mcu_fd_io__bi_t\$1	(58.9910, 294.9550)	(59.3800, 296.3000)	1.3450
gf180mcu_fd_io__bi_t\$1	(68.1450, 294.9550)	(68.5340, 296.3000)	1.3450
gf180mcu_fd_io__bi_t\$1	(59.3800, 294.9550)	(68.1450, 296.3000)	1.3450
gf180mcu_fd_io__bi_t\$1	(46.1000, 317.8650)	(47.3450, 318.5050)	1.2450
gf180mcu_fd_io__bi_t\$1	(46.1000, 312.7450)	(47.3450, 317.8650)	1.2450

NW.3 : Min. Nwell to DNWELL space : 3.1

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2073:external2

Structure (lower left x, y) (upper right x, y) Distance

trackA	(1497.9000, 2360.3920)	(1499.4000, 2363.1050)	1.5000
trackA	(1497.9000, 2367.2550)	(1499.4000, 2369.9680)	1.5000
trackA	(1497.9000, 2368.0020)	(1499.4000, 2370.7150)	1.5000
trackA	(1497.9000, 2374.8650)	(1499.4000, 2377.5780)	1.5000
trackA	(1497.9000, 2375.6120)	(1499.4000, 2378.3250)	1.5000
trackA	(1497.9000, 2382.4750)	(1499.4000, 2385.1880)	1.5000
trackA	(1497.9000, 2383.2220)	(1499.4000, 2385.9350)	1.5000
trackA	(1497.9000, 2390.0850)	(1499.4000, 2392.7980)	1.5000
trackA	(1497.9000, 2390.8320)	(1499.4000, 2393.5450)	1.5000
trackA	(1497.9000, 2397.6950)	(1499.4000, 2400.4080)	1.5000
trackA	(1497.9000, 2398.4420)	(1499.4000, 2401.1550)	1.5000
trackA	(1497.9000, 2405.3050)	(1499.4000, 2408.0180)	1.5000
trackA	(1497.9000, 2406.0520)	(1499.4000, 2408.7650)	1.5000
trackA	(1497.9000, 2412.9150)	(1499.4000, 2414.1750)	1.5000
trackA	(1497.9000, 2414.1750)	(1499.4000, 2416.8880)	2.6625
trackA	(1497.2160, 2414.1750)	(1499.4000, 2416.3750)	2.6625
trackA	(1497.9000, 2413.6620)	(1499.4000, 2416.3750)	2.6625
trackA	(1497.9000, 2414.1750)	(1500.0840, 2416.3750)	2.6625
trackA	(1497.9000, 2393.5450)	(1499.4000, 2397.6950)	1.5000
trackA	(1497.9000, 2401.1550)	(1499.4000, 2405.3050)	1.5000
trackA	(1497.9000, 2385.9350)	(1499.4000, 2390.0850)	1.5000
trackA	(1497.9000, 2408.7650)	(1499.4000, 2412.9150)	1.5000
trackA	(1497.9000, 2378.3250)	(1499.4000, 2382.4750)	1.5000
trackA	(1497.9000, 2370.7150)	(1499.4000, 2374.8650)	1.5000
trackA	(1497.9000, 2363.1050)	(1499.4000, 2367.2550)	1.5000
trackA	(2115.0900, 2027.8700)	(2117.2800, 2030.0500)	2.1800
trackA	(2076.8300, 2027.8700)	(2079.0200, 2030.0500)	2.1800
trackA	(2079.0200, 2027.8700)	(2115.0900, 2030.0500)	2.1800
trackA	(2117.2800, 2027.0580)	(2118.0900, 2030.0500)	2.3255
trackA	(2117.2800, 2027.8700)	(2118.0900, 2030.8620)	2.3255
trackA	(2115.8860, 2027.8700)	(2118.0900, 2030.0500)	2.3255
trackA	(2117.2800, 2027.8700)	(2119.4840, 2030.0500)	2.3255

PAD.16 : Max pad opening space to nearest S/L guard ring (Inner edge
of GUARD_RING_MK marking) = 200.0

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:4549:not_interacting

Structure (lower left x, y) (upper right x, y)

Bondpad_5LM\$1 (2.0000, 2.0000) (62.0000, 62.0000)

PAD.17 : Pad opening space to active circuit COMP = 15.0

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:4555:external2

WARNING: The error count of 301 for this check exceeds the limit set in
the runset. Details only available for the first 100.

Check was stopped early because error limit was reached.

Structure (lower left x, y) (upper right x, y) Distance

trackA (375.4650, 2864.0470) (387.5000, 2877.5180) 12.8260
trackA (447.5000, 2864.0470) (459.5350, 2877.5180) 12.8260
trackA (475.4650, 2864.0470) (487.5000, 2877.5180) 12.8260
trackA (372.9100, 2869.5150) (462.0900, 2873.0000) 3.4850
trackA (378.6450, 2864.4000) (387.5000, 2878.0070) 11.3500
trackA (376.2650, 2865.9000) (391.8580, 2873.0000) 11.3500
trackA (378.6450, 2860.9400) (387.5000, 2874.5470) 13.7815
trackA (376.8470, 2862.4400) (389.2980, 2873.0000) 13.7815
trackA (447.5000, 2864.4000) (456.2650, 2878.0730) 11.2800
trackA (443.0520, 2865.9000) (458.6450, 2873.0000) 11.2800
trackA (447.5000, 2860.9400) (456.2650, 2874.6130) 13.7235
trackA (445.6120, 2862.4400) (458.1530, 2873.0000) 13.7235
trackA (472.9100, 2869.5150) (562.0900, 2873.0000) 3.4850
trackA (478.6450, 2864.4000) (487.5000, 2878.0070) 11.3500
trackA (476.2650, 2865.9000) (491.8580, 2873.0000) 11.3500
trackA (478.6450, 2860.9400) (487.5000, 2874.5470) 13.7815
trackA (476.8470, 2862.4400) (489.2980, 2873.0000) 13.7815
trackA (575.4650, 2864.0470) (587.5000, 2877.5180) 12.8260
trackA (647.5000, 2864.0470) (659.5350, 2877.5180) 12.8260
trackA (547.5000, 2864.0470) (559.5350, 2877.5180) 12.8260

trackA	(675.4650, 2864.0470)	(687.5000, 2877.5180)	12.8260
trackA	(572.9100, 2869.5150)	(662.0900, 2873.0000)	3.4850
trackA	(578.6450, 2864.4000)	(587.5000, 2878.0070)	11.3500
trackA	(576.2650, 2865.9000)	(591.8580, 2873.0000)	11.3500
trackA	(578.6450, 2860.9400)	(587.5000, 2874.5470)	13.7815
trackA	(576.8470, 2862.4400)	(589.2980, 2873.0000)	13.7815
trackA	(647.5000, 2864.4000)	(656.2650, 2878.0730)	11.2800
trackA	(643.0520, 2865.9000)	(658.6450, 2873.0000)	11.2800
trackA	(647.5000, 2860.9400)	(656.2650, 2874.6130)	13.7235
trackA	(645.6120, 2862.4400)	(658.1530, 2873.0000)	13.7235
trackA	(547.5000, 2864.4000)	(556.2650, 2878.0730)	11.2800
trackA	(543.0520, 2865.9000)	(558.6450, 2873.0000)	11.2800
trackA	(547.5000, 2860.9400)	(556.2650, 2874.6130)	13.7235
trackA	(545.6120, 2862.4400)	(558.1530, 2873.0000)	13.7235
trackA	(672.9100, 2869.5150)	(762.0900, 2873.0000)	3.4850
trackA	(678.6450, 2864.4000)	(687.5000, 2878.0070)	11.3500
trackA	(676.2650, 2865.9000)	(691.8580, 2873.0000)	11.3500
trackA	(678.6450, 2860.9400)	(687.5000, 2874.5470)	13.7815
trackA	(676.8470, 2862.4400)	(689.2980, 2873.0000)	13.7815
trackA	(775.4650, 2864.0470)	(787.5000, 2877.5180)	12.8260
trackA	(847.5000, 2864.0470)	(859.5350, 2877.5180)	12.8260
trackA	(747.5000, 2864.0470)	(759.5350, 2877.5180)	12.8260
trackA	(772.9100, 2869.5150)	(862.0900, 2873.0000)	3.4850
trackA	(778.6450, 2864.4000)	(787.5000, 2878.0070)	11.3500
trackA	(776.2650, 2865.9000)	(791.8580, 2873.0000)	11.3500
trackA	(778.6450, 2860.9400)	(787.5000, 2874.5470)	13.7815
trackA	(776.8470, 2862.4400)	(789.2980, 2873.0000)	13.7815
trackA	(847.5000, 2864.4000)	(856.2650, 2878.0730)	11.2800
trackA	(843.0520, 2865.9000)	(858.6450, 2873.0000)	11.2800
trackA	(847.5000, 2860.9400)	(856.2650, 2874.6130)	13.7235
trackA	(845.6120, 2862.4400)	(858.1530, 2873.0000)	13.7235
trackA	(747.5000, 2864.4000)	(756.2650, 2878.0730)	11.2800
trackA	(743.0520, 2865.9000)	(758.6450, 2873.0000)	11.2800
trackA	(747.5000, 2860.9400)	(756.2650, 2874.6130)	13.7235
trackA	(745.6120, 2862.4400)	(758.1530, 2873.0000)	13.7235
trackA	(975.4650, 2864.0470)	(987.5000, 2877.5180)	12.8260
trackA	(875.4650, 2864.0470)	(887.5000, 2877.5180)	12.8260
trackA	(947.5000, 2864.0470)	(959.5350, 2877.5180)	12.8260
trackA	(972.9100, 2869.5150)	(1062.0900, 2873.0000)	3.4850
trackA	(978.6450, 2864.4000)	(987.5000, 2878.0070)	11.3500
trackA	(976.2650, 2865.9000)	(991.8580, 2873.0000)	11.3500
trackA	(978.6450, 2860.9400)	(987.5000, 2874.5470)	13.7815
trackA	(976.8470, 2862.4400)	(989.2980, 2873.0000)	13.7815
trackA	(872.9100, 2869.5150)	(962.0900, 2873.0000)	3.4850

trackA	(878.6450, 2864.4000)	(887.5000, 2878.0070)	11.3500
trackA	(876.2650, 2865.9000)	(891.8580, 2873.0000)	11.3500
trackA	(878.6450, 2860.9400)	(887.5000, 2874.5470)	13.7815
gf180mcu_fd_io__dvss\$1	(7.5000, 62.0000)	(67.5000, 74.4150)	12.4150
gf180mcu_fd_io__dvss\$1	(1.2850, 62.0000)	(17.5280, 67.8950)	6.9945
gf180mcu_fd_io__dvss\$1	(3.7350, 53.3750)	(7.5000, 76.5200)	6.9945
gf180mcu_fd_io__dvss\$1	(57.4720, 62.0000)	(73.7150, 67.8950)	6.9945
gf180mcu_fd_io__dvss\$1	(67.5000, 53.3750)	(71.2650, 76.5200)	6.9945
gf180mcu_fd_io__dvss\$1	(0.0000, 62.0000)	(75.0000, 65.4850)	3.4850
gf180mcu_fd_io__dvss\$1	(5.2550, 62.0000)	(69.7450, 67.6100)	5.6100
gf180mcu_fd_io__dvss\$1	(7.5000, 62.0000)	(67.5000, 70.6100)	8.6100
gf180mcu_fd_io__dvdd\$1	(7.5000, 62.0000)	(67.5000, 74.7000)	12.7000
gf180mcu_fd_io__dvdd\$1	(57.4720, 62.0000)	(73.7150, 67.8950)	6.9945
gf180mcu_fd_io__dvdd\$1	(67.5000, 53.3750)	(71.2650, 76.5200)	6.9945
gf180mcu_fd_io__dvdd\$1	(1.2850, 62.0000)	(17.5280, 67.8950)	6.9945
gf180mcu_fd_io__dvdd\$1	(3.7350, 53.3750)	(7.5000, 76.5200)	6.9945
gf180mcu_fd_io__dvdd\$1	(0.0000, 62.0000)	(75.0000, 65.4850)	3.4850
gf180mcu_fd_io__dvdd\$1	(5.2550, 62.0000)	(69.7450, 67.8950)	5.8950
gf180mcu_fd_io__dvdd\$1	(7.5000, 62.0000)	(67.5000, 70.8950)	8.8950
gf180mcu_fd_io__bi_t\$1	(0.0000, 62.0000)	(75.0000, 65.4850)	3.4850
gf180mcu_fd_io__bi_t\$1	(7.5990, 62.0000)	(67.1810, 75.6900)	13.6900
gf180mcu_fd_io__bi_t\$1	(67.5000, 55.0580)	(73.4550, 75.7670)	9.0575
gf180mcu_fd_io__bi_t\$1	(60.0980, 62.0000)	(73.9050, 68.8250)	9.0575
gf180mcu_fd_io__bi_t\$1	(1.1650, 62.0000)	(73.5350, 67.2200)	5.2200
gf180mcu_fd_io__bi_t\$1	(4.0850, 62.0000)	(70.7350, 69.3100)	7.3100
gf180mcu_fd_io__bi_t\$1	(7.5000, 62.0000)	(67.5000, 71.9700)	9.9700
gf180mcu_fd_io__bi_t\$1	(1.2350, 55.1960)	(7.5000, 75.6290)	9.2645
gf180mcu_fd_io__bi_t\$1	(0.7850, 62.0000)	(14.5920, 68.8250)	9.2645
gf180mcu_fd_io__asig_5p0\$1	(0.0000, 62.0000)	(75.0000, 65.4850)	3.4850
gf180mcu_fd_io__asig_5p0\$1	(7.5000, 62.0000)	(67.5000, 73.4050)	11.4050
gf180mcu_fd_io__asig_5p0\$1	(5.2350, 53.1320)	(7.5000, 76.8280)	6.3760
gf180mcu_fd_io__asig_5p0\$1	(1.2850, 62.0000)	(19.0000, 67.9600)	6.3760
gf180mcu_fd_io__asig_5p0\$1	(7.0050, 62.0000)	(67.9950, 67.9600)	5.9600
gf180mcu_fd_io__asig_5p0\$1	(7.5000, 62.0000)	(67.5000, 71.1700)	9.1700
gf180mcu_fd_io__asig_5p0\$1	(67.5000, 53.1320)	(69.7650, 76.8280)	6.3760
gf180mcu_fd_io__asig_5p0\$1	(56.0000, 62.0000)	(73.7150, 67.9600)	6.3760

PAD.18 : Pad opening space to active circuit Poly2 = 15.0

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:4560:external2

WARNING: The error count of 301 for this check exceeds the limit set in the runset. Details only available for the first 100.

Check was stopped early because error limit was reached.

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Structure      ( lower left x, y )  ( upper right x, y)  Distance
-----
trackA         (378.2050, 2863.9400) (387.5000, 2878.1330) 11.4230
trackA         (376.7050, 2866.3600) (391.6550, 2873.0000) 11.4230
trackA         (378.2050, 2861.2270) (387.5000, 2874.6730) 13.7260
trackA         (376.7050, 2862.9000) (389.2950, 2873.0000) 13.7260
trackA         (447.5000, 2863.9400) (456.7050, 2878.2030) 11.3500
trackA         (443.2550, 2866.3600) (458.2050, 2873.0000) 11.3500
trackA         (447.5000, 2861.1570) (456.7050, 2874.7430) 13.6655
trackA         (445.6150, 2862.9000) (458.2050, 2873.0000) 13.6655
trackA         (478.2050, 2863.9400) (487.5000, 2878.1330) 11.4230
trackA         (476.7050, 2866.3600) (491.6550, 2873.0000) 11.4230
trackA         (478.2050, 2861.2270) (487.5000, 2874.6730) 13.7260
trackA         (476.7050, 2862.9000) (489.2950, 2873.0000) 13.7260
trackA         (578.2050, 2863.9400) (587.5000, 2878.1330) 11.4230
trackA         (576.7050, 2866.3600) (591.6550, 2873.0000) 11.4230
trackA         (578.2050, 2861.2270) (587.5000, 2874.6730) 13.7260
trackA         (576.7050, 2862.9000) (589.2950, 2873.0000) 13.7260
trackA         (647.5000, 2863.9400) (656.7050, 2878.2030) 11.3500
trackA         (643.2550, 2866.3600) (658.2050, 2873.0000) 11.3500
trackA         (647.5000, 2861.1570) (656.7050, 2874.7430) 13.6655
trackA         (645.6150, 2862.9000) (658.2050, 2873.0000) 13.6655
trackA         (547.5000, 2863.9400) (556.7050, 2878.2030) 11.3500
trackA         (543.2550, 2866.3600) (558.2050, 2873.0000) 11.3500
trackA         (547.5000, 2861.1570) (556.7050, 2874.7430) 13.6655
trackA         (545.6150, 2862.9000) (558.2050, 2873.0000) 13.6655
trackA         (678.2050, 2863.9400) (687.5000, 2878.1330) 11.4230
trackA         (676.7050, 2866.3600) (691.6550, 2873.0000) 11.4230
trackA         (678.2050, 2861.2270) (687.5000, 2874.6730) 13.7260
trackA         (676.7050, 2862.9000) (689.2950, 2873.0000) 13.7260
trackA         (778.2050, 2863.9400) (787.5000, 2878.1330) 11.4230
trackA         (776.7050, 2866.3600) (791.6550, 2873.0000) 11.4230
trackA         (778.2050, 2861.2270) (787.5000, 2874.6730) 13.7260
trackA         (776.7050, 2862.9000) (789.2950, 2873.0000) 13.7260
trackA         (847.5000, 2863.9400) (856.7050, 2878.2030) 11.3500
trackA         (843.2550, 2866.3600) (858.2050, 2873.0000) 11.3500
trackA         (847.5000, 2861.1570) (856.7050, 2874.7430) 13.6655
trackA         (845.6150, 2862.9000) (858.2050, 2873.0000) 13.6655
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trackA	(878.2050, 2863.9400)	(887.5000, 2878.1330)	11.4230
trackA	(876.7050, 2866.3600)	(891.6550, 2873.0000)	11.4230
trackA	(878.2050, 2861.2270)	(887.5000, 2874.6730)	13.7260
trackA	(876.7050, 2862.9000)	(889.2950, 2873.0000)	13.7260
trackA	(747.5000, 2863.9400)	(756.7050, 2878.2030)	11.3500
trackA	(743.2550, 2866.3600)	(758.2050, 2873.0000)	11.3500
trackA	(747.5000, 2861.1570)	(756.7050, 2874.7430)	13.6655
trackA	(745.6150, 2862.9000)	(758.2050, 2873.0000)	13.6655
trackA	(978.2050, 2863.9400)	(987.5000, 2878.1330)	11.4230
trackA	(976.7050, 2866.3600)	(991.6550, 2873.0000)	11.4230
trackA	(978.2050, 2861.2270)	(987.5000, 2874.6730)	13.7260
trackA	(976.7050, 2862.9000)	(989.2950, 2873.0000)	13.7260
trackA	(1047.5000, 2863.9400)	(1056.7050, 2878.2030)	11.3500
trackA	(1043.2550, 2866.3600)	(1058.2050, 2873.0000)	11.3500
trackA	(1047.5000, 2861.1570)	(1056.7050, 2874.7430)	13.6655
trackA	(1045.6150, 2862.9000)	(1058.2050, 2873.0000)	13.6655
trackA	(1078.2050, 2863.9400)	(1087.5000, 2878.1330)	11.4230
trackA	(1076.7050, 2866.3600)	(1091.6550, 2873.0000)	11.4230
trackA	(1078.2050, 2861.2270)	(1087.5000, 2874.6730)	13.7260
trackA	(1076.7050, 2862.9000)	(1089.2950, 2873.0000)	13.7260
trackA	(947.5000, 2863.9400)	(956.7050, 2878.2030)	11.3500
trackA	(943.2550, 2866.3600)	(958.2050, 2873.0000)	11.3500
trackA	(947.5000, 2861.1570)	(956.7050, 2874.7430)	13.6655
trackA	(945.6150, 2862.9000)	(958.2050, 2873.0000)	13.6655
trackA	(1178.2050, 2863.9400)	(1187.5000, 2878.1330)	11.4230
trackA	(1176.7050, 2866.3600)	(1191.6550, 2873.0000)	11.4230
trackA	(1178.2050, 2861.2270)	(1187.5000, 2874.6730)	13.7260
trackA	(1176.7050, 2862.9000)	(1189.2950, 2873.0000)	13.7260
trackA	(1247.5000, 2863.9400)	(1256.7050, 2878.2030)	11.3500
trackA	(1243.2550, 2866.3600)	(1258.2050, 2873.0000)	11.3500
trackA	(1247.5000, 2861.1570)	(1256.7050, 2874.7430)	13.6655
trackA	(1245.6150, 2862.9000)	(1258.2050, 2873.0000)	13.6655
trackA	(1147.5000, 2863.9400)	(1156.7050, 2878.2030)	11.3500
trackA	(1143.2550, 2866.3600)	(1158.2050, 2873.0000)	11.3500
trackA	(1147.5000, 2861.1570)	(1156.7050, 2874.7430)	13.6655
trackA	(1145.6150, 2862.9000)	(1158.2050, 2873.0000)	13.6655
trackA	(1378.2050, 2863.9400)	(1387.5000, 2878.1330)	11.4230
trackA	(1376.7050, 2866.3600)	(1391.6550, 2873.0000)	11.4230
trackA	(1378.2050, 2861.2270)	(1387.5000, 2874.6730)	13.7260
trackA	(1376.7050, 2862.9000)	(1389.2950, 2873.0000)	13.7260
trackA	(1447.5000, 2863.9400)	(1456.7050, 2878.2030)	11.3500
trackA	(1443.2550, 2866.3600)	(1458.2050, 2873.0000)	11.3500
trackA	(1447.5000, 2861.1570)	(1456.7050, 2874.7430)	13.6655
trackA	(1445.6150, 2862.9000)	(1458.2050, 2873.0000)	13.6655

trackA	(1278.2050, 2863.9400)	(1287.5000, 2878.1330)	11.4230
trackA	(1276.7050, 2866.3600)	(1291.6550, 2873.0000)	11.4230
trackA	(1278.2050, 2861.2270)	(1287.5000, 2874.6730)	13.7260
trackA	(1276.7050, 2862.9000)	(1289.2950, 2873.0000)	13.7260
trackA	(1347.5000, 2863.9400)	(1356.7050, 2878.2030)	11.3500
trackA	(1343.2550, 2866.3600)	(1358.2050, 2873.0000)	11.3500
trackA	(1347.5000, 2861.1570)	(1356.7050, 2874.7430)	13.6655
trackA	(1345.6150, 2862.9000)	(1358.2050, 2873.0000)	13.6655
gf180mcu_fd_io__dvss\$1	(7.5000, 62.0000)	(67.5000, 76.0750)	14.0750
gf180mcu_fd_io__dvss\$1	(7.5000, 62.0000)	(67.5000, 74.8550)	12.8550
gf180mcu_fd_io__dvdd\$1	(7.8650, 62.0000)	(67.1350, 76.3600)	14.3600
gf180mcu_fd_io__dvdd\$1	(7.5000, 62.0000)	(67.5000, 75.1400)	13.1400
gf180mcu_fd_io__bi_t\$1	(16.0210, 62.0000)	(32.9090, 74.7700)	12.7700
gf180mcu_fd_io__bi_t\$1	(7.5000, 62.0000)	(23.5390, 74.7700)	12.7700
gf180mcu_fd_io__bi_t\$1	(27.7610, 62.0000)	(44.6490, 74.7700)	12.7700
gf180mcu_fd_io__bi_t\$1	(18.3910, 62.0000)	(35.2790, 74.7700)	12.7700
gf180mcu_fd_io__bi_t\$1	(39.5010, 62.0000)	(56.3890, 74.7700)	12.7700
gf180mcu_fd_io__bi_t\$1	(30.1310, 62.0000)	(47.0190, 74.7700)	12.7700
gf180mcu_fd_io__bi_t\$1	(51.2410, 62.0000)	(67.5000, 74.7700)	12.7700
gf180mcu_fd_io__bi_t\$1	(41.8710, 62.0000)	(58.7590, 74.7700)	12.7700

PAD.19a_M1 : Pad opening to non-pad circuit Metal1, 2, 3, 4,5 up to
Top Metal-1 = 6.0

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:4578:external2

Structure	(lower left x, y)	(upper right x, y)	Distance
trackA	(2869.4600, 2192.7630)	(2873.0000, 2209.7390)	3.5400
trackA	(62.0000, 2192.7630)	(65.5400, 2209.7390)	3.5400
trackA	(62.0000, 2192.7630)	(67.6650, 2209.7390)	5.6650
trackA	(62.0000, 1703.5970)	(65.5400, 1720.5730)	3.5400
trackA	(2869.4600, 1703.5970)	(2873.0000, 1720.5730)	3.5400
trackA	(2867.3350, 1703.5970)	(2873.0000, 1720.5730)	5.6650
trackA	(2869.4600, 1214.4310)	(2873.0000, 1231.4070)	3.5400
trackA	(62.0000, 1214.4310)	(65.5400, 1231.4070)	3.5400
trackA	(62.0000, 725.2650)	(65.5400, 742.2410)	3.5400
trackA	(2869.4600, 725.2650)	(2873.0000, 742.2410)	3.5400
gf180mcu_fd_io__dvss\$1	(2.6560, 62.0000)	(72.3440, 65.5400)	3.5400
gf180mcu_fd_io__dvss\$1	(5.5230, 62.0000)	(69.4770, 67.6650)	5.6650

gf180mcu_fd_io__dvdd\$1	(2.6560, 62.0000)	(72.3440, 65.5400)	3.5400
gf180mcu_fd_io__dvdd\$1	(6.7270, 62.0000)	(68.2730, 67.9500)	5.9500
gf180mcu_fd_io__bi_t\$1	(2.6560, 62.0000)	(72.3440, 65.5400)	3.5400
gf180mcu_fd_io__asig_5p0\$1	(2.6560, 62.0000)	(72.3440, 65.5400)	3.5400

 PAD.19a_M2 : Pad opening to non-pad circuit Metal1, 2, 3, 4,5 up to
 Top Metal-1 = 6.0

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
 mcu_drc.rs:4582:external2

WARNING: The error count of 227 for this check exceeds the limit set in
 the runset. Details only available for the first 100.

 Structure (lower left x, y) (upper right x, y) Distance

trackA	(2141.6870, 2867.0500)	(2143.3130, 2873.0000)	5.9500
trackA	(2141.5400, 2867.0500)	(2142.5400, 2873.0000)	5.9500
trackA	(2140.7670, 2867.0500)	(2142.5400, 2873.0000)	5.9500
trackA	(2129.6900, 2867.0500)	(2131.4630, 2873.0000)	5.9500
trackA	(2129.6900, 2867.0500)	(2130.6900, 2873.0000)	5.9500
trackA	(2128.9170, 2867.0500)	(2130.6900, 2873.0000)	5.9500
trackA	(2117.6870, 2867.0500)	(2119.6130, 2873.0000)	5.9500
trackA	(2117.3870, 2867.0500)	(2118.8400, 2873.0000)	5.9500
trackA	(2116.1600, 2867.0500)	(2118.8400, 2873.0000)	5.9500
trackA	(2116.1600, 2867.0500)	(2117.2330, 2873.0000)	5.9500
trackA	(2115.3870, 2867.0500)	(2116.9330, 2873.0000)	5.9500
trackA	(2104.3100, 2867.0500)	(2106.0830, 2873.0000)	5.9500
trackA	(2104.1600, 2867.0500)	(2105.2330, 2873.0000)	5.9500
trackA	(2103.5370, 2867.0500)	(2104.9330, 2873.0000)	5.9520
trackA	(2093.3870, 2867.0500)	(2094.2330, 2873.0000)	5.9910
trackA	(2092.4600, 2867.0500)	(2094.1600, 2873.0000)	5.9500
trackA	(2092.1600, 2867.0500)	(2093.2330, 2873.0000)	5.9500
trackA	(2091.6870, 2867.0500)	(2092.9330, 2873.0000)	5.9575
trackA	(2441.6870, 2867.0500)	(2443.3130, 2873.0000)	5.9500
trackA	(2441.5400, 2867.0500)	(2442.5400, 2873.0000)	5.9500
trackA	(2440.7670, 2867.0500)	(2442.5400, 2873.0000)	5.9500
trackA	(2393.3870, 2867.0500)	(2394.2330, 2873.0000)	5.9910
trackA	(2392.4600, 2867.0500)	(2394.1600, 2873.0000)	5.9500
trackA	(2392.1600, 2867.0500)	(2393.2330, 2873.0000)	5.9500
trackA	(2391.6870, 2867.0500)	(2392.9330, 2873.0000)	5.9575

trackA (2541.6870, 2867.0500) (2543.3130, 2873.0000) 5.9500
trackA (2541.5400, 2867.0500) (2542.5400, 2873.0000) 5.9500
trackA (2540.7670, 2867.0500) (2542.5400, 2873.0000) 5.9500
trackA (2529.6900, 2867.0500) (2531.4630, 2873.0000) 5.9500
trackA (2529.6900, 2867.0500) (2530.6900, 2873.0000) 5.9500
trackA (2528.9170, 2867.0500) (2530.6900, 2873.0000) 5.9500
trackA (2517.6870, 2867.0500) (2519.6130, 2873.0000) 5.9500
trackA (2517.3870, 2867.0500) (2518.8400, 2873.0000) 5.9500
trackA (2516.1600, 2867.0500) (2518.8400, 2873.0000) 5.9500
trackA (2516.1600, 2867.0500) (2517.2330, 2873.0000) 5.9500
trackA (2515.3870, 2867.0500) (2516.9330, 2873.0000) 5.9500
trackA (2504.3100, 2867.0500) (2506.0830, 2873.0000) 5.9500
trackA (2504.1600, 2867.0500) (2505.2330, 2873.0000) 5.9500
trackA (2503.5370, 2867.0500) (2504.9330, 2873.0000) 5.9520
trackA (2493.3870, 2867.0500) (2494.2330, 2873.0000) 5.9910
trackA (2492.4600, 2867.0500) (2494.1600, 2873.0000) 5.9500
trackA (2492.1600, 2867.0500) (2493.2330, 2873.0000) 5.9500
trackA (2491.6870, 2867.0500) (2492.9330, 2873.0000) 5.9575
trackA (2342.4830, 2867.3350) (2344.5170, 2873.0000) 5.9815
trackA (2342.1830, 2867.3350) (2344.4600, 2873.0000) 5.8920
trackA (2341.5400, 2867.3350) (2344.1600, 2873.0000) 5.6650
trackA (2341.5400, 2867.3350) (2342.5400, 2873.0000) 5.6650
trackA (2340.4600, 2867.3350) (2342.5400, 2873.0000) 5.6650
trackA (2340.1600, 2867.3350) (2342.4370, 2873.0000) 5.7670
trackA (2339.5630, 2867.3350) (2342.1370, 2873.0000) 5.8305
trackA (2292.4830, 2867.3350) (2295.4370, 2873.0000) 5.7525
trackA (2292.4600, 2867.3350) (2294.4600, 2873.0000) 5.7080
trackA (2292.4600, 2867.3350) (2294.1600, 2873.0000) 5.6650
trackA (2292.1600, 2867.3350) (2293.4600, 2873.0000) 5.6650
trackA (2290.4830, 2867.3350) (2293.4600, 2873.0000) 5.6730
trackA (62.0000, 2493.3870) (67.9500, 2494.2330) 5.9910
trackA (62.0000, 2492.4600) (67.9500, 2494.1600) 5.9500
trackA (62.0000, 2492.1600) (67.9500, 2493.2330) 5.9500
trackA (62.0000, 2491.6870) (67.9500, 2492.9330) 5.9575
trackA (62.0000, 2341.6870) (67.9500, 2343.3130) 5.9500
trackA (62.0000, 2341.5400) (67.9500, 2342.5400) 5.9500
trackA (62.0000, 2340.7670) (67.9500, 2342.5400) 5.9500
trackA (62.0000, 2442.4830) (67.6650, 2444.5170) 5.9815
trackA (62.0000, 2442.1830) (67.6650, 2444.4600) 5.8920
trackA (62.0000, 2441.5400) (67.6650, 2444.1600) 5.6650
trackA (62.0000, 2441.5400) (67.6650, 2442.5400) 5.6650
trackA (62.0000, 2440.4600) (67.6650, 2442.5400) 5.6650
trackA (62.0000, 2440.1600) (67.6650, 2442.4370) 5.7670
trackA (62.0000, 2439.5630) (67.6650, 2442.1370) 5.8305

trackA	(62.0000, 2392.4830)	(67.6650, 2395.4370)	5.7525
trackA	(62.0000, 2392.4600)	(67.6650, 2394.4600)	5.7080
trackA	(62.0000, 2392.4600)	(67.6650, 2394.1600)	5.6650
trackA	(62.0000, 2392.1600)	(67.6650, 2393.4600)	5.6650
trackA	(62.0000, 2390.4830)	(67.6650, 2393.4600)	5.6730
trackA	(62.0000, 2242.4830)	(67.6650, 2244.5170)	5.9815
trackA	(62.0000, 2242.1830)	(67.6650, 2244.4600)	5.8920
trackA	(62.0000, 2241.5400)	(67.6650, 2244.1600)	5.6650
trackA	(62.0000, 2241.5400)	(67.6650, 2242.5400)	5.6650
trackA	(62.0000, 2240.4600)	(67.6650, 2242.5400)	5.6650
trackA	(62.0000, 2240.1600)	(67.6650, 2242.4370)	5.7670
trackA	(62.0000, 2239.5630)	(67.6650, 2242.1370)	5.8305
trackA	(62.0000, 2230.4830)	(67.6650, 2232.6670)	5.9350
trackA	(62.0000, 2230.1830)	(67.6650, 2232.4600)	5.8525
trackA	(62.0000, 2229.6900)	(67.6650, 2232.1600)	5.6650
trackA	(62.0000, 2229.6900)	(67.6650, 2230.6900)	5.6650
trackA	(62.0000, 2228.4600)	(67.6650, 2230.6900)	5.6650
trackA	(62.0000, 2228.1600)	(67.6650, 2230.4370)	5.7970
trackA	(62.0000, 2227.7130)	(67.6650, 2230.1370)	5.8680
trackA	(2867.3350, 1714.1830)	(2873.0000, 1716.5170)	5.8920
trackA	(2867.3350, 1714.5400)	(2873.0000, 1716.8170)	5.8170
trackA	(2867.3350, 1714.8400)	(2873.0000, 1718.5170)	5.6650
trackA	(2867.3350, 1716.1600)	(2873.0000, 1718.8170)	5.6650
trackA	(2867.3350, 1716.1600)	(2873.0000, 1718.8400)	5.6650
trackA	(2867.3350, 1716.5630)	(2873.0000, 1718.8400)	5.6650
trackA	(2867.3350, 1716.8630)	(2873.0000, 1720.5400)	5.6650
trackA	(2867.3350, 1718.5630)	(2873.0000, 1720.8170)	5.9145
trackA	(2867.3350, 1727.7130)	(2873.0000, 1730.5170)	5.7805
trackA	(2867.3350, 1728.5400)	(2873.0000, 1730.6900)	5.7285
trackA	(2867.3350, 1728.8400)	(2873.0000, 1730.6900)	5.6650
trackA	(2867.3350, 1729.6900)	(2873.0000, 1730.8400)	5.6650

 PL.12 : V5_Xtor enclose 5V COMP

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
 mcu_drc.rs:2354:not

 Structure (lower left x, y) (upper right x, y)

trackA	(1280.5250, 2287.7250)	(1463.2250, 2428.7950)
trackA	(1462.8450, 2413.4150)	(1463.2250, 2415.8750)

trackA (1462.8450, 2405.8050) (1463.2250, 2408.2650)
 trackA (1462.8450, 2398.1950) (1463.2250, 2400.6550)
 trackA (1462.8450, 2390.5850) (1463.2250, 2393.0450)
 trackA (1462.8450, 2382.9750) (1463.2250, 2385.4350)
 trackA (1462.8450, 2375.3650) (1463.2250, 2377.8250)
 trackA (1462.8450, 2367.7550) (1463.2250, 2370.2150)
 trackA (1496.5400, 2329.1250) (1548.8300, 2417.0350)
 trackA (1496.5400, 2413.4150) (1496.9000, 2415.8750)
 trackA (1496.5400, 2405.8050) (1496.9000, 2408.2650)
 trackA (1496.5400, 2398.1950) (1496.9000, 2400.6550)
 trackA (1496.5400, 2390.5850) (1496.9000, 2393.0450)
 trackA (1496.5400, 2382.9750) (1496.9000, 2385.4350)
 trackA (1496.5400, 2375.3650) (1496.9000, 2377.8250)
 trackA (1496.5400, 2367.7550) (1496.9000, 2370.2150)
 trackA (1356.6500, 2358.4650) (1411.8900, 2421.9750)
 trackA (1356.6500, 2387.1350) (1357.0300, 2387.8350)
 trackA (1356.6500, 2381.2850) (1357.0300, 2381.9850)
 trackA (1356.6500, 2375.4350) (1357.0300, 2376.1350)
 trackA (1356.6500, 2369.5850) (1357.0300, 2370.2850)
 trackA (1341.1100, 2363.4850) (1349.6300, 2394.4950)
 trackA (1349.2500, 2387.1350) (1349.6300, 2387.8350)
 trackA (1349.2500, 2381.2850) (1349.6300, 2381.9850)
 trackA (1349.2500, 2375.4350) (1349.6300, 2376.1350)
 trackA (1349.2500, 2369.5850) (1349.6300, 2370.2850)
 trackA (1415.5500, 2361.1550) (1455.1300, 2421.9750)
 trackA (1454.7500, 2413.4150) (1455.1300, 2415.8750)
 trackA (1454.7500, 2405.8050) (1455.1300, 2408.2650)
 trackA (1454.7500, 2398.1950) (1455.1300, 2400.6550)
 trackA (1454.7500, 2390.5850) (1455.1300, 2393.0450)
 trackA (1454.7500, 2382.9750) (1455.1300, 2385.4350)
 trackA (1454.7500, 2375.3650) (1455.1300, 2377.8250)
 trackA (1454.7500, 2367.7550) (1455.1300, 2370.2150)

 PL.3 : Min. Poly2 Spacing : 0.24

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
 mcu_drc.rs:2299:external1

 Structure (lower left x, y) (upper right x, y) Distance

trackA (1395.0500, 2390.3920) (1395.2500, 2390.5250) 0.2000

trackA (1395.0500, 2390.8750) (1395.2500, 2391.0080) 0.2000
trackA (1395.0500, 2390.5250) (1395.2500, 2390.8750) 0.2000

PL.3b_MV : Min Poly2 space on COMP for low active sheet resistivity
(guideline)

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2312:outside

Structure (lower left x, y) (upper right x, y)

trackA (494.2900, 1175.4050) (495.1100, 1175.7250)
gf180mcu_fd_sc_mcu7t5v0__dffrnq_1 (7.2800, 0.7800) (7.5200, 1.1400)
gf180mcu_fd_sc_mcu7t5v0__dffrnq_1 (6.4400, 0.7800) (6.6800, 1.1400)

PL.4 : Min. Poly2 Extension beyond COMP to form end cap : 0.22

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2324:internal1

Structure (lower left x, y) (upper right x, y) Distance

trackA (1358.0100, 2368.5250) (1358.0900, 2368.6150) 0.0900
trackA (1358.0900, 2368.5250) (1358.2910, 2368.6150) 0.0900
trackA (1358.9500, 2368.5250) (1359.3900, 2368.6150) 0.0900
trackA (1358.7490, 2368.5250) (1358.9500, 2368.6150) 0.0900
trackA (1367.3200, 2368.5250) (1367.4000, 2368.6150) 0.0900
trackA (1367.4000, 2368.5250) (1367.6010, 2368.6150) 0.0900
trackA (1368.2600, 2368.5250) (1368.7000, 2368.6150) 0.0900
trackA (1368.0590, 2368.5250) (1368.2600, 2368.6150) 0.0900
trackA (1376.6300, 2368.5250) (1376.7100, 2368.6150) 0.0900
trackA (1376.7100, 2368.5250) (1376.9110, 2368.6150) 0.0900
trackA (1377.5700, 2368.5250) (1378.0100, 2368.6150) 0.0900
trackA (1377.3690, 2368.5250) (1377.5700, 2368.6150) 0.0900
trackA (1385.9400, 2368.5250) (1386.0200, 2368.6150) 0.0900
trackA (1386.0200, 2368.5250) (1386.2210, 2368.6150) 0.0900
trackA (1386.8800, 2368.5250) (1387.3200, 2368.6150) 0.0900
trackA (1386.6790, 2368.5250) (1386.8800, 2368.6150) 0.0900

```

trackA (1358.0100, 2383.0250) (1358.3100, 2383.1750) 0.1500
trackA (1358.7300, 2383.0250) (1359.3900, 2383.1750) 0.1500
trackA (1367.3200, 2383.0250) (1367.6200, 2383.1750) 0.1500
trackA (1368.0400, 2383.0250) (1368.7000, 2383.1750) 0.1500
trackA (1376.6300, 2383.0250) (1376.9300, 2383.1750) 0.1500
trackA (1377.3500, 2383.0250) (1378.0100, 2383.1750) 0.1500
trackA (1385.9400, 2383.0250) (1386.2400, 2383.1750) 0.1500
trackA (1386.6600, 2383.0250) (1387.3200, 2383.1750) 0.1500

```

PL.6 : (Poly2 gate not touching YMTP_MK) with 90 degree bends are not allowed.

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2336:external1_error

	Structure (lower left x, y)	(upper right x, y)	Distance
trackA	(1358.0000, 2390.5150)	(1358.0100, 2390.5250)	0.0000
trackA	(1359.3900, 2390.5150)	(1359.4000, 2390.5250)	0.0000
trackA	(1367.3100, 2390.5150)	(1367.3200, 2390.5250)	0.0000
trackA	(1368.7000, 2390.5150)	(1368.7100, 2390.5250)	0.0000
trackA	(1376.6200, 2390.5150)	(1376.6300, 2390.5250)	0.0000
trackA	(1378.0100, 2390.5150)	(1378.0200, 2390.5250)	0.0000
trackA	(1385.9300, 2390.5150)	(1385.9400, 2390.5250)	0.0000
trackA	(1387.3200, 2390.5150)	(1387.3300, 2390.5250)	0.0000

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2337:internal1_error

	Structure (lower left x, y)	(upper right x, y)	Distance
trackA	(1358.0100, 2383.6150)	(1358.0200, 2383.6250)	0.0000
trackA	(1358.0100, 2390.2750)	(1358.0200, 2390.2850)	0.0000
trackA	(1359.3800, 2383.6150)	(1359.3900, 2383.6250)	0.0000
trackA	(1359.3800, 2390.2750)	(1359.3900, 2390.2850)	0.0000
trackA	(1367.3200, 2383.6150)	(1367.3300, 2383.6250)	0.0000
trackA	(1367.3200, 2390.2750)	(1367.3300, 2390.2850)	0.0000
trackA	(1368.6900, 2383.6150)	(1368.7000, 2383.6250)	0.0000
trackA	(1368.6900, 2390.2750)	(1368.7000, 2390.2850)	0.0000
trackA	(1376.6300, 2383.6150)	(1376.6400, 2383.6250)	0.0000
trackA	(1376.6300, 2390.2750)	(1376.6400, 2390.2850)	0.0000

```

trackA (1378.0000, 2383.6150) (1378.0100, 2383.6250) 0.0000
trackA (1378.0000, 2390.2750) (1378.0100, 2390.2850) 0.0000
trackA (1385.9400, 2383.6150) (1385.9500, 2383.6250) 0.0000
trackA (1385.9400, 2390.2750) (1385.9500, 2390.2850) 0.0000
trackA (1387.3100, 2383.6150) (1387.3200, 2383.6250) 0.0000
trackA (1387.3100, 2390.2750) (1387.3200, 2390.2850) 0.0000

```

PL.8 : Poly2 coverage over the entire die shall be >= 14%

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2815:density

Structure Window (x1,y1) (x2,y2)

Report = Value

trackA (0.0000, 0.0000) (2935.0000, 2935.0000)

Min ratio = 0.1036

Max ratio = 0.1036

Avg ratio = 0.1036

Min areaL1 = 892830.6962

Max areaL1 = 892830.6962

Avg areaL1 = 892830.6962

Min areaW = 8614225.0000

Max areaW = 8614225.0000

Avg areaW = 8614225.0000

PP.11 : Butting Pplus and NCOMP is forbidden within 0.43um of Nwell
edge (for outside DNWELL) and of LVPWELL edge (for inside DNWELL case)

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2646:and

Structure (lower left x, y) (upper right x, y)

trackA (1351.8510, 2366.3540) (1352.7090, 2366.3550)

trackA (1351.8510, 2372.2040) (1352.7090, 2372.2050)

trackA (1351.8510, 2378.0540) (1352.7090, 2378.0550)

trackA (1351.8510, 2383.9040) (1352.7090, 2383.9050)

trackA (1351.8510, 2389.7540) (1352.7090, 2389.7550)

PP.12 : Pplus overlap with N-channel Poly2 gate extension is forbidden
within 0.32um of N-channel gate

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2654:and

Structure (lower left x, y) (upper right x, y)

trackA (1348.7600, 2367.1250) (1349.0800, 2367.6250)
trackA (1349.8000, 2367.1250) (1350.1200, 2367.6250)
trackA (1348.7600, 2372.9750) (1349.0800, 2373.4750)
trackA (1348.7600, 2378.8250) (1349.0800, 2379.3250)
trackA (1348.7600, 2384.6750) (1349.0800, 2385.1750)
trackA (1348.7600, 2390.5250) (1349.0800, 2391.0250)
trackA (1349.8000, 2372.9750) (1350.1200, 2373.4750)
trackA (1349.8000, 2378.8250) (1350.1200, 2379.3250)
trackA (1349.8000, 2384.6750) (1350.1200, 2385.1750)
trackA (1349.8000, 2390.5250) (1350.1200, 2391.0250)
trackA (1358.0100, 2368.5250) (1358.3100, 2368.5650)
trackA (1358.7300, 2368.5250) (1359.0500, 2368.5650)
trackA (1367.3200, 2368.5250) (1367.6200, 2368.5650)
trackA (1368.0400, 2368.5250) (1368.3600, 2368.5650)
trackA (1376.6300, 2368.5250) (1376.9300, 2368.5650)
trackA (1377.3500, 2368.5250) (1377.6700, 2368.5650)
trackA (1385.9400, 2368.5250) (1386.2400, 2368.5650)
trackA (1386.6600, 2368.5250) (1386.9800, 2368.5650)
trackA (1357.7400, 2390.2750) (1358.0600, 2391.0250)
trackA (1358.9800, 2390.2750) (1359.3000, 2391.0250)
trackA (1367.0500, 2390.2750) (1367.3700, 2391.0250)
trackA (1368.2900, 2390.2750) (1368.6100, 2391.0250)
trackA (1376.3600, 2390.2750) (1376.6800, 2391.0250)
trackA (1377.6000, 2390.2750) (1377.9200, 2391.0250)
trackA (1385.6700, 2390.2750) (1385.9900, 2391.0250)
trackA (1386.9100, 2390.2750) (1387.2300, 2391.0250)
trackA (1454.2600, 2365.2950) (1454.5800, 2365.7950)
trackA (1455.3000, 2365.2950) (1455.6200, 2365.7950)
trackA (1454.2600, 2372.9050) (1454.5800, 2373.4050)
trackA (1454.2600, 2380.5150) (1454.5800, 2381.0150)
trackA (1454.2600, 2388.1250) (1454.5800, 2388.6250)

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trackA (1454.2600, 2395.7350) (1454.5800, 2396.2350)
trackA (1454.2600, 2403.3450) (1454.5800, 2403.8450)
trackA (1454.2600, 2410.9550) (1454.5800, 2411.4550)
trackA (1454.2600, 2418.5650) (1454.5800, 2419.0650)
trackA (1455.3000, 2372.9050) (1455.6200, 2373.4050)
trackA (1455.3000, 2380.5150) (1455.6200, 2381.0150)
trackA (1455.3000, 2388.1250) (1455.6200, 2388.6250)
trackA (1455.3000, 2395.7350) (1455.6200, 2396.2350)
trackA (1455.3000, 2403.3450) (1455.6200, 2403.8450)
trackA (1455.3000, 2410.9550) (1455.6200, 2411.4550)
trackA (1455.3000, 2418.5650) (1455.6200, 2419.0650)

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PP.2 : Min. Pplus Space : 0.4
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/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2514:external1

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WARNING: The error count of 132 for this check exceeds the limit set in
the runset. Details only available for the first 100.

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-----
Structure ( lower left x, y ) ( upper right x, y ) Distance
-----
trackA (1357.8000, 2389.5450) (1358.1400, 2389.7550) 0.2100
trackA (1358.9000, 2389.5450) (1359.2400, 2389.7550) 0.2100
trackA (1367.1100, 2389.5450) (1367.4500, 2389.7550) 0.2100
trackA (1368.2100, 2389.5450) (1368.5500, 2389.7550) 0.2100
trackA (1385.7300, 2389.5450) (1386.0700, 2389.7550) 0.2100
trackA (1386.8300, 2389.5450) (1387.1700, 2389.7550) 0.2100
trackA (1376.4200, 2389.5450) (1376.7600, 2389.7550) 0.2100
trackA (1377.5200, 2389.5450) (1377.8600, 2389.7550) 0.2100
trackA (1358.1400, 2389.5450) (1358.9000, 2389.7550) 0.2100
trackA (1367.4500, 2389.5450) (1368.2100, 2389.7550) 0.2100
trackA (1376.7600, 2389.5450) (1377.5200, 2389.7550) 0.2100
trackA (1386.0700, 2389.5450) (1386.8300, 2389.7550) 0.2100
trackA (516.4350, 1226.4260) (516.8250, 1226.5150) 0.3900
trackA (516.4350, 1226.1250) (516.5240, 1226.5150) 0.3900
trackA (510.9860, 1226.1250) (511.0750, 1226.5150) 0.3900
trackA (510.6850, 1226.4260) (511.0750, 1226.5150) 0.3900
trackA (581.4860, 1226.1250) (581.5750, 1226.5150) 0.3900
trackA (581.1850, 1226.4260) (581.5750, 1226.5150) 0.3900
trackA (586.9350, 1226.4260) (587.3250, 1226.5150) 0.3900

```

trackA	(586.9350, 1226.1250)	(587.0240, 1226.5150)	0.3900
trackA	(511.0750, 1226.1250)	(516.4350, 1226.5150)	0.3900
trackA	(510.6850, 1226.5150)	(511.0750, 1254.8750)	0.3900
trackA	(516.4350, 1226.5150)	(516.8250, 1254.8750)	0.3900
trackA	(581.5750, 1226.1250)	(586.9350, 1226.5150)	0.3900
trackA	(581.1850, 1226.5150)	(581.5750, 1254.8750)	0.3900
trackA	(586.9350, 1226.5150)	(587.3250, 1254.8750)	0.3900
trackA	(651.9860, 1226.1250)	(652.0750, 1226.5150)	0.3900
trackA	(651.6850, 1226.4260)	(652.0750, 1226.5150)	0.3900
trackA	(657.4350, 1226.4260)	(657.8250, 1226.5150)	0.3900
trackA	(657.4350, 1226.1250)	(657.5240, 1226.5150)	0.3900
trackA	(727.9350, 1226.4260)	(728.3250, 1226.5150)	0.3900
trackA	(727.9350, 1226.1250)	(728.0240, 1226.5150)	0.3900
trackA	(722.4860, 1226.1250)	(722.5750, 1226.5150)	0.3900
trackA	(722.1850, 1226.4260)	(722.5750, 1226.5150)	0.3900
trackA	(652.0750, 1226.1250)	(657.4350, 1226.5150)	0.3900
trackA	(651.6850, 1226.5150)	(652.0750, 1254.8750)	0.3900
trackA	(657.4350, 1226.5150)	(657.8250, 1254.8750)	0.3900
trackA	(722.5750, 1226.1250)	(727.9350, 1226.5150)	0.3900
trackA	(722.1850, 1226.5150)	(722.5750, 1254.8750)	0.3900
trackA	(727.9350, 1226.5150)	(728.3250, 1254.8750)	0.3900
trackA	(510.6850, 1254.8750)	(511.0750, 1254.9640)	0.3900
trackA	(516.4350, 1254.8750)	(516.8250, 1254.9640)	0.3900
trackA	(516.4350, 1260.3260)	(516.8250, 1260.4150)	0.3900
trackA	(510.6850, 1260.3260)	(511.0750, 1260.4150)	0.3900
trackA	(510.6850, 1288.7750)	(511.0750, 1288.8640)	0.3900
trackA	(510.9860, 1288.7750)	(511.0750, 1289.1650)	0.3900
trackA	(516.4350, 1288.7750)	(516.5240, 1289.1650)	0.3900
trackA	(516.4350, 1288.7750)	(516.8250, 1288.8640)	0.3900
trackA	(581.1850, 1254.8750)	(581.5750, 1254.9640)	0.3900
trackA	(581.1850, 1260.3260)	(581.5750, 1260.4150)	0.3900
trackA	(586.9350, 1254.8750)	(587.3250, 1254.9640)	0.3900
trackA	(586.9350, 1260.3260)	(587.3250, 1260.4150)	0.3900
trackA	(581.1850, 1288.7750)	(581.5750, 1288.8640)	0.3900
trackA	(581.4860, 1288.7750)	(581.5750, 1289.1650)	0.3900
trackA	(586.9350, 1288.7750)	(587.0240, 1289.1650)	0.3900
trackA	(586.9350, 1288.7750)	(587.3250, 1288.8640)	0.3900
trackA	(511.0750, 1288.7750)	(516.4350, 1289.1650)	0.3900
trackA	(510.6850, 1260.4150)	(511.0750, 1288.7750)	0.3900
trackA	(516.4350, 1260.4150)	(516.8250, 1288.7750)	0.3900
trackA	(581.5750, 1288.7750)	(586.9350, 1289.1650)	0.3900
trackA	(581.1850, 1260.4150)	(581.5750, 1288.7750)	0.3900
trackA	(586.9350, 1260.4150)	(587.3250, 1288.7750)	0.3900
trackA	(651.6850, 1254.8750)	(652.0750, 1254.9640)	0.3900

trackA	(651.6850, 1260.3260)	(652.0750, 1260.4150)	0.3900
trackA	(657.4350, 1254.8750)	(657.8250, 1254.9640)	0.3900
trackA	(657.4350, 1260.3260)	(657.8250, 1260.4150)	0.3900
trackA	(722.1850, 1254.8750)	(722.5750, 1254.9640)	0.3900
trackA	(727.9350, 1254.8750)	(728.3250, 1254.9640)	0.3900
trackA	(727.9350, 1260.3260)	(728.3250, 1260.4150)	0.3900
trackA	(722.1850, 1260.3260)	(722.5750, 1260.4150)	0.3900
trackA	(651.6850, 1288.7750)	(652.0750, 1288.8640)	0.3900
trackA	(651.9860, 1288.7750)	(652.0750, 1289.1650)	0.3900
trackA	(657.4350, 1288.7750)	(657.5240, 1289.1650)	0.3900
trackA	(657.4350, 1288.7750)	(657.8250, 1288.8640)	0.3900
trackA	(722.1850, 1288.7750)	(722.5750, 1288.8640)	0.3900
trackA	(722.4860, 1288.7750)	(722.5750, 1289.1650)	0.3900
trackA	(727.9350, 1288.7750)	(728.0240, 1289.1650)	0.3900
trackA	(727.9350, 1288.7750)	(728.3250, 1288.8640)	0.3900
trackA	(652.0750, 1288.7750)	(657.4350, 1289.1650)	0.3900
trackA	(651.6850, 1260.4150)	(652.0750, 1288.7750)	0.3900
trackA	(657.4350, 1260.4150)	(657.8250, 1288.7750)	0.3900
trackA	(722.5750, 1288.7750)	(727.9350, 1289.1650)	0.3900
trackA	(722.1850, 1260.4150)	(722.5750, 1288.7750)	0.3900
trackA	(727.9350, 1260.4150)	(728.3250, 1288.7750)	0.3900
trackA	(537.3900, 1306.7150)	(537.4790, 1307.1050)	0.3900
trackA	(531.4410, 1306.7150)	(531.5300, 1307.1050)	0.3900
trackA	(545.3900, 1306.7150)	(545.4790, 1307.1050)	0.3900
trackA	(539.4410, 1306.7150)	(539.5300, 1307.1050)	0.3900
trackA	(561.3500, 1306.7150)	(561.4390, 1307.1050)	0.3900
trackA	(555.4010, 1306.7150)	(555.4900, 1307.1050)	0.3900
trackA	(563.4010, 1306.7150)	(563.4900, 1307.1050)	0.3900
trackA	(561.3500, 1358.4750)	(561.4390, 1358.8650)	0.3900
trackA	(555.4010, 1358.4750)	(555.4900, 1358.8650)	0.3900
trackA	(563.4010, 1358.4750)	(563.4900, 1358.8650)	0.3900
op_buffer	(6.7000, -73.2400)	(6.9650, -72.9400)	0.3000
op_buffer	(-6.9650, -73.2400)	(-6.7000, -72.9400)	0.3000
op_buffer	(-6.9650, -41.0000)	(-6.7000, -40.7000)	0.3000
op_buffer	(6.7000, -41.0000)	(6.9650, -40.7000)	0.3000
op_buffer	(-6.7000, -73.2400)	(6.7000, -72.9400)	0.3000
op_buffer	(-6.7000, -41.0000)	(6.7000, -40.7000)	0.3000

PP.3c(ii) : Pplus space to NCOMP outside DNWELL for NCOMP space to
Nwell < 0.43 : 0.16

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2539:external2

WARNING: The error count of 108 for this check exceeds the limit set in
the runset. Details only available for the first 100.

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Structure          ( lower left x, y ) ( upper right x, y) Distance  
-----  
trackA             (458.1060, 1158.0255) (458.2780, 1158.0850) 0.0000  
trackA             (458.1060, 1157.9250) (458.1700, 1158.0850) 0.0000  
trackA             (462.0620, 1158.0255) (462.2340, 1158.0850) 0.0000  
trackA             (462.1700, 1157.9250) (462.2340, 1158.0850) 0.0000  
trackA             (465.9460, 1158.0255) (466.1180, 1158.0850) 0.0000  
trackA             (465.9460, 1157.9250) (466.0100, 1158.0850) 0.0000  
trackA             (469.9020, 1158.0255) (470.0740, 1158.0850) 0.0000  
trackA             (470.0100, 1157.9250) (470.0740, 1158.0850) 0.0000  
trackA             (473.7860, 1158.0255) (473.9580, 1158.0850) 0.0000  
trackA             (473.7860, 1157.9250) (473.8500, 1158.0850) 0.0000  
trackA             (477.7420, 1158.0255) (477.9140, 1158.0850) 0.0000  
trackA             (477.8500, 1157.9250) (477.9140, 1158.0850) 0.0000  
trackA             (481.6260, 1158.0255) (481.7980, 1158.0850) 0.0000  
trackA             (481.6260, 1157.9250) (481.6900, 1158.0850) 0.0000  
trackA             (485.5820, 1158.0255) (485.7540, 1158.0850) 0.0000  
trackA             (485.6900, 1157.9250) (485.7540, 1158.0850) 0.0000  
trackA             (489.4660, 1158.0255) (489.6380, 1158.0850) 0.0000  
trackA             (489.4660, 1157.9250) (489.5300, 1158.0850) 0.0000  
trackA             (493.4220, 1158.0255) (493.5940, 1158.0850) 0.0000  
trackA             (493.5300, 1157.9250) (493.5940, 1158.0850) 0.0000  
trackA             (497.3060, 1158.0255) (497.4780, 1158.0850) 0.0000  
trackA             (497.3060, 1157.9250) (497.3700, 1158.0850) 0.0000  
trackA             (458.1060, 1162.4450) (458.2780, 1162.5045) 0.0000  
trackA             (458.1060, 1162.4450) (458.1700, 1162.6050) 0.0000  
trackA             (458.1060, 1163.1055) (458.2780, 1163.1650) 0.0000  
trackA             (458.1060, 1163.0050) (458.1700, 1163.1650) 0.0000  
trackA             (462.0620, 1161.8850) (462.2340, 1161.9445) 0.0000  
trackA             (462.1700, 1161.8850) (462.2340, 1162.0450) 0.0000  
trackA             (462.0620, 1162.5455) (462.2340, 1162.6050) 0.0000  
trackA             (462.1700, 1162.4450) (462.2340, 1162.6050) 0.0000  
trackA             (469.9020, 1161.8850) (470.0740, 1161.9445) 0.0000  
trackA             (470.0100, 1161.8850) (470.0740, 1162.0450) 0.0000  
trackA             (469.9020, 1162.5455) (470.0740, 1162.6050) 0.0000  
trackA             (470.0100, 1162.4450) (470.0740, 1162.6050) 0.0000  
trackA             (477.7420, 1161.8850) (477.9140, 1161.9445) 0.0000  
trackA             (477.8500, 1161.8850) (477.9140, 1162.0450) 0.0000
```


trackA	(477.7420, 1162.5455)	(477.9140, 1162.6050)	0.0000
trackA	(477.8500, 1162.4450)	(477.9140, 1162.6050)	0.0000
trackA	(485.5820, 1161.8850)	(485.7540, 1161.9445)	0.0000
trackA	(485.6900, 1161.8850)	(485.7540, 1162.0450)	0.0000
trackA	(485.5820, 1162.5455)	(485.7540, 1162.6050)	0.0000
trackA	(485.6900, 1162.4450)	(485.7540, 1162.6050)	0.0000
trackA	(493.4220, 1161.8850)	(493.5940, 1161.9445)	0.0000
trackA	(493.5300, 1161.8850)	(493.5940, 1162.0450)	0.0000
trackA	(493.4220, 1162.5455)	(493.5940, 1162.6050)	0.0000
trackA	(493.5300, 1162.4450)	(493.5940, 1162.6050)	0.0000
trackA	(497.3060, 1162.4450)	(497.4780, 1162.5045)	0.0000
trackA	(497.3060, 1162.4450)	(497.3700, 1162.6050)	0.0000
trackA	(497.3060, 1163.1055)	(497.4780, 1163.1650)	0.0000
trackA	(497.3060, 1163.0050)	(497.3700, 1163.1650)	0.0000
trackA	(458.1060, 1182.0450)	(458.2780, 1182.1045)	0.0000
trackA	(458.1060, 1182.0450)	(458.1700, 1182.2050)	0.0000
trackA	(465.9460, 1182.0450)	(466.1180, 1182.1045)	0.0000
trackA	(465.9460, 1182.0450)	(466.0100, 1182.2050)	0.0000
trackA	(458.1060, 1182.7055)	(458.2780, 1182.7650)	0.0000
trackA	(458.1060, 1182.6050)	(458.1700, 1182.7650)	0.0000
trackA	(465.9460, 1182.7055)	(466.1180, 1182.7650)	0.0000
trackA	(465.9460, 1182.6050)	(466.0100, 1182.7650)	0.0000
trackA	(473.7860, 1182.0450)	(473.9580, 1182.1045)	0.0000
trackA	(473.7860, 1182.0450)	(473.8500, 1182.2050)	0.0000
trackA	(481.6260, 1182.0450)	(481.7980, 1182.1045)	0.0000
trackA	(481.6260, 1182.0450)	(481.6900, 1182.2050)	0.0000
trackA	(473.7860, 1182.7055)	(473.9580, 1182.7650)	0.0000
trackA	(473.7860, 1182.6050)	(473.8500, 1182.7650)	0.0000
trackA	(481.6260, 1182.7055)	(481.7980, 1182.7650)	0.0000
trackA	(481.6260, 1182.6050)	(481.6900, 1182.7650)	0.0000
trackA	(489.4660, 1182.0450)	(489.6380, 1182.1045)	0.0000
trackA	(489.4660, 1182.0450)	(489.5300, 1182.2050)	0.0000
trackA	(497.3060, 1182.0450)	(497.4780, 1182.1045)	0.0000
trackA	(497.3060, 1182.0450)	(497.3700, 1182.2050)	0.0000
trackA	(489.4660, 1182.7055)	(489.6380, 1182.7650)	0.0000
trackA	(489.4660, 1182.6050)	(489.5300, 1182.7650)	0.0000
trackA	(497.3060, 1182.7055)	(497.4780, 1182.7650)	0.0000
trackA	(497.3060, 1182.6050)	(497.3700, 1182.7650)	0.0000
trackA	(458.1060, 1201.6850)	(458.2780, 1201.7445)	0.0000
trackA	(458.1060, 1201.6850)	(458.1700, 1201.8450)	0.0000
trackA	(462.0620, 1201.6850)	(462.2340, 1201.7445)	0.0000
trackA	(462.1700, 1201.6850)	(462.2340, 1201.8450)	0.0000
trackA	(465.9460, 1201.6850)	(466.1180, 1201.7445)	0.0000
trackA	(465.9460, 1201.6850)	(466.0100, 1201.8450)	0.0000

trackA	(469.9020, 1201.6850)	(470.0740, 1201.7445)	0.0000
trackA	(470.0100, 1201.6850)	(470.0740, 1201.8450)	0.0000
trackA	(473.7860, 1201.6850)	(473.9580, 1201.7445)	0.0000
trackA	(473.7860, 1201.6850)	(473.8500, 1201.8450)	0.0000
trackA	(477.7420, 1201.6850)	(477.9140, 1201.7445)	0.0000
trackA	(477.8500, 1201.6850)	(477.9140, 1201.8450)	0.0000
trackA	(481.6260, 1201.6850)	(481.7980, 1201.7445)	0.0000
trackA	(481.6260, 1201.6850)	(481.6900, 1201.8450)	0.0000
gf180mcu_fd_sc_mcu7t5v0__endcap	(0.2000, 1.8560)	(0.2595, 2.0280)	0.0000
gf180mcu_fd_sc_mcu7t5v0__endcap	(0.2000, 1.8560)	(0.3600, 1.9200)	0.0000
gf180mcu_fd_io__bi_t\$1	(6.6350, 199.3000)	(6.7740, 199.3800)	0.0800
gf180mcu_fd_io__bi_t\$1	(68.2260, 199.3000)	(68.3650, 199.3800)	0.0800
gf180mcu_fd_io__bi_t\$1	(68.4600, 199.0230)	(68.5550, 199.1520)	0.0950
gf180mcu_fd_io__bi_t\$1	(6.4450, 199.0230)	(6.5400, 199.1520)	0.0950
gf180mcu_fd_io__bi_t\$1	(6.4450, 132.1980)	(6.5400, 132.3270)	0.0950
gf180mcu_fd_io__bi_t\$1	(68.4600, 132.1980)	(68.5550, 132.3270)	0.0950
gf180mcu_fd_io__bi_t\$1	(6.7740, 199.3000)	(68.2260, 199.3800)	0.0800
gf180mcu_fd_io__bi_t\$1	(68.4600, 132.3270)	(68.5550, 199.0230)	0.0950
gf180mcu_fd_io__bi_t\$1	(6.4450, 132.3270)	(6.5400, 199.0230)	0.0950
gf180mcu_fd_io__bi_t\$1	(9.8200, 71.7350)	(65.1850, 71.8100)	0.0750

PP.4a : Pplus space to related N-channel gate at a butting edge parallel
to gate : 0.32

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2562:external2

Structure (lower left x, y) (upper right x, y) Distance

trackA	(1368.7000, 2383.6250)	(1368.8550, 2383.9050)	0.2800
trackA	(1367.1650, 2383.6250)	(1367.3200, 2383.9050)	0.2800
trackA	(1357.8550, 2383.6250)	(1358.0100, 2383.9050)	0.2800
trackA	(1378.0100, 2383.6250)	(1378.1650, 2383.9050)	0.2800
trackA	(1385.7850, 2383.6250)	(1385.9400, 2383.9050)	0.2800
trackA	(1359.3900, 2383.6250)	(1359.5450, 2383.9050)	0.2800
trackA	(1387.3200, 2383.6250)	(1387.4750, 2383.9050)	0.2800
trackA	(1376.4750, 2383.6250)	(1376.6300, 2383.9050)	0.2800
trackA	(1358.0100, 2383.6250)	(1359.3900, 2383.9050)	0.2800
trackA	(1367.3200, 2383.6250)	(1368.7000, 2383.9050)	0.2800
trackA	(1376.6300, 2383.6250)	(1378.0100, 2383.9050)	0.2800
trackA	(1385.9400, 2383.6250)	(1387.3200, 2383.9050)	0.2800

PP.5a : Pplus overlap of P-channel gate : 0.23

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2579:enclose

Structure (lower left x, y) (upper right x, y) Distance

Unnamed_02d9ae27	(-8.5400, 18.3550)	(-8.4920, 18.5800)	0.2250
Unnamed_02d9ae27	(-8.8680, 18.3550)	(-8.8200, 18.5800)	0.2250
Unnamed_02d9ae27	(-8.8200, 18.3550)	(-8.5400, 18.5800)	0.2250
Unnamed_02d9ae27	(-5.9200, 18.3550)	(-5.8720, 18.5800)	0.2250
Unnamed_02d9ae27	(-6.2480, 18.3550)	(-6.2000, 18.5800)	0.2250
Unnamed_02d9ae27	(-6.2000, 18.3550)	(-5.9200, 18.5800)	0.2250
Unnamed_02d9ae27	(-4.7800, 18.3550)	(-4.7320, 18.5800)	0.2250
Unnamed_02d9ae27	(-5.1080, 18.3550)	(-5.0600, 18.5800)	0.2250
Unnamed_02d9ae27	(-5.0600, 18.3550)	(-4.7800, 18.5800)	0.2250
Unnamed_02d9ae27	(-2.2600, 18.3550)	(-2.2120, 18.5800)	0.2250
Unnamed_02d9ae27	(-2.5880, 18.3550)	(-2.5400, 18.5800)	0.2250
Unnamed_02d9ae27	(-2.5400, 18.3550)	(-2.2600, 18.5800)	0.2250
Unnamed_02d9ae27	(-1.1200, 18.3550)	(-1.0720, 18.5800)	0.2250
Unnamed_02d9ae27	(-1.4480, 18.3550)	(-1.4000, 18.5800)	0.2250
Unnamed_02d9ae27	(-1.4000, 18.3550)	(-1.1200, 18.5800)	0.2250
Unnamed_02d9ae27	(1.4000, 18.3550)	(1.4480, 18.5800)	0.2250
Unnamed_02d9ae27	(1.0720, 18.3550)	(1.1200, 18.5800)	0.2250
Unnamed_02d9ae27	(1.1200, 18.3550)	(1.4000, 18.5800)	0.2250
Unnamed_02d9ae27	(2.5400, 18.3550)	(2.5880, 18.5800)	0.2250
Unnamed_02d9ae27	(2.2120, 18.3550)	(2.2600, 18.5800)	0.2250
Unnamed_02d9ae27	(2.2600, 18.3550)	(2.5400, 18.5800)	0.2250
Unnamed_02d9ae27	(5.0600, 18.3550)	(5.1080, 18.5800)	0.2250
Unnamed_02d9ae27	(4.7320, 18.3550)	(4.7800, 18.5800)	0.2250
Unnamed_02d9ae27	(4.7800, 18.3550)	(5.0600, 18.5800)	0.2250
Unnamed_02d9ae27	(6.2000, 18.3550)	(6.2480, 18.5800)	0.2250
Unnamed_02d9ae27	(5.8720, 18.3550)	(5.9200, 18.5800)	0.2250
Unnamed_02d9ae27	(5.9200, 18.3550)	(6.2000, 18.5800)	0.2250
Unnamed_02d9ae27	(8.8200, 18.3550)	(8.8680, 18.5800)	0.2250
Unnamed_02d9ae27	(8.4920, 18.3550)	(8.5400, 18.5800)	0.2250
Unnamed_02d9ae27	(8.5400, 18.3550)	(8.8200, 18.5800)	0.2250

PP.5b : Pplus extension beyond COMP for the COMP (1) inside NWELL
(2) outside LVPWELL but inside DNWELL : 0.16

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2587:enclose

Structure (lower left x, y) (upper right x, y) Distance

trackA	(1358.3000, 2374.9350)	(1358.7400, 2375.0450)	0.1100
trackA	(1358.1840, 2374.9350)	(1358.3000, 2375.0450)	0.1100
trackA	(1358.7400, 2374.9350)	(1358.8560, 2375.0450)	0.1100
trackA	(1367.6100, 2374.9350)	(1368.0500, 2375.0450)	0.1100
trackA	(1367.4940, 2374.9350)	(1367.6100, 2375.0450)	0.1100
trackA	(1368.0500, 2374.9350)	(1368.1660, 2375.0450)	0.1100
trackA	(1376.9200, 2374.9350)	(1377.3600, 2375.0450)	0.1100
trackA	(1376.8040, 2374.9350)	(1376.9200, 2375.0450)	0.1100
trackA	(1377.3600, 2374.9350)	(1377.4760, 2375.0450)	0.1100
trackA	(1386.2300, 2374.9350)	(1386.6700, 2375.0450)	0.1100
trackA	(1386.1140, 2374.9350)	(1386.2300, 2375.0450)	0.1100
trackA	(1386.6700, 2374.9350)	(1386.7860, 2375.0450)	0.1100

PP.5c(ii) : Pplus extension beyond COMP inside DNWELL for LVPWELL
overlap of Pplus < 0.43 : 0.16

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2594:enclose

Structure (lower left x, y) (upper right x, y) Distance

trackA	(1502.5650, 2335.1450)	(1502.5815, 2335.1765)	0.0165
trackA	(1523.3985, 2335.1450)	(1523.4150, 2335.1765)	0.0165
trackA	(1523.3985, 2371.5835)	(1523.4150, 2371.6150)	0.0165
trackA	(1502.5650, 2371.5835)	(1502.5815, 2371.6150)	0.0165
trackA	(1514.2235, 2374.5450)	(1514.2400, 2374.5765)	0.0165
trackA	(1502.5600, 2374.5450)	(1502.5765, 2374.5765)	0.0165
trackA	(1502.5600, 2374.5450)	(1502.5915, 2374.5615)	0.0165
trackA	(1502.5650, 2371.5985)	(1502.5965, 2371.6150)	0.0165
trackA	(1502.5650, 2335.1450)	(1502.5965, 2335.1615)	0.0165
trackA	(1514.2085, 2374.5450)	(1514.2400, 2374.5615)	0.0165
trackA	(1523.3835, 2335.1450)	(1523.4150, 2335.1615)	0.0165

```

trackA (1523.3835, 2371.5985) (1523.4150, 2371.6150) 0.0165
trackA (1502.5600, 2410.9835) (1502.5765, 2411.0150) 0.0165
trackA (1514.2235, 2410.9835) (1514.2400, 2411.0150) 0.0165
trackA (1502.5600, 2410.9985) (1502.5915, 2411.0150) 0.0165
trackA (1514.2085, 2410.9985) (1514.2400, 2411.0150) 0.0165

```

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-----
PP.5d(ii) : Pplus extension beyond COMP outside DNWELL for Pplus space
to Nwell < 0.43 : 0.16
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/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2605:enclose

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WARNING: The error count of 176 for this check exceeds the limit set in the runset. Details only available for the first 100.

```

-----
Structure          ( lower left x, y )  ( upper right x, y )  Distance
-----
io_secondary_5p0    (12.9105, 36.5980)  (12.9800, 36.6300)  0.0000
io_secondary_5p0    (12.9800, 36.4730)  (13.0130, 36.6300)  0.1065
io_secondary_5p0    (-32.4200, 36.5980) (-32.3505, 36.6300)  0.0000
io_secondary_5p0    (-32.4530, 36.4730) (-32.4200, 36.6300)  0.1065
io_secondary_5p0    (-32.4200, 36.5235) (-32.3505, 36.6300)  0.0000
io_secondary_5p0    (12.9105, 36.5235)  (12.9800, 36.6300)  0.0000
io_secondary_5p0    (12.9800, 48.7205)  (13.0120, 48.7900)  0.0000
io_secondary_5p0    (12.9800, 36.6300)  (13.0120, 36.6995)  0.0000
io_secondary_5p0    (12.9800, 36.6300)  (13.0865, 36.6995)  0.0000
io_secondary_5p0    (12.9800, 48.7205)  (13.0865, 48.7900)  0.0000
io_secondary_5p0    (12.9800, 48.7900)  (13.1370, 48.8230)  0.1065
io_secondary_5p0    (12.9800, 36.5970)  (13.1370, 36.6300)  0.1065
io_secondary_5p0    (-32.4520, 48.7205) (-32.4200, 48.7900)  0.0000
io_secondary_5p0    (-32.4520, 36.6300) (-32.4200, 36.6995)  0.0000
io_secondary_5p0    (-32.5265, 36.6300) (-32.4200, 36.6995)  0.0000
io_secondary_5p0    (-32.5265, 48.7205) (-32.4200, 48.7900)  0.0000
io_secondary_5p0    (-32.5770, 36.5970) (-32.4200, 36.6300)  0.1065
io_secondary_5p0    (-32.5770, 48.7900) (-32.4200, 48.8230)  0.1065
io_secondary_5p0    (12.9105, 48.7900)  (12.9800, 48.8220)  0.0000
io_secondary_5p0    (12.9800, 48.7900)  (13.0130, 48.9470)  0.1065
io_secondary_5p0    (-32.4200, 48.7900) (-32.3505, 48.8220)  0.0000
io_secondary_5p0    (-32.4530, 48.7900) (-32.4200, 48.9470)  0.1065
io_secondary_5p0    (-32.4200, 48.7900) (-32.3505, 48.8965)  0.0000
io_secondary_5p0    (12.9105, 48.7900)  (12.9800, 48.8965)  0.0000

```

gf180mcu_fd_io__dvss\$1	(15.3650, 322.2645)	(15.5520, 322.4150)	0.1095
gf180mcu_fd_io__dvss\$1	(15.3650, 302.9650)	(15.5520, 303.1155)	0.1095
gf180mcu_fd_io__dvss\$1	(15.3650, 322.2550)	(15.5250, 322.4150)	0.1030
gf180mcu_fd_io__dvss\$1	(15.3650, 302.9650)	(15.5250, 303.1250)	0.1030
gf180mcu_fd_io__dvss\$1	(59.4480, 322.2645)	(59.6350, 322.4150)	0.1095
gf180mcu_fd_io__dvss\$1	(59.4480, 302.9650)	(59.6350, 303.1155)	0.1095
gf180mcu_fd_io__dvss\$1	(59.4750, 322.2550)	(59.6350, 322.4150)	0.1030
gf180mcu_fd_io__dvss\$1	(59.4750, 302.9650)	(59.6350, 303.1250)	0.1030
gf180mcu_fd_io__dvss\$1	(66.9575, 191.0770)	(67.1550, 191.2200)	0.0895
gf180mcu_fd_io__dvss\$1	(66.9575, 70.4500)	(67.1550, 70.5930)	0.0895
gf180mcu_fd_io__dvss\$1	(66.9950, 191.0600)	(67.1550, 191.2200)	0.0800
gf180mcu_fd_io__dvss\$1	(66.9950, 70.4500)	(67.1550, 70.6100)	0.0800
gf180mcu_fd_io__dvss\$1	(7.8450, 191.0770)	(8.0425, 191.2200)	0.0895
gf180mcu_fd_io__dvss\$1	(7.8450, 70.4500)	(8.0425, 70.5930)	0.0895
gf180mcu_fd_io__dvss\$1	(7.8450, 191.0600)	(8.0050, 191.2200)	0.0800
gf180mcu_fd_io__dvss\$1	(7.8450, 70.4500)	(8.0050, 70.6100)	0.0800
gf180mcu_fd_io__dvdd\$1	(15.3650, 322.2645)	(15.5520, 322.4150)	0.1095
gf180mcu_fd_io__dvdd\$1	(15.3650, 302.9650)	(15.5520, 303.1155)	0.1095
gf180mcu_fd_io__dvdd\$1	(15.3650, 322.2550)	(15.5250, 322.4150)	0.1030
gf180mcu_fd_io__dvdd\$1	(15.3650, 302.9650)	(15.5250, 303.1250)	0.1030
gf180mcu_fd_io__dvdd\$1	(59.4480, 322.2645)	(59.6350, 322.4150)	0.1095
gf180mcu_fd_io__dvdd\$1	(59.4480, 302.9650)	(59.6350, 303.1155)	0.1095
gf180mcu_fd_io__dvdd\$1	(59.4750, 322.2550)	(59.6350, 322.4150)	0.1030
gf180mcu_fd_io__dvdd\$1	(59.4750, 302.9650)	(59.6350, 303.1250)	0.1030
gf180mcu_fd_io__dvdd\$1	(66.9575, 191.3620)	(67.1550, 191.5050)	0.0895
gf180mcu_fd_io__dvdd\$1	(66.9575, 70.7350)	(67.1550, 70.8780)	0.0895
gf180mcu_fd_io__dvdd\$1	(66.9950, 191.3450)	(67.1550, 191.5050)	0.0800
gf180mcu_fd_io__dvdd\$1	(66.9950, 70.7350)	(67.1550, 70.8950)	0.0800
gf180mcu_fd_io__dvdd\$1	(7.8450, 191.3620)	(8.0425, 191.5050)	0.0895
gf180mcu_fd_io__dvdd\$1	(7.8450, 70.7350)	(8.0425, 70.8780)	0.0895
gf180mcu_fd_io__dvdd\$1	(7.8450, 191.3450)	(8.0050, 191.5050)	0.0800
gf180mcu_fd_io__dvdd\$1	(7.8450, 70.7350)	(8.0050, 70.8950)	0.0800
nmos_clamp_20_50_4\$2	(61.8625, 3.0000)	(62.0600, 3.1430)	0.0895
nmos_clamp_20_50_4\$2	(61.9000, 3.0000)	(62.0600, 3.1600)	0.0800
nmos_clamp_20_50_4\$2	(61.8625, 123.6270)	(62.0600, 123.7700)	0.0895
nmos_clamp_20_50_4\$2	(61.9000, 123.6100)	(62.0600, 123.7700)	0.0800
nmos_clamp_20_50_4\$2	(2.7500, 3.0000)	(2.9475, 3.1430)	0.0895
nmos_clamp_20_50_4\$2	(2.7500, 3.0000)	(2.9100, 3.1600)	0.0800
nmos_clamp_20_50_4\$2	(2.7500, 123.6270)	(2.9475, 123.7700)	0.0895
nmos_clamp_20_50_4\$2	(2.7500, 123.6100)	(2.9100, 123.7700)	0.0800
gf180mcu_fd_io__bi_t\$1	(52.2865, 293.1990)	(52.4050, 293.4200)	0.0225
gf180mcu_fd_io__bi_t\$1	(22.5950, 293.1990)	(22.7135, 293.4200)	0.0225
gf180mcu_fd_io__bi_t\$1	(52.2450, 293.2600)	(52.4050, 293.4200)	0.0165
gf180mcu_fd_io__bi_t\$1	(22.5950, 293.2600)	(22.7550, 293.4200)	0.0165

gf180mcu_fd_io__asig_5p0\$1	(9.5845, 70.5700)	(9.6150, 70.6540)	0.0000
gf180mcu_fd_io__asig_5p0\$1	(9.5845, 100.2160)	(9.6150, 100.3000)	0.0000
gf180mcu_fd_io__asig_5p0\$1	(9.4550, 70.5850)	(9.6150, 70.6540)	0.0000
gf180mcu_fd_io__asig_5p0\$1	(9.4550, 100.2160)	(9.6150, 100.2850)	0.0000
gf180mcu_fd_io__asig_5p0\$1	(65.2880, 70.5235)	(65.3850, 70.5700)	0.0000
gf180mcu_fd_io__asig_5p0\$1	(9.6150, 70.5235)	(9.7120, 70.5700)	0.0000
gf180mcu_fd_io__asig_5p0\$1	(9.6150, 70.4395)	(9.7120, 70.5700)	0.0000
gf180mcu_fd_io__asig_5p0\$1	(65.2880, 70.4395)	(65.3850, 70.5700)	0.0000
gf180mcu_fd_io__asig_5p0\$1	(65.3850, 70.4115)	(65.4060, 70.5700)	0.1305
gf180mcu_fd_io__asig_5p0\$1	(9.5940, 70.4115)	(9.6150, 70.5700)	0.1305
gf180mcu_fd_io__asig_5p0\$1	(65.2880, 100.3000)	(65.3850, 100.3465)	0.0000
gf180mcu_fd_io__asig_5p0\$1	(9.6150, 100.3000)	(9.7120, 100.3465)	0.0000
gf180mcu_fd_io__asig_5p0\$1	(9.6150, 100.3000)	(9.7120, 100.4305)	0.0000
gf180mcu_fd_io__asig_5p0\$1	(65.2880, 100.3000)	(65.3850, 100.4305)	0.0000
gf180mcu_fd_io__asig_5p0\$1	(9.5940, 100.3000)	(9.6150, 100.4585)	0.1305
gf180mcu_fd_io__asig_5p0\$1	(65.3850, 100.3000)	(65.4060, 100.4585)	0.1305
gf180mcu_fd_io__asig_5p0\$1	(65.3850, 70.5700)	(65.4155, 70.6540)	0.0000
gf180mcu_fd_io__asig_5p0\$1	(65.3850, 100.2160)	(65.4155, 100.3000)	0.0000
gf180mcu_fd_io__asig_5p0\$1	(65.3850, 100.2160)	(65.5450, 100.2850)	0.0000
gf180mcu_fd_io__asig_5p0\$1	(65.3850, 70.5850)	(65.5450, 70.6540)	0.0000
gf180mcu_fd_io__asig_5p0\$1	(10.1050, 108.0450)	(10.1750, 108.1360)	0.0510
gf180mcu_fd_io__asig_5p0\$1	(64.8250, 108.0450)	(64.8950, 108.1360)	0.0510
gf180mcu_fd_io__asig_5p0\$1	(10.1050, 108.0450)	(10.1460, 108.1540)	0.0910
gf180mcu_fd_io__asig_5p0\$1	(64.8540, 108.0450)	(64.8950, 108.1540)	0.0910
gf180mcu_fd_io__asig_5p0\$1	(10.1050, 136.8040)	(10.1750, 136.8950)	0.0510
gf180mcu_fd_io__asig_5p0\$1	(64.8250, 136.8040)	(64.8950, 136.8950)	0.0510
gf180mcu_fd_io__asig_5p0\$1	(10.1050, 136.7860)	(10.1460, 136.8950)	0.0910
gf180mcu_fd_io__asig_5p0\$1	(64.8540, 136.7860)	(64.8950, 136.8950)	0.0910
gf180mcu_fd_io__asig_5p0\$1	(10.1050, 136.8040)	(10.2135, 136.8950)	0.0410
gf180mcu_fd_io__asig_5p0\$1	(10.1050, 108.0450)	(10.2135, 108.1360)	0.0410
gf180mcu_fd_io__asig_5p0\$1	(64.7865, 136.8040)	(64.8950, 136.8950)	0.0410
gf180mcu_fd_io__asig_5p0\$1	(64.7865, 108.0450)	(64.8950, 108.1360)	0.0410

PP.6 : Pplus overlap with PCOMP butted to NCOMP : 0.22

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2617:internal1

Structure (lower left x, y) (upper right x, y) Distance

trackA (1367.3700, 2391.7750) (1368.2900, 2391.7950) 0.0200

trackA (1367.1510, 2391.7750) (1367.3700, 2391.7950) 0.0200
trackA (1368.2900, 2391.7750) (1368.5090, 2391.7950) 0.0200
trackA (1376.6800, 2391.7750) (1377.6000, 2391.7950) 0.0200
trackA (1376.4610, 2391.7750) (1376.6800, 2391.7950) 0.0200
trackA (1377.6000, 2391.7750) (1377.8190, 2391.7950) 0.0200
trackA (1358.0600, 2391.7750) (1358.9800, 2391.7950) 0.0200
trackA (1357.8410, 2391.7750) (1358.0600, 2391.7950) 0.0200
trackA (1358.9800, 2391.7750) (1359.1990, 2391.7950) 0.0200
trackA (1385.9900, 2391.7750) (1386.9100, 2391.7950) 0.0200
trackA (1385.7710, 2391.7750) (1385.9900, 2391.7950) 0.0200
trackA (1386.9100, 2391.7750) (1387.1290, 2391.7950) 0.0200
trackA (1358.3000, 2388.8350) (1358.7400, 2388.8550) 0.0200
trackA (1367.6100, 2388.8350) (1368.0500, 2388.8550) 0.0200
trackA (1376.9200, 2388.8350) (1377.3600, 2388.8550) 0.0200
trackA (1386.2300, 2388.8350) (1386.6700, 2388.8550) 0.0200

V1.1: Min/max Via1 size : 0.26

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2765:not_length_edge

WARNING: The error count of 102 for this check exceeds the limit set in
the runset. Details only available for the first 100.

Check was stopped early because error limit was reached.

Structure (lower left x, y) (upper right x, y) Distance

Unnamed_02d9ae27 (-10.5300, 14.1250) (-10.5300, 14.3900) 0.2650
Unnamed_02d9ae27 (-10.2700, 14.1250) (-10.2700, 14.3900) 0.2650
Unnamed_02d9ae27 (-9.3300, 14.1250) (-9.3300, 14.3900) 0.2650
Unnamed_02d9ae27 (-9.0700, 14.1250) (-9.0700, 14.3900) 0.2650
Unnamed_02d9ae27 (-8.5300, 14.1250) (-8.5300, 14.3900) 0.2650
Unnamed_02d9ae27 (-8.2700, 14.1250) (-8.2700, 14.3900) 0.2650
Unnamed_02d9ae27 (-7.7300, 14.1250) (-7.7300, 14.3900) 0.2650
Unnamed_02d9ae27 (-7.4700, 14.1250) (-7.4700, 14.3900) 0.2650
Unnamed_02d9ae27 (-6.9300, 14.1250) (-6.9300, 14.3900) 0.2650
Unnamed_02d9ae27 (-6.6700, 14.1250) (-6.6700, 14.3900) 0.2650
Unnamed_02d9ae27 (-6.7600, 10.2850) (-6.7600, 10.5500) 0.2650
Unnamed_02d9ae27 (-6.5000, 10.2850) (-6.5000, 10.5500) 0.2650
Unnamed_02d9ae27 (-6.1300, 14.1250) (-6.1300, 14.3900) 0.2650

Unnamed_02d9ae27 (-5.8700, 14.1250) (-5.8700, 14.3900) 0.2650
Unnamed_02d9ae27 (-5.6200, 17.6600) (-5.6200, 17.9250) 0.2650
Unnamed_02d9ae27 (-5.3600, 17.6600) (-5.3600, 17.9250) 0.2650
Unnamed_02d9ae27 (-5.3300, 14.1250) (-5.3300, 14.3900) 0.2650
Unnamed_02d9ae27 (-5.0700, 14.1250) (-5.0700, 14.3900) 0.2650
Unnamed_02d9ae27 (-4.5300, 14.1250) (-4.5300, 14.3900) 0.2650
Unnamed_02d9ae27 (-4.2700, 14.1250) (-4.2700, 14.3900) 0.2650
Unnamed_02d9ae27 (-4.4800, 10.2850) (-4.4800, 10.5500) 0.2650
Unnamed_02d9ae27 (-4.2200, 10.2850) (-4.2200, 10.5500) 0.2650
Unnamed_02d9ae27 (-3.7300, 14.1250) (-3.7300, 14.3900) 0.2650
Unnamed_02d9ae27 (-3.4700, 14.1250) (-3.4700, 14.3900) 0.2650
Unnamed_02d9ae27 (-2.9300, 14.1250) (-2.9300, 14.3900) 0.2650
Unnamed_02d9ae27 (-2.6700, 14.1250) (-2.6700, 14.3900) 0.2650
Unnamed_02d9ae27 (-2.1300, 14.1250) (-2.1300, 14.3900) 0.2650
Unnamed_02d9ae27 (-1.8700, 14.1250) (-1.8700, 14.3900) 0.2650
Unnamed_02d9ae27 (-1.9600, 13.2400) (-1.9600, 13.4950) 0.2550
Unnamed_02d9ae27 (-1.7000, 13.2400) (-1.7000, 13.4950) 0.2550
Unnamed_02d9ae27 (-1.3300, 14.1250) (-1.3300, 14.3900) 0.2650
Unnamed_02d9ae27 (-1.0700, 14.1250) (-1.0700, 14.3900) 0.2650
Unnamed_02d9ae27 (-0.5300, 14.1250) (-0.5300, 14.3900) 0.2650
Unnamed_02d9ae27 (-0.2700, 14.1250) (-0.2700, 14.3900) 0.2650
Unnamed_02d9ae27 (0.2700, 14.1250) (0.2700, 14.3900) 0.2650
Unnamed_02d9ae27 (0.5300, 14.1250) (0.5300, 14.3900) 0.2650
Unnamed_02d9ae27 (0.5600, 10.2850) (0.5600, 10.5500) 0.2650
Unnamed_02d9ae27 (0.8200, 10.2850) (0.8200, 10.5500) 0.2650
Unnamed_02d9ae27 (1.0700, 14.1250) (1.0700, 14.3900) 0.2650
Unnamed_02d9ae27 (1.3300, 14.1250) (1.3300, 14.3900) 0.2650
Unnamed_02d9ae27 (1.7000, 17.6600) (1.7000, 17.9250) 0.2650
Unnamed_02d9ae27 (1.9600, 17.6600) (1.9600, 17.9250) 0.2650
Unnamed_02d9ae27 (1.8700, 14.1250) (1.8700, 14.3900) 0.2650
Unnamed_02d9ae27 (2.1300, 14.1250) (2.1300, 14.3900) 0.2650
Unnamed_02d9ae27 (2.6700, 14.1250) (2.6700, 14.3900) 0.2650
Unnamed_02d9ae27 (2.9300, 14.1250) (2.9300, 14.3900) 0.2650
Unnamed_02d9ae27 (2.8400, 10.2850) (2.8400, 10.5500) 0.2650
Unnamed_02d9ae27 (3.1000, 10.2850) (3.1000, 10.5500) 0.2650
Unnamed_02d9ae27 (3.4700, 14.1250) (3.4700, 14.3900) 0.2650
Unnamed_02d9ae27 (3.7300, 14.1250) (3.7300, 14.3900) 0.2650
Unnamed_02d9ae27 (4.2700, 14.1250) (4.2700, 14.3900) 0.2650
Unnamed_02d9ae27 (4.5300, 14.1250) (4.5300, 14.3900) 0.2650
Unnamed_02d9ae27 (5.0700, 14.1250) (5.0700, 14.3900) 0.2650
Unnamed_02d9ae27 (5.3300, 14.1250) (5.3300, 14.3900) 0.2650
Unnamed_02d9ae27 (5.3600, 13.2400) (5.3600, 13.4950) 0.2550
Unnamed_02d9ae27 (5.6200, 13.2400) (5.6200, 13.4950) 0.2550
Unnamed_02d9ae27 (5.8700, 14.1250) (5.8700, 14.3900) 0.2650

Unnamed_02d9ae27 (6.1300, 14.1250) (6.1300, 14.3900) 0.2650
Unnamed_02d9ae27 (6.6700, 14.1250) (6.6700, 14.3900) 0.2650
Unnamed_02d9ae27 (6.9300, 14.1250) (6.9300, 14.3900) 0.2650
Unnamed_02d9ae27 (7.4700, 14.1250) (7.4700, 14.3900) 0.2650
Unnamed_02d9ae27 (7.7300, 14.1250) (7.7300, 14.3900) 0.2650
Unnamed_02d9ae27 (8.2700, 14.1250) (8.2700, 14.3900) 0.2650
Unnamed_02d9ae27 (8.5300, 14.1250) (8.5300, 14.3900) 0.2650
Unnamed_02d9ae27 (9.0700, 14.1250) (9.0700, 14.3900) 0.2650
Unnamed_02d9ae27 (9.3300, 14.1250) (9.3300, 14.3900) 0.2650
Unnamed_02d9ae27 (10.2700, 14.1250) (10.2700, 14.3900) 0.2650
Unnamed_02d9ae27 (10.5300, 14.1250) (10.5300, 14.3900) 0.2650
Unnamed_02d9ae27 (-10.5300, 26.3300) (-10.5300, 26.5950) 0.2650
Unnamed_02d9ae27 (-10.2700, 26.3300) (-10.2700, 26.5950) 0.2650
Unnamed_02d9ae27 (-9.3300, 26.3300) (-9.3300, 26.5950) 0.2650
Unnamed_02d9ae27 (-9.0700, 26.3300) (-9.0700, 26.5950) 0.2650
Unnamed_02d9ae27 (-8.5300, 26.3300) (-8.5300, 26.5950) 0.2650
Unnamed_02d9ae27 (-8.2700, 26.3300) (-8.2700, 26.5950) 0.2650
Unnamed_02d9ae27 (-7.7300, 26.3300) (-7.7300, 26.5950) 0.2650
Unnamed_02d9ae27 (-7.4700, 26.3300) (-7.4700, 26.5950) 0.2650
Unnamed_02d9ae27 (-6.9300, 26.3300) (-6.9300, 26.5950) 0.2650
Unnamed_02d9ae27 (-6.6700, 26.3300) (-6.6700, 26.5950) 0.2650
Unnamed_02d9ae27 (-6.7600, 19.2700) (-6.7600, 19.5350) 0.2650
Unnamed_02d9ae27 (-6.5000, 19.2700) (-6.5000, 19.5350) 0.2650
Unnamed_02d9ae27 (-6.7600, 20.8700) (-6.7600, 21.1350) 0.2650
Unnamed_02d9ae27 (-6.5000, 20.8700) (-6.5000, 21.1350) 0.2650
Unnamed_02d9ae27 (-6.1300, 26.3300) (-6.1300, 26.5950) 0.2650
Unnamed_02d9ae27 (-5.8700, 26.3300) (-5.8700, 26.5950) 0.2650
Unnamed_02d9ae27 (-5.6200, 19.2700) (-5.6200, 19.5350) 0.2650
Unnamed_02d9ae27 (-5.3600, 19.2700) (-5.3600, 19.5350) 0.2650
Unnamed_02d9ae27 (-5.6200, 20.8700) (-5.6200, 21.1350) 0.2650
Unnamed_02d9ae27 (-5.3600, 20.8700) (-5.3600, 21.1350) 0.2650
Unnamed_02d9ae27 (-5.3300, 26.3300) (-5.3300, 26.5950) 0.2650
Unnamed_02d9ae27 (-5.0700, 26.3300) (-5.0700, 26.5950) 0.2650
Unnamed_02d9ae27 (-4.5300, 26.3300) (-4.5300, 26.5950) 0.2650
Unnamed_02d9ae27 (-4.2700, 26.3300) (-4.2700, 26.5950) 0.2650
Unnamed_02d9ae27 (-4.4800, 19.2700) (-4.4800, 19.5350) 0.2650
Unnamed_02d9ae27 (-4.2200, 19.2700) (-4.2200, 19.5350) 0.2650
Unnamed_02d9ae27 (-4.4800, 20.8700) (-4.4800, 21.1350) 0.2650
Unnamed_02d9ae27 (-4.2200, 20.8700) (-4.2200, 21.1350) 0.2650
Unnamed_02d9ae27 (-3.7300, 26.3300) (-3.7300, 26.5950) 0.2650
Unnamed_02d9ae27 (-3.4700, 26.3300) (-3.4700, 26.5950) 0.2650
Unnamed_02d9ae27 (-3.1000, 19.2700) (-3.1000, 19.5350) 0.2650
Unnamed_02d9ae27 (-2.8400, 19.2700) (-2.8400, 19.5350) 0.2650

V2.1: Min/max Via2 size : 0.26

/evprj182/projects/GF180MCU/combined-pdk/dk_synopsys/pdk-180/DRC_ICV/DRC/ICV/gf180
mcu_drc.rs:2765:not_length_edge

WARNING: The error count of 102 for this check exceeds the limit set in
the runset. Details only available for the first 100.

Check was stopped early because error limit was reached.

Structure (lower left x, y) (upper right x, y) Distance

trackA (2004.0700, 346.6150) (2004.1150, 346.6150) 0.0450
trackA (2004.1150, 346.4050) (2004.1150, 346.6150) 0.2100
trackA (2004.0700, 347.2350) (2004.1150, 347.2350) 0.0450
trackA (2004.1150, 347.0250) (2004.1150, 347.2350) 0.2100
trackA (2004.0700, 347.8550) (2004.1150, 347.8550) 0.0450
trackA (2004.1150, 347.6450) (2004.1150, 347.8550) 0.2100
trackA (2004.3300, 346.6650) (2004.3300, 346.8750) 0.2100
trackA (2004.3300, 346.6650) (2004.3750, 346.6650) 0.0450
trackA (2004.3300, 347.2850) (2004.3300, 347.4950) 0.2100
trackA (2004.3300, 347.2850) (2004.3750, 347.2850) 0.0450
trackA (2004.3300, 347.9050) (2004.3300, 348.1150) 0.2100
trackA (2004.3300, 347.9050) (2004.3750, 347.9050) 0.0450
trackA (2004.6900, 346.6150) (2004.7350, 346.6150) 0.0450
trackA (2004.7350, 346.4050) (2004.7350, 346.6150) 0.2100
trackA (2004.6900, 347.2350) (2004.7350, 347.2350) 0.0450
trackA (2004.7350, 347.0250) (2004.7350, 347.2350) 0.2100
trackA (2004.6900, 347.8550) (2004.7350, 347.8550) 0.0450
trackA (2004.7350, 347.6450) (2004.7350, 347.8550) 0.2100
trackA (2004.9500, 346.6650) (2004.9500, 346.8750) 0.2100
trackA (2004.9500, 346.6650) (2004.9950, 346.6650) 0.0450
trackA (2004.9500, 347.2850) (2004.9500, 347.4950) 0.2100
trackA (2004.9500, 347.2850) (2004.9950, 347.2850) 0.0450
trackA (2004.9500, 347.9050) (2004.9500, 348.1150) 0.2100
trackA (2004.9500, 347.9050) (2004.9950, 347.9050) 0.0450
trackA (2005.3100, 346.6150) (2005.3550, 346.6150) 0.0450
trackA (2005.3550, 346.4050) (2005.3550, 346.6150) 0.2100
trackA (2005.3100, 347.2350) (2005.3550, 347.2350) 0.0450
trackA (2005.3550, 347.0250) (2005.3550, 347.2350) 0.2100
trackA (2005.3100, 347.8550) (2005.3550, 347.8550) 0.0450

trackA	(2005.3550, 347.6450) (2005.3550, 347.8550) 0.2100
trackA	(2005.5700, 346.6650) (2005.5700, 346.8750) 0.2100
trackA	(2005.5700, 346.6650) (2005.6150, 346.6650) 0.0450
trackA	(2005.5700, 347.2850) (2005.5700, 347.4950) 0.2100
trackA	(2005.5700, 347.2850) (2005.6150, 347.2850) 0.0450
trackA	(2005.5700, 347.9050) (2005.5700, 348.1150) 0.2100
trackA	(2005.5700, 347.9050) (2005.6150, 347.9050) 0.0450
trackA	(2005.9300, 346.6150) (2005.9750, 346.6150) 0.0450
trackA	(2005.9750, 346.4050) (2005.9750, 346.6150) 0.2100
trackA	(2005.9300, 347.2350) (2005.9750, 347.2350) 0.0450
trackA	(2005.9750, 347.0250) (2005.9750, 347.2350) 0.2100
trackA	(2005.9300, 347.8550) (2005.9750, 347.8550) 0.0450
trackA	(2005.9750, 347.6450) (2005.9750, 347.8550) 0.2100
trackA	(2006.1900, 346.6650) (2006.1900, 346.8750) 0.2100
trackA	(2006.1900, 346.6650) (2006.2350, 346.6650) 0.0450
trackA	(2006.1900, 347.2850) (2006.1900, 347.4950) 0.2100
trackA	(2006.1900, 347.2850) (2006.2350, 347.2850) 0.0450
trackA	(2006.1900, 347.9050) (2006.1900, 348.1150) 0.2100
trackA	(2006.1900, 347.9050) (2006.2350, 347.9050) 0.0450
trackA	(2015.5350, 346.6650) (2015.5350, 346.8750) 0.2100
trackA	(2015.5350, 346.4050) (2015.5350, 346.6150) 0.2100
trackA	(2015.5350, 347.2850) (2015.5350, 347.4950) 0.2100
trackA	(2015.5350, 347.0250) (2015.5350, 347.2350) 0.2100
trackA	(2016.1550, 346.6650) (2016.1550, 346.8750) 0.2100
trackA	(2016.1550, 346.4050) (2016.1550, 346.6150) 0.2100
trackA	(2016.1550, 347.2850) (2016.1550, 347.4950) 0.2100
trackA	(2016.1550, 347.0250) (2016.1550, 347.2350) 0.2100
trackA	(2015.5350, 347.9050) (2015.5350, 348.1150) 0.2100
trackA	(2015.5350, 347.6450) (2015.5350, 347.8550) 0.2100
trackA	(2016.1550, 347.9050) (2016.1550, 348.1150) 0.2100
trackA	(2016.1550, 347.6450) (2016.1550, 347.8550) 0.2100
trackA	(2016.7750, 346.6650) (2016.7750, 346.8750) 0.2100
trackA	(2016.7750, 347.2850) (2016.7750, 347.4950) 0.2100
trackA	(2016.7750, 347.9050) (2016.7750, 348.1150) 0.2100
trackA	(2016.7750, 346.4050) (2016.7750, 346.6150) 0.2100
trackA	(2016.7750, 347.0250) (2016.7750, 347.2350) 0.2100
trackA	(2016.7750, 347.6450) (2016.7750, 347.8550) 0.2100
trackA	(2017.9650, 346.6650) (2017.9650, 346.8750) 0.2100
trackA	(2017.7550, 346.6650) (2017.9650, 346.6650) 0.2100
trackA	(2018.0150, 346.4050) (2018.0150, 346.6150) 0.2100
trackA	(2018.0150, 346.6150) (2018.2250, 346.6150) 0.2100
trackA	(2017.9650, 347.2850) (2017.9650, 347.4950) 0.2100
trackA	(2017.7550, 347.2850) (2017.9650, 347.2850) 0.2100
trackA	(2018.0150, 347.0250) (2018.0150, 347.2350) 0.2100

trackA	(2018.0150, 347.2350)	(2018.2250, 347.2350)	0.2100
trackA	(2017.9650, 347.9050)	(2017.9650, 348.1150)	0.2100
trackA	(2017.7550, 347.9050)	(2017.9650, 347.9050)	0.2100
trackA	(2018.0150, 347.6450)	(2018.0150, 347.8550)	0.2100
trackA	(2018.0150, 347.8550)	(2018.2250, 347.8550)	0.2100
trackA	(2018.5850, 346.6650)	(2018.5850, 346.8750)	0.2100
trackA	(2018.3750, 346.6650)	(2018.5850, 346.6650)	0.2100
trackA	(2018.6350, 346.4050)	(2018.6350, 346.6150)	0.2100
trackA	(2018.6350, 346.6150)	(2018.8450, 346.6150)	0.2100
trackA	(2018.5850, 347.2850)	(2018.5850, 347.4950)	0.2100
trackA	(2018.3750, 347.2850)	(2018.5850, 347.2850)	0.2100
op_buffer	(-37.8950, -37.7050)	(-37.8950, -37.4400)	0.2650
op_buffer	(-37.6350, -37.7050)	(-37.6350, -37.4400)	0.2650
op_buffer	(-8.6850, -38.8050)	(-8.6850, -38.5400)	0.2650
op_buffer	(-8.4250, -38.8050)	(-8.4250, -38.5400)	0.2650
op_buffer	(6.7350, -37.7050)	(6.7350, -37.4400)	0.2650
op_buffer	(6.9950, -37.7050)	(6.9950, -37.4400)	0.2650
op_buffer	(9.7350, -38.8050)	(9.7350, -38.5400)	0.2650
op_buffer	(9.9950, -38.8050)	(9.9950, -38.5400)	0.2650
Unnamed_02d9ae27	(-11.5300, 26.3350)	(-11.5300, 26.5900)	0.2550
Unnamed_02d9ae27	(-11.2700, 26.3350)	(-11.2700, 26.5900)	0.2550
Unnamed_02d9ae27	(7.5000, 10.2850)	(7.5000, 10.5500)	0.2650
Unnamed_02d9ae27	(7.7600, 10.2850)	(7.7600, 10.5500)	0.2650
Unnamed_02d9ae27	(7.5000, 12.4350)	(7.5000, 12.7000)	0.2650
Unnamed_02d9ae27	(7.7600, 12.4350)	(7.7600, 12.7000)	0.2650
Unnamed_02d9ae27	(12.0000, 25.4450)	(12.0000, 25.7000)	0.2550
Unnamed_02d9ae27	(12.2600, 25.4450)	(12.2600, 25.7000)	0.2550